Transient-testing platforms and automation techniques for LDOs and buck regulators

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Introduction

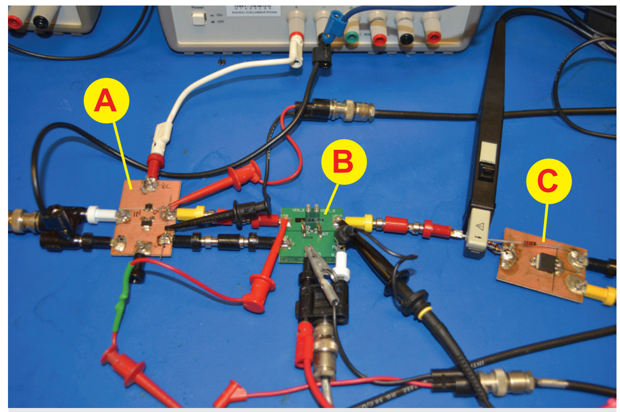
With mobile processors in wireless devices operating in the gigahertz range, there is increasing consumer demand for higher performance, longer battery life, smaller size, and lower cost. Therefore, the design of power management circuits is becoming an increasingly complex issue. Low dropout regulators (LDOs) and switching regulators are indispensable components in portable systems with standalone regulators and power management units (PMUs). As high-speed and portable communications devices employ regulators that require faster response time, it is necessary to rigorously validate regulator performance and merits in order to ensure reliable power management products. Key performance parameters include line transient, load transient, startup, load and line regulation, and several others. To have a complete analysis of these parameters, it is necessary to have state-of-the-art tools for the hardware test platform and mature methodology. These tools allow accurate and high sample rates for parameter characterization in addition to supporting automation techniques that speeds up testing and ensures repeatable results.

Implementing high-edge-rate and reusable test apparatus

For an accurate assessment of the key parameters of a regulator, it is necessary to generate steps in line voltage and load current that are fast with respect to the regulator's control-loop response time. Lab equipment and many commercial instruments that use operational amplifiers (op amps), passive components, and large driver chains can limit the rise and fall times of the stimulus signals with large excursions. To obtain high-speed edge rates for load transients (>> 1 A/µs) and line transients (>> 0.1 V/µs, with input caps), practically no off-the-shelf products are available.

It is possible for a slow-transient stimulus to make a poor regulator look good. In response, incremental research and development (R&D) led to simpler designs that are low in parasitic L and C, which can be readily built and duplicated for use in design and application labs. Setting up a respectable test jig is half the solution. To achieve optimal response, the device under test (DUT) must be properly wired or socketed onto the printed circuit board (PCB). Also important is proper selection of optimal ground and supply conduits, bypassing, charge reservoirs, and external support components. After all, it is the merits of the DUT that should be ascertained, not the parasitic or the unwanted effects from improper components and physical layout.

Figure 1. Antiquated setup for transient testing



A. Emitter followers and pulse generator create V_{IN} step voltage during line transient tests.

B. Device under test (DUT) is an LDO evaluation board (EVB).

C. PCB for NMOS transient load switch. A constant load is applied during line transient tests.

Preamble on test hardware challenges and limitations

In a load-transient test, the regulator's input is powered by a constant voltage source and the output is rapidly switched to a greater resistive load or current sink. A line-transient test is similar in that a line-voltage step is rapidly injected at the regulator input while its output is supported with a constant load. Figure 1 shows a typical test setup for transient testing. The setup is relatively modularized for ease of assembly and the long cable lengths were adequate for legacy technology. However, this setup is not satisfactory for today's requirement because of parasitics, ground loops, and higher voltages and currents.

Test-jig parasitics and automation

A transient-testing program for semi-automated testing was initiated in January of 2013 for PMUs and regulators. A universal regulator test bed was conceived and constructed to verify its merits. Figures 2 and 3 show an LDO regulator test jig that can accommodate an evaluation board (EVB) via machined socket pins for semi-automated testing. The schematic is shown in Figure 4.

Figure 2. Transient test jig with LDO EVB (blue PCB)

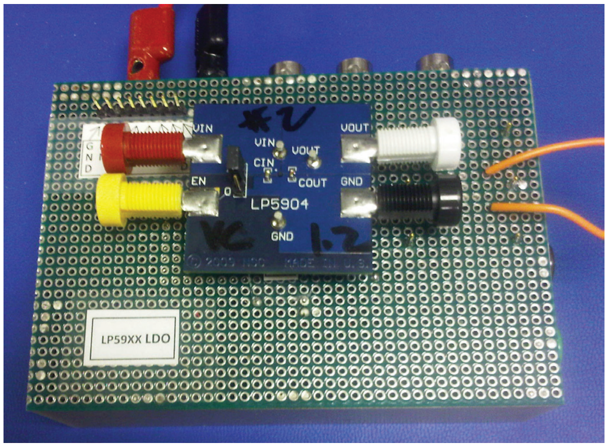
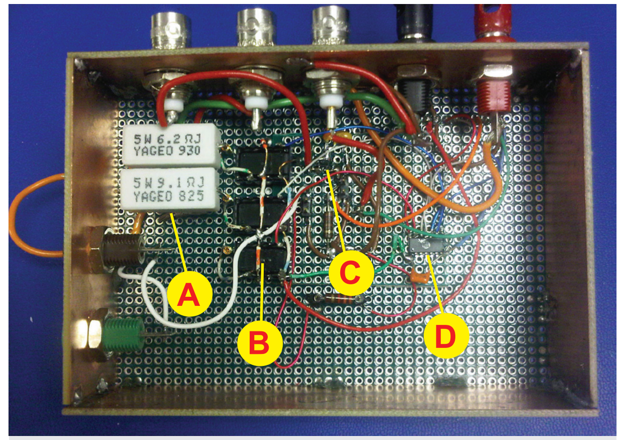
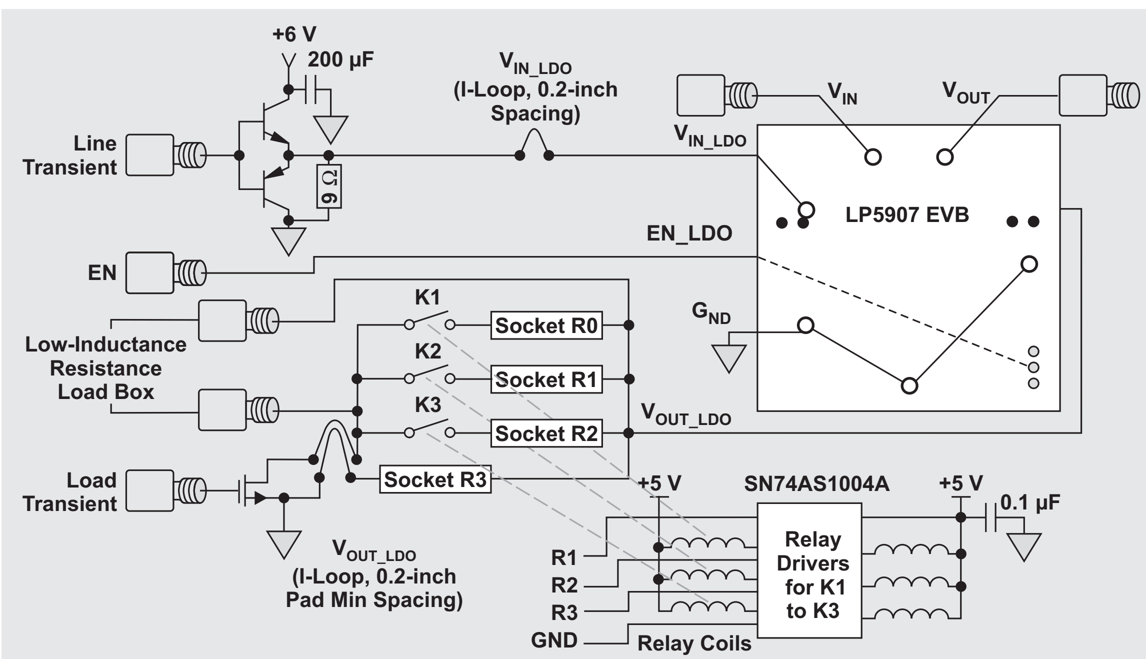


Figure 3. Back side of LDO test jig



A. NFET load step switch (under resistors).
B. Relays to select load.
C. NPN follower.
D. 48-mA relay drivers.

Figure 4. Schematic for the LDO test jig



Figures 5 through 7 show a similar transient test jig and schematic for a buck regulator.

Figure 5. Transient test jig and buck-regulator EVB (green PCB)

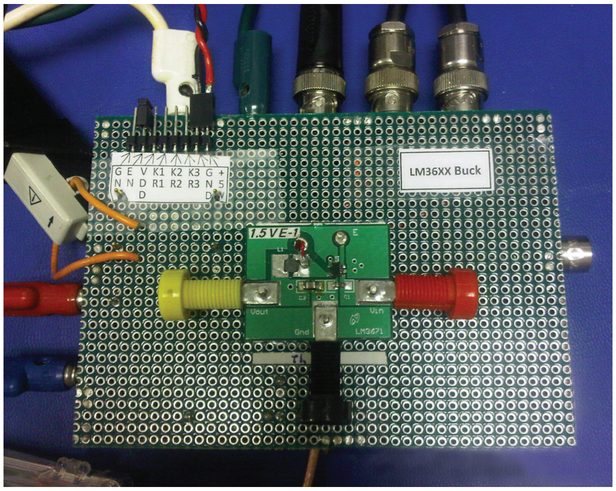
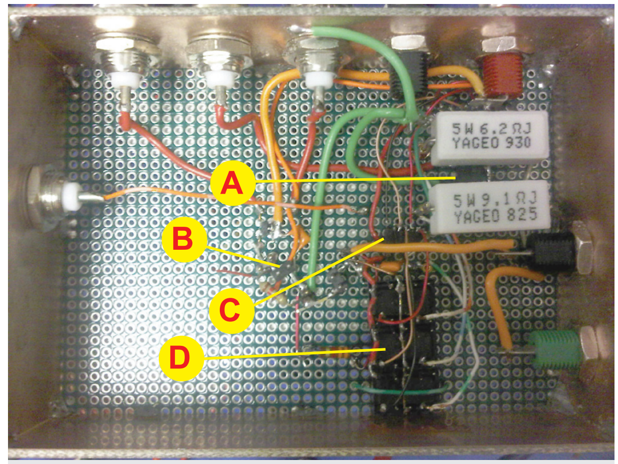
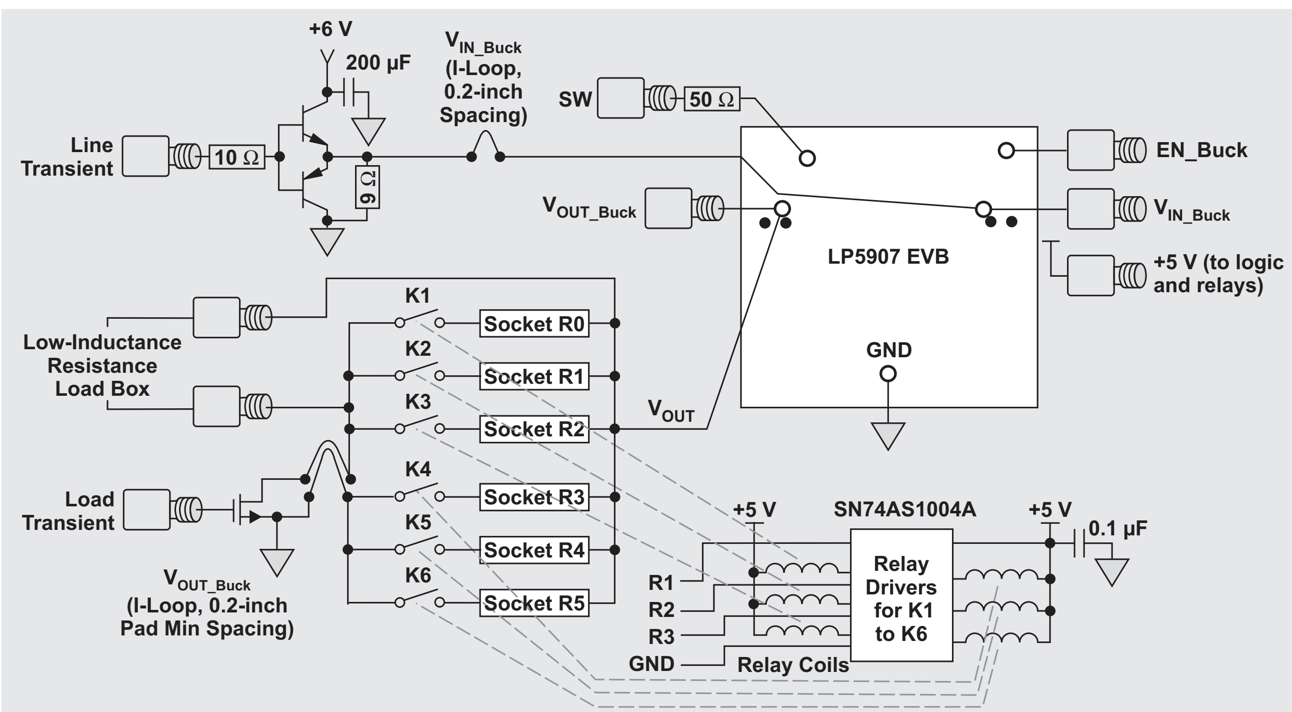


Figure 6. Back side of buck-regulator test jig



A. NFET load step switch (under resistors).
B. NPN follower for line step.
C. 48-mA relay drivers.
D. Relays to select load.

Figure 7. Schematic for the buck regulator test jig

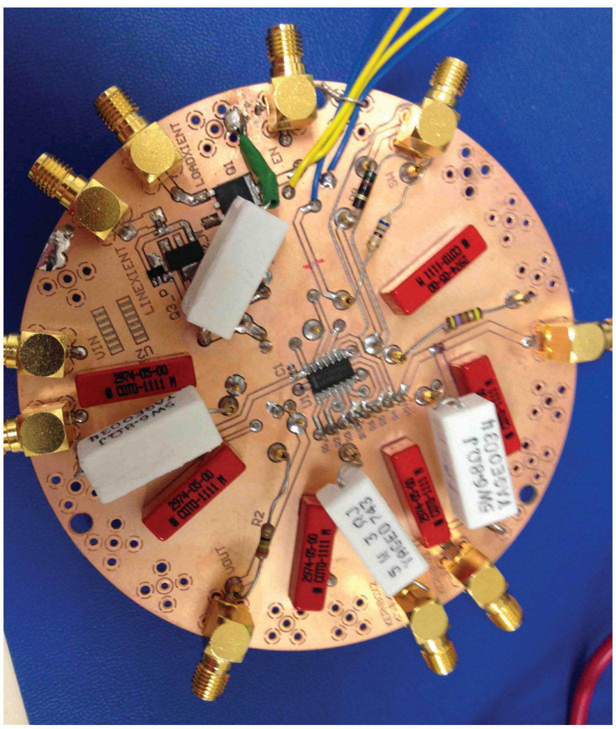


Further enhancements

The test jigs were successful in achieving the design goals in that they significantly reduced parasitics and current loops, thus enabling faster edge-rate stimulus for validating targeted products. In June of 2013, a follow-up enhanced design for a higher-performance, integrated transient test jig. This jig is capable of accommodating today's high-bandwidth and fast-edge-rate products and future generations.

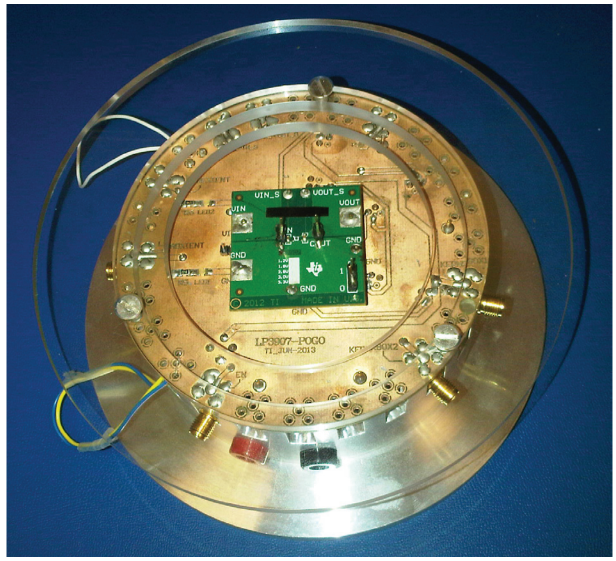
As shown in Figure 8, the enhanced jig was designed with a circular PCB configuration and can either adapt an EVB of a DUT for maximum flexibility. An alternate DUT layout is to solder it on the PCB for optimal performance. Radio frequency (RF) plumbing was used on the board and PCB traces were matched and impedance controlled. The jig also provides a rechargeable battery pack that provides clean and quiet power to the DUT for low-noise applications.

Figure 8. Enhanced test jig with resistive loads on board



For more extreme test requirements, the jig was redesigned to interface with temperature-cycling, air-stream systems that can be sealed air tight with no leakage, which will avoid icing at extreme temperatures. The result is the castle-shaped metal housing structure shown in Figure 9 that supports a personality card PCB for the EVB. An alternative could be a circular PCB with a direct on-board DUT mount. Also, a high-temperature transparent plastic adapter was included to interface to a temp-cycling housing.

Figure 9. Temperature-cycling test jig with personality PCB for PMUs

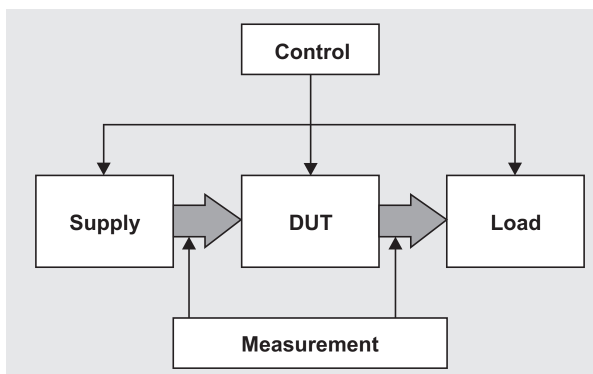


Architecture and automated test flow

A block diagram of the test environment for the automated test platform is shown in Figure 10.

The supply block provides all the voltage inputs and the line-transient input to the DUT. The load block provides multiple resistive loads that are controlled with relays. The control block is responsible for interfacing with the DUT and also for changing the supply and load settings. The measurement block is responsible for measuring the input and output voltages and currents.

Figure 10. Generic test environment



LDO test jig

Based on the jig schematic in Figure 4, the line-transient input is connected to a function generator to provide the line transient input to the LDO. Since the function generator cannot source a lot of current, an emitter follower is used to increase the current being sourced to the input. A 9-Ω resistor is connected at the output of the emitter follower circuit to provide fast discharge of the input capacitor during the fall time of the input line transient.

For tests that do not require a line transient, a constant DC voltage is provided through the line transient input, which is connected to the input of the LDO. The enable (EN) input is available to provide a pulse for the startup test using a function generator. In other test cases, the enable pin is supplied with a constant DC voltage for regular enable operation. The load-transient input is also controlled by a function generator that switches the NMOSFET continuously for a load-transient test. There is a base load (1-mA load for the LDO), which is always connected to the output of the LDO. However, it can be disconnected, if required. Three other resistive loads are controlled by using three relays. In turn, these relays are controlled via a computer through a USB relay controller.

Buck test jig

The system architecture of the buck-regulator test jig shown in Figure 7 is virtually the same as for the LDO jig. The only major change is the addition of three new relays. These were added because of the complicated nature of the load-transient tests for a buck IC. Unlike a LDO, load transients consist of different base current for load-transient testing. For example, for a LDO, the load transients required are 1 mA to 20 mA, 1 mA to 100 mA and 1 mA to 250 mA. However, for a buck, the various load-transient tests require 1 mA to 50 mA, 50 mA to 400 mA, 200 mA to 400 mA, and 0.6 A to 1 A. Hence, there are additional relays. The PCB design has some other changes. The buck is a switching regulator, thus, there is an additional switching pin to probe. This pin is isolated from other parts of the board by creating 20-mm segregation on both sides of this trace and pin. The tests for the buck test platform are exactly the same as for the LDO platform.

PCB design and issues

There are two major concerns on the layout of the redesigned automation test platform for high-performance validation. The first concern is maintaining high edge rates and signal integrity of the stimuli. The test setup is designed to produce fast line and load transients for the DUT. However, impedance mismatches and cross-talk between traces can significantly affect these high-speed lines. The second concern is voltage drops in power lines caused by attenuation from long traces. Hence, proper PCB design following good RF techniques is required. Also, it is necessary to measure a signal as close to its origin as possible to mitigate voltage drop or parasitic effects.

Lab equipment deployed

For line/load-transient and startup testing, the test platform includes a programmable power supply, three function generators, one oscilloscope, and a test jig. The power supply is used to provide power to the test circuitry required to carry out line- and load-transient testing. The power supply is also used to power the enable pin of the DUT and the relay driver chip, which allows the user to select different loads for a particular test. The function generators are used for generating pulse waveforms (using the arbitrary function waveform) for the line-transient step, load-transient step, and to pulse the enable pin.

The oscilloscope measures the input and output voltages and currents. The test platform is also used to observe the enable pin for the startup test. Designed as a plug-and-play test platform where the DUT needs to be installed on the test jig, this architecture methodology allows the reuse of the platform for different DUTs. The test setup relies on instruments that are controlled by a laptop running LabVIEW® software and connected via a general purpose interface bus (GPIB). All instruments, except for the oscilloscope, are daisy chained using GPIB cables that are connected to the laptop using a USB to GPIB cable. The oscilloscope is directly connected to the laptop with a USB cable. BNC to SMA cables are used to measure or probe all the signals.

LabVIEW tool (LVT) for test automation

Visual basic routines for virtual instruments (VIs) are written to automate the transient tests. These tests consist of three blocks. The first block of the LVT test selects the loads for the test. The second block includes the feedback correction loop that continuously measures the rise and fall times of the input-transient stimulus and corrects for the output of the function generator until the correct rise and fall times are measured by the oscilloscope. The third block of the LVT test captures a screenshot of the output and input voltage once the feedback is completed. It also obtains the measured rise and fall times and the maximum and minimum output voltages. The LVT obtains the minimum, maximum and mean of all the parameters directly from the scope. It also calculates the average of the maximum and minimum value measured. The LVT then populates a matrix of measurements and graphs that are displayed on the front panel. These measurements are also written to a text file in the Text Files folder. The screen shots are saved to a pen drive inserted into the oscilloscope. The name of these files are decided based on the kind of load and edge-rate setting. However, the names can be changed in the block diagram of the LVT.

Conclusion

The platform for automating high-speed transient testing is very multi-disciplinary because it requires capabilities beyond typical validation and test R&D. Included are a wide range of disciplines such as basic knowledge of startup-and-transient behavior characteristics for linear and switching regulators, best practices plus novel techniques for test and measurement, board-level system design, and software development.

With the prototyping test jigs for both LDO and buck ICs, the proposed test procedures can be validated and automated for line-transient, load-transient and startup tests. Stimulus edge rates can be achieved in the nanosecond range with proper drive, interfacing, and termination. High-speed waveform-capture sampling can be done with high-performance test equipment and probes. Serial-interface control of device modes, operation, and test equipment can be programmed on the fly to automate testing. Furthermore, closed-loop control and monitoring facilitates programming the timed events and electrical parametric stimuli in addition to accurately logging response time delays.

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