Powering precision ADCs: Average versus transient current

Luke Allen
Applications Engineer

Bryan Lizon
Applications Manager

Introduction

Understanding the analog-to-digital converter (ADC) data-sheet power-supply parameters can help you design more reliable precision data acquisition (DAQ) systems. Specifically, it is important to understand that current consumption in an ADC data sheet is an average value specified at steady-state operating conditions. These measured current values therefore do not characterize transient current demand, even though ADC transient currents can be orders of magnitude larger than the specified ADC current. Transient currents can occur when transitioning between different ADC modes of operation and are most significant when initially powering the device. Moreover, the circuitry and components surrounding the ADC can cause additional transient current demand.

This article delves into the topic of ADC transient current demand by first introducing how a typical ADC data sheet specifies current, and then sharing the results of several tests that quantify transient current demand under different operating conditions. Multiple power-supply configurations that can source both average and transient currents are discussed, and finally the effects of various power-down methods are compared.

Power-supply specifications

Current consumption in an ADC data sheet is an average value specified at steady-state operating conditions. An ADC with many different operating conditions requires the specification of several current values. These conditions can include an average ADC supply current that scales relative to the data rate or increased current demand when enabling internal features such as programmable gain amplifiers (PGAs) or voltage references (VREFs). As an example, **Table 1** shows the data-sheet power-supply specifications at different operating conditions for TI's **ADS1261**, a 24-bit, 40-kSPS, 11-channel delta-sigma ADC with an integrated PGA and VREF.

Power Supply						
Parameter		**Test Conditions**	**MIN**	**TYP**	**MAX**	**Unit**
I_{AVVD}, I_{AVSS}	Analog supply current	PGA Bypass		2.7	4.5	mA
		PGA mode, gain = 1 to 32		3.8	6	
		PGA mode, gain = 64 or 128		4.3	6.5	
		Power-down mode		2	8	µA
I_{AVVD}, I_{AVSS}	Analog supply current (by function)	Voltage reference		0.2		mA
		40-kSPS mode		0.5		
		Current sources		As programmed		
I_{DVDD}	Digital supply current	20 SPS		0.4	0.65	mA
		40 kSPS		0.6	0.85	
		Power-down mode		30	50	µA
P_D	Power dissipation	PGA mode		20	32	mW
		Power-down mode		0.1	0.2	

***Table 1.** The data-sheet power-supply specifications for the ADS1261.*

The highlighted PGA Bypass section in **Table 1** shows that the average analog current drawn by the **ADS1261** during normal operation with the PGA bypassed is 2.7 mA (typical) or 4.5 mA (maximum). The highlighted "by function" section indicates how much the current increases when enabling each function. All of these supply-current specifications are characterized by measuring the average current drawn by the device after the current settles.

Data-sheet power-supply specifications therefore average out any transient current demand that the device or supporting circuitry requires during normal operation. This is important because transient currents during startup and switching can be significantly larger than the values specified in the data sheet. A reliable system design must be able to account for both average and transient current demand.

Transient currents

One challenge with transient currents is that their magnitude and duration can vary significantly as a result of the ADC operating conditions and surrounding circuitry. ADC data sheets therefore rarely specify transient currents. However, it is possible to measure transient currents for a given system configuration by probing with an oscilloscope across a small-value resistor placed in series with the power-supply trace. You can then use Ohm's law to determine the resulting current.

The **ADS1261** has an evaluation module (EVM) that incorporates such a resistor between the power-supply output and the ADC AVDD pin. **Figure 1** shows the relevant portion of the EVM schematic that includes a 10-Ω measurement resistor (R33). Measuring the average or transient voltage drop across this resistor and then dividing by 10 Ω calculates the average or transient current drawn by the **ADS1261**, respectively. I performed multiple tests under a variety of conditions to better understand the transient current behavior of this ADC.

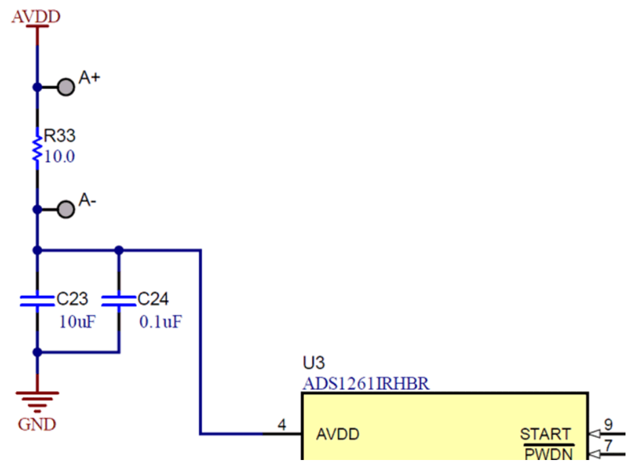

***Figure 1.** Transient current test circuit using the ADS1261 EVM.*

The first transient current test was a power-up test with the recommended 10-µF (C23) and 0.1-µF (C24) decoupling capacitors from AVDD to ground installed. **Figure 2** shows the **ADS1261** transient current under these conditions.

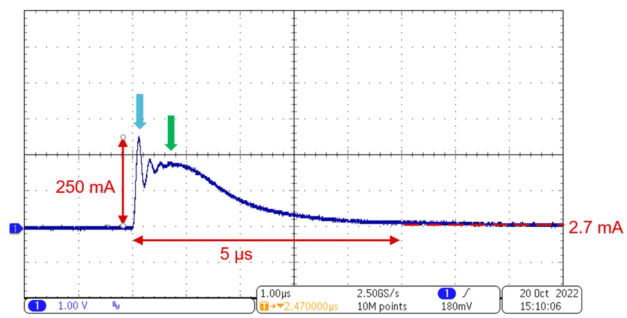

***Figure 2.** Measured transient current at power up with decoupling capacitors installed.*

Recall from the **ADS1261** power-supply specifications in **Table 1** that the average current with the PGA disabled is 2.7 mA (typical) or 4.5 mA (maximum). However, the blue arrow in **Figure 2** points to a 250-mA transient spike that occurs when the **ADS1261** is initially powered. This transient is >90 times the typical current and >55 times the maximum current specified in the data sheet. Similar current spikes can occur when the ADC undergoes any change in state.

The green arrow in Figure 2 identifies a second transient current required to charge up the decoupling capacitors. Under normal operating conditions, the decoupling capacitors store supplemental charge to provide extra current when transients occur. This extra charge helps maintain a steady supply voltage such that ADC operation remains unaffected. The capacitors must be charged up to the supply voltage from an uncharged state when the system is powered, however. Unpowered capacitors behave like a short at the instant the system powers up, resulting in a large inrush current. The magnitude of the inrush current increases as the value of the decoupling capacitor increases.

To measure only the transient current that the ADC requires, the second transient current test removed the recommended 10- and 0.1-μF decoupling capacitors from AVDD to ground in Figure 1. Figure 3 shows the ADS1261 transient current under these conditions.

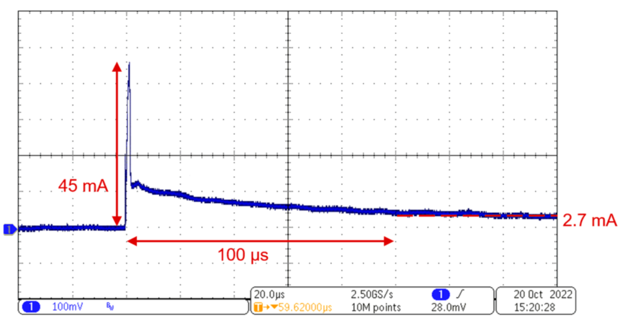

Figure 3. *Measured transient current at power up with decoupling capacitors removed.*

The 45-mA transient spike in Figure 1 represents only the power-up current required by the ADC attributable to switching. As expected, the ADC-only transient is smaller compared to the 250-mA spike that occurred when the decoupling capacitors were installed. However, this reduced transient magnitude comes at the cost of a significantly longer time for the ADC to reach the steady-state current because the capacitors no longer provide any supplemental charge. Additionally, this 45-mA transient is still 10 times the maximum ADC current specification of 4.5 mA listed in Table 1.

I performed a third set of tests to verify that different functions can also cause transient current spikes. Enabling the ADS1261 VREF was one such function that produced a spike. Figure 4 shows the observed behavior of this transient current.

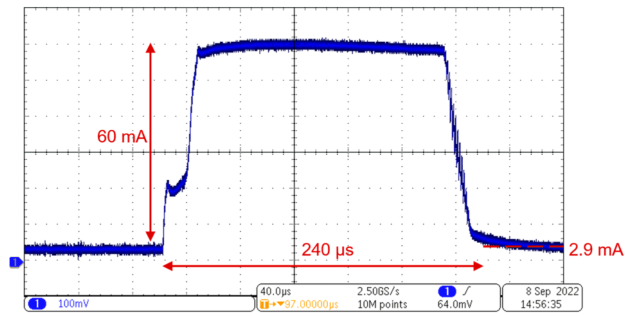

Figure 4. *Measured transient current with the ADS1261 VREF enabled.*

Recall from Table 1 that the typical ADS1261 VREF current is 0.2 mA. Operating the ADC with the PGA disabled (2.7 mA) and the internal VREF enabled should yield 2.9 mA of total current. However, the 60-mA measured transient current in Figure 4 is >20 times the expected value. This transient largely results from the inrush current required to charge a filtering capacitor placed between the VREF output pin and ground.

One interesting characteristic of Figure 4 is that the current demand remains constant at 60 mA for essentially the entire transient pulse. This behavior results from an inherent current limit designed into the ADS1261 internal VREF, which helps protect the ADC in case the REFOUT pin shorts to ground.

I performed some additional function tests that did not show any measurable transient current, although I did not test all operating conditions. Also, I should note that this behavior is not limited to the ADS1261; it is possible to observe the transient currents documented in this article with all precision ADCs.

Power-supply circuit options

Transient currents can cause issues such as voltage droop that may lead to unstable ADC operation. Therefore, it is important to design power supplies to accommodate both average and transient current demand. Review the benefits and challenges of three different power-supply options:

- Low dropout regulators (LDOs). TI recommends using LDOs to power precision ADCs. LDOs offer many benefits, such as excellent noise performance; low voltage ripple; and a small, simple implementation. The most important benefit of an LDO is its ability to reliably maintain the output voltage during transients while also providing low quiescent current. For more information on how to select the best LDO for any application, see Related Website section below.
- Linear regulators. Linear regulators with standard dropout voltages can also be a good option if selecting an LDO is cost-prohibitive. Linear regulators can reliably maintain the output voltage during transients while also providing low quiescent current similar to LDOs. The challenge with linear regulators is that the dropout voltage is significantly larger, which can require specific voltage rails just to power these devices. Linear regulators also tend to come in larger packages because they are less efficient and must dissipate more heat. Additional heat can raise the temperature of a closed system, which can contribute to drift errors in precision systems.
- Shunt regulators. One of the most cost-effective power-supply options is a shunt regulator. The cost savings come at the expense of the additional complexity required to design a reliable power-supply circuit. As an example, a precision ADC requiring bipolar supply operation might use the TLV431 – a low-voltage, adjustable shunt regulator – to generate ±2.5-V rails. You can use the TLV431 for this purpose because it has a low VREF. However, one challenge with this regulator is that it can supply only a limited amount of current. The TLV431 data sheet also requires a cathode current of ≥1 mA. These two restrictions limit the output-current capabilities of the standard setup shown in Figure 5 and Figure 6.

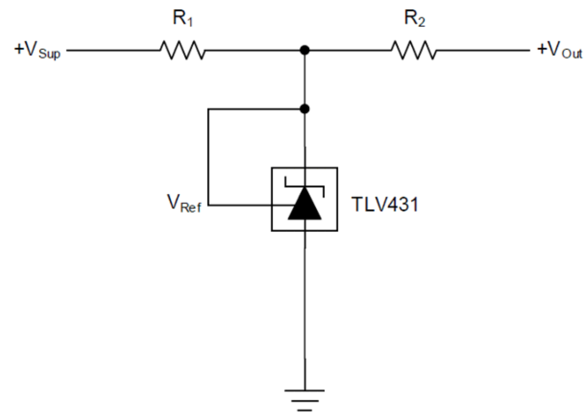

Figure 5. *Current-limited shunt regulator circuit with positive output.*

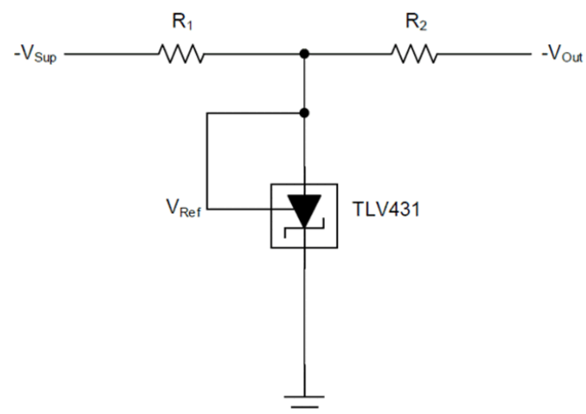

Figure 6. *Current-limited shunt regulator circuit with negative output.*

Figure 5 and Figure 6 show that both the cathode current and the current supplied to the ADC must flow through resistor R1. This configuration limits the supply current to (VSUP – VREF) / R1, resulting in two design challenges. First, current flowing continuously through R1 consumes power even with no applied load. Attempting to reduce R1 to increase the available supply current also proportionally increases the static power dissipation. Second, the maximum current set by R1 generally cannot support the hundreds of milliamperes of transient current that the ADC requires. An inability to provide the necessary current causes the supply voltage to droop, and can lead to unstable ADC operation.

Mitigate these issues by adding two components to the circuit in **Figure 5** and **Figure 6**. **Figure 7** and **Figure 8** show a modified shunt regulator circuit that includes a transistor and a bias resistor, Rb.

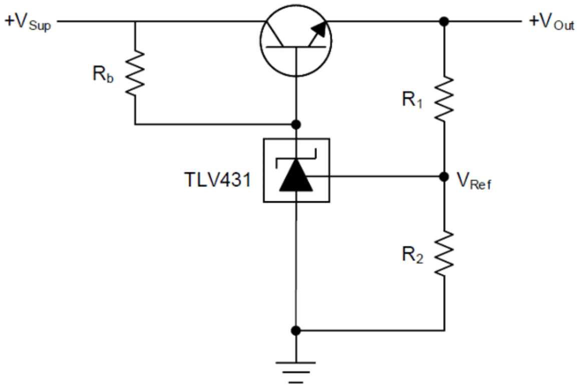

Figure 7. *Improved shunt regulator circuit with positive output.*

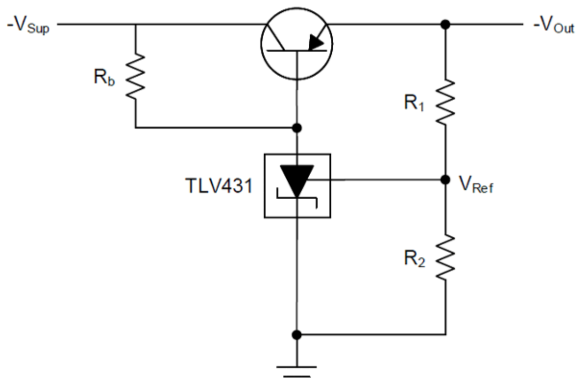

Figure 8. *Improved shunt regulator circuit with negative output.*

The power-supply circuit in **Figure 7** and **Figure 8** can provide more current compared to the system in **Figure 5** and **Figure 6** because the transistor eliminates any resistance between the supply input (VSUP) and output (VOUT). This new circuit can also maintain a cathode current of ≥1 mA by installing Rb instead of relying on R1. Resistors R1 and R2 therefore are only required to set the output voltage as per **Equation 1**.

$$V_{out} = \left(1 + \frac{R_1}{R_2}\right) \times V_{ref} \qquad (1)$$

For more information on how to use a voltage reference as a shunt regulator, see **Related Website** section below.

Low-power systems: Power down or power off?

Low-power DAQ systems often conserve energy by using different power-down methods. Some ADCs offer a power-down mode that helps reduce system power consumption by putting the device in a low-power state when it is not in use. The ADC data sheet then specifies the current consumption in this mode. Another popular power-saving technique is to simply turn off the power supply when the ADC is not in use and turn the power supply back on when needed. This method should result in no power consumption while the system is off.

The latter method is subject to the transient currents discussed in this article, however, because any capacitors must recharge every time the supply cycles. You can estimate how much current the system consumes when the supply is turned off by using the standard equations for charge (Q) and current (I), and then compare this value to the ADC data-sheet value in power-down mode.

For example, the **ADS1261** data sheet recommends 10- and 0.1-µF decoupling capacitors in parallel from AVDD to AVSS. The data sheet also specifies that AVDD must be 5 V. **Equation 2** and **Equation 3** calculate that the average current is 50.5 µA if the power supply cycles once per second:

$$Q = C \times V = 10.1\ \mu F \times 5\ V = 50.5\ \mu C \qquad (2)$$

$$I = \frac{Q}{t} = \frac{50.5\ \mu C}{1\ s} = 50.5\ \mu A \qquad (3)$$

where, C = 10.1 µF (10 µF + 0.1 µF), V = 5 V and t = 1 s.

Recall from the green highlighted section in **Table 1** that the **ADS1261** power-down current in power-down mode is only 8 µA (maximum). Comparing both options reveals that using the ADC power-down mode conserves >6 times more power relative to turning off the supplies. Therefore, it is important to consider the effect that transient currents can have on overall power consumption. Choosing to put the ADC in a power-down state can often be the more energy-efficient solution.

Related Website

- Download these e-books:
  - Texas Instruments: ***LDO Basics***
  - Texas Instruments: ***Tips and Tricks for Designing with Voltage References***
- Check out these TI E2E™ design support forums technical articles:
  - **How to Choose an LDO or Switching Regulator**
  - **How to Use a Voltage Reference as a Voltage Regulator**
- Texas Instruments: ***Understanding Stability Boundary Conditions Charts in TL431, TL432 Data Sheets***
- Find an LDO for your next precision ADC design using the **LDO parametric search**