Logic Solutions for PC100 SDRAM Registered DIMMs

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TEXAS INSTRUMENTS

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Contents

List of Illustrations

List of Tables

Introduction

Design of high-performance personal computer (PC) systems that are capable of meeting the needs imposed by modern operating systems and software includes the use of large banks of SDRAMs on DIMMs (see Figure 1). To meet the demands of stable functionality over the broad spectrum of operating environments, meet system timing needs, and to support data integrity, the loads presented by the large banks of SDRAMs on the DIMM modules require the use of buffers/drivers in the address and control signal paths. The PC SDRAM DIMM that is designed to operate at 100 MHz is known to the industry as PC100.[1] This report discusses some of the logic solutions that Texas Instruments (TI™) has available for the registered PC100 DIMM that provide improved performance, cost savings, and design optimization.

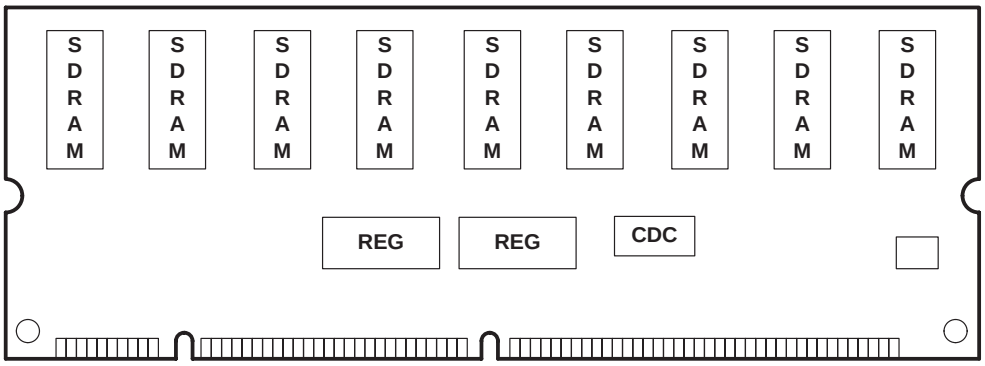


Figure 1. Registered SDRAM DIMM

Background

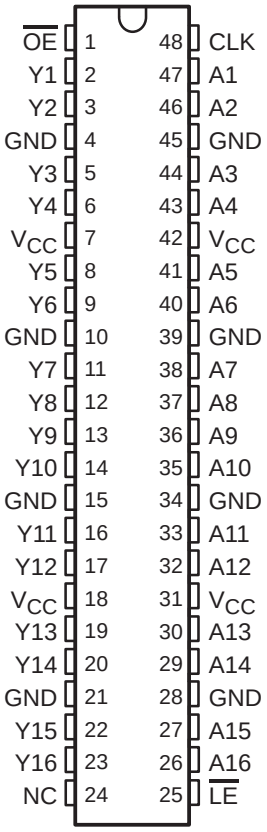
The 168-pin, 8-byte, registered SDRAM DIMM is a JEDEC-defined device.[2] Some of the defined signal paths include data signals, address signals, and control signals (see Table 1). There are up to 36 SDRAM integrated circuits (ICs) on the DIMM, with an SDRAM IC density of up to 128 megabits. This presents a large, highly capacitive load on the address and control signal paths to the memory controller. This load must be buffered with a logic buffer/driver IC. The buffer/driver IC choice that the designer makes is a way of differentiating the DIMM design to provide a competitive edge. The factors that *must* be considered in IC selection include propagation delay time (t_{pd}), input current (I_I), and output current versus voltage (IV) characteristics. But, there are the additional factors of bit-density and glue-logic requirements that, when properly considered, can result in a DIMM design that is simpler, more reliable, and more cost effective. To solve these needs, TI offers the ALVC family of devices. This application report addresses the following devices with respect to this application (see Figure 2):

- SN74ALVC16334[3]
- SN74ALVC162334[4]
- SN74ALVC16835[5]
- SN74ALVC162835[6]
- SN74ALVC162836[7]

Table 1. 168-Pin DIMM Pin Assignments

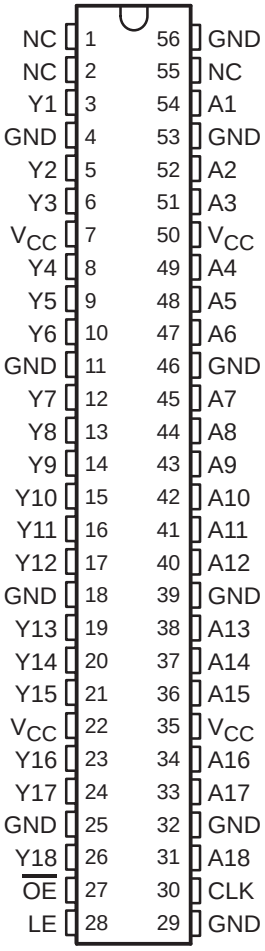
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	V_{SS}	29	DQMB1	57	DQ18	85	V_{SS}	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	V_{CC}	87	DQ33	115	$\overline{RAS}$	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	Vref NC	90	V_{CC}	118	A3	146	Vref NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	V_{CC}	101	DQ45	129	$\overline{S3}$	157	V_{CC}
18	V_{CC}	46	DQMB2	74	DQ28	102	V_{CC}	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	A13	160	DQ62
21	CB0	49	V_{CC}	77	DQ31	105	CB4	133	V_{CC}	161	DQ63
22	CB1	50	NC	78	V_{SS}	106	CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CK2	107	V_{SS}	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V_{CC}	54	V_{SS}	82	SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	V_{CC}	112	DQMB4	140	DQ49	168	V_{CC}

SN74ALVC16334
OR
SN74ALVC162334



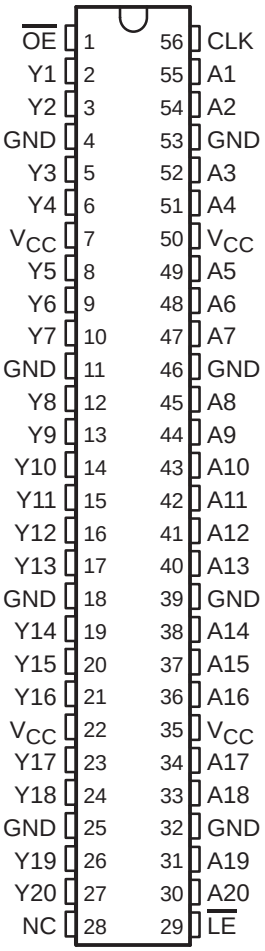
NC – No internal connection

SN74ALVC16835
OR
SN74ALVC162835



NC – No internal connection

SN74ALVC162836



NC – No internal connection

Figure 2. Pinouts (Top View)

Device Information

The devices being examined are members of the Texas Instruments Widebus™ family. They are manufactured using TI's EPIC™ (Enhanced-Performance Implanted CMOS) submicron process. These devices provide ESD protection exceeding 2000 V per MIL-STD-883, Method 3015, and exceeding 200 V using machine model (C = 200 pF, R = 0).

The SN74ALVC16334 and SN74ALVC162334 devices are 16-bit universal bus drivers with 3-state outputs, designed for 2.3-V to 3.6-V V_{CC} operation (see Table 2 and Figure 3). When the active-low latch-enable ($\overline{LE}$) input is low, the device operates in the transparent mode and the Y outputs follow the A inputs. If the clock (CLK) input is held in a high or low state, the device operates like a D-type latch, and the Y output data is latched when $\overline{LE}$ is taken high. If the CLK input is clocked when $\overline{LE}$ is high, the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by the active-low output-enable ($\overline{OE}$) input. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled. The SN74ALVC162334 also provides equivalent 26-Ω series resistors on the output port. Both the SN74ALVC16334 and SN74ALVC162334 devices are offered in 48-pin packages, which reduces the amount of required board space, as compared with the other devices being examined.

Table 2. Function Table for SN74ALVC16334 and SN74ALVC162334 Devices

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L	X	Y_0†

† Output level before the indicated steady-state input conditions were established

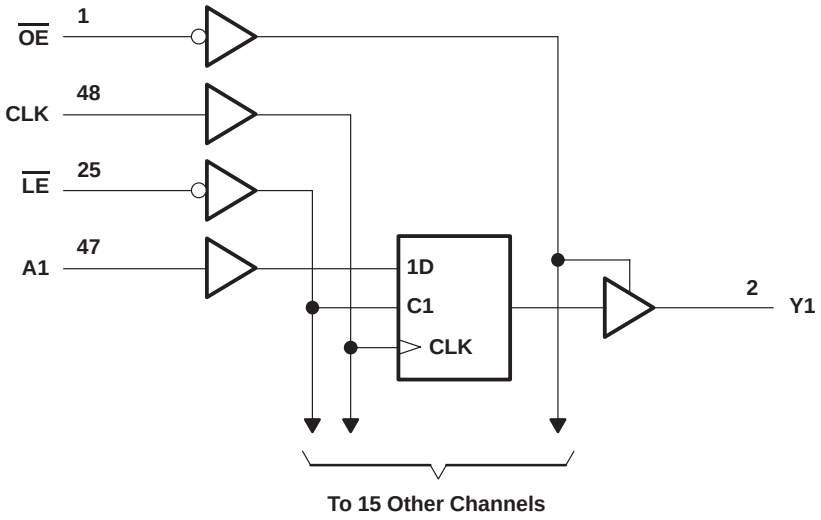


Figure 3. Logic Diagram for SN74ALVC16334 and SN74ALVC162334 Devices

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The SN74ALVC16835 and SN74ALVC162835 devices are 18-bit universal bus drivers with 3-state outputs, designed for 2.3-V to 3.6-V V_{CC} operation (see Table 3 and Figure 4). When LE is high, the device operates in the transparent mode and the Y outputs follow the A inputs. If CLK is held in a high or low state, the device operates like a D-type latch, and the Y output data is latched when LE is taken low. If CLK is clocked when LE is low, the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by the $\overline{OE}$. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled. The SN74ALVC162835 also provides 26-Ω equivalent series resistors on the output port.

Table 3. Function Table for SN74ALVC16835 and SN74ALVC162835 Devices

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	Y_0†

† Output level before the indicated steady-state input conditions were established.

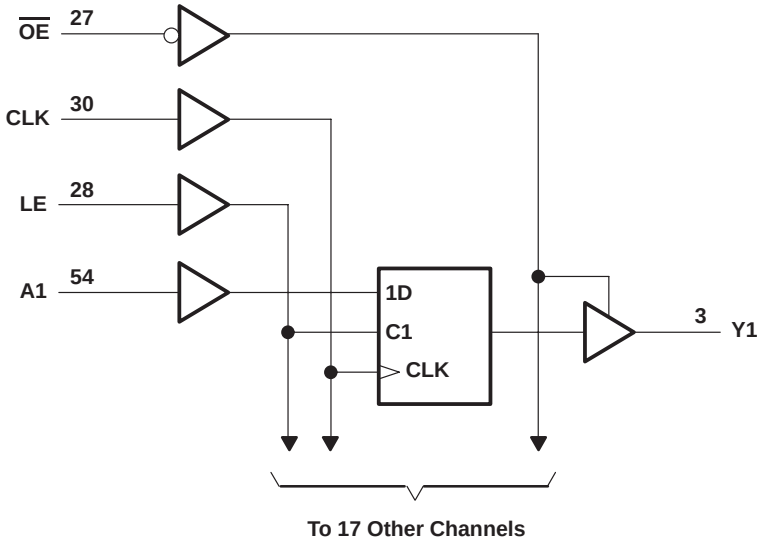

Figure 4. Logic Diagram for SN74ALVC16835 and SN74ALVC162835 Devices

The SN74ALVC162836 device is a 20-bit universal bus driver with 3-state outputs, designed for 2.3-V to 3.6-V V_{CC} operation (see Table 4 and Figure 5). When $\overline{LE}$ is low, the device operates in the transparent mode and the Y outputs follow the A inputs. If CLK is held in a high or low state, the device operates like a D-type latch, and the Y output data is latched when $\overline{LE}$ is taken high. If CLK is clocked when $\overline{LE}$ is high, the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by $\overline{OE}$. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled. The SN74ALVC162836 also provides 26-Ω equivalent series resistors on the output port.

Table 4. Function Table for SN74ALVC162836 Device

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L	X	Y_0†

† Output level before the indicated steady-state input conditions were established

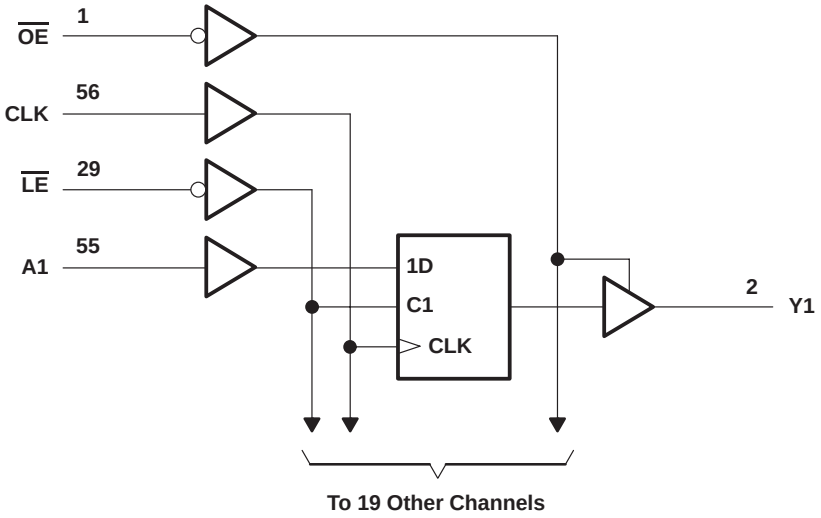

Figure 5. Logic Diagram for SN74ALVC162836 Device

The logic functionality of these devices is similar with one exception: the polarity of the latch-enable input. The ’835 function uses an active-high latch-enable control input, while the ’334 and ’836 functions use an active-low latch-enable control input. The latch-enable input is controlled, in the DIMM application, by the register enable (REGE) signal from the motherboard. REGE, when low, permits the DIMM to operate in the buffered mode. When REGE is high, the DIMM operates in the registered mode. REGE performs the logical-inverse function of the LE signal. To utilize an ’835-type device, an inverter is necessary between the DIMM’s REGE pin and the ’835 IC’s LE pin (see Figure 6). The SN74AHC microgate, packaged in the plastic small-outline transistor (SOT) package, is an ideal single-gate device for the inverter application. When utilizing the ’334- and ’836-type devices, the $\overline{\text{LE}}$ control input performs the *same* logical function as the REGE signal, and therefore, no inverter is necessary (see Figure 7). The elimination of an inverter from the DIMM by the choice of a ’334- or ’836-type device saves board space, simplifies board layout and trace routing, decreases costs, and increases the reliability of the DIMM. The use of the ’334 furthers these benefits by utilizing a 48-pin package, as opposed to the 56-pin package.

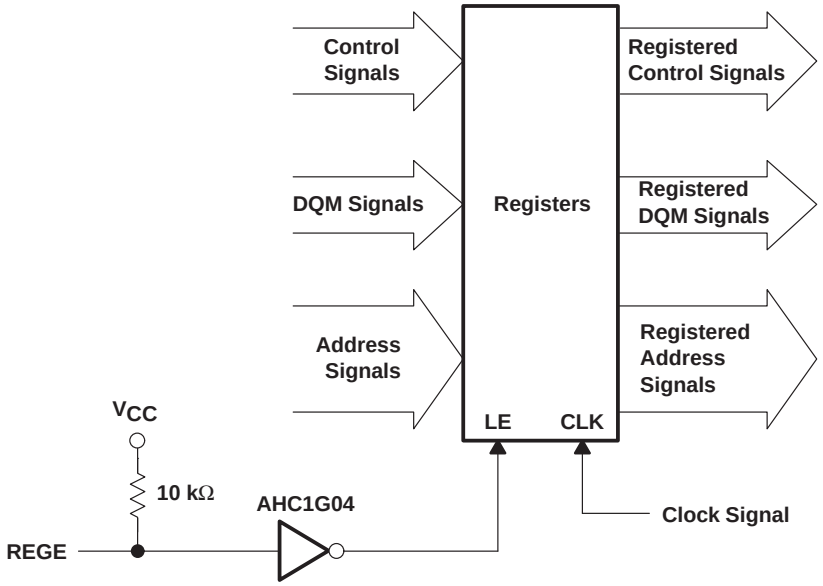

Figure 6. Inverted REGE Wiring for SN74ALVC16835 and SN74ALVC162835 Devices

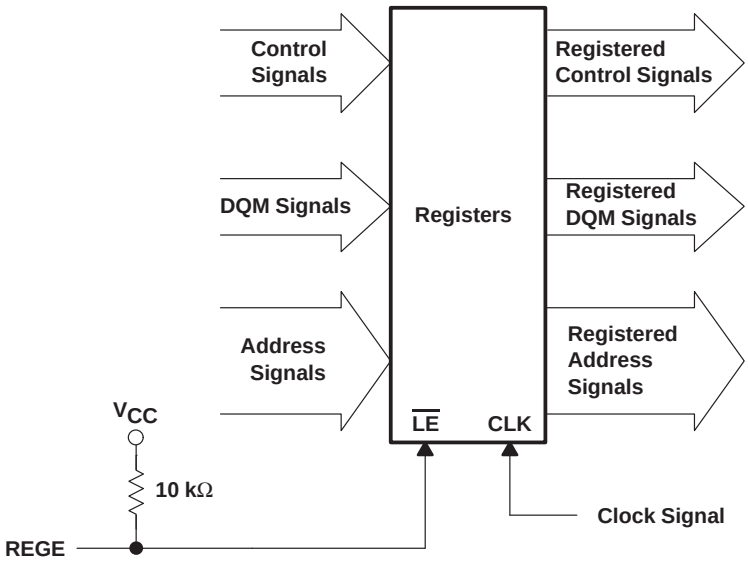

Figure 7. Straight-In REGE Wiring for SN74ALVC16334, SN74ALVC162334, and SN74ALVC162836 Devices

The bit density of the buffer/register IC should be considered when selecting a device for a DIMM design. The use of ICs with bit densities that result in the least number of unused inputs results in the most economical and optimal design.

The 64-MB DIMM has 28 signals that must pass through the buffer/register. The use of two 18-bit devices, like the ’835, results in eight unused bits; this is not an optimal solution. The use of two 16-bit devices, like the ’334, on the 64-MB DIMM would result in only four unused bits. While not an ideal bit density for the application, it represents a significant improvement (see Figure 8).

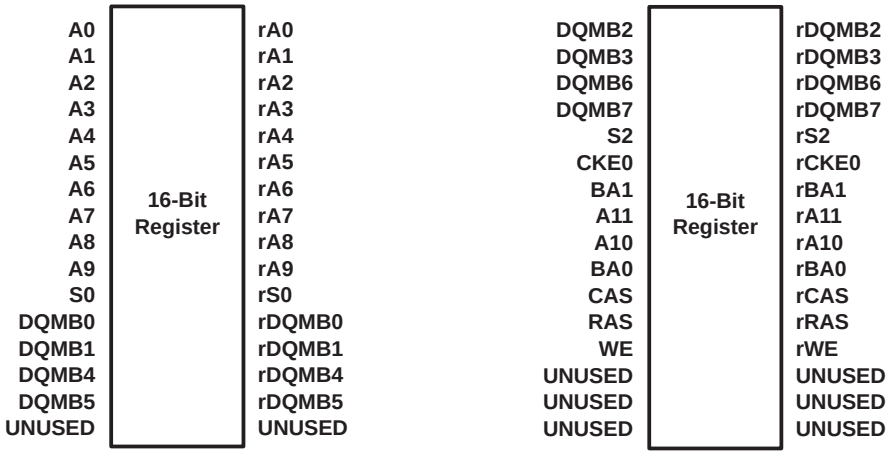

Figure 8. 64-MB DIMM Register Wiring

The 128-MB DIMM has 29 signals that must pass through the buffer/register. The use of two 18-bit devices, like the ’835, results in seven unused bits. The use of two 16-bit devices, like the ’334, on the 128-MB DIMM, would result in only three unused bits (see Figure 9).

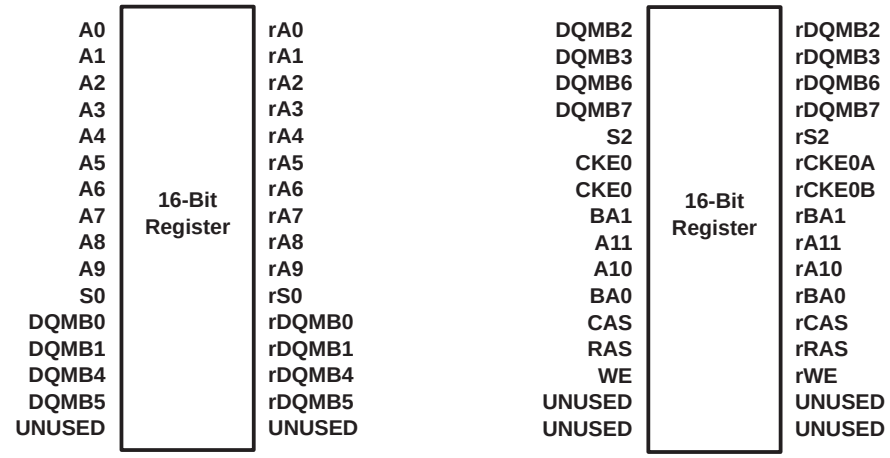

Figure 9. 128-MB DIMM Register Wiring

The 256-MB and 512-MB DIMMs have 50 signals that must pass through the buffer/register. The use of three 18-bit devices, like the ’835, results in four unused bits. The use of two 16-bit devices, like the ’334, and one 20-bit device, like the ’836, results in only two unused bits (see Figure 10).

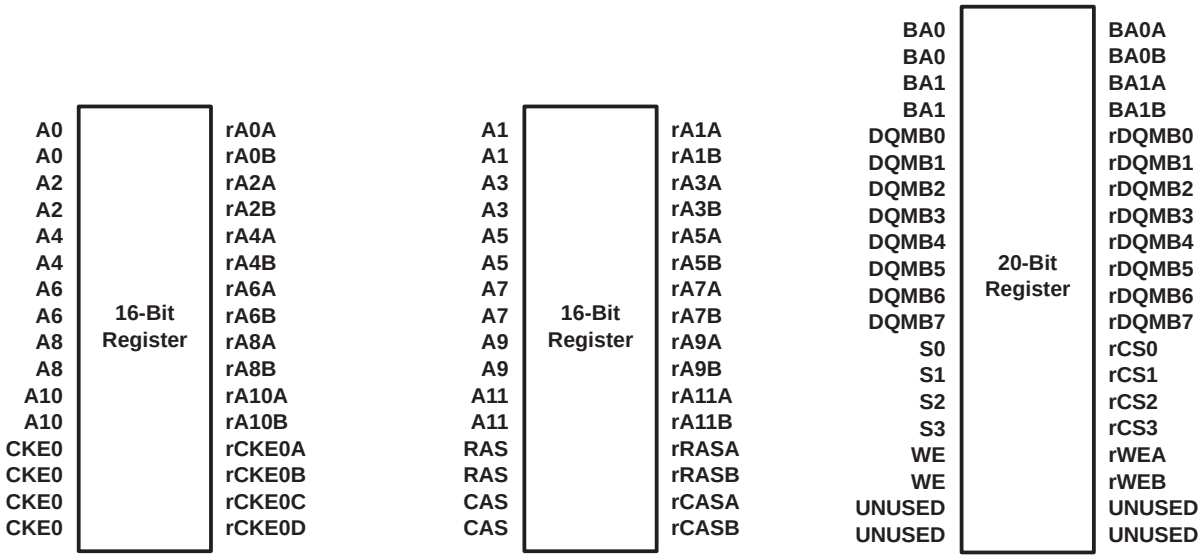

Figure 10. 256-MB and 512-MB DIMM Register Wiring

Minimizing the number of unused inputs becomes particularly important when considering the specifics of the DIMM application. Due to contention with the weak pullups in the output circuit of the memory controller, the buffer/register device *cannot* utilize bus hold on the inputs. Since unused CMOS inputs *must* be held at a valid logic high or low voltage, pullup or pulldown resistors are required on any unused buffer/register inputs.

Examination of the electrical characteristics of the outputs is a critical portion of a successful DIMM design. The output must have an output impedance that minimizes overshoots and undershoots for signal integrity. The selection of a component with equivalent 26-Ω series damping resistors on the output port is sometimes necessary to improve the impedance match with the distributed load of the DIMM. The opposing characteristic that must be considered is having sufficient drive to meet the timing requirements. Typically, in a CMOS totem-pole output structure, the p-channel pullup transistor is weaker than the n-channel pulldown transistor. Therefore, the factor to analyze with regard to output drive capability is I_{OH}, as the t_{PLH} time is the limiting factor to the device t_{pd}. The ’334 and ’836 devices have a p-channel output transistor that is almost twice as strong as the pullup output of the ’835 device. This results in much better overall electrical characteristics for this application. To aid the design engineer in analysis of electrical characteristics, TI makes IBIS models available on the Internet. The latest versions of IBIS models can be obtained from TI’s website, at http://www.ti.com.

Tables 5 through 9 show component specifications for products included in this report. Figures 11 through 15 show output characteristic comparisons to the Intel™ PC100 requirement

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Table 5. SN74ALVC16334 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC16334 V_{CC} = 3.3 V ± 0.3 V, T_A = –40°C to 85°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1	4.1	ns
I_I	$V_I = V_{CC}$ or GND			±5	µA

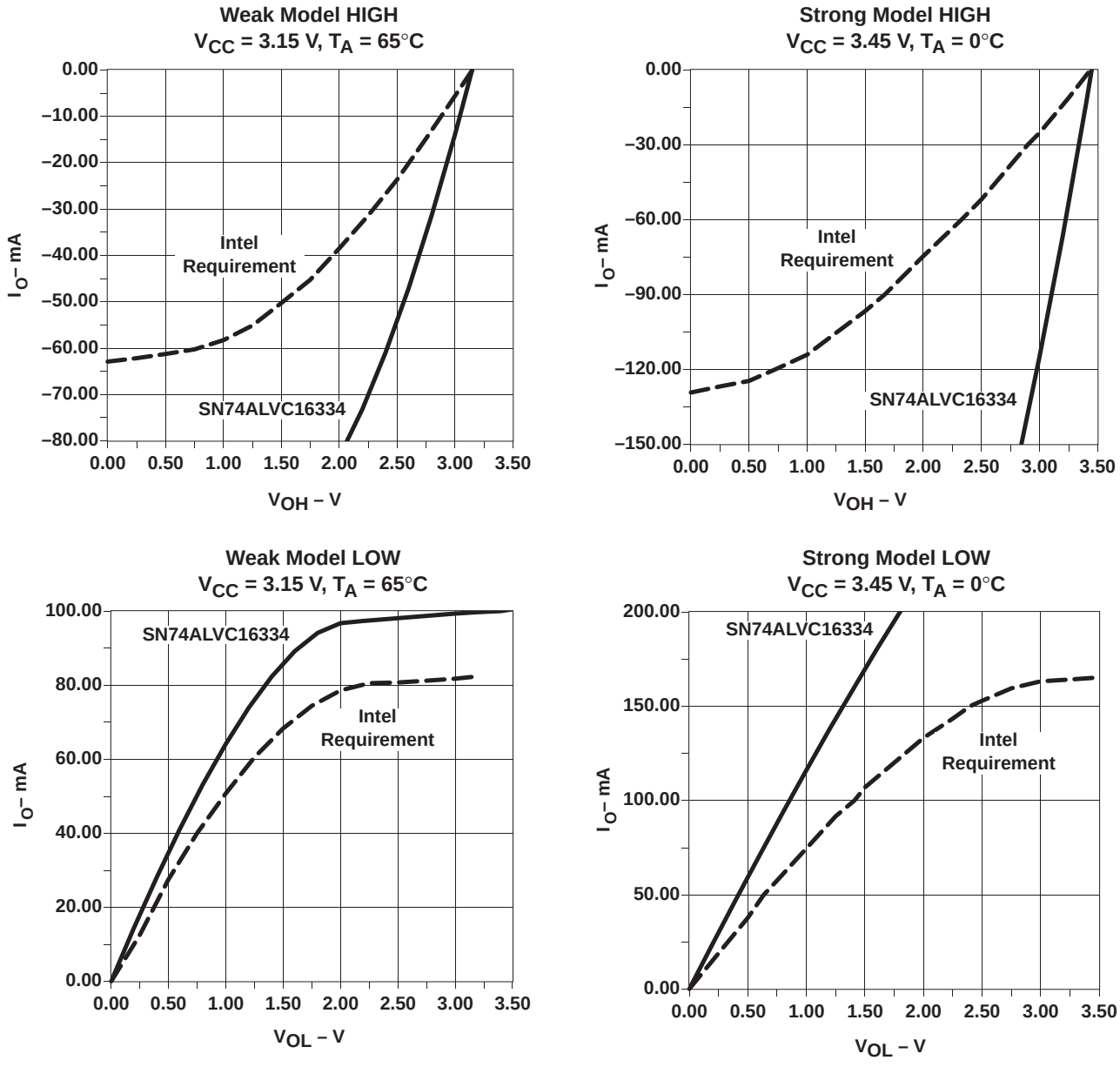


Figure 11. IV Characteristics for SN74ALVC16334 Register Output

Table 6. SN74ALVC162334 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC162334 V_{CC} = 3.3 V ± 0.3 V, T_A = –40°C to 85°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1	4.9	ns
I_I	$V_I = V_{CC}$ or GND			±5	µA

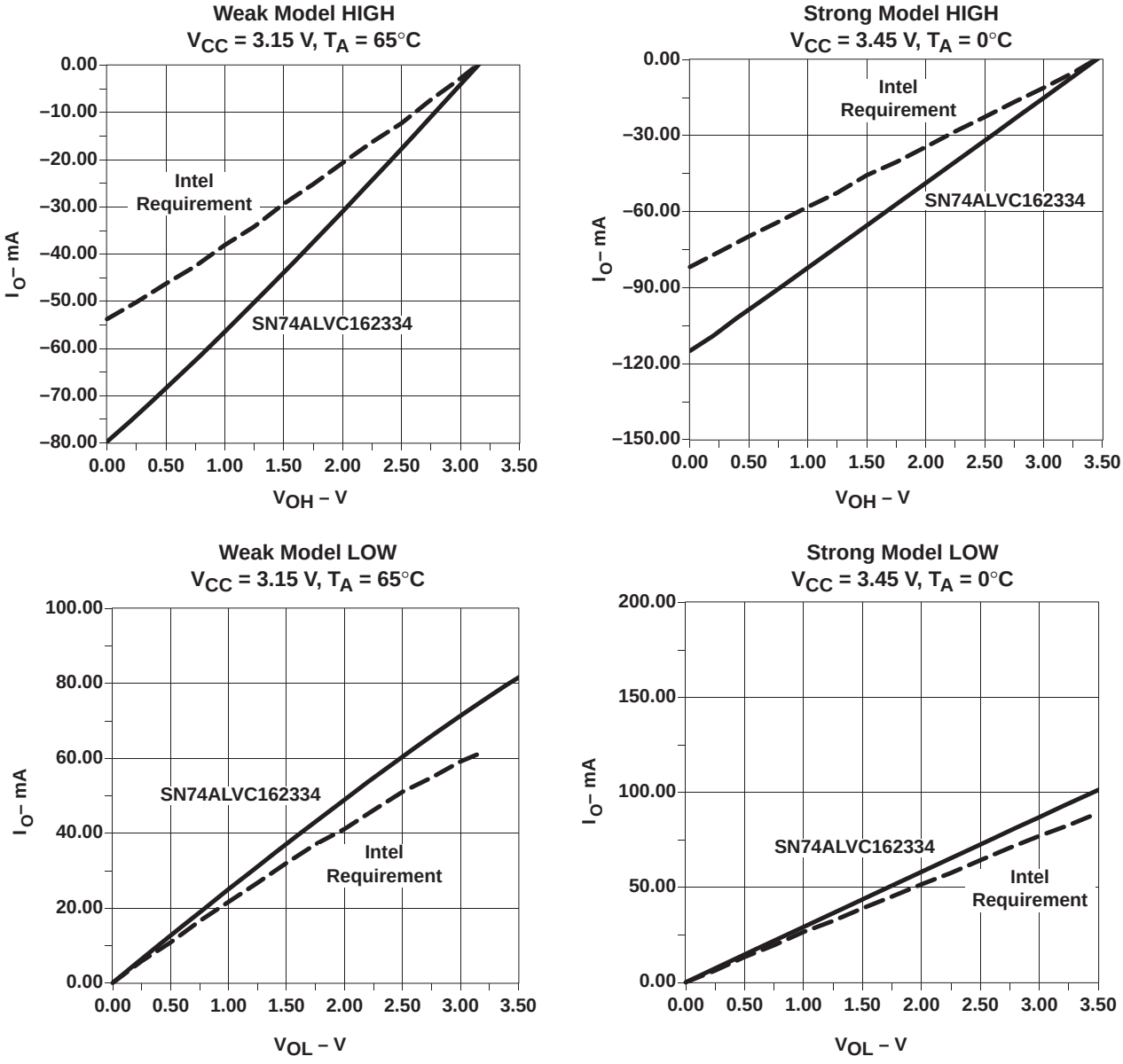


Figure 12. IV Characteristics for SN74ALVC162334 Register Output

Table 7. SN74ALVC16835 Component Specifications

PARAMETER	CONDITIONS		INTEL REQUIREMENTS V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C to 65°C		SN74ALVC16835 V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C to 65°C		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1.7	4.5	1.7	4.5	ns
I_I	$V_I = V_{CC}$ or GND			±10		±5	µA

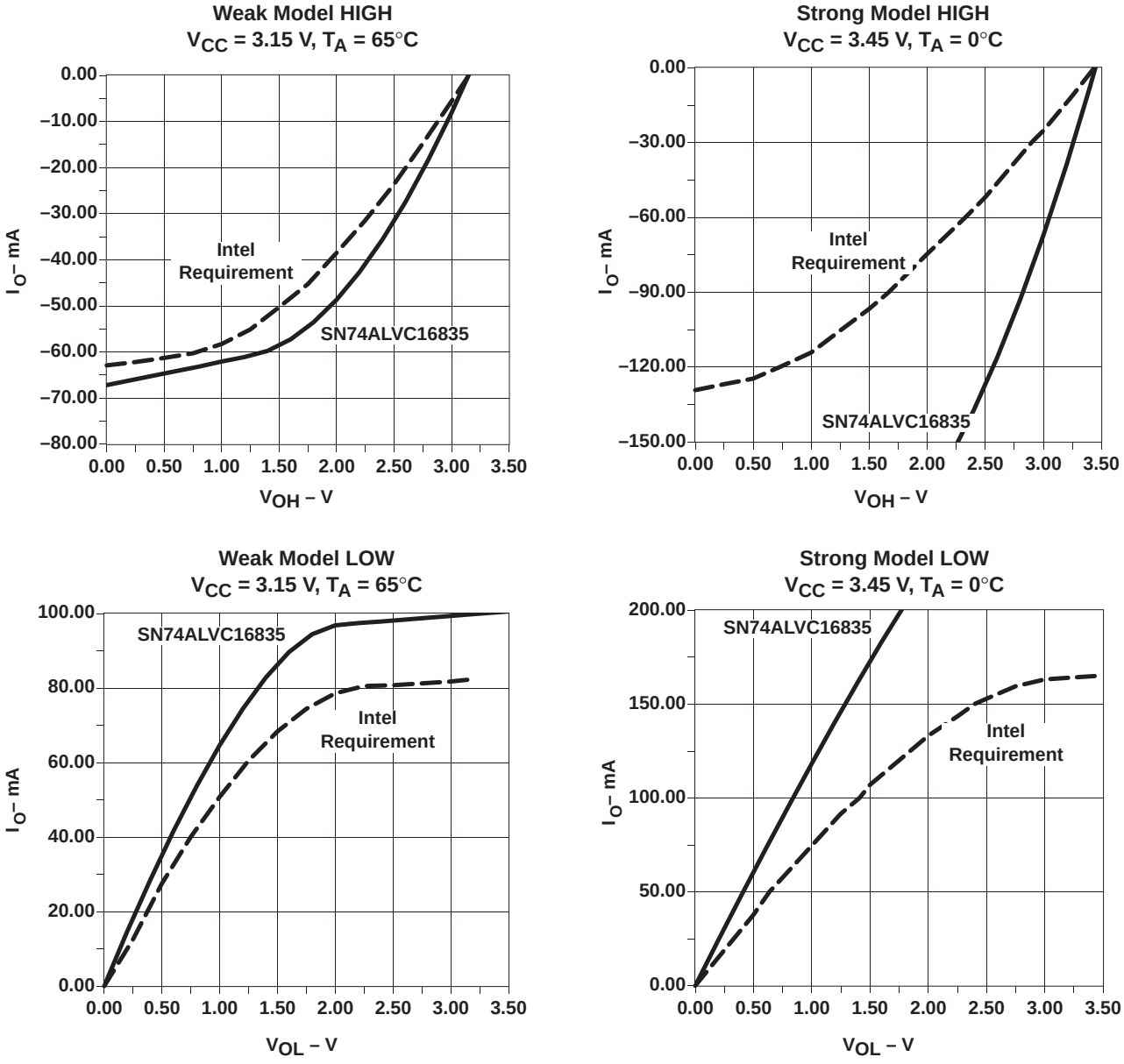


Figure 13. IV Characteristics for SN74ALVC16835 Register Output

Table 8. SN74ALVC162835 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC162835 V_{CC} = 3.3 V ± 0.15 V, T_A = –40°C to 85°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1.4	5.4	ns
I_I	$V_I = V_{CC}$ or GND			±5	µA

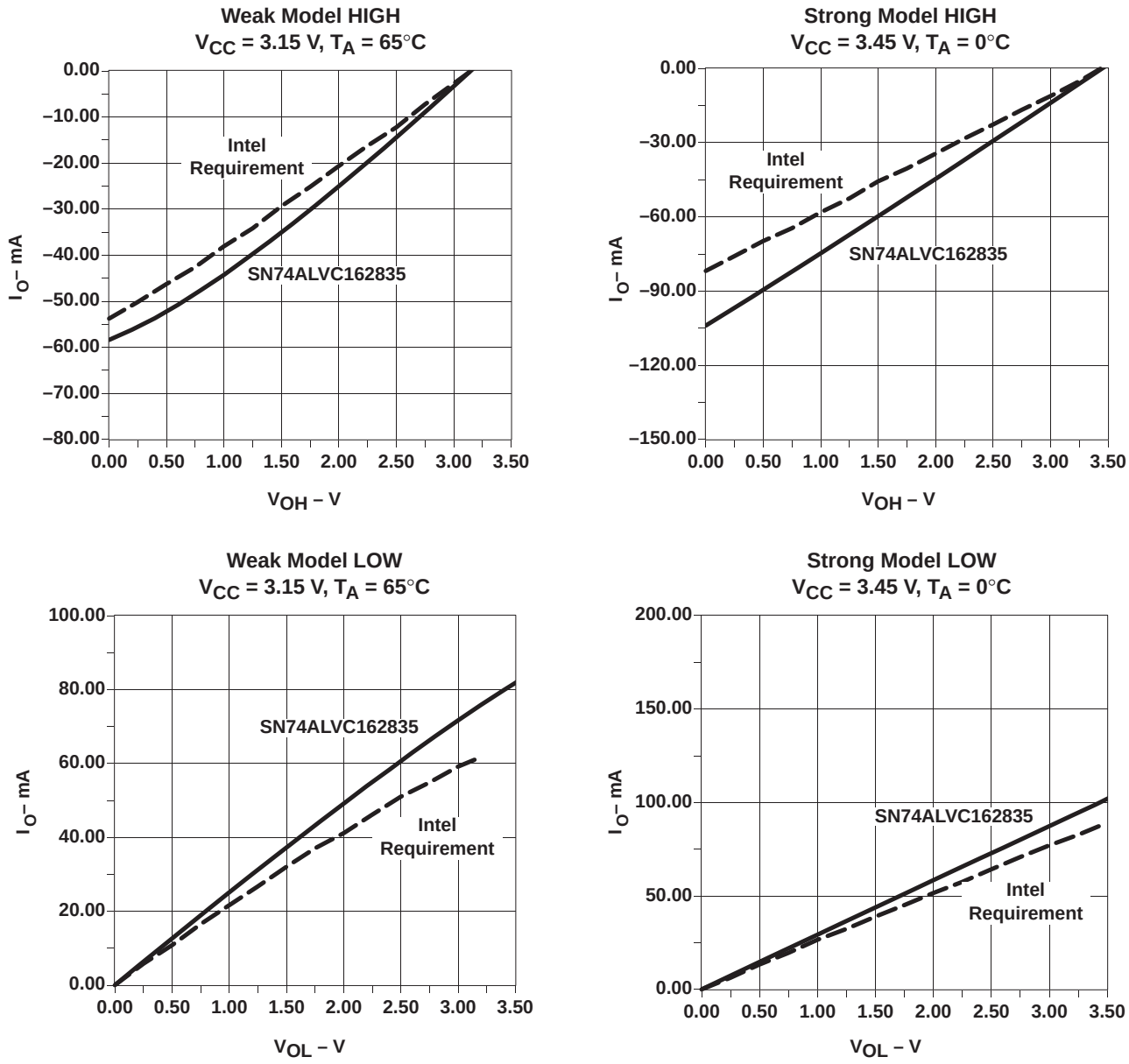


Figure 14. IV Characteristics for SN74ALVC162835 Register Output

Table 9. SN74ALVC162836 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC162836 V_{CC} = 3.3 V ± 0.15 V, T_A = –40°C to 65°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1.1	5	ns
I_I	$V_I = V_{CC}$ or GND			±5	µA

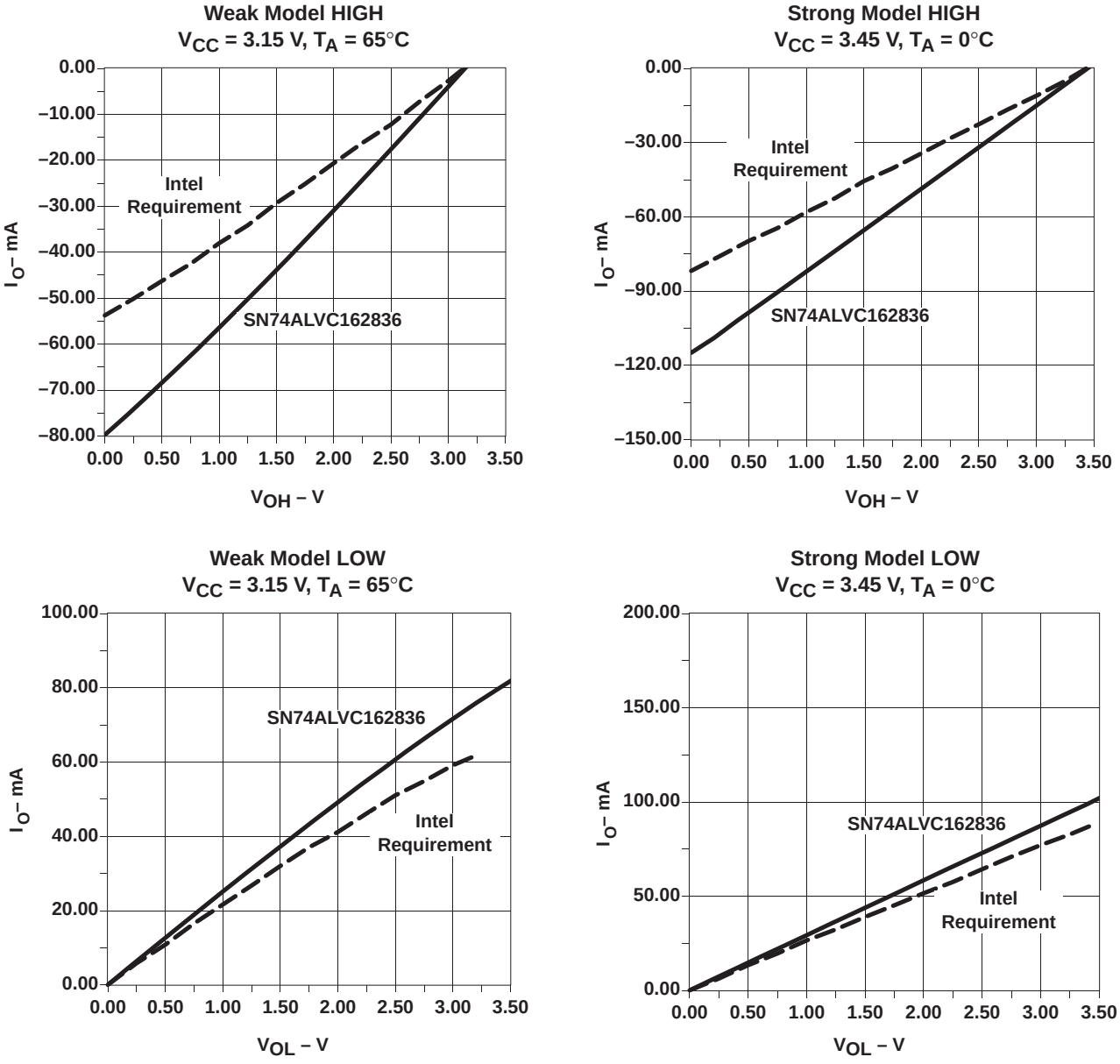
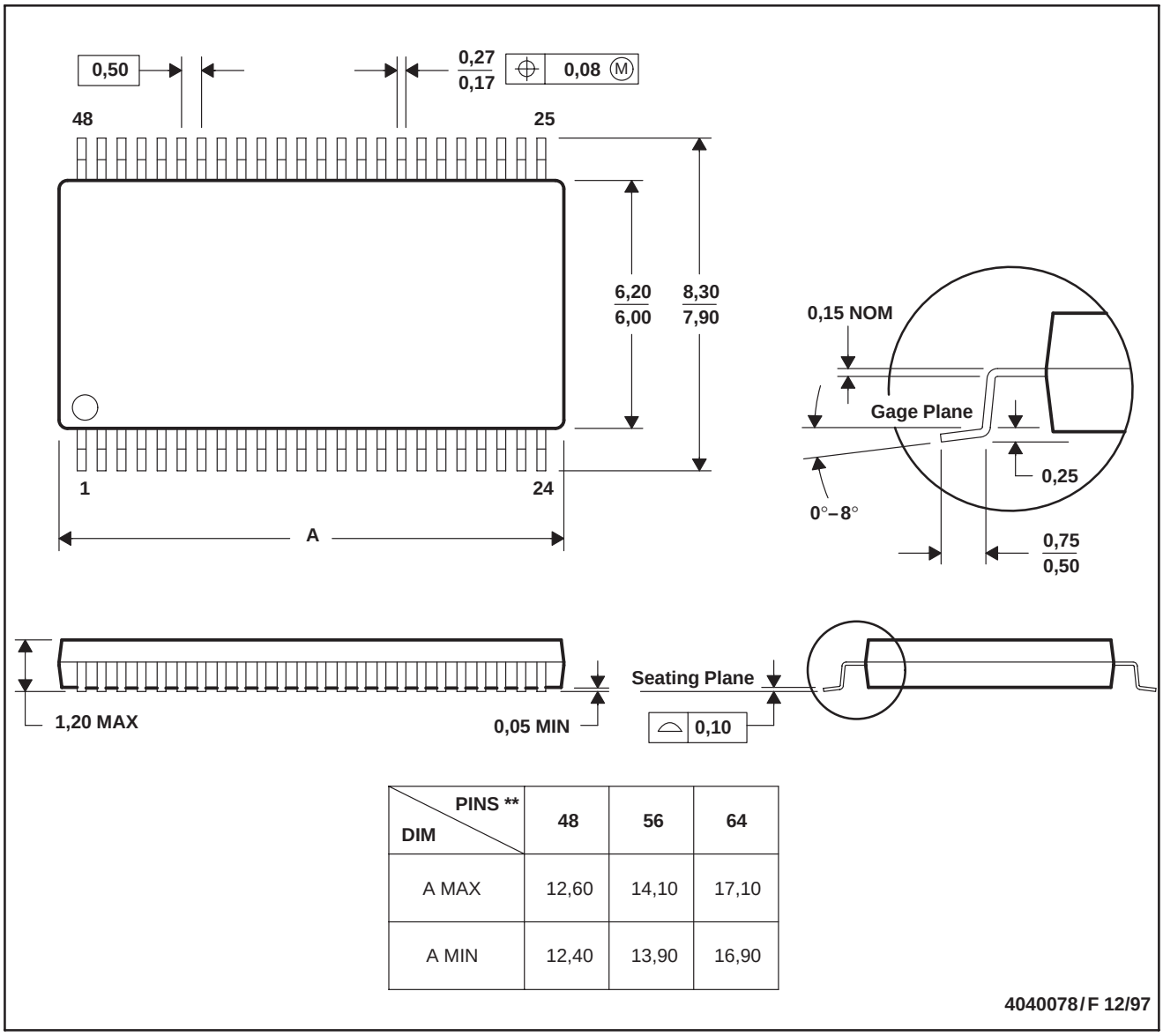


Figure 15. IV Characteristics for SN74ALVC162836 Register Output

All of the devices considered are available in the JEDEC standard SSOP (DL), TSSOP (DGG), and TVSOP (DGV) packages.[8] The mechanical data for the TSSOP (DGG) is shown in Figure 16.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion, which should not exceed 0,15.
D. Falls within JEDEC MO-153

Figure 16. Package Outline

Benefits of Alternative Solutions

Evaluating an alternative buffer/driver IC solution is a way of differentiating the DIMM design from the standard reference design to provide a competitive edge. Tables 10 and 11 include many of the factors to be considered.

Table 10. Features

DEVICE	PINS	BITS	LE LOGIC	SERIES RESISTOR
ALVC16334	48	16	$\overline{LE}$ = REGE	No
ALVC162334	48	16	$\overline{LE}$ = REGE	Yes
ALVC16835	56	18	LE ≠ REGE	No
ALVC162835	56	18	LE ≠ REGE	Yes
ALVC162836	56	20	$\overline{LE}$ = REGE	Yes

Table 11. Benefits

DEVICE	DRIVE	EXTERNAL LOGIC	SERIES-DAMPING RESISTOR	UNUSED INPUTS
ALVC16334	High	No added inverter cost	External resistor necessary for impedance match	Minimum pullups
ALVC162334	High	No added inverter cost	Better impedance match No external resistor cost	Minimum pullups
ALVC16835	Low	Added inverter cost	External resistor necessary for impedance match	Additional pullups
ALVC162835	Low	Added inverter cost	Better impedance match No external resistor cost	Additional pullups
ALVC162836	High	No added inverter cost	Better impedance match No external resistor cost	Minimum pullups

After reviewing the factors shown in Tables 10 and 11, the devices in Table 12 should be considered for application component selection.

Table 12. Application Component Selection

DIMM SIZE IN MEGABYTES	COMPONENT SELECTION
64	ALVC162334 × 2
128	ALVC162334 × 2
256	ALVC162334 × 2 + ALVC162836 × 1
512	ALVC162334 × 2 + ALVC162836 × 1

Differentiating the DIMM design from the standard reference design by considering the components listed in Table 12 can help provide a more cost-effective design. By choosing a component that has improved matching of bit density to the number of signals to be buffered/registered, a number of pullup resistors can be eliminated from the board. By choosing a component that uses an $\overline{LE}$ control input, which logically is the same as the REGE signal, an inverter can be eliminated from the design. These improvements save board space, simplify board layout and trace routing, decrease costs, and increase the reliability of the DIMM. Selecting a component with improved output drive characteristics simplifies the design engineer's job of ensuring signal integrity and meeting timing requirements.

Conclusion

The PC100 design originated before the availability of the SN74ALVC16334, SN74ALVC162334, and SN74ALVC162836 devices. The SN74ALVC16835 and SN74ALVC162835 were the only parts available that fit the application at the start of the project. TI has since offered these additional components for use in the PC SDRAM registered DIMM. With respect to performance, cost effectiveness, and design optimization, the ’334, ’2334, and ’2836 devices represent an optimal choice over the ’835 and ’2835.

Glossary

A

ALVC Advanced low-voltage CMOS

C

CMOS Complementary metal-oxide semiconductor

D

DIMM Dual in-line memory module

DQM Data mask

E

ESD Electrostatic discharge

I

I_I Input current

I_{OH} High-level output current

IV Current vs. voltage

J

JEDEC Joint Electronic Device Engineering Council

L

LE Active-high latch enable

$\overline{LE}$ Active-low latch enable

P

PC Personal computer

R

REGE Register enable

S

SDRAM Synchronous dynamic random-access memory

SOT Small outline transistor

T

TI™ Texas Instruments Incorporated

t_{pd} Propagation delay time

t_{PLH} Propagation delay time, low-to-high level output

TSSOP Thin shrink small-outline package

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