Application Report
SNAA036B–January 2007–Revised May 2013

AN-1558 Clocking High-Speed A/D Converters

ABSTRACT

Extremely high-speed ADCs (>1 GSPS) demand a low-jitter sample clock in order to preserve signal-to-noise ratio (SNR). These 8- and 10-bit converters have best-case noise floors set by quantization noise. For an N-bit ADC sampling a full-scale sinusoid, the well known expression for SNR (in dB) is: SNR = 6.02N + 1.76. This sets the best case noise floor for an 8-bit ADC at −49.9 dBc. The noise floor degrades from this point due to factors such as jitter on the sample clock, intrinsic aperture jitter of the ADC, spurious components arising from non-linearities in the ADC quantizer, and other internal noise such as thermal noise. In this article, we look at the strategy for optimizing the performance of the sample clock based on PLL/VCO characteristics. This means minimizing overall integrated phase noise, which minimizes clock jitter.

Contents

List of Figures

List of Tables

1 Overview

The root-mean-square (RMS) jitter of the sample clock combines with the intrinsic RMS aperture jitter of the ADC in a root-sum-square fashion to produce a total affective jitter. Total RMS jitter is:

$$\sigma_T = \sqrt{\sigma^2_{Clk} + \sigma^2_{aperture}} \tag{1}$$

The SNR due to total jitter is:

$$SNR_{dB} = 20 \bullet \log\left(\frac{1}{2\pi f_{in}\sigma_T}\right) = 20 \bullet \log\left(\frac{1}{2\pi f_{in}\sqrt{\sigma^2_{Clk} + \sigma^2_{aperture}}}\right) \tag{2}$$

Solving for the maximum allowable clock jitter given some target SNR and ADC aperture jitter:

$$\sigma_{Clk} = \sqrt{\frac{1}{(2\pi f_{in})^2 \bullet 10^{\frac{SNR}{10}}} - \sigma^2_{aperture}} \tag{3}$$

The aperture jitter specification for Texas Instruments ADC08D1500 8-bit, 1.5 GSPS converter is 400 femtoseconds (fs.). Using this value and a maximum input frequency of 748 MHz (f_{IN}), Table 1 lists the allowable sample clock jitter for target SNR due to total jitter.

Table 1. Jitter SNR and Allowable Clock Jitter, With Total SNR

Target Jitter SNR (dB) (Aperture Jitter and Clock Jitter)	Allowable Clock Jitter (fs.)	Total SNR Due to Quantization Noise and Jitter (dB) $SNR = 10 \log\left(\frac{1}{\frac{1}{10^{\frac{SNR_J}{10}}} + \frac{1}{10^{\frac{SNR_Q}{10}}}}\right)$ (4)
54	142	48.5
53	259	48.2
52	354	47.8
51	447	47.4
50	541	46.9
49	640	46.4
48	747	45.8
47	862	45.2
46	989	44.5

The third column of Table 1 shows the combined SNR due to quantization noise and jitter for an 8-bit ADC, using a quantization noise SNR of 49.9 dB.

The allowable jitter (column 2) required to achieve a total SNR that is close to 49.9 dB is extremely difficult to achieve at a reasonable cost. However, achieving RMS clock jitter below 500 fs is possible using TI's LMX2531LQ1500E frequency synthesizer combined with a high quality crystal reference oscillator. The LMX2531LQ1500E is shown in Figure 1.

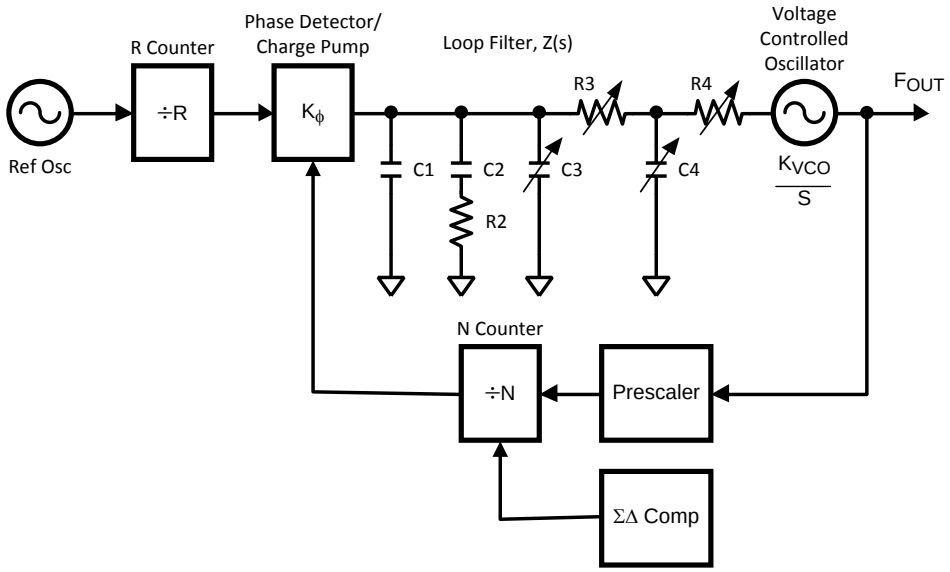

Figure 1. LMX2531LQ1500E Block Diagram

For this example, use the LMX2531LQ1500E to generate a fixed 1.5 GHz sample clock that can drive any of TI's GSPS ADCs. Because the ADC clock is fixed, you can design the loop filter to achieve optimized phase noise performance, giving best jitter performance. Each functional block in Figure 1 contributes some form of noise. Table 2 lists the low and high frequency approximations for their noise transfer functions.

Table 2. Noise Transfer Functions, T(f)

Noise Source	Low Frequency Transfer Function Approximation	High Frequency Transfer Function Approximation
Reference Oscillator	N/R	G(s)
R Divider	N	G(s)
N Divider	N	G(s)
Phase Detector	N/KΦ	G(s)

G(s) is the forward transfer function:

$$G(s) = \frac{K_{\phi} \bullet K_{VCO} \bullet Z(s)}{s} \tag{5}$$

Optimizing the PLL noise bandwidth means minimizing the following integral for each noise path through the PLL:

$$\int_{f1}^{f2} S_N(f) \bullet |T(f)|^2 \, df \tag{6}$$

Sn(f) represents the specific noise source PSD and T(f) the noise transfer function. Using the approximations for T(f) from Table 2 gives us guidance for choosing the PLL parameters that optimize noise performance:

- Maximize the phase comparator charge pump gain (Kf) to minimize the noise contribution of the phase detector (up to a point).
- The N-divider and R-divider noise contributions are proportional to the value of N2. Choose a phase comparator frequency that results in the smallest possible integer value for N, subject to the maximum phase detector frequency.
- Choose a low noise reference oscillator at the compare frequency, or an integer multiple of the compare frequency. A multiple of the compare frequency provides additional benefit by reducing reference noise.
- Designing the loop filter to have a phase margin of approximately 80 degrees flattens its response and suppresses VCO noise near the loop bandwidth.

The final task is to design the loop transfer function T(f) subject to minimizing Equation 6 for each noise source, which is extremely difficult without the aid of automated tools. TI's Web-based design environment WEBENCH® features its EasyPLL tool that assists the user in selecting a PLL/VCO, entering design parameters, selecting loop components, and running simulations to test the design.

Using EasyPLL, a 1.5 GHz sample clock was designed using the LMX2531LQ1500E and a 60 MHz crystal oscillator as a reference, with the following final design parameters:

- F_{OSC} = 60 MHz, with phase noise = −158 dBc at 10 kHz offset.
- Compare frequency = 30 MHz, R = 2, N = 50
- 2nd order loop filter, C1= 220 pF, C2 = 150 nF, R2 = 1.0 kΩ, C3=C4=R3=R4=0.
- Loop bandwidth = 22.85 kHz
- K_{Φ} = 1.26 mA

These values resulted in a clock with only 401 fs of jitter (100 Hz to 20 MHz bandwidth).

Figure 2 shows the single-sideband phase noise plot of the clock.

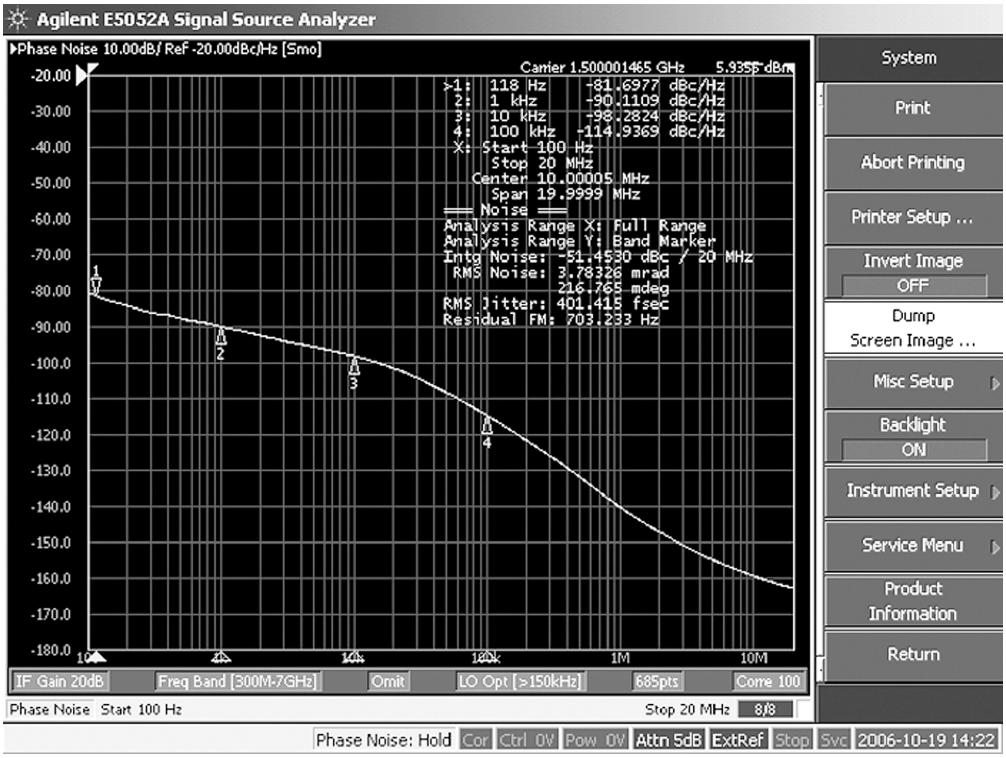

Figure 2. Single-Sided Phase Noise Plot of a 1.5 GHz ADC Clock

2 References

Dean Banerjee, *PLL Performance: Simulation and Design,* 4th Edition, Dogear Publishing, Indianapolis, 2006.

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