ADC12DL065,LMH6550

A Walk Along the Signal Path (High-Speed Signal Path)

Literature Number: SNAA120

SIGNAL PATH designer℠

Expert tips, tricks, and techniques for signal-path designs

No. 101

A Walk Along the Signal Path

— By Kurt Rentel and Juergen Kuehnel

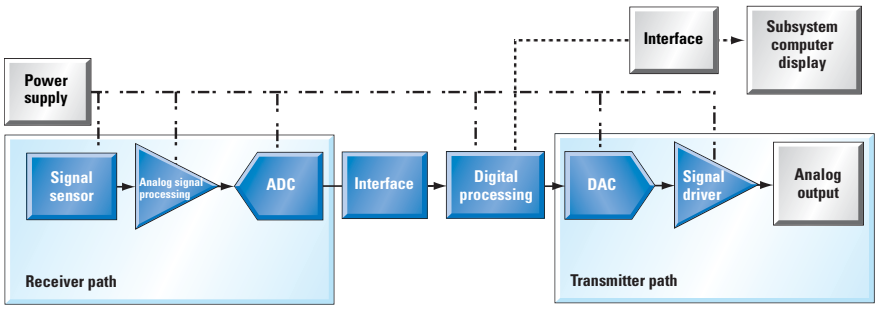


Figure 1. Generic signal path

When designing a high-speed mixed-signal system, it is good engineering practice to evaluate the block-level signal fidelity through the entire chain step by step. This premier issue of *Signal Path Designer* focuses on the design of an input or receiver path. The transmitter or output path will be discussed in a future issue. A typical receiver or measurement system is composed of a signal sensor, analog signal processing block, data converter, interface, and digital processing block (*see Figure 1*). Only the analog and mixed-signal portions of the design will be addressed here. Each signal-path block must be carefully selected to achieve desired results.

System performance requirements

System performance requirements must be translated into the specifications of the key signal-path components to achieve the best tradeoffs between performance, power consumption, size, and ease of use. This article will walk through a step-by-step design of a typical receiver system that has two signal paths (*see Figure 2*). Each path begins with a sensor operating at frequencies from DC to 27 MHz and has a single-ended 200Ω output. Sensor signal amplitudes range from 2 mVpp to 1 Vpp and unwanted high-frequency interference is present on both channels. System requirements dictate that minimum signals must be at least 6 dB higher than the system noise for proper signal processing and that maximum signals should not be clipped anywhere in the signal path. As is often the case, power consumption of the design should be minimized.

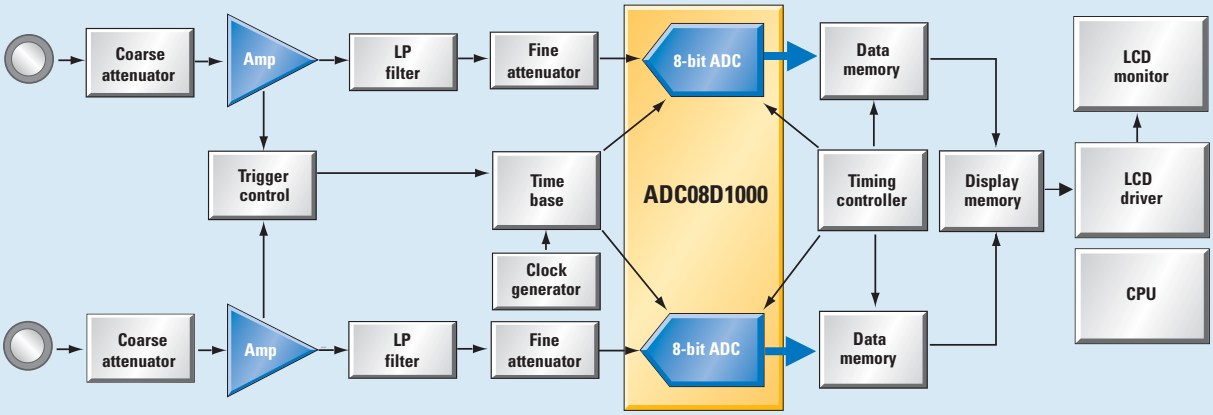
NEXT ISSUE:

Maximizing Signal-Path Performance

National Semiconductor
The Sight & Sound of Information

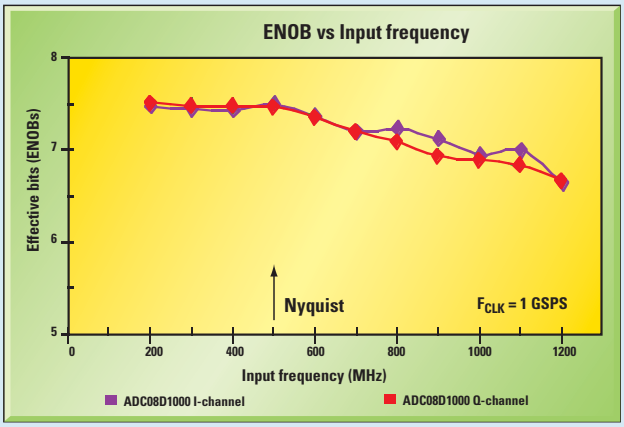
High-Performance Test and Measurement Solution

Simplified oscilloscope



NEW! ADC08D1000 Performance (typical):

- 7.5 Effective number of bits (ENOB) at Nyquist
- Bit error rate 10^{-18}
- DNL ± 0.25 LSB
- Crosstalk -71 dB
- Operating power of only 1.6W



ADC08D1000 Features:

- Interleaving mode enables up to 2 GSPS operation
- Choice of single or dual data rate output clocking
- Multiple ADC synchronization capability
- Demultiplexed LVDS outputs simplify data capture

Other pin-compatible members of National's ultra-high speed 8-bit family include:

- ADC081000 (Single 8-bit 1 GSPS)
- ADC08D500 (Dual 8-bit 500 MSPS)

High-speed amplifiers and comparators for test and measurement

Part number	Type	SSBW (MHz, A_V = 1)	Slew rate (V/µs, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (dBc)	Voltage noise (nV/√Hz)	Package
NEW! LMH6550	Fully differential ADC driver with disable	400	3000	20.0	-92 / -103 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! LMH6551	Fully differential ADC driver	370	2400	12.5	-94 / -96 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! LMH6702	Ultra-low distortion CFB op amp	1.7 GHz[1]	3100[1]	12.5	-63 / -70 at 60 MHz, R_L=100Ω	1.8	SOIC-8, SOT23-5
NEW! LMH6574	4:1 Mux, -70 dB crosstalk	500[1]	2200	13.0	-65 / -86 at 5 MHz, R_L=100Ω	5.0	SOIC-14
Part number	**Type**	**Resonse time (ns)**	**Rise/ Fall times**	**I_{CC} (mA/ch)**	**CMVR**	**Output config**	**Package**
LMV7219	7 ns, 2.7V to 5V comparator w/ RRO	7	1.3 ns	1.1	-0.2V to 3.8V	Push-pull	SC70-5, SOT23-5

[1] A_V = +2

A Walk Along the Signal Path

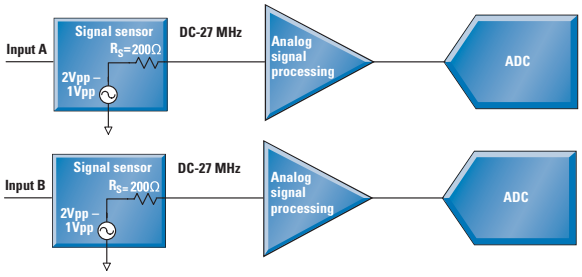


Figure 2. Two signal-path receiver system

Selecting the ADC

With the system specifications in hand, designers can begin working on the heart of the input signal path — the analog-to-digital converter (ADC). Key specifications for high-speed ADCs are bits or resolution and sample rate. Since the signal has a dynamic range of 2 mVpp to 1 Vpp or 54 dB and the minimum signal must be at least 6 dB above the noise level of the ADC, the ADC needs a minimum signal-to-noise-ratio (SNR) of 60 dB (54 dB + 6 dB). Theoretically, a 10-bit ADC can have 62 dB SNR, which would meet this requirement. However, 10-bit ADCs don't achieve this theoretical limit. In addition, other components in the chain will contribute noise to the system. Designers will also want to keep the ADC input signal smaller than full scale, which helps eliminate the risk of overdrive. With all of this in mind, a 12-bit converter that can provide 68 to 70 dB SNR is a good choice.

With the ADC resolution set at 12 bits, sample rate selection is the next step. For an input signal from DC to 27 MHz, a sample rate of at least 54 MSPS is needed. This allows the full signal frequency range to be digitized by the ADC with no undesired aliasing or folding of signals to frequencies where they might be misinterpreted. This frequency folding or aliasing is discussed in many textbooks and application notes on ADCs and sampling.

Looking at the system requirements, there are two other considerations for the ADC. The system has two channels, making a dual ADC beneficial and minimum power consumption is desired. The target ADC specifications are 12-bit resolution, greater than 54 MSPS sample rate, low power consumption, and a dual format. A part that meets these targets is the ADC12DL065, a 12-bit, 65 MSPS, dual ADC with 69 dB SNR and very low (360 mW) power consumption.

The ADC12DL065 has other specifications that are important to note as the rest of the signal path is designed. First are the ADC's input characteristics. Its full-scale differential input range is 2 Vpp, common-mode input voltage is 1.5V and input capacitance is 8 pF (*see Figure 3*). Looking at AC specifications for the ADC12DL065, it has excellent SNR and has a spurious-free dynamic range (SFDR) of 85 dB at 30 MHz, ensuring that spurious tones produced by the ADC will be much smaller than desired signals. Another consideration in dual ADCs is the interaction between the two channels; the ADC12DL065 has 90 dB rejection of signals from one ADC input to the other, so that the signals on one channel do not interfere with signals on the other.

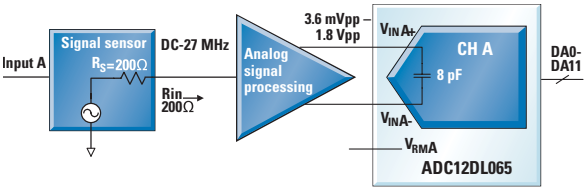


Figure 3. Input "A" signal-path receiver system

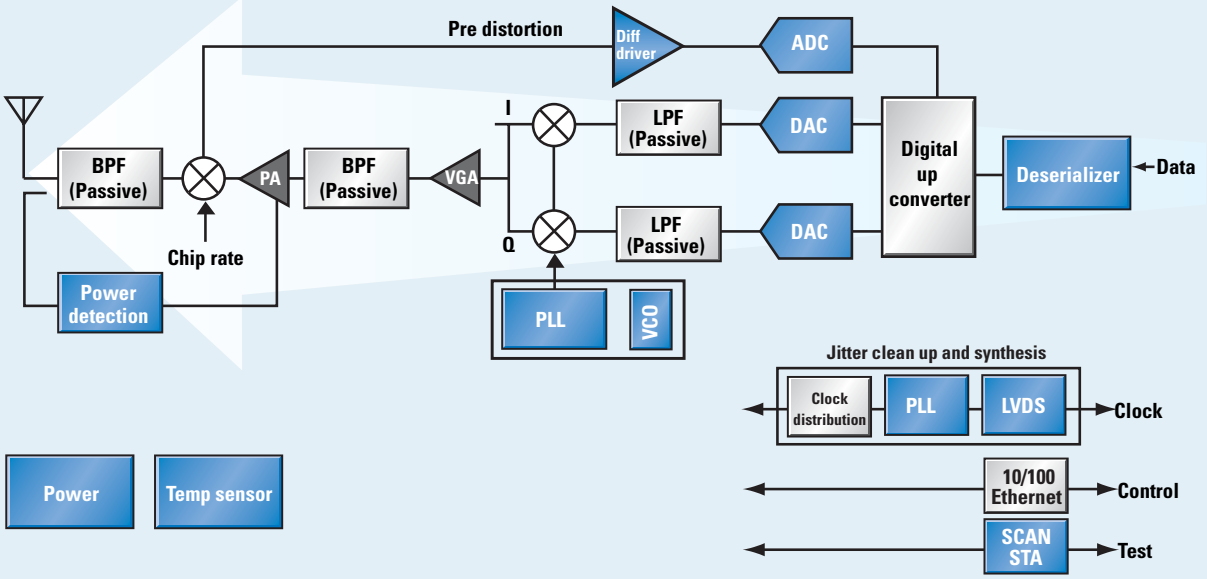
The analog signal conditioning block

Next, the analog signal conditioning block should be designed to complement the performance of the ADC. Functions in this key block are filtering to remove unwanted high-frequency signals, impedance matching for the sensor outputs, conversion from the sensor's single-ended signals to the ADC's differential signals, amplification to match signal levels to the ADC input range, and level shifting to match the ADC common-mode input level. The designer should select components to minimize the component count in this block.

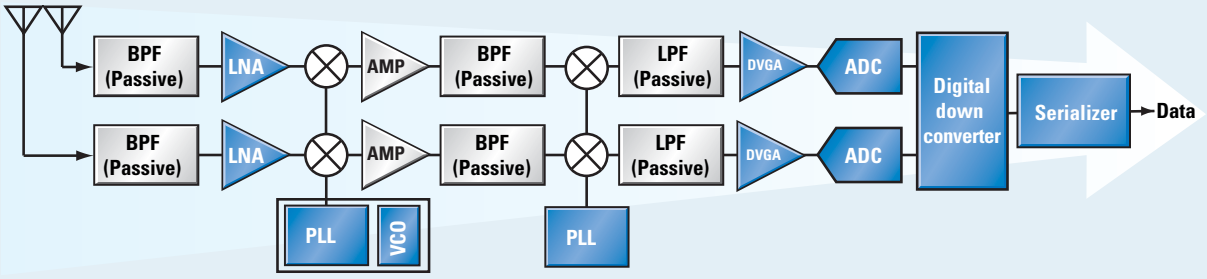
Because there are high-frequency signals that need

Signal-Path Solutions for Communications

Wireless basestation transmitter



Wireless basestation receiver



High-speed amplifiers for communications

Product ID	Type	SSBW (MHz, A_V = 1)	Slew rate (V/µs, A_V=1)	I_{CC} (mA/ch)	2nd/3rd HD (dBc)	Voltage noise (nV/√Hz)	Package
NEW! **LMH6550**	Fully differential ADC driver w/ disable	400	3000	20.0	-92 / -103 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6551**	Fully differential ADC driver	370	2400	12.5	-94 / -96 at 5 MHz, R_L=800Ω	6.0	SOIC-8, MSOP-8
NEW! **LMH6703**	1.2 GHz low distortion op amp w/shutdown	1.2 GHz[2]	4200[2]	11.0	-69 / -90 at 20 MHz, R_L=100Ω	2.3	SOIC-8, SOT23-6
NEW! **LMH6704**	650 MHz programmable gain buffer w/shutdown	650[2]	3000	11.5	-62 / -78 at 10 MHz, R_L=100Ω	9.3	SOIC-8, SOT23-6
LMH6502	Linear in dB, variable gain amplifier	130[1]	1800[1]	27.0	-55 / -57 at 20 MHz, R_L=100Ω	7.7	SOIC-14, TSSOP-14
LMH6503	Linear in V/V, variable gain amplifier	135[1]	1800[1]	37.0	-60 / -61 at 20 MHz, R_L=100Ω	6.6	SOIC-14, TSSOP-14
LMH6504	Linear in dB, variable gain amplifier	150[1]	1500[1]	11.0	-47 / -55 at 20 MHz, R_L=100Ω	4.4	SOIC-8, MSOP-8
CLC5526	Digitally controlled variable gain amplifier	350	—	48.0	-67 / -71 at 150 MHz, R_L=100Ω	2.2	SSOP-20

[1] A_V = +10 [2] A_V = +2

RF detection for communication

Product ID	Application	Detector	Channel	Range	Package
LMV227	CDMA 2000, WCDMA, UMTS	Log amp	1	40 dB, 2.1 GHz	Micro SMD, LLP®
LMV225/226/228	World phone, IMT 2000, UMTS	Log amp	1	40 dB, 2.1 GHz	Micro SMD, LLP
NEW! **LMV232**	3GPP2, World phone	Mean square	2	20 dB, 2.2 GHz	Micro SMD
LMV242/243	GSM/GPRS, TD_SCDMA_MC	Log amp	1	55 dB, 2.1 GHz	Micro SMD, LLP

Crosspoint switch

Part number	Description	Input compatibility	Output	Speed/Ch (Mbps)	Package	Comments
NEW! **SCAN90CP02**	2 x2 Crosspoint	LVDS/LVPECL/CML	LVDS	1500	LLP-28, LQFP-32	Programmable pre-emphasis, 6.5 kV ESD, JTAG

SerDes products

Part number	Description	Mux ratio	Function	# Ser	# Des	Bus speed (MHz)	Payload/Channel (Mbps)	Total payload (Mbps)
SCAN921025	10:1 Serializer w/embedded clock	10:1	Serializers	1	–	20-80	800	800
SCAN921226	1:10 Deserializer w/embedded clock	1:10	Deserializers	–	1	20-80	800	800
SCAN926260	Six-channel 1:10 Deserializers w/embedded clock	1:10	Deserializers	–	6	25-66	660	3960
SCAN928028	Eight-channel 10:1 Serializers w/embedded clock	10:1	Serializers	8	–	25-66	660	5280
DS92LV16	16:1/1:16 Serializer/Deserializer w/embedded clock	16:1	SerDes	1	1	25-80	1280	1280 x 2
DS92LV18	18:1/1:18 Serializer/Deserializer w/embedded clock	18:1	SerDes	1	1	15-66	1188	1188 x 2

High-speed ADCs and DDC for communications

					Dynamic performance				
Part number	Resolution	Speed (MSPS)	Supply voltage	Power (mW)	SFDR (dB)	THD (dB)	ENOB (bit)	SNR (dB)	Package
8-bit ADCs									
NEW! **ADC081000**	8 bit	1000	1.9	1450	58	-57	7.5	48	LQFP-128 Exp. Pad
NEW! **ADC08D1000**	8-bit dual	1000	1.9	1600	55	-55	7.4	47	LQFP-128 Exp. Pad
10-bit ADCs									
ADC10040	10 bit	40	3	55	80	-77	9.6	59	TSSOP-28
ADC10065	10 bit	65	3	68	80	-72	9.5	59	TSSOP-28
ADC10080	10 bit	80	3	78	78	-74	9.5	59	TSSOP-28
ADC10D040	10-bit dual	40	3.3	257	72	-69	9.5	60	TQFP-48
NEW! **ADC10DL065**	10-bit dual	65	3	320	80	-78	9.8	60	TQFP-64
12-bit ADCs									
ADC12040	12 bit	40	5	340	84	-80	11.2	69	LQFP-32
ADC12L066	12 bit	66	3.3	357	80	-77	10.7	66	LQFP-32
NEW! **ADC12L080**	12 bit	80	3.3	425	80	-77	10.7	66	LQFP-32
ADC12D040	12-bit dual	40	5	600	80	-78	10.9	68	TQFP-64
NEW! **ADC12DL040**	12-bit dual	40	3.3	360	86	-83	11.1	69	TQFP-64
NEW! **ADC12DL065**	12-bit dual	65	3.3	360	86	-83	11.1	69	TQFP-64
ADC12DL066	12-bit dual	66	3.3	686	81	-78	10.7	66	TQFP-64
CLC5957	12 bit	70	5	640	72	–	–	65	TSSOP-48

Digital down converter	Description
CLC5903	14-bit input resolution, 78 MSPS, DDC with AGC control and 1.8V core supply voltage. Power consumption is only 290 mW. SFDR is 100 dB, SNR is 127 dB and tuning resolution is 0.02 Hz.

A Walk Along the Signal Path

to be removed and also a need to reduce the bandwidth of the input noise to the ADC, this design uses a simple, passive, single-pole, low-pass filter between the amplifier and ADC. A 3 dB bandwidth of 32 MHz is chosen for two reasons:

- To minimize attenuation of signals at the upper end of the input signal range
- To reduce the aliasing or folding of noise and unwanted signals from frequencies beyond half of the ADC sample rate into the frequency band of interest

A filter as specified here is often called an anti-alias filter, since it eliminates or reduces the effect of aliasing (*see Figure 4*). Depending on the amplitude and frequency of the unwanted AC signals, a steeper, multi-pole filter might be required, but for this application the single-pole filter is sufficient. The filter is a simple resistor-capacitor (R-C) filter with values that will be chosen after the design of the amplifier block that precedes the filter.

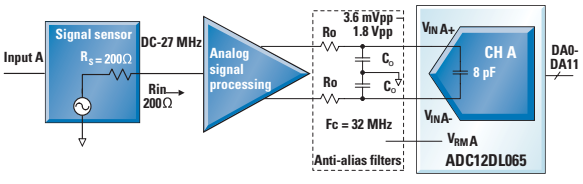


Figure 4. Anti-alias filter

Selecting the amplifier

The designer's next step is to look at one of the more demanding requirements for the analog signal-processing block–the function of single-ended-to-differential conversion (*see Figure 5*). This is often done with transformers, but since the signal frequency range includes DC, the transformer will not work and a single-ended to differential amplifier will be required. This amplifier can also provide amplification, level shifting, and impedance-matching functions.

The process of converting system specifications to amplifier specifications is similar to the process for selecting the ADC. Key high-speed amplifier specifications are bandwidth, gain, noise, and distortion. To avoid degradation of the signal before it gets to the ADC, an amplifier bandwidth of several times the 27 MHz signal bandwidth is desired. Since the full-scale ADC input is 2 Vpp and the maximum signal is 1 Vpp, an amplifier gain of two would amplify the 1 Vpp maximum signal to exactly match the ADC full scale. To avoid the possibility of the amplified signal overdriving and clipping the signal at the ADC input, the gain will be set slightly lower at 1.8. The SNR of the ADC12DL065 is 69 dB. This means that the total noise of the ADC is 69 dB below the 2 Vpp full scale input level or about 250 µVrms.

The amplifier output noise should be at least a factor of two smaller than this or less than 125 µVrms. To translate this noise level into the noise voltage and current specifications for the amplifier, the bandwidth of the amplifier output signal and the gain of the amplifier must be taken into account. The previously selected anti-alias filter bandwidth of 32 MHz sets the bandwidth of the amplifier noise presented to the ADC, and the amplifier gain is set at 1.8. ADC input noise due to amplifier input voltage noise is calculated with the following equation:

$$Vnadc = Vnamp * \sqrt{BW} * (1+Gain) =$$
$$Vnamp * \sqrt{32\ MHz} * 2.8 <= 125\ \mu Vrms$$

So the input noise of the amplifier, Vnamp, needs to be less than 8 nV/$\sqrt{Hz}$. There may also be noise contribution from the input currents of the differential amplifier and that contribution will be checked later when the resistor values around the amplifier have been set. Distortion is not a key specification of this system, but the amplifier distortion should be in the same range as the ADC distortion. A single amplifier for each channel will be selected to facilitate clean PC board layout and to maximize rejection of high-frequency interference between the two amplifier inputs.

The requirement is for a single-ended-to-differential amplifier with a bandwidth greater than 80 MHz at a gain of 1.8, input noise less than

8 nV/√Hz, and distortion terms suppressed by greater than 70 dB. National's new LMH6550 differential, high-speed op amp meets these requirements well. Gain bandwidth product for this amplifier is 400 MHz, so at a gain of 1.8, the bandwidth will be 140 MHz (400 MHz /(1+1.8)). Input voltage noise of the LMH6550 is 6 nV/√Hz, which is better than the 8 nV /√Hz requirement, and the amplifier's distortion for a 20 MHz 2 Vpp signal is typically 70 dB, which is in the same range as the distortion of the ADC.

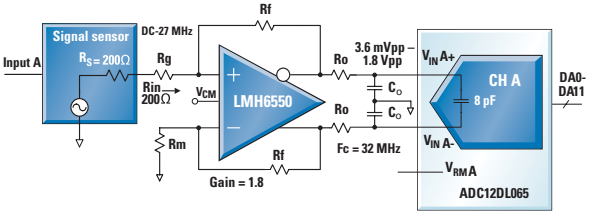


Figure 5. Single-end-to-differential amplifier configuration

Using a few simple equations, differential operational amplifiers like the LMH6550 can be set to a range of gains and input impedances by properly selecting the external gain and feedback resistors. The desired amplifier gain is 1.8, and the desired input resistance is 200 Ohms.

Using the following equations, the resistor values are selected:

Rin = Rs = 200Ω
Rg=Rin/(1+Gain)=200Ω/(1+1.8) = 71.4Ω
Rf = Gain x (Rg+Rs) = 1.8 x (71.4Ω + 200Ω) = 488.5Ω
Rm = Rg + Rs = (71.4Ω + 200Ω) = 271.4Ω

A quick check of the amplifier input-noise current contribution with these resistance values reveals that the amplifier noise is dominated by the voltage noise term that was previously calculated, so the contribution from input-noise current will be ignored.

The values for the resistors and capacitors in the anti-alias filter can be selected now that the amplifier characteristics are known. The desired cutoff frequency for the filter is 32 MHz. The equation for the cutoff frequency is:

$$Fc=1/(2\pi*Ro*(Co + Cadc*2))$$

The LMH6550 datasheet includes an example of an anti-alias filter with a 50 MHz cutoff frequency, and the suggested Ro is 56Ω. This Ro value will be used in this design and Co will be adjusted for the 32 MHz cutoff frequency.

Co =1/ (2π*Ro*Fc) – Cadc*2 =
1/ (2π* 56Ω * 32 MHz) – 8 pF*2 = 72.8 pF

All of these resistor and capacitor values can be adjusted to allow for more commonly available values.

One final function is required of the amplifier – signal shifting to match the common-mode input of the ADC. Common-mode voltage adjustment is accomplished simply in the LMH6550 by applying the desired common-mode voltage, 1.5V from the ADC12DL065 reference output pin, to the amplifier Vcm input. The resulting amplifier output common-mode voltage will be 1.5V and will match the ADC input common-mode voltage.

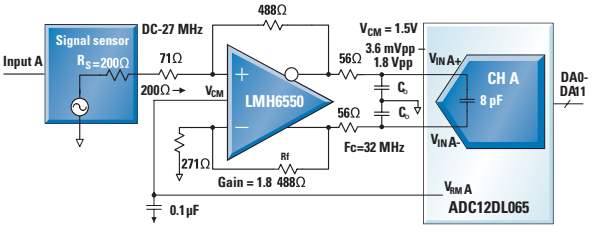


Figure 6. Final input "A" receiver system configuration

Summary

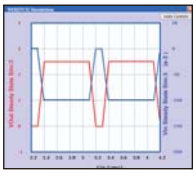
By walking systematically through this signal-path design, the designer selected components resulting in a high-performance, low-power compact design that meets all of the original design targets (*see Figure 6*). The LMH6550 and ADC12DL065 offer complementary operation in signal-path applications such as this one, and therefore, the design was simple and straightforward. Actually, building and testing this circuit is the best measure of the success of the design. When tested on the bench, this circuit met or exceeded the desired system performance in all areas. ■

Design Tools

WEBENCH® Active Filter Designer online tools

Design, build, and test amplifier circuits in this FREE online design and prototyping environment

- **Customize** circuit requirements and device selections
- **Design** advanced, highly customized filters for all standard filter types
- **View** design aspects such as bill of materials, operating values, and recommended alternate components
- **View and compare** waveforms from your online simulation using the multi-waveform viewer
- **Receive** samples in 24 hours



webench.national.com

WaveVision 4.0 evaluation board

Test and evaluate A/D converters with National's easy-to use WaveVision 4.0 evaluation board. Each evaluation board comes complete with USB and software.

Features and benefits:

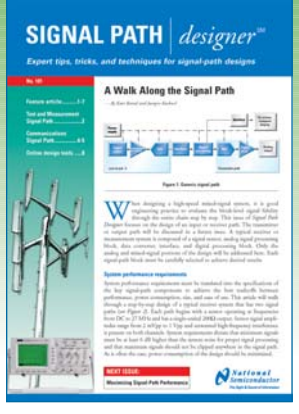
- Plug-n-play ADC evaluation board
- USB interface to PC
- PC-based data capture
- Easy data capture and evaluation
- Highlighted harmonic and SFDR frequencies
- Easy waveform examination
- Produces and displays FFT plots
- Dynamic performance parameter readout with FFT
- Produces and displays histograms

National Semiconductor
2900 Semiconductor Drive
PO Box 58090
Santa Clara, CA 95052
1 800 272 9959

Visit our website at:
signalpath.national.com

For more information, send email to:
new.feedback@nsc.com

Don't miss a single issue!



Subscribe now to receive email alerts when new issues are available:

signalpath.national.com/designer

National Semiconductor
The Sight & Sound of Information

570088-001

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap		
Wireless Connectivity	www.ti.com/wirelessconnectivity		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265