Frequency Margining Using TI High Performance Clock Generators

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ABSTRACT

Crystal oscillators and/or multiple output clock generators are critical in today's high performance consumer, computing and communications systems. Deciding an optimal clock rate for the system can sometimes require several rounds of prototyping and validation. Clock Generator and Oscillator ICs with the right hooks to margin the synthesized clock can help to streamline the overall product development cycle and optimize performance of the end system. LMK03328 and LMK03318 are TI's high performance programmable clock generators with 100fs (typical) integrated RMS jitter (12 kHz – 20 MHz) that also support multiple frequency margining modes. This application note will describe the benefits of frequency margining in various applications, highlight common approaches in the industry for frequency margining and describe the flexible frequency margining features on LMK03328 and LMK03318 that are preferred by system architects.

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1 Frequency Margining using TI High Performance Clock Generators

There are various applications that could benefit from frequency margining. Some of the potential use cases of frequency margining are explained below.

FPGA-based applications can optimize their power and throughput by selecting an optimal reference clock rate. The ability to quickly change the FPGA reference clock enables system designers to help analyze timing margins and make the necessary logic updates to improve overall system performance / stability and reduce time-to-market. Serializer/ Deserializer (SerDes) transceivers in complex FPGA implementations can potentially benefit from clock rate optimization as well.

In 10Gb/s Ethernet applications as an example, it is critical to stress every node in the network to the full 10Gb/s rate to find potential errors in frame reception and forwarding. System throughput is defined as the highest rate at which the system under test can forward the payload without losses. In order to ensure interoperability within the framework of the IEEE802.3ae standard for 10Gb/s Ethernet, every node in the network must be tested at the maximum achievable throughput. The reference clock rate impacts the maximum achievable throughput and IEEE802.3ae standard allows the reference clock to be skewed from nominal rate by +/-100ppm. The frequency margining features on LMK03328 and LMK03318 allows customers to margin the reference clock by +/-100ppm to test Ethernet nodes at maximum throughput.

Dynamically modulating the reference frequency of CPUs/DSPs in certain data processing applications can potentially enhance system efficiency. As an example, the reference frequency of CPUs/DSPs can dynamically scale down under low load operation and scale back up for operation under heavy load. In another scenario, CPU clock speeds can be reduced when the temperature of the board exceeds a certain threshold thereby protecting the system from thermal issues.

The ability to margin the reference frequency helps to uncover, isolate, or even work-around system timing margin or signal integrity issues early on in the design cycle. System architects can then quickly make the necessary course corrections thereby improving the overall system robustness.

Previous approaches to frequency margining have proven to be highly inefficient and time-consuming. One approach involves procuring fixed frequency oscillators from vendors that are offset by fixed amounts of frequency ppm error with respect to each other. Reworking boards to support these various oscillators proves to be inefficient especially when multiple boards needed to be tested over voltage and temperature corners.

The alternate option of including a multiplexer on-board to select between multiple oscillators proves to be rather limiting because of the small number of discrete frequencies that the system could be potentially tested with. In addition, a significant amount of phase discontinuity was introduced when switching between the frequencies.

The use of external frequency references like signal generators for frequency margining testing of ICs typically requires long PCB traces from the IC to edge or vertical mount SMA connectors that could result in a sub-optimal layout of the prototype board.

High performance I^{2}C programmable clock generators such as LMK03328 and LMK03318 with frequency margining capabilities are able to address all the shortcomings of the approaches described above. These clock generators offer the flexibility to adjust the output frequency in coarse or fine frequency increments and decrements. They have high performance Fractional-N PLLs that can be programmed to output a wide range of frequencies overcoming the frequency coverage inflexibility of fixed frequency oscillators. Silicon ICs have significantly higher mean time between failures (MTBF) compared to quartz based oscillators which translates to higher reliability.

LMK03328 and LMK03318 offers coarse and fine frequency margining capabilities. Coarse margining refers to margining the output frequency in large steps. This is often in terms of % change with respect to the nominal frequency. This form of margining is primarily used for CPU performance testing, FPGA logic timing analysis etc.

On LMK03328 and LMK03318, coarse margining is accomplished by changing the output dividers via I^{2}C register write. It is valid for changes in the output divide anywhere between 8 and 256. Output frequency changes initiated by changing the output divider value do not result in any glitches in the output frequency. The output divider dynamic delay control register bits (Register 24 [5:0]) need to be enabled for the output channels where glitch-free margining is desired. The waveforms below highlight the response observed at the output when the output divider is updated via I^{2}C.
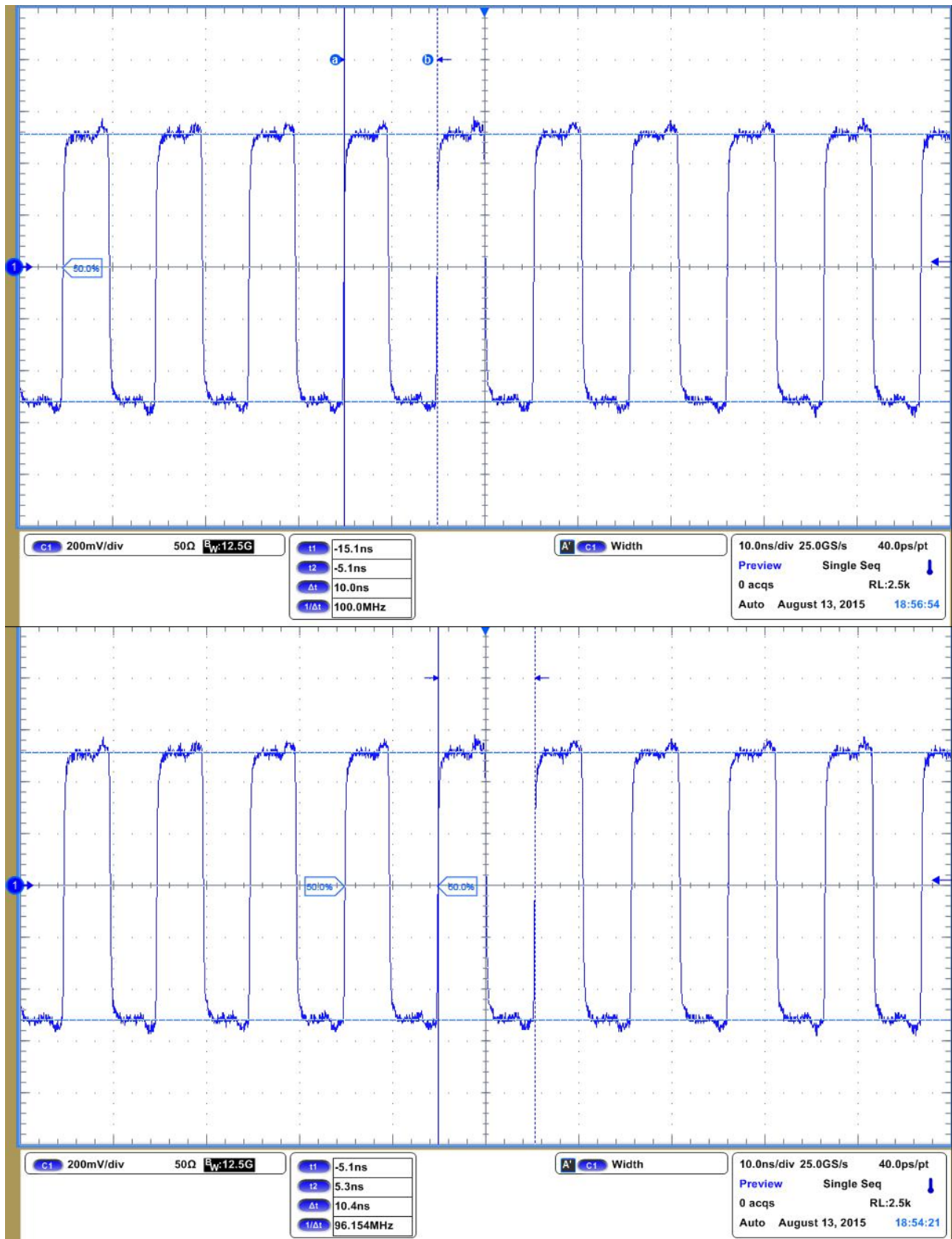
Figure 1. Coarse Frequency Margining Reference Frequency = 50 MHz, VCO Frequency = 5000 MHz, Post Divider = 2 Output Divider = 25 (Top), Output Divider = 26 (Bottom)

The top waveform in the Figure 1 above corresponds to an output divider setting of 25. The output frequency was therefore 100 MHz. The bottom waveform in the Figure 1 above corresponds to output divider setting of 26. The output frequency was therefore 96.154 MHz. There are no glitches or runt pulses as the output frequency transitions from 100 MHz to 96.154 MHz.

Fine frequency margining, also known as ppm margining, could be used to evaluate Ethernet-based systems for standards compliance as well as improving system throughput. On LMK03328 and LMK03318, fine frequency margining can be achieved in two ways. The first approach is via tuning the fractional portion of the feedback divider. The numerator and denominator of the fractional portion of the feedback divider are 22 bits. The denominator can be set between 1 to 4194303 and the numerator from 0 to 4194303. It is highly recommended to re-calibrate the PLL(s) after the fractional portion of the feedback divider has been updated via I2C. Toggling the software reset or the PLL power-down register bits will restart calibration.

The second approach is via programming LMK03328 and LMK03318 on-chip crystal load capacitance when operating with a pullable crystal reference on the secondary inputs. Parallel resonant AT-cut crystals between 10MHz to 52 MHz are supported. Under nominal conditions, the on-chip crystal load capacitance of LMK03328 and LMK03318 can be programmed to operate the crystal at its fundamental frequency as specified by the crystal manufacturer. The crystal frequency can be increased or decreased by operating it at a load capacitance that is different from the nominal capacitance. The amount of pullability (ppm per capacitance) depends on the trim sensitivity of the selected crystal. In LMK03328 and LMK03318, the default crystal load capacitance can be programmed via I2C (or loaded from EEPROM) and controlled via software register and/or hardware pin. These modes are explained in detail in the datasheet.

In order to estimate the binary code required to be programmed into LMK03328 and LMK03318 crystal margining registers to cause a desired shift in the output clock frequency, the methodology stated in Appendix 1 can be followed.

Fine frequency margining by varying the crystal load capacitance via programming the binary code could result in significant improvement in the overall integrated RMS phase noise compared to fractional feedback divider based margining. In the case of the former, the PLL can be in integer mode and only the reference crystal frequency is varied. In the case of the latter, the PLL is in fractional mode resulting in spurs in the output phase noise. Figure 2, Figure 3, Figure 4 highlight the difference in the output clock phase noise using the two fine frequency margining approaches.

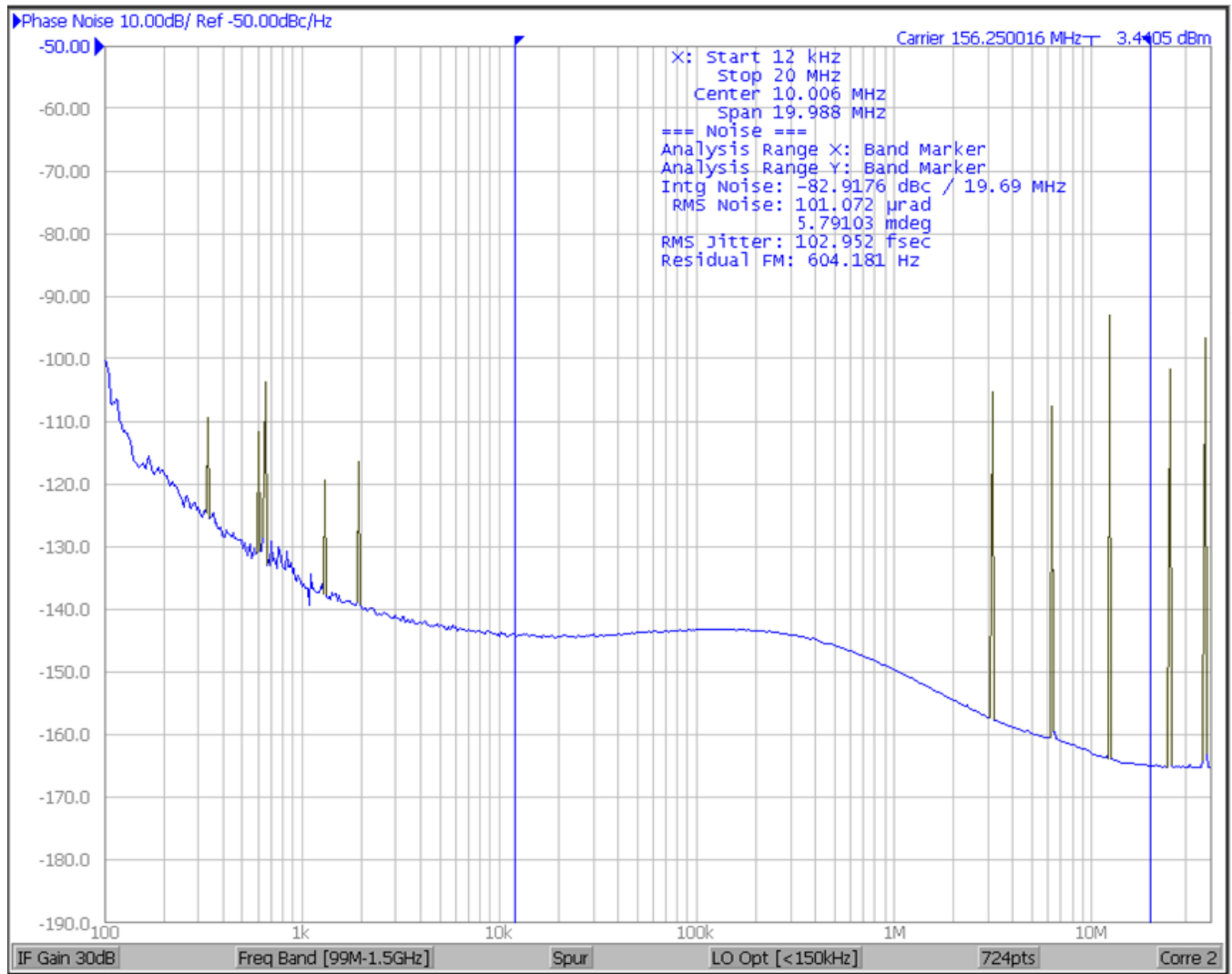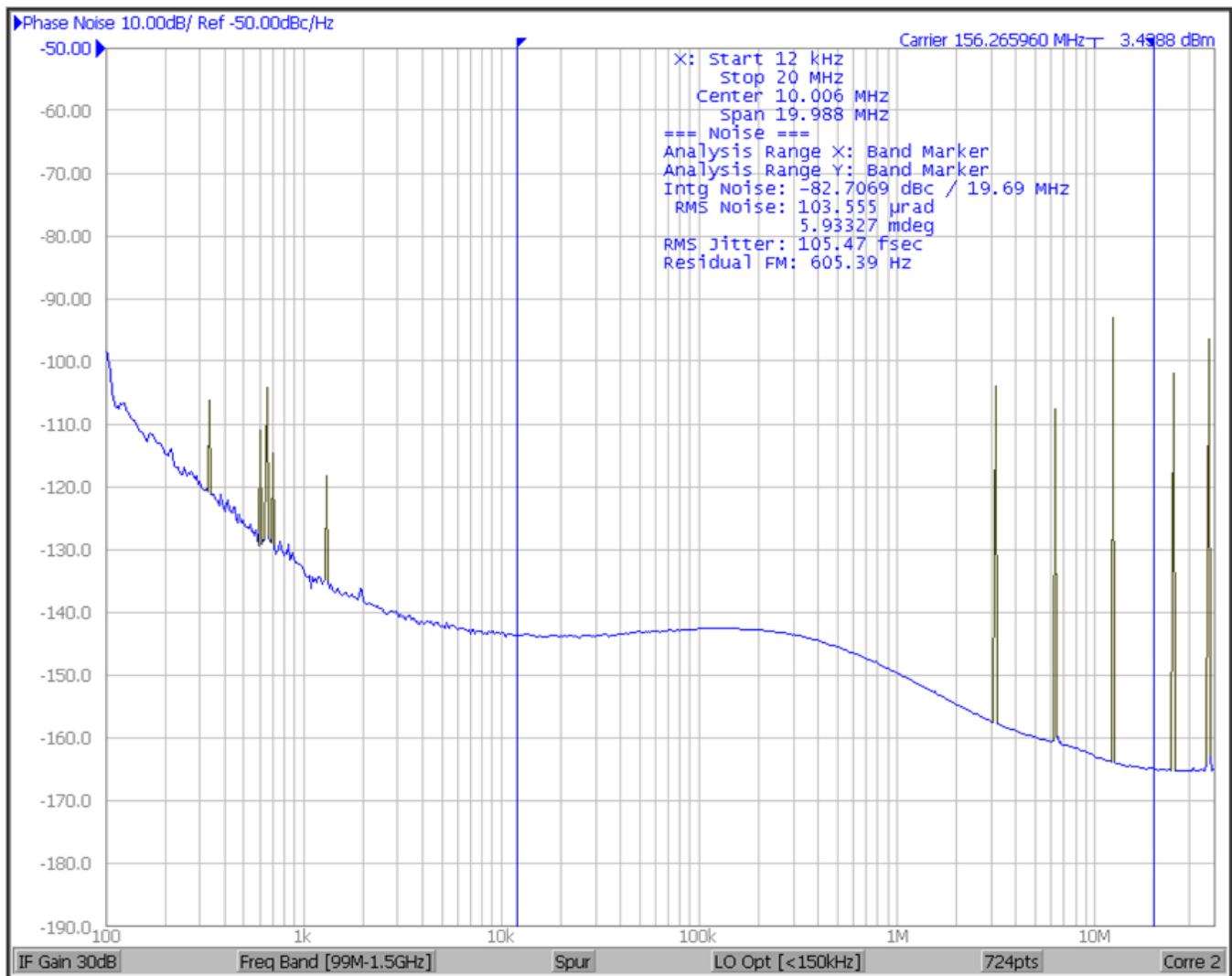**Figure 2. Output Clock = 156.25 MHz, Nominal Binary Code = 440**

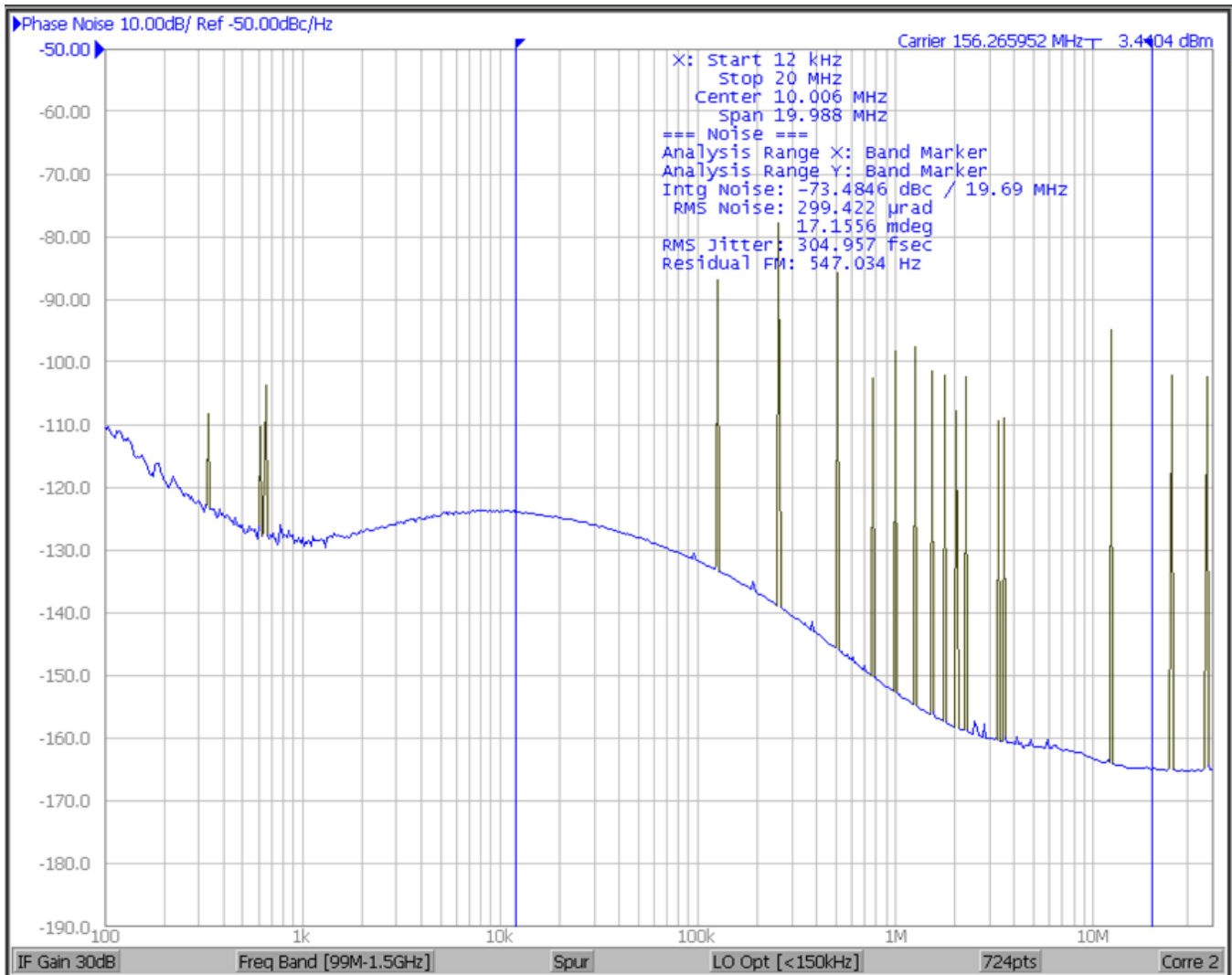**Figure 3. Output Clock = 156.25 MHz + 100ppm, Binary Code = 120**

Figure 4. Output Clock = 156.25 MHz + 100ppm, PLL in Fractional-N Mode

From Figure 4, it can be seen that operating the PLL in Fractional-N mode to change the output frequency by +100ppm results in additional spurs. In this scenario, the integrated RMS jitter goes up from ~100fs (nominal) to ~300fs (+100ppm) using this approach (results may vary depending on the fractional mode settings and is use-case specific). In contrast, by programming the binary code for the crystal to result in the 100ppm shift in the output frequency has minimal impact on the integrated RMS jitter. When evaluating high performance systems, using fine frequency margining, changing the crystal load capacitance by programming the required binary code into the device via I2C is the preferred option. Ideally, the setup for frequency margining should not add significant jitter to the output clock.

In summary, frequency margining provides system designers and architects the necessary flexibility to evaluate the performance of today's highly complex systems. In addition to proving ultra-low integrated RMS jitter, high performance clock generators from Texas Instruments such as LMK03328 have flexible frequency margining hooks to enhance system performance and robustness.

2   Appendix 1: Design Procedure for Programming the Crystal Frequency Margining Offset for LMK033x8

The following describes the steps needed to compute the required binary code to be programmed to LMK03328 and LMK03318 to generate a particular frequency offset under nominal conditions of supply voltage and temperature.

2.1   Step 1

Acquire the trim sensitivity vs crystal load capacitance data from the crystal manufacturer. Ensure that the part-part variation in the crystal trim sensitivity especially for lower values of the crystal load capacitance is not significant.

Example: For the 50 MHz (3.2x2.5mm) AT-cut crystal on LMK03328 and LMK03318 EVM, the trim sensitivity vs crystal load capacitance data is shown below.

Table 1. Crystal Trim Sensitivity vs Crystal Load Capacitance

Crystal Load Capacitance (in pF)	Trim Sensitivity (ppm/pF)
6	28.46
7	21.58
8	16.92
9	13.62
10	11.2
11	9.37
12	7.96
13	6.84
14	5.95
15	5.21
16	4.61
17	4.1
18	3.68

2.2 Step 2

From the above crystal data, using a curve fitting tool (such as Excel), compute the trendline equation.

$y = 0.00255405883468085x^4 - 0.147238260958206x^3 + 3.22588517502173x^2 - 32.6298356034598x + 136.486948520535$

where

- 'y' is the crystal Trim sensitivity in ppm/pF
- 'x' is the crystal load capacitance in pF   (1)

NOTE: Please send a request to clock_support@list.ti.com for assistance with this step.
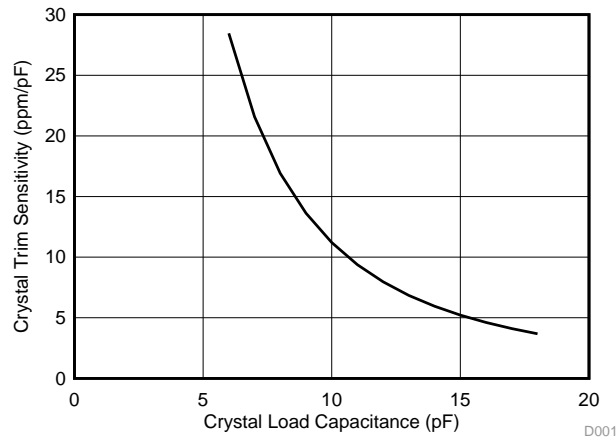

Figure 5. Crystal Trim Sensitivity vs Crystal Load Capacitance

2.3 Step 3

Integrate Equation 1 to compute the crystal frequency pulling curve vs load capacitance. Note that there is a negative sign in the result and a constant term due to the integration.

$\int y\, dx = -(0.00051081176693617x^5 - 0.0368095652395515x^4 + 1.07529505834057x^3 - 16.3149178017299x + 136.486948520535x + C)$ (2)

2.4 Step 4

Constant C in Equation 2 can be calculated by substituting x with the recommended crystal load capacitance value for ~0ppm frequency error. The crystal on LMK03328 EVM is rated for 0 ppm at 9pF. Substituting x = 9 and y=0 in the equation from step 3 gives C = -479.419

$\int y\, dx = -(0.00051081176693617x^5 - 0.0368095652395515x^4 + 1.07529505834057x^3 - 16.3149178017299x + 136.486948520535x - 479.419)$ (3)

2.5 Step 5

In Equation 3, the unit for 'x' is pF. On LMK03328 and LMK03318, binary codes from 0 through 1023 effectively map to the crystal load capacitance. Binary code 0 corresponds to an internal load capacitance of roughly 1.6pF. The total capacitance (internal + external) corresponding to the binary code setting of 0 is 1.6pF + effective PCB trace capacitance (crystal trace on PCB). On LMK03328 and LMK03318, the crystal PCB trace capacitance is roughly 1.35pF. The capacitance per binary code is roughly 14fF.
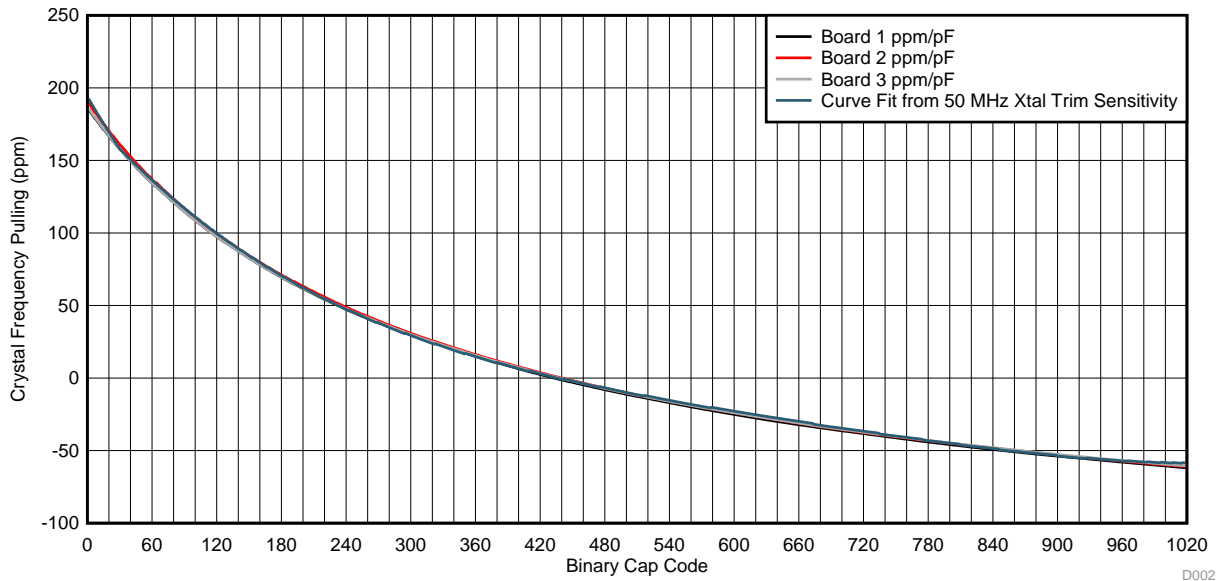

Figure 6. Crystal Frequency Pulling vs Binary Cap Code Setting

In Figure 6, three boards were used for measuring the crystal frequency pulling in ppm vs binary cap code setting in the lab. The procedure highlighted in the steps above was used to generate the blue curve (Curve Fit from 50 MHz crystal Trim Sensitivity). The measured data correlates well with estimation based on crystal trim sensitivity. Hence the process outlined in steps 1 to 5 can be used to estimate the binary code that needs to be programmed into the device to result in the required shift in frequency ppm shift at the output. The binary code needed to achieve a certain ppm shift will depend on the crystal trim sensitivity and PCB crystal trace capacitance. It is worth noting that the procedure outlined above assumes that the crystal is at nominal room temperature and changes in crystal temperature beyond nominal room temperature could result in additional frequency shifts in the output frequency.

Under nominal conditions, the steps highlighted above should get the user pretty close to the desired frequency ppm shift at the output but further fine tuning could be required to achieve the exact ppm desired.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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