Application Note

Driving Multiple Loads With a Single LVCMOS Oscillator

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ABSTRACT

In an effort to reduce cost and simplify BOM, designers of some systems want to drive multiple loads with a single clock source in applications where the signal integrity of the clock is not critical. Low frequency, single-ended LVCMOS clock signals can be a good target for this type of cost reduction since jitter requirements are usually relaxed and the cost of an oscillator can be relatively high relative to the receiver that this is clocking. However, this technique can raise a number of questions about the specific routing implementation and the affect on signal integrity. How does co-location of loads affect signal integrity? What is the longest acceptable trace length between multiple loads? How many receivers can a single clock source drive while maintaining acceptable rise or fall times, and how does this affect ringing and signal reflections? This application note discusses the transmission line effects of splitting a trace into multiple loads, and provides some recommended topologies based on IBIS simulation results using the LMK6C and CDC6C low-jitter, high-performance, bulk-acoustic-wave (BAW) fixed-frequency LVCMOS oscillators.

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Trademarks

1 Introduction and Test Methodology

When clocking a system at high frequencies or with long trace lengths, cables and PCB traces are usually treated as transmission lines and not just as a simple wire. As a general rule, the estimate is that transmission line effects need to be considered when the propagation delay through the trace or cable is greater than 0.25 times the signal's rise time. For example, a typical PCB made of FR-4 material can have a signal propagation delay of around 150ps/in. Assuming a signal rise time of 1ns, then any trace longer than around 1.5 inches can behave like a transmission line and can have signal integrity concerns if not addressed.

The following simulation results show the effects of driving multiple loads with a single LVCMOS oscillator using various routing schemes. To perform the simulations, we designed a 4-layered stackup in Altium Designer and determined the trace width needed to create a nominal 50Ω characteristic trace impedance. This particular stackup was chosen such that traces with a nominal 50Ω impedance can be closely matched to the pad size of 0201 passive components, resulting in minimal reflections when the signal passes through onboard resistors and capacitors.

With this stackup we designed a series of PCB layouts to emulate several different methods of routing a driver to multiple loads . The layout files were then converted for use in IBIS SI simulations using a 25MHz TI BAW Oscillator as the driver.

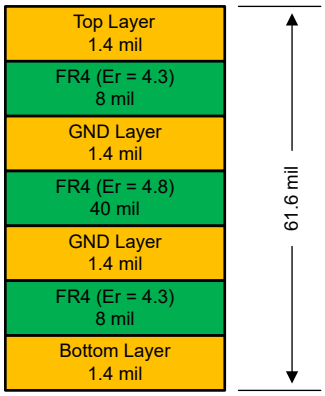

Figure 1-1. Stackup Used in Load Board Simulation

Table 1-1. Trace Impedance vs. Thickness Using Load Board Stackup

Trace Thickness (mil)	Characteristic Impedance (Z_0) of Trace
9	60Ω
13	50Ω
20	40Ω

When routing to multiple loads, line resistors can be placed for 50Ω impedance matching. Each routing scheme drives either one, two, or four loads with a combined capacitance of 10pF. The overall load capacitance was constant across all test configurations to make sure that the routing topology was the only variable that was changed. Figure 1-2 demonstrates how increasing the overall capacitive load on an LVCMOS oscillator output can increase rise and fall times and can degrade performance. This factor was eliminated from the experiment by using a constant 10pF load to account for the worst case scenario of driving four loads, each with the nominal load capacitance of 2.5pF. Section 3 contains a more in-depth description of the various trace and load topologies that were tested.

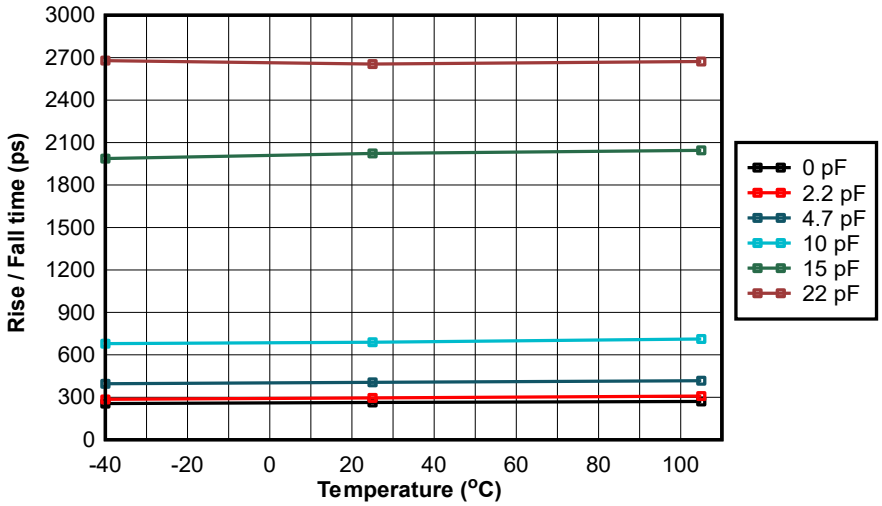

Figure 1-2. LMK6C Rise or Fall time (ps) vs Temperature and Load Capacitance for 25MHz Output Frequency, 3.3V Supply

2 Simulation Setup

IBIS SI simulations were ran in MentorGraphics' Hyperlynx tool. Altium board files were exported to a free-form SI schematic, modeling the effect of transmission lines and stubs for actual PCB trace routing and layer stackup. Figure 2-1 shows a simplified simulation example with a LVCMOS clock driver, transmission line model, and load capacitance. After extracting PCB layout to an SI model, a series of transmission line models are added to the circuit to represent trace interconnects, passive component pads, stubs, and other factors impacting the trace impedance. The Hyperlynx waveform viewer allows the user to change the clock oscillation frequency along with the time and vertical scaling, similarly to a traditional oscilloscope. The probe is placed at the load capacitor rather than the driver to simulate what a receiver can detect in a real system.

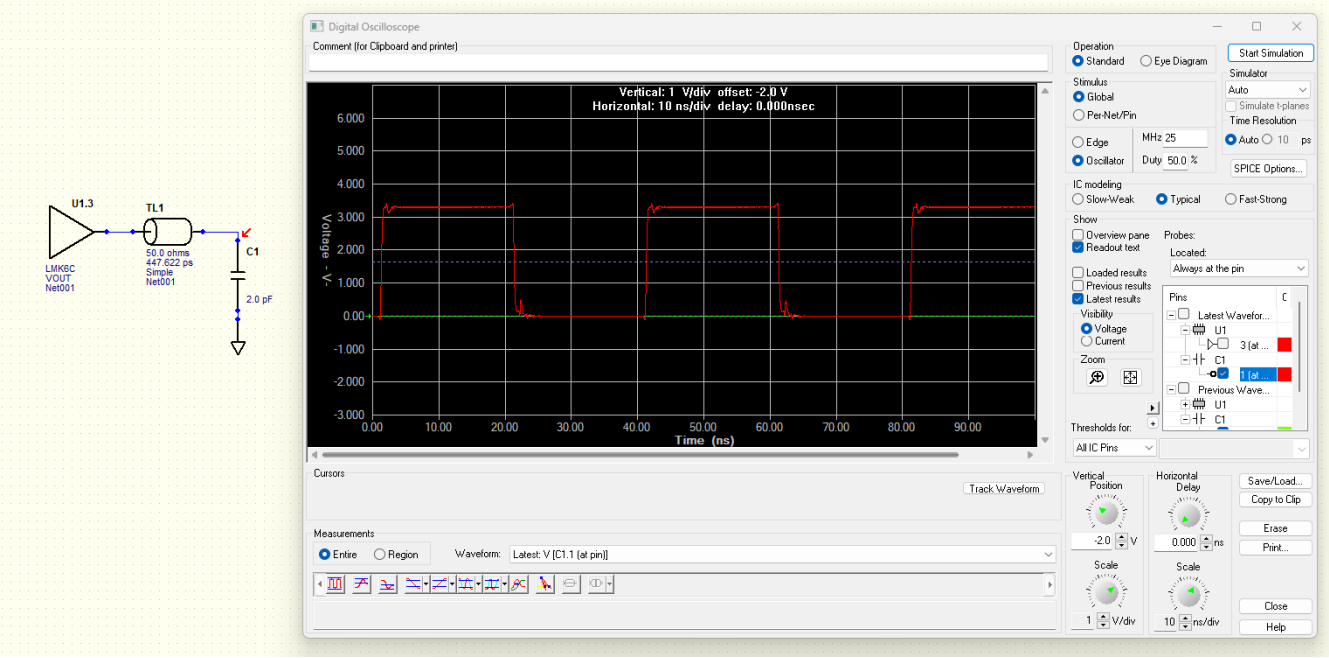

Figure 2-1. Hyperlynx SI Simulation Setup

3 Routing Topologies and Simulation Results

3.1 Single-Line

This is the typical configuration for a single-ended signal. The single line configuration is recommended for the best signal integrity since the number of nodes are reduced to only one load per line. The single-line, single-load configuration is used as a benchmark for the other topologies that were tested.

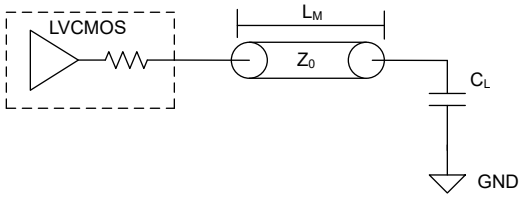

Figure 3-1. Single Line, Single Load Topology

The single-line, multi-load configuration is a good option for driving multiple loads when the separation between them is small. Some common use cases for this topology include driving two clock input pins on the same device, or multiple devices that are closely located. To be considered a single-line in the context of this study, the distance between loads need to be limited to under 1". The assumption is that each load is an equal distance from the main line, therefore L_S is the same length for each receiver.

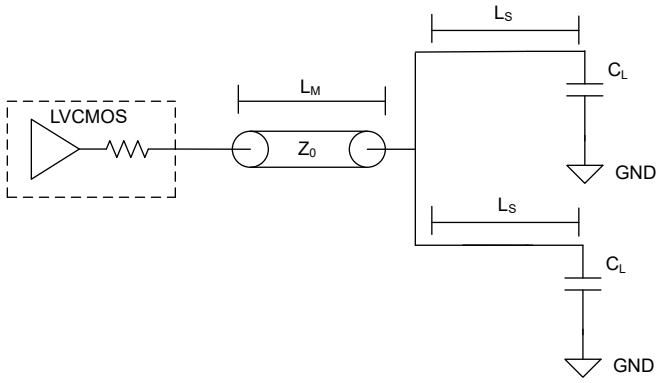

Figure 3-2. Single Line, Multiple Loads Topology

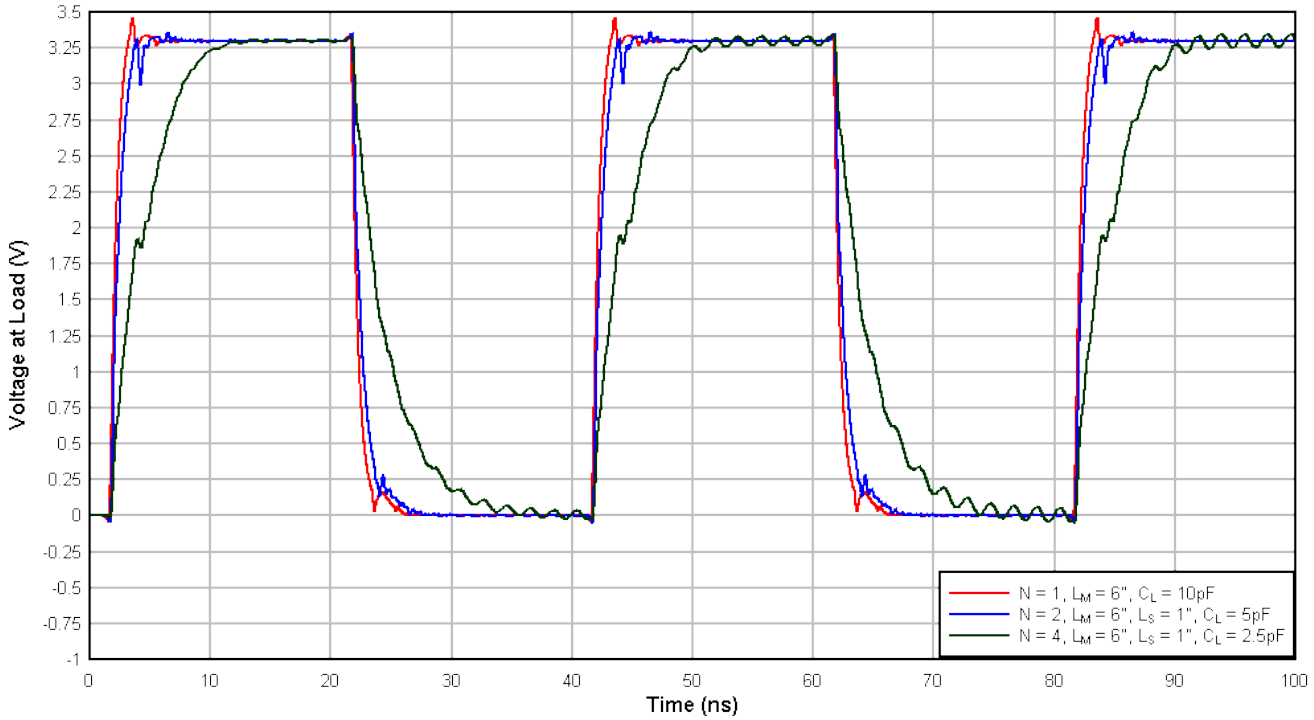

Figure 3-3. Single Line Simulation Results

Table 3-1. Single Line Rise or Fall Time

Number of Loads	Trace Length - L_M	Rise Time (ns)	Fall Time (ns)
1	6"	0.676	0.763
2	6"	0.938	1.105
4	6"	4.010	3.946

For single line configurations, driving two loads produces acceptable signal quality with only slightly longer rise and fall times and almost no measurable reflection artifacts.

With the addition of four loads, the rise/fall time slows significantly but there are still minimal reflections in the waveform.

3.2 Star Line

The star line configuration is an alternative design designed for when loads are not co-located on a board. This configuration starts out as a single output line from the driver, then splits off closer to the receiver side. Star line routing is similar to the single-line approach, but with receivers that are further than 1" apart.

Line resistors (R_t) are added to aid in impedance matching so the driver *sees* a continuous 50Ω impedance. R_t is calculated according to the formula in Equation 1.

$$R_t = \frac{N-1}{N+1} \times Z_0 \quad (1)$$

Where N is equal to the number of loads being driven and Z_0 is equal to the characteristic impedance of the trace.

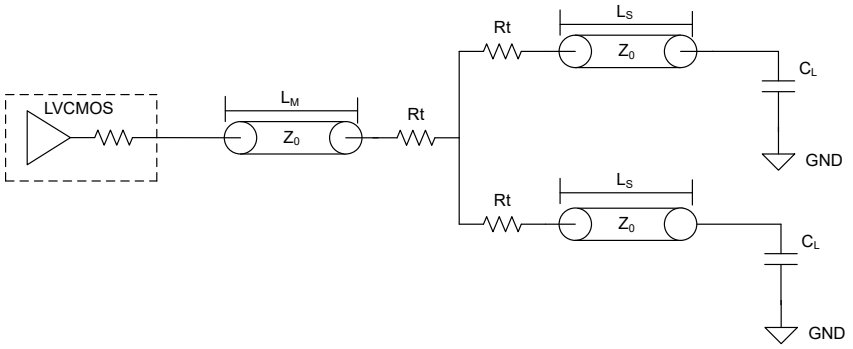

Figure 3-4. Star Line Topology

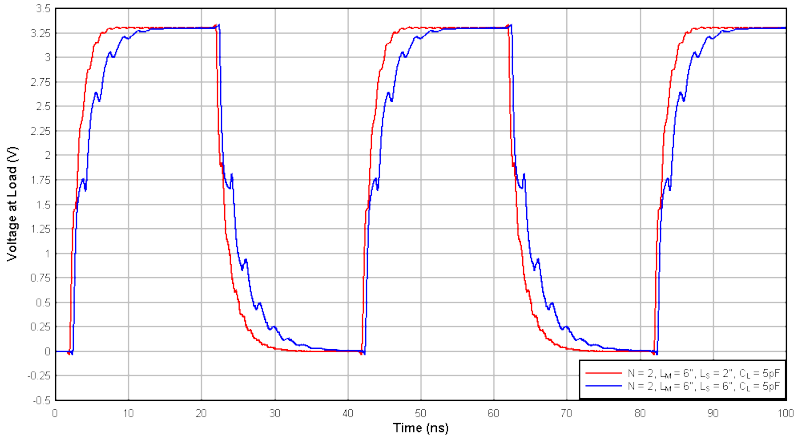

Figure 3-5. Star Line Simulation Results

Table 3-2. Star Line Rise/Fall Time

Number of Loads	Trace Length - L_S	Rise Time (ns)	Fall Time (ns)
2	2"	1.858	2.206
2	6"	2.839	3.980

For star line configurations, as this is similar to the single line configuration, with only 2" of split trace length we see the rise and fall times are increased with very slight rippling. As the trace length increases to 6", rippling worsens and rise/fall time further increase. While this signal can be adequate to some receivers, increasing the split line length further can result in unacceptable signal integrity.

3.3 Split Line

The split line configuration can be used when loads are not co-located on a board. In this topology, the traces branch out close to the driver and behave as independent transmission lines for the majority of the trace distance.

Line resistors (R_t) are again added for impedance matching according to Equation 1.

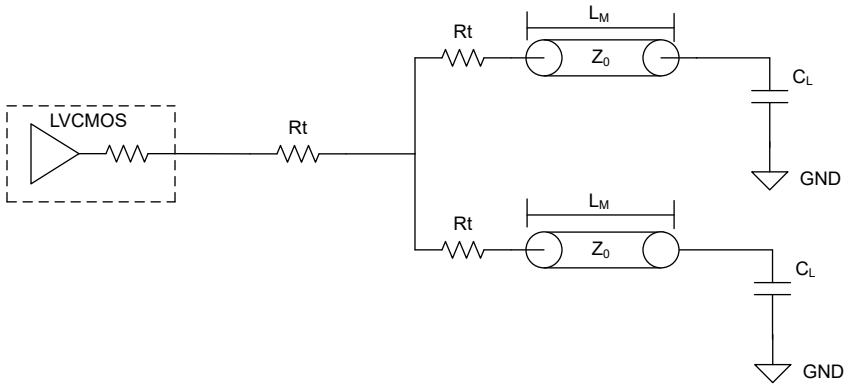

Figure 3-6. Split Line Topology

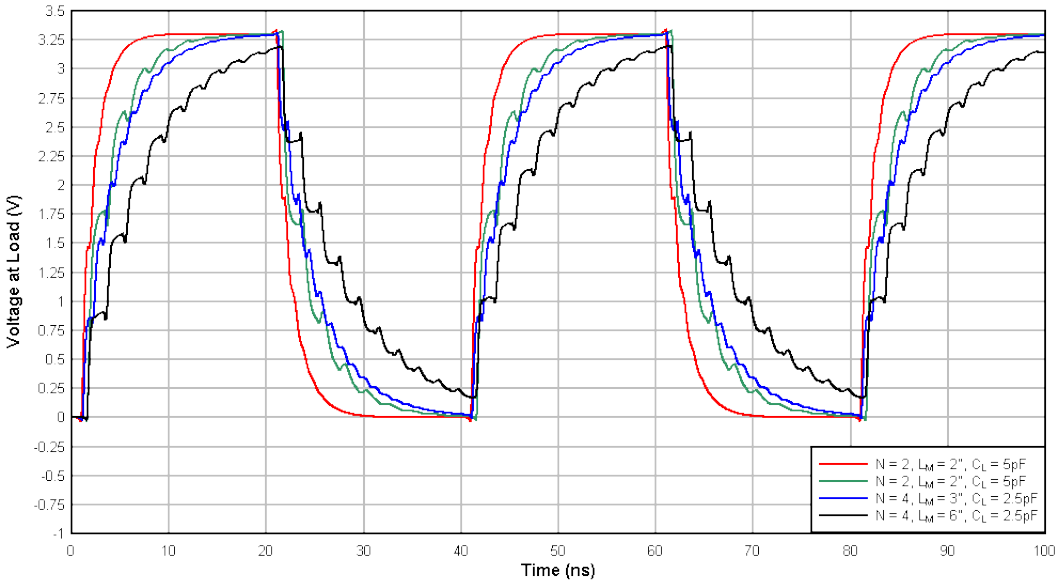

Figure 3-7. Split Line Simulation Results

Table 3-3. Split Line Rise or Fall Time

Number of Loads	Trace Length - L_M	Rise Time (ns)	Fall Time (ns)
2	2"	1.971	2.228
2	6"	3.762	4.556
4	3"	4.781	5.630
4	6"	7.998	10.16

For split line configurations, the number of loads and line length have a more drastic impact on signal integrity compared to the star line topology. As more loads are added an the trace length increases, the signal integrity worsens with more severe ringing and slower rise/fall times.

3.4 Star Line vs. Split Line

The star line and split line topologies were compared in a scenario driving two loads with a capacitance of 5pF each routed through a total of 8 inches of PCB traces. As shown in Figure 3-8, the star line approach results in better signal integrity and faster rise or fall times.

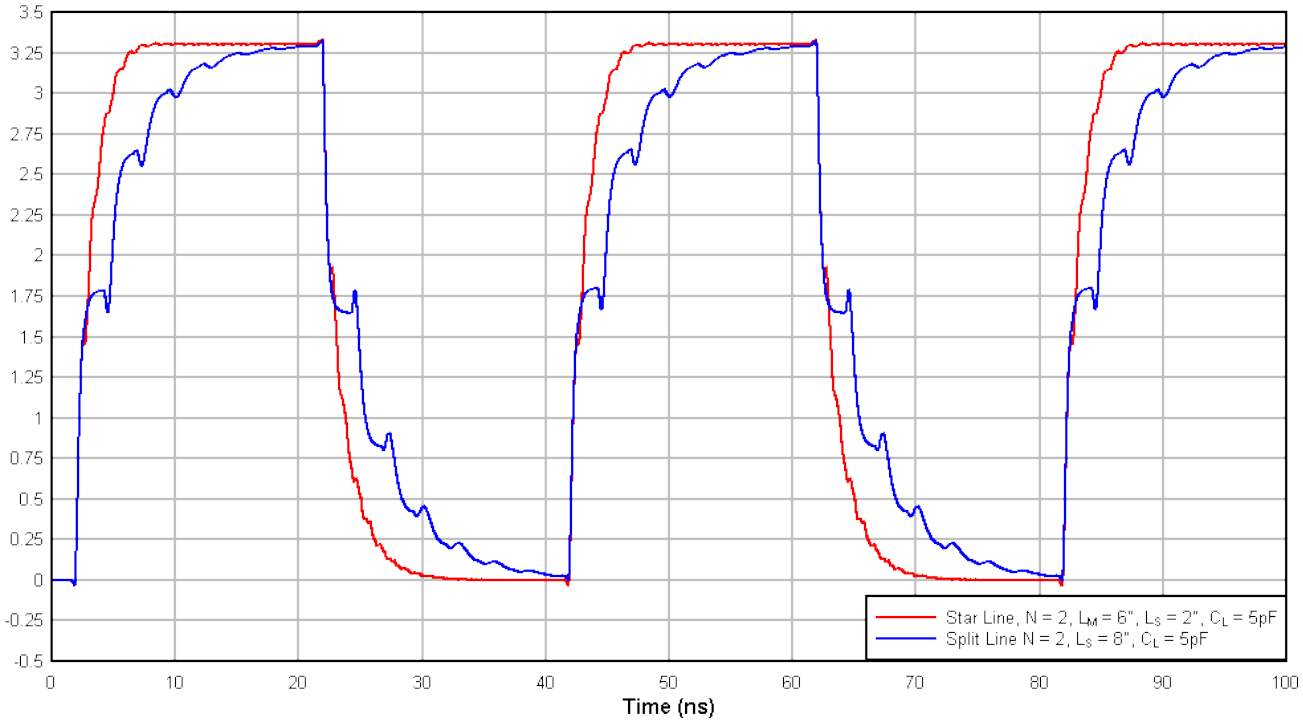

Figure 3-8. Star Line vs. Split Line Simulation Results

4 Lab Measurements

4.1 Lab Measurement Setup

To confirm the conclusions from the simulation results, a load board was designed with multiple routing schemes. This load board fans out a clock output from the onboard LVCMOS oscillator to loads with both the split-line and star-line topologies with different trace lengths. The load board contains the following trace routing configurations:

1. 2" Single trace with 1 via
2. 2" Single trace with 2 vias
3. 1" Single trace with no via
4. 2" Single trace with no via
5. 2" Trace fanned out to 2 loads, split near driver (split-line topology)
6. 2" Trace fanned out to 2 loads, split near load (star-line topology)
7. 2" Trace fanned out to 3 loads, split near driver (split-line topology)
8. 2" Trace fanned out to 3 loads, split near load (star-line topology)
9. 1.5" Trace fanned out to 3 loads, split near load (star-line topology)
10. 1.6" Trace fanned out to 4 loads, split near load (star-line topology)

A picture of the load board design along with coupon boards to add additional trace length is shown in Figure 4-1:

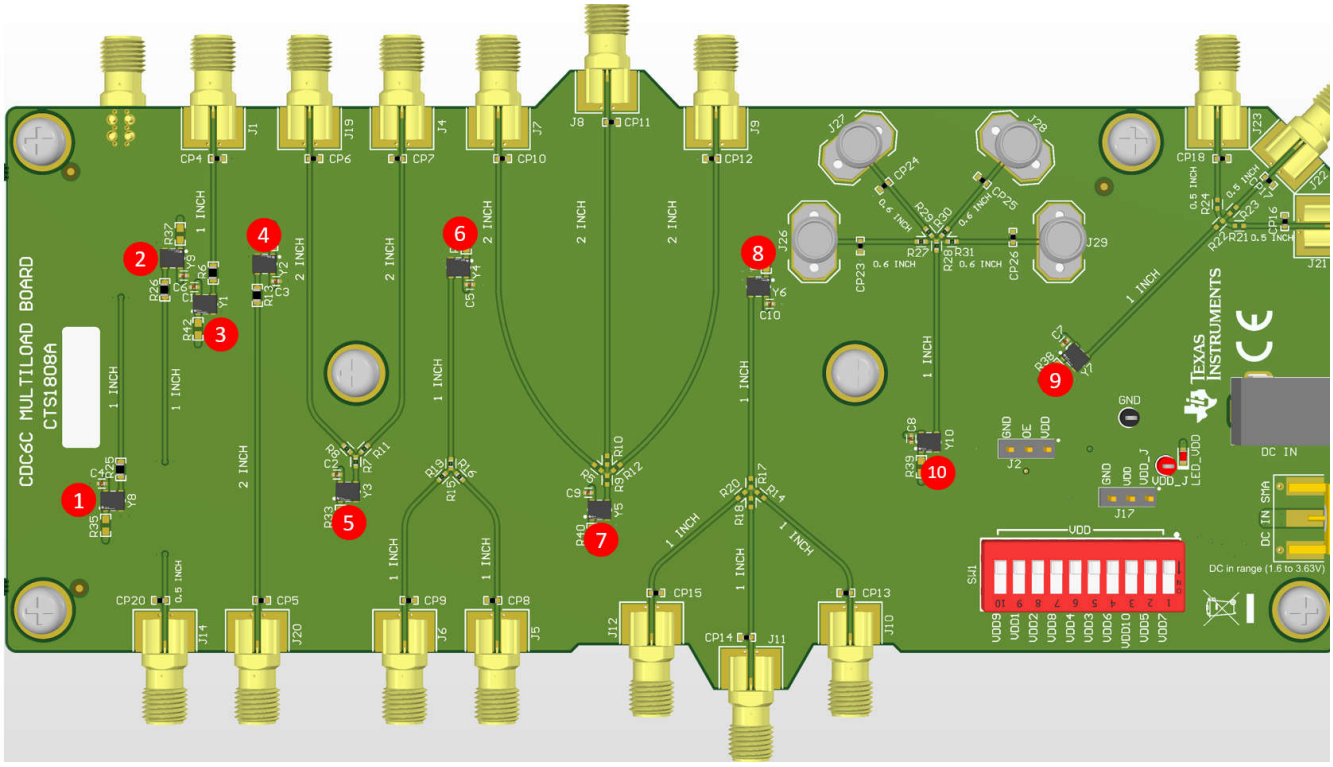

Figure 4-1. Oscillator Multi-Load Fanout Board

The layer stackup of the load board matches the simulation load board shown in Figure 1-1.

4.2 Lab Measurement Results and Correlation to Simulation Data

The board layout parameters were extracted and a signal integrity simulation was ran in Hyperlynx using the same procedure described in Section 2 with a 2pF load capacitance at each output. The measurements collected with this board and a comparison with the predicted values based on simulation results are given below.

Table 4-1. Rise or Fall Time and Jitter Results for Different Routing Topologies on Multi-Load Board

Trace Type	Trace Description	Jitter (fs) Measurement	Rise time (ps) Measurement	Fall time (ps) Measurement	Rise time (ps) Simulation	Fall time (ps) Simulation
1	2” Single with 1 via	335	250	263	263	245
2	2” Single with 2 vias	335	249	257	270	266
3	1” Single with no via	333	238	254	277	204
4	2” Single with no via	334	251	259	263	244
5	2” Double split near driver	336	1780	1870	1475	1640
6	2” Double split near load	332	1283	1422	1050	1190
7	2” Triple split near driver	350	2895	3023	2904	3180
8	2” Triple split near load	350	2051	2210	1715	1990
9	1.5” Triple split near load	349	1693	1837	1248	1420
10	1.6” Quadruple split near load	376	2385	2380	1796	2080

From the results shown in Table 4-1, the trace routing topology had very little impact on jitter performance. Note that jitter measurements were taken with a phase noise analyzer that contains an internal 50Ω termination, which reduces reflections measured at the receiver compared to a high-impedance, purely capacitive load. The rise/fall time trends of the simulated measurements closely correlate with the lab measurements. Trace numbering of the x-axis in Figure 4-2 corresponds to the same numbering scheme used in Table 4-1 and the labels on Figure 4-1. Simulation results become less closely coupled compared to the lab measurements as the routing fanout increases. This is mainly the result of unmodeled parasitic capacitances of the SMA adapters, cables, and probes in the test setup. Based on this correlation from lab measurements vs. simulation data, you can expect the simulation rise/fall time results to match the real measurement results within ±25% margin. This margin accounts for part-to-part variation, PCB manufacturing tolerances of the copper pour thickness affecting parasitic capacitance and characteristic trace impedance, and other environmental factors. To summarize, system designers can use IBIS simulations to confidently estimate the rise/fall time and signal integrity of clock signals for different routing schemes when driving multiple loads.

Output amplitude maintained rail-to-rail specifications in all routing topologies with a 2pF load, but can be degraded as the number of loads or total load capacitance increases. In both the simulations and real lab measurements, routing with the split near the load (star-line topology) results in better performance.

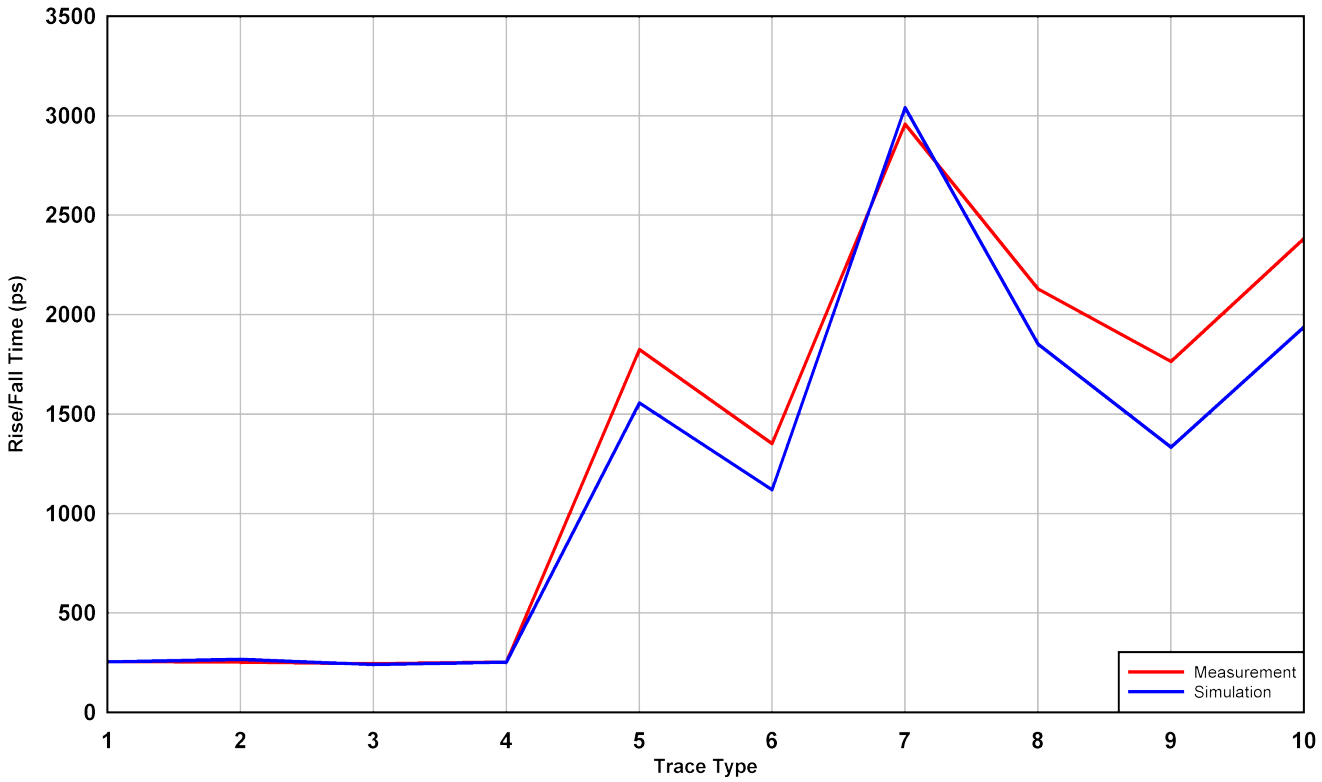

Figure 4-2. Simulation vs. Measurement: Averaged Rise or Fall Time Results with Different Routing Topologies on Multi-Load Board

5 Trace Length Mismatch Between Loads

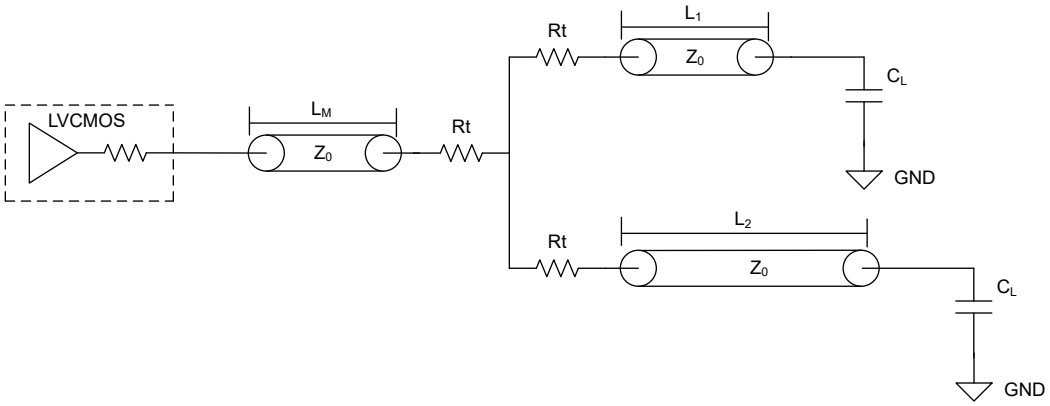

Figure 5-1. Trace Length Mismatch When Driving Multiple Loads

Excessive signal reflections can occur if the trace lengths between receivers are not closely matched when driving multiple loads. When trace lengths are mismatched, ringing can be induced based on the difference of propagation delay between the paths to each receiver. For example, consider a situation where an LVCMOS driver is split to drive multiple loads where one load is 1 inch away and the other load is 3 inches from the driver. A typical PCB can have a propagation delay of around 150ps per inch of trace length. In this scenario the shorter path can have around 150ps of propagation delay for the signal to be transmitted from the driver to the receiver. The longer path can have around 450ps of propagation delay.

A typical LVCMOS receiver has a high input impedance so almost all of the power is reflected from the receiver back through the transmission line until this is terminated at the driver. The signal from the shorter path can begin to reflect back from the load before this has propagated completely through the longer path. From the perspective of the load closer to the driver, the rising edge can see an undershoot at the delta between the propagation delays (450ps – 150ps = 300ps for this example), and the longer path can see an overshoot. The opposite effect can happen for the falling edges of the clock signal. The longer the mismatch is between receivers, the worse the overshoot and ringing can be. To maintain signal integrity and minimize the effect of excessive reflections, keep the propagation delay difference between signal paths less than 100ps when driving multiple loads with a LVCMOS driver.

The following figures show simulation results for mismatched trace lengths between multiple loads.

Figure 5-2 shows Star line topology, R_t = 17Ω, Propagation delay = 150ps/inch of trace length.

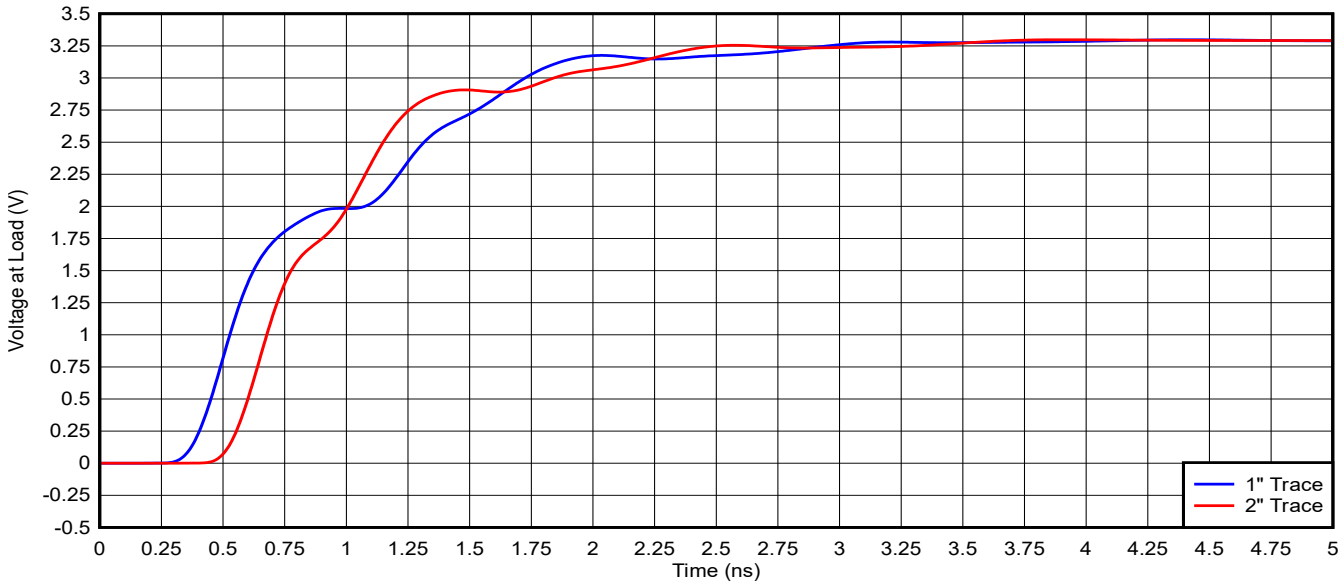

Figure 5-2. Trace Length Mismatch: Rising Edge With 1" and 2" Traces

Figure 5-3 shows Star line topology, R_t = 17Ω, Propagation delay = 150ps/inch of trace length.

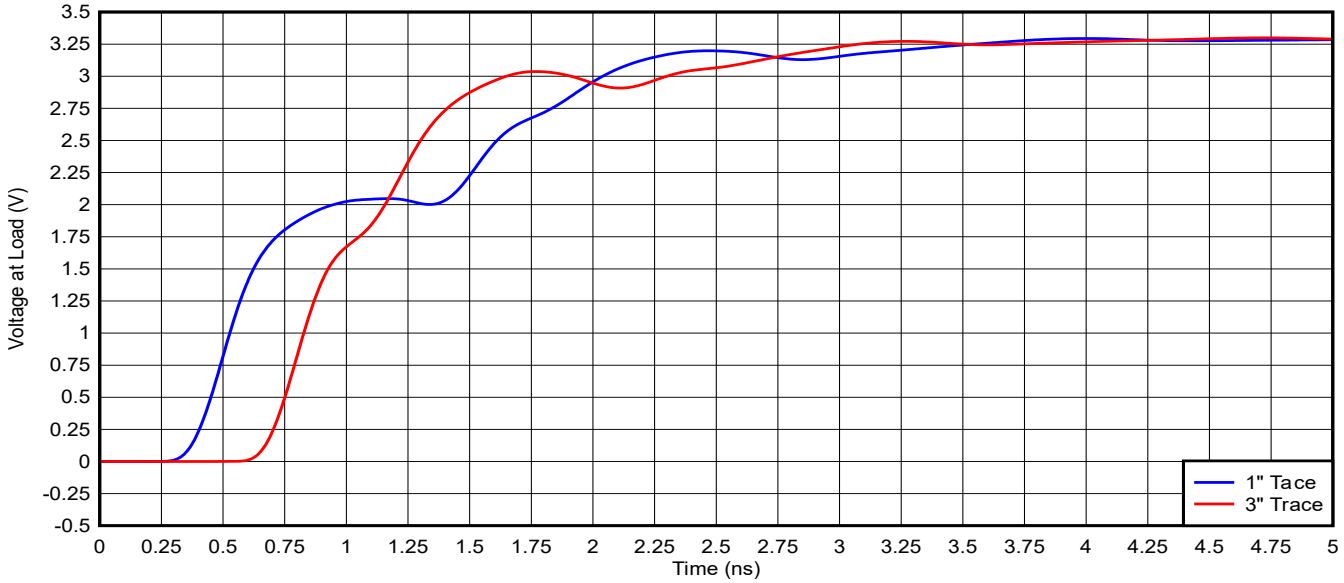

Figure 5-3. Trace Length Mismatch: Rising Edge With 1" and 3" Traces

Figure 5-4 shows Star line topology, R_t = 17Ω, Propagation delay = 150ps/inch of trace length.

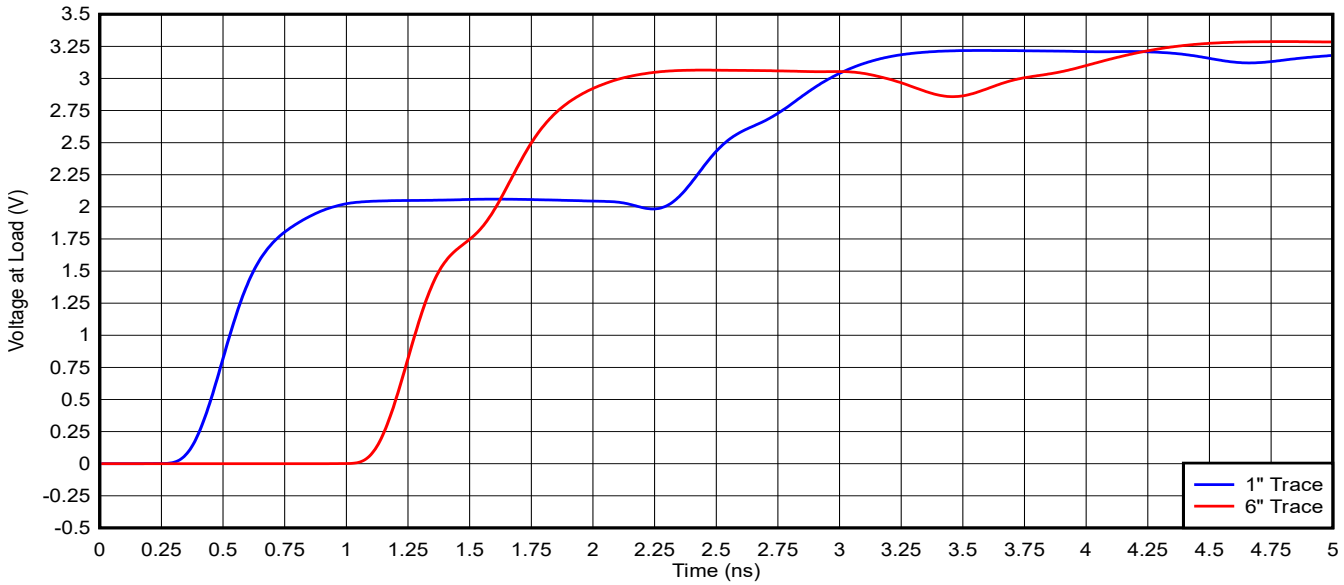

Figure 5-4. Trace Length Mismatch: Rising Edge With 1" and 6" Traces

In the case where multiple loads all have mismatched lengths, the result can be something that appears like a *stair step* response with a series of reflections at varying time intervals instead of a clean rising edge.

6 Application Example: FPD-Link

FPD-Link devices require an external REFCLK, typically 25MHz or 27MHz LVCMOS in most applications. For this experiment, one LVCMOS oscillator generated the REFCLK signal for two DS90UB971 serializer and US90UB9702 deserializer pairs. REFCLK was generated with a CDC6C BAW oscillator, and fanned out to the two FPD-Link SerDes pairs using trace 3 on the multi-load board (fanned out to 2 loads, 2" trace length split near the oscillator). A smaller coupon board was used to add an additional 2" of trace length, for 4" in total. SMA to 2-pin female header cables connected the multi-load board to the external REFCLK header on two DS90UB9702 EVMs.

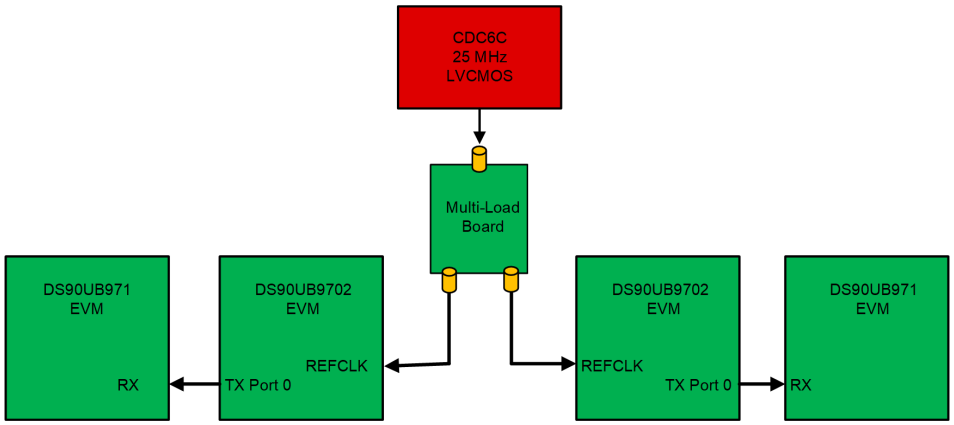

Figure 6-1. CDC6C Providing REFCLK for 2 FPD-Link SerDes Pairs: Block Diagram

With both FPD-Link SerDes pairs sharing a REFCLK, link was established without any errors. An Eye Opening Margin (EOM) test was performed to make sure that each pair was generating a stable link. Both DS90UB971/9702 pairs were able to maintain link simultaneously with a shared REFCLK signal across a sweep of EQ settings. This test confirms that this can be possible for a single LVCMOS oscillator to drive multiple loads in some applications.

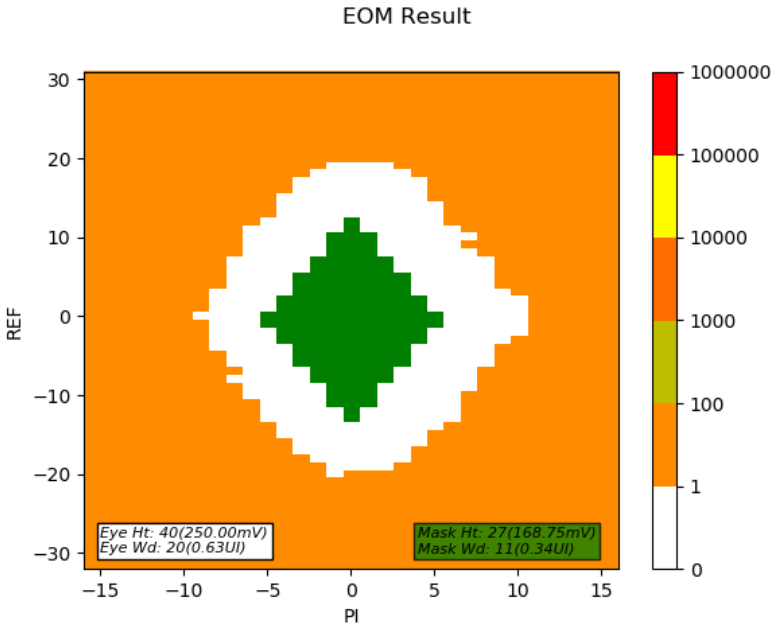

Figure 6-2. FPD-Link Eye Opening Margin (EOM) Result

7 Summary

These simulation results and lab measurements have shown some of the factors to determine if driving multiple loads with a single LVCMOS oscillator is feasible in a system. Driving multiple loads from a single LVCMOS oscillator can always degrade signal integrity in some way. For best performance one can limit the numbers of loads which needs to be directly driven by an oscillator by using a *Clock Buffer*.

Guidelines for driving multiple loads with a single oscillator:

- Limit the number of loads to 2 to minimize performance degradation in terms of reduced rise or fall time, excessive signal reflections, and reduced signal amplitude
- Maximize common trace length before branching out to individual receivers as shown in Star Line topologies
- Limit total receiver capacitance to achieve fast rise/fall time

These guidelines can provide a basis for driving multiple loads in your system. By reducing the number of loads, reducing the branch trace length, and reducing the total parasitic and receiver capacitance, you can minimize the negative consequences of driving multiple loads with a single oscillator in your system. The Star Line topology best models this kind of routing situation. If achieving absolute best performance is a priority, traces can never be split into multiple loads and instead a clock buffer like the *4-Channel Output LVCMOS 1.8-V Buffer* can be used to fanout the clock signal and drive multiple loads.

8 References

- Texas Instruments, *LMK6x Low Jitter, High-Performance BAW Oscillator,* data sheet.
- Texas Instruments, *CDC6Cx Low Power LVCMOS Output BAW Oscillator*, data sheet.
- Texas Instruments, *LMK1C110x 1.8-V, 2.5-V, and 3.3-V LVCMOS Clock Buffer Family,* data sheet.

9 Revision History

Changes from Revision A (April 2025) to Revision B (May 2025) **Page**

- Added *Trace Length Mismatch Between Loads* section....12

Changes from Revision * (August 2024) to Revision A (April 2025) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document 1
- Added *Simulation Setup* section....3
- Updated single-line termination images.... 4
- Updated star-line termination images....6
- Updated split line termination images....7
- Updated image.... 8
- Added *Lab Measurement Setup* section.... 9
- Added *Lab Measurement Results and Correlation to Simulation Data* section....10
- Added *Application Example: FPD-Link* section.... 14
- Added additional detail to guidelines and general recommendations for driving multiple loads....15
- Added *CDC6Cx* data sheet reference.... 15

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