156.25MHz / 312.5MHz,
LVPECL,
PHY Recovered

25MHz, LVDS,
PHY Recovered or Local

100MHz, LVDS,
PHY Backup

1PPS, LVCMOS

48MHz, LVCMOS

LMK6CE048
BAW OSC

I2C/SPI

IN0
IN1
IN2 **LMK5B33414**
Network Synchronizer
&
IN3 Jitter Cleaner
XO
SDA/SDI
SCL/SCK

312.5MHz, HSDS

25MHz, LVDS

IN0 OUT[0:2]
LMK1D1204
1:4 LVDS Buffer
OUT3

25MHz, LVDS

Test Point

156.25MHz, LVDS

50MHz, HSDS

1-PPS, 1.8V LVCMOS

Test Point

1-PPS, 1.8V LVCMOS

25MHz, HSDS

LMK3H0102
PCIe Clock
Generator

25MHz, LVCMOS

100MHz, LP-HCSL

100MHz, LP-HCSL

8x DIFF

3x DIFF

SYNC0
SYNC1
CPU
CPLD_REFCLK
PCIE_REFCLK

PCIe

PLL_REFCLKP/N_0
PLL_REFCLKP/N_1
PLL_REFCLKP/N_2
PLL_REFCLKP/N_3
PLL_REFCLKP/N_4
PLL_REFCLKP/N_5
PLL_REFCLKP/N_6
PLL_REFCLKP/N_7

TIMESTAMP_REFCLK
PTP_SYNC_0
PTP_SYNC_1

MGMT_REFCLK

PROG_REFCLK

112G or 224G PAM-4 SerDes
800G Switch

PCIE_REFCLK

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TID #: N/A	Project Title: 400G & 800G Network Switch Reference Design	
Number: N/A Rev: B	Sheet Title: Network Switch Block Diagram	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 1 of 7
Drawn By: Riley Nguyen	File: Network Switch Block Diagram.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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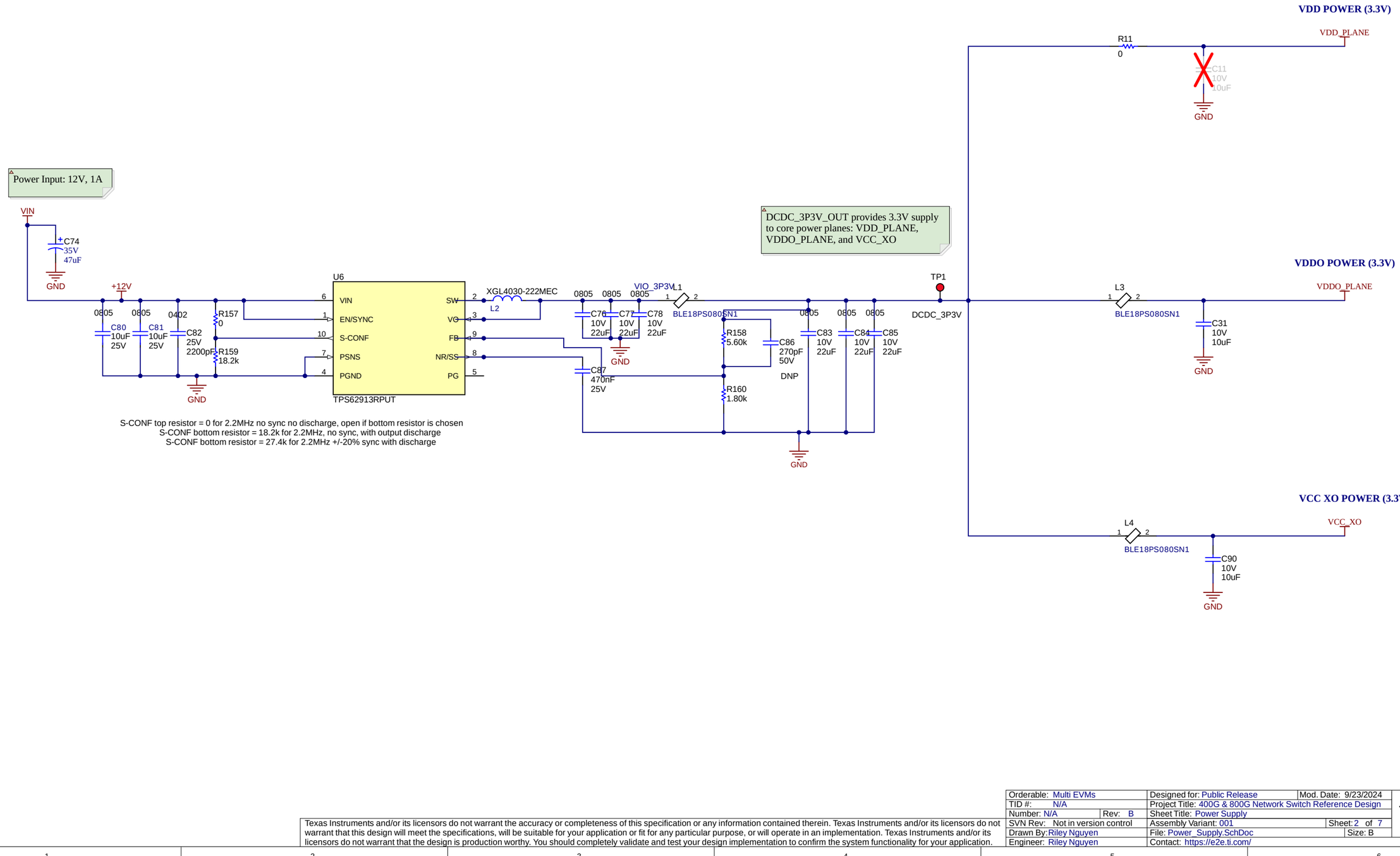

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Number: N/A Rev: B	Sheet Title: Power Supply	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 2 of 7
Drawn By: Riley Nguyen	File: Power_Supply.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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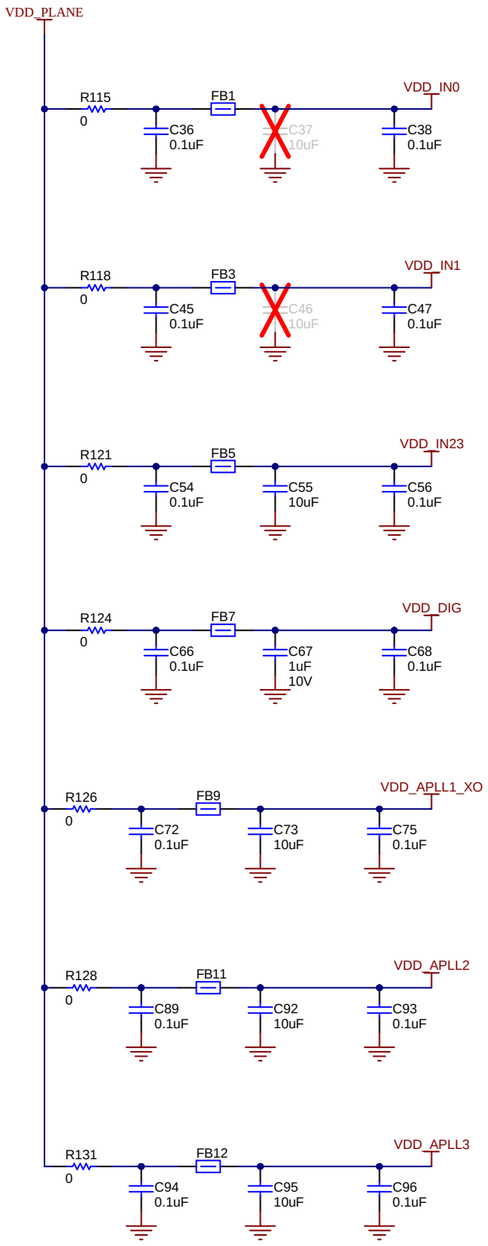
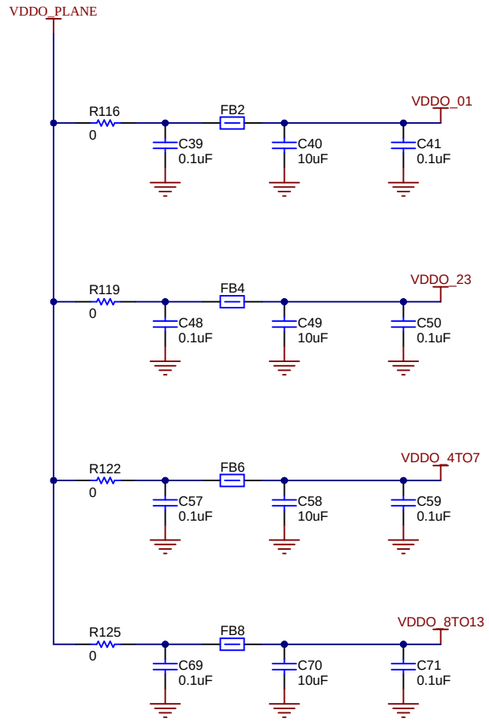
LMK5B33414 VDD CORE SUPPLY

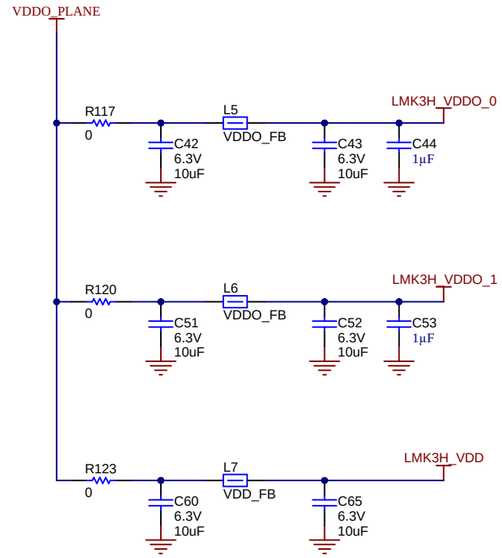


LMK5B33414 VDDO OUTPUT SUPPLY



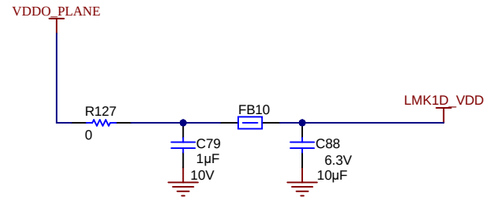
Place C38, C47, C56, C68, C75, C93, C96, C41, C50, C59, C71 close to LMK3B33414

LMK3H0102 VDD & VDDO SUPPLY

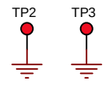


Place C44, C53 close to LMK3H0102

LMK1D1204 LDD SUPPLY



GND TEST POINTS



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TID #: N/A	Project Title: 400G & 800G Network Switch Reference Design	
Number: N/A Rev: B	Sheet Title: Power Distribution	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 3 of 7
Drawn By: Riley Nguyen	File: Power_Dist.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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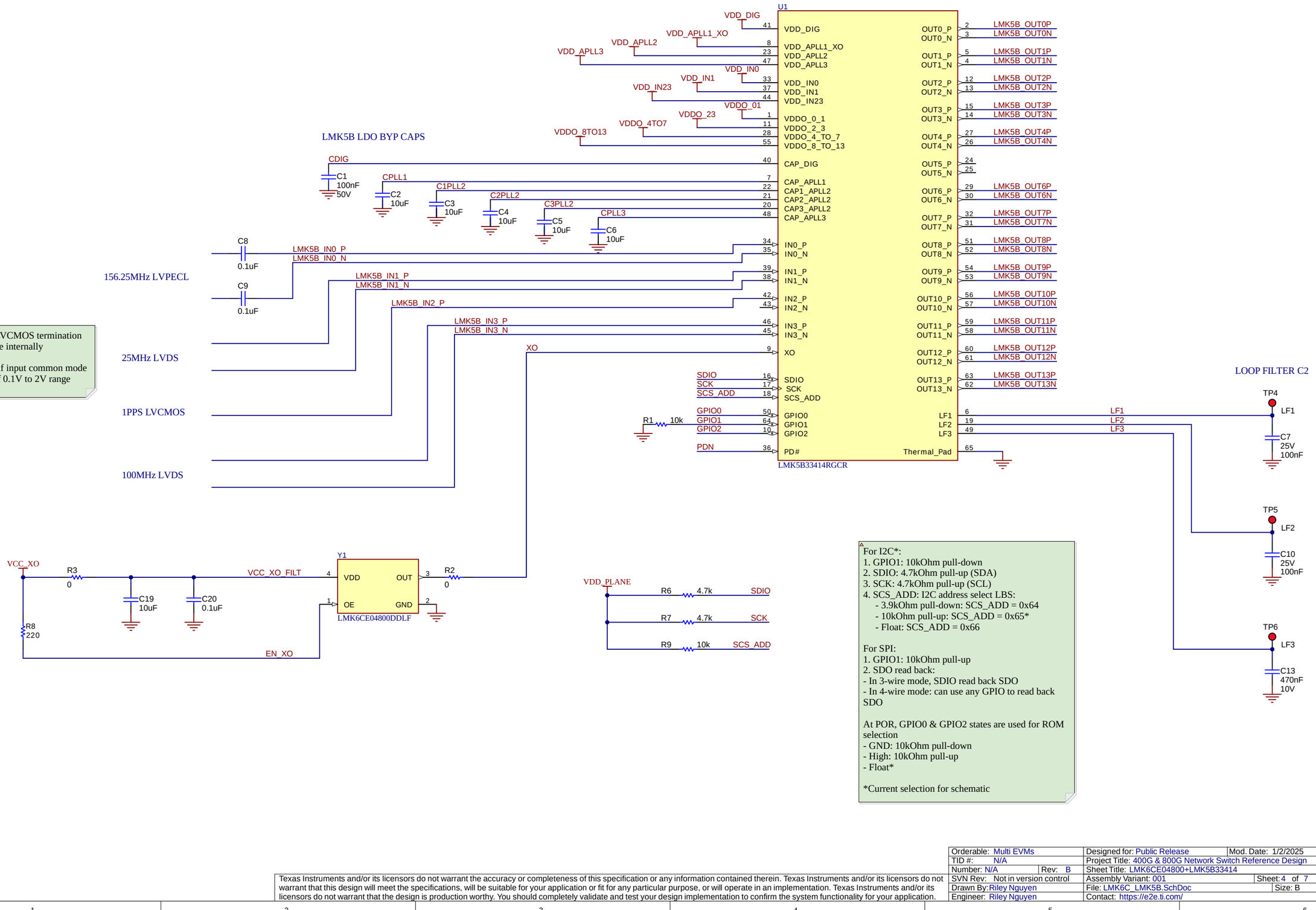

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TID #: N/A	Project Title: 400G & 800G Network Switch Reference Design	
Number: N/A Rev: B	Sheet Title: LMK6CE04800+LMK5B33414	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 4 of 7
Drawn By: Riley Nguyen	File: LMK6C_LMK5B.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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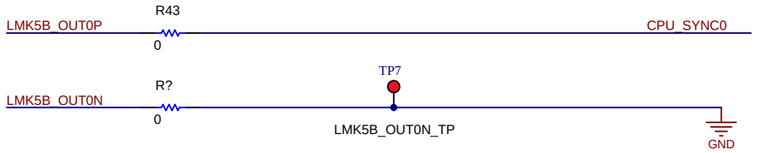
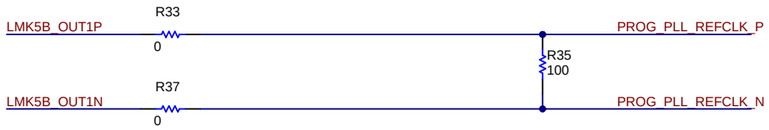
1. For HSDS/LVDS outputs, 100Ohm load is not present internally. Place external 100Ohm load close to receiver side.

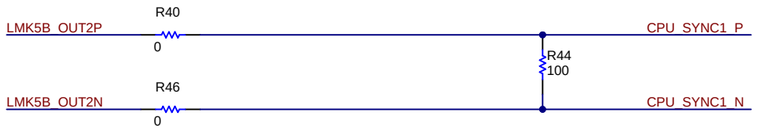
2. Termination on OUT3 is placed close LMK1D1204 IN0, page 6.



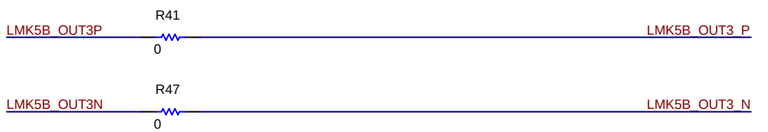
1PPS 1.8V LVCMOS
To CPU



50MHz HSDS
To 112G/224G PAM4 SerDes

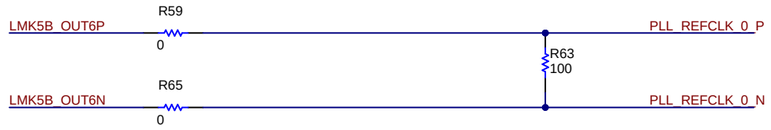


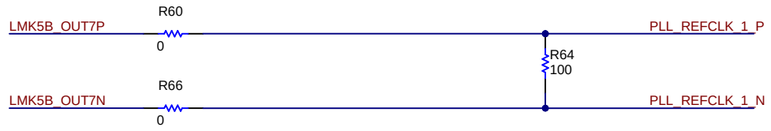
25MHz LVDS
To CPU

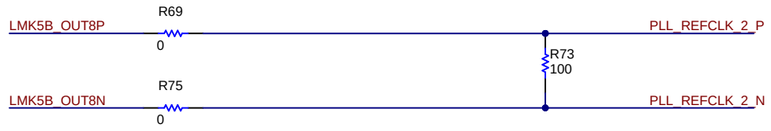


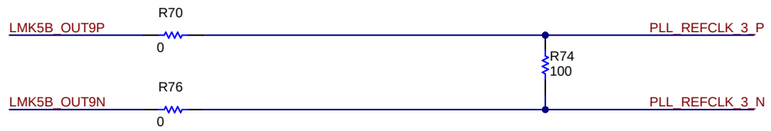
25MHz LVDS
To LMK1D1204

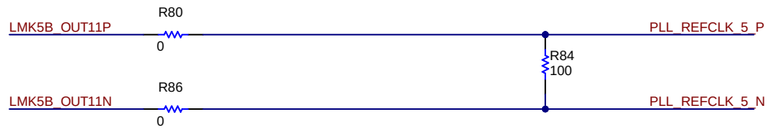
156.25MHz HSDS
To 112G/224G PAM4 SerDes

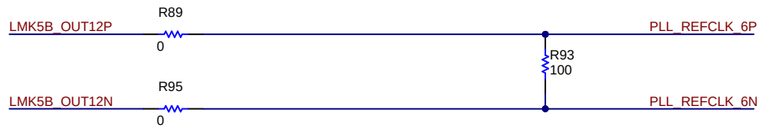


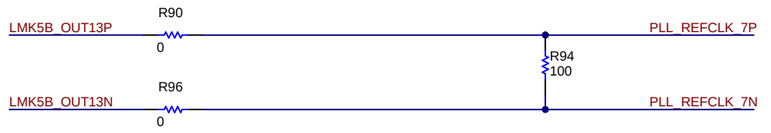












312.5MHz HSDS
To 112G/224G PAM4 SerDes

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TID #: N/A		Project Title: 400G & 800G Network Switch Reference Design	
Number: N/A	Rev: B	Sheet Title: LMK5B33414 Outputs	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 5 of 7
Drawn By: Riley Nguyen		File: LMK5B_Outputs.SchDoc	Size: B
Engineer: Riley Nguyen		Contact: https://e2e.ti.com/	

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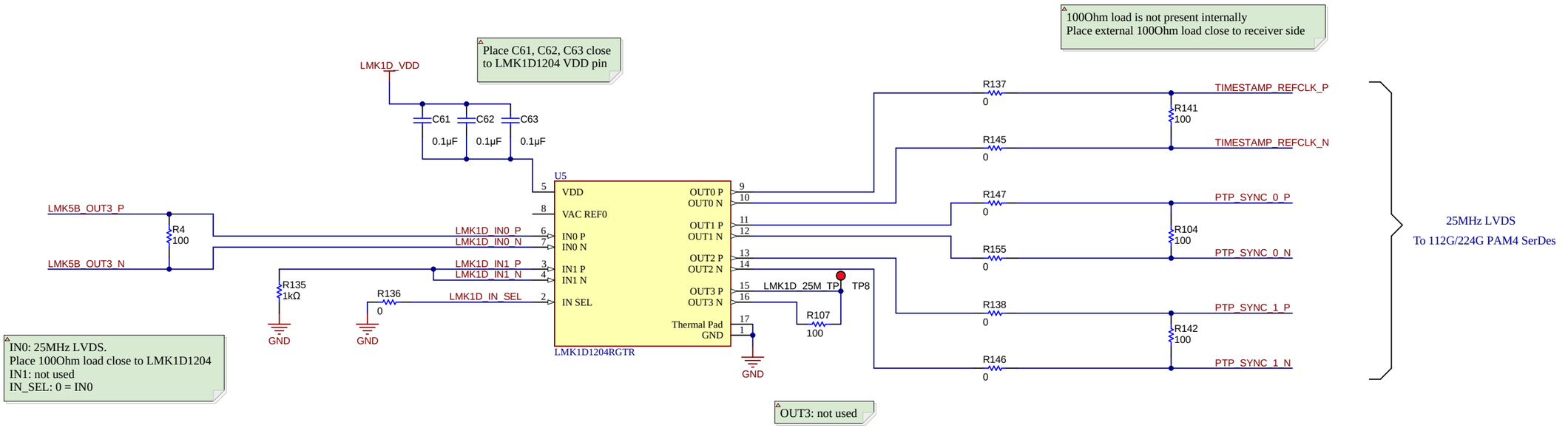

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Number: N/A	Rev: B	Sheet Title: LMK1D1204	
SVN Rev: Not in version control		Assembly Variant: 001	Sheet: 6 of 7
Drawn By: Riley Nguyen		File: LMK1D.SchDoc	Size: B
Engineer: Riley Nguyen		Contact: https://e2e.ti.com/	

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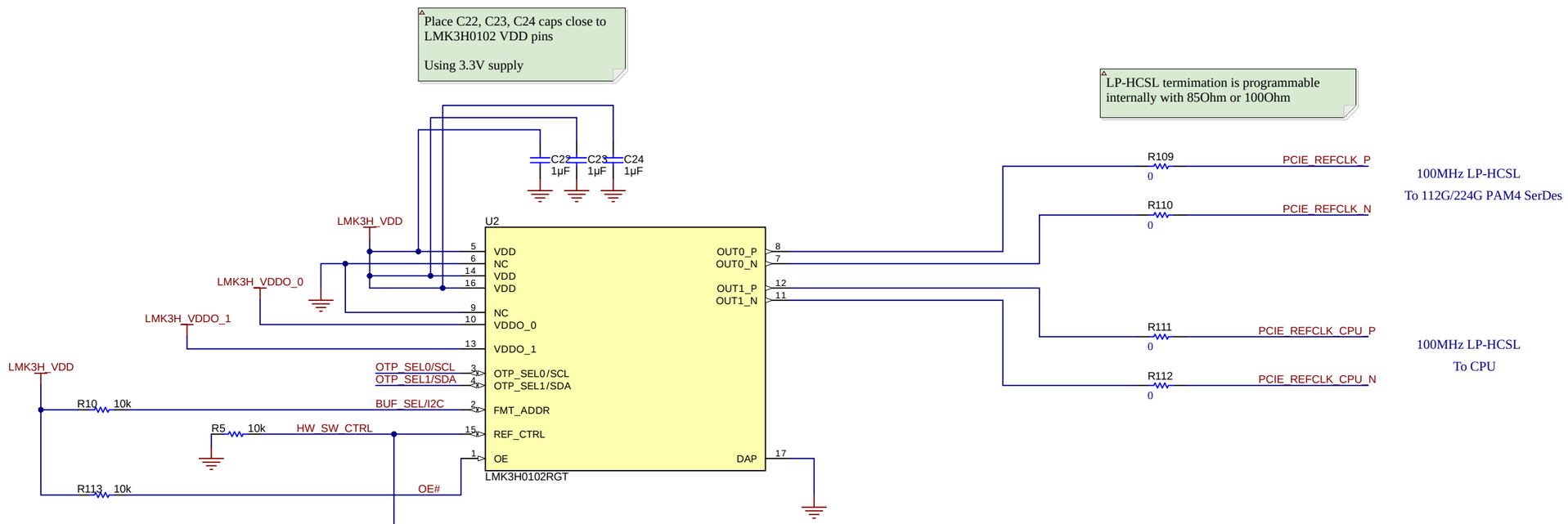
Place C22, C23, C24 caps close to LMK3H0102 VDD pins

Using 3.3V supply

LP-HCSL termination is programmable internally with 85Ohm or 100Ohm



Place R114 close to REF_CTRL pin for LVCMOS termination

For I2C:
1. REF_CTRL: 10kOhm pull-up*
2. FMT_ADDR: I2C address
   - 3.9kOhm pull-down: 0x68
   - 10kOhm pull-up: 0x69*
   - Tied to SDA: 0x6A
   - Tied to SCL: 0x6B
3. OTP_SEL0/SCL and OTP_SEL1/SDA: I2C SCL and SDA

For OTP (one time programming):
1. REF_CTRL: 10kOhm pull-down
2. FMT_ADDR: ignored by default or can be used to control output format by overriting OUT_FMT_SRC_SEL = 1
3. OTP_SEL0/SCL and OTP_SEL1/SDA: use for OTP page selection

OE:
1. 10kOhm pull-up: enable all outputs*
2. 3.9kOhm pull-down: disable all outputs

After POR: REF_CLK is used as CMOS output*

*Current selection for schematic

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TID #: N/A	Project Title: 400G & 800G Network Switch Reference Design	
Number: N/A Rev: B	Sheet Title: LMK3H0102	
SVN Rev: Not in version control	Assembly Variant: 001	Sheet: 7 of 7
Drawn By: Riley Nguyen	File: LMK3H.SchDoc	Size: B
Engineer: Riley Nguyen	Contact: https://e2e.ti.com/	

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