National Semiconductor

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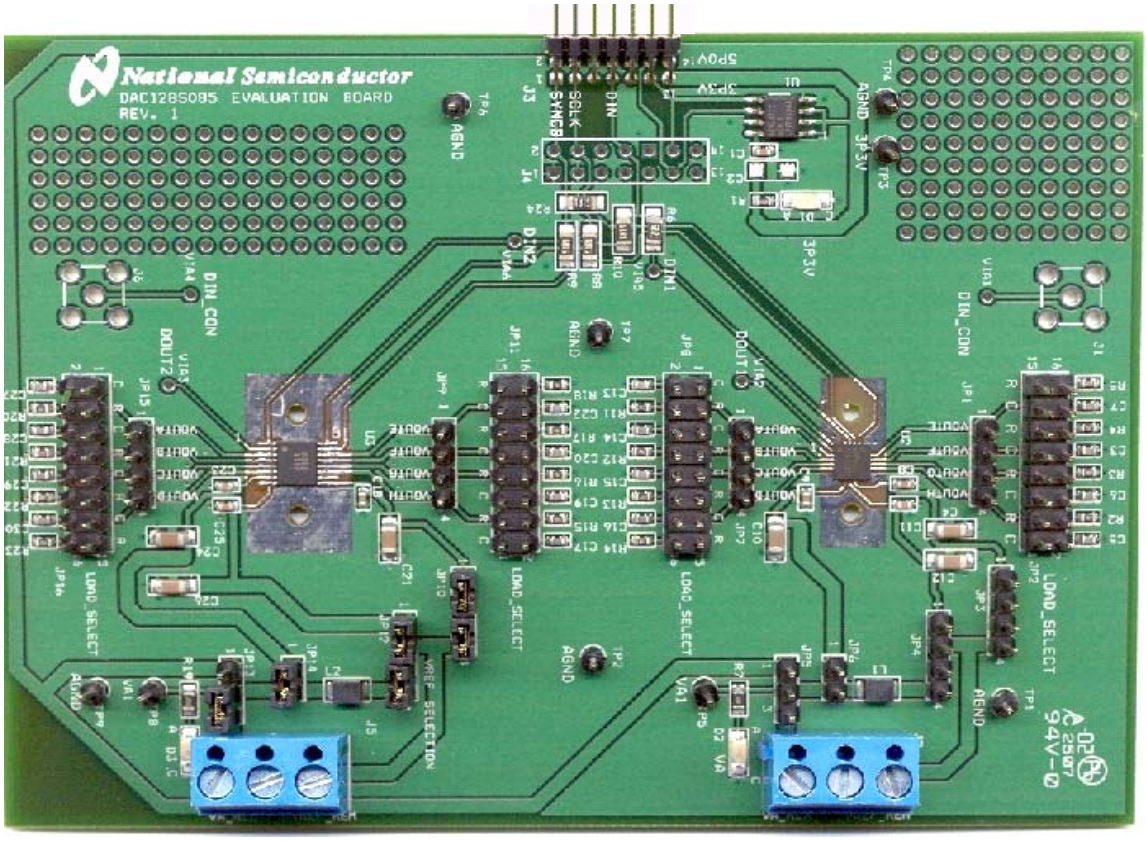
KTD

Evaluation Board User's Guide

DAC128S085 12-Bit, DAC108S085 10-Bit, DAC088S085 8-Bit

OCTAL Micro Power Digital-to-Analog Converter with Daisy Chain Capability



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1.0 Introduction

The DAC128S085EB Design Kit (consisting of the DAC128S085 Evaluation Board and this User's Guide) is designed to ease evaluation and design-in of the National Semiconductor DAC128S085 12-Bit, DAC108S085 10-Bit, and DAC088S085 8-Bit OCTAL Micro Power Digital-to-Analog Converter with Daisy Chain Capability. This family of pin-compatible DACs will be referenced throughout this document as the DAC128S085.

The evaluation board can be used in either of two modes. In the Stand-Alone mode suitable test equipment, such as a pattern generator and signal analyzer, can be used with the board to evaluate the DAC128S085 performance.

In the Computer mode, data capture and evaluation are simplified by connecting this board to National Semiconductor's Data Capture Board (order number WAVEVSN BRD 4.1 or higher). The Data Capture (referenced throughtout this document as the WV4) Board is connected to a personal computer running WaveVision software through a USB port. The WaveVision 4 software runs on Microsoft Windows, and the latest version can be downloaded from the web at http://www.national.com/adc.

Note: WaveVision Software version 4.4 or later is required to evaluate this part with the WV4 Evaluation System.

The WaveVision software allows the user to drive the DAC128S085 with a variety of preset and custom waveforms. The software also allows the user to select the clock frequency of the serial interface.

Data transmitted to the DAC128S085 via a serial interface is converted to an analog waveform by U2/U3, the DAC128S085. The board supports two different packages, LLP (U2) and TSSOP (U3), and these packages can either be driven simultaneously or individually.

Note: The eval board contains two packages with separate headers for outputs, loads, power, ect. For the remainder of this document, the headers for the different packages are separated by a forward slash, with the first value being for the LLP and the second value being for the TSSOP (LLP/TSSOP).

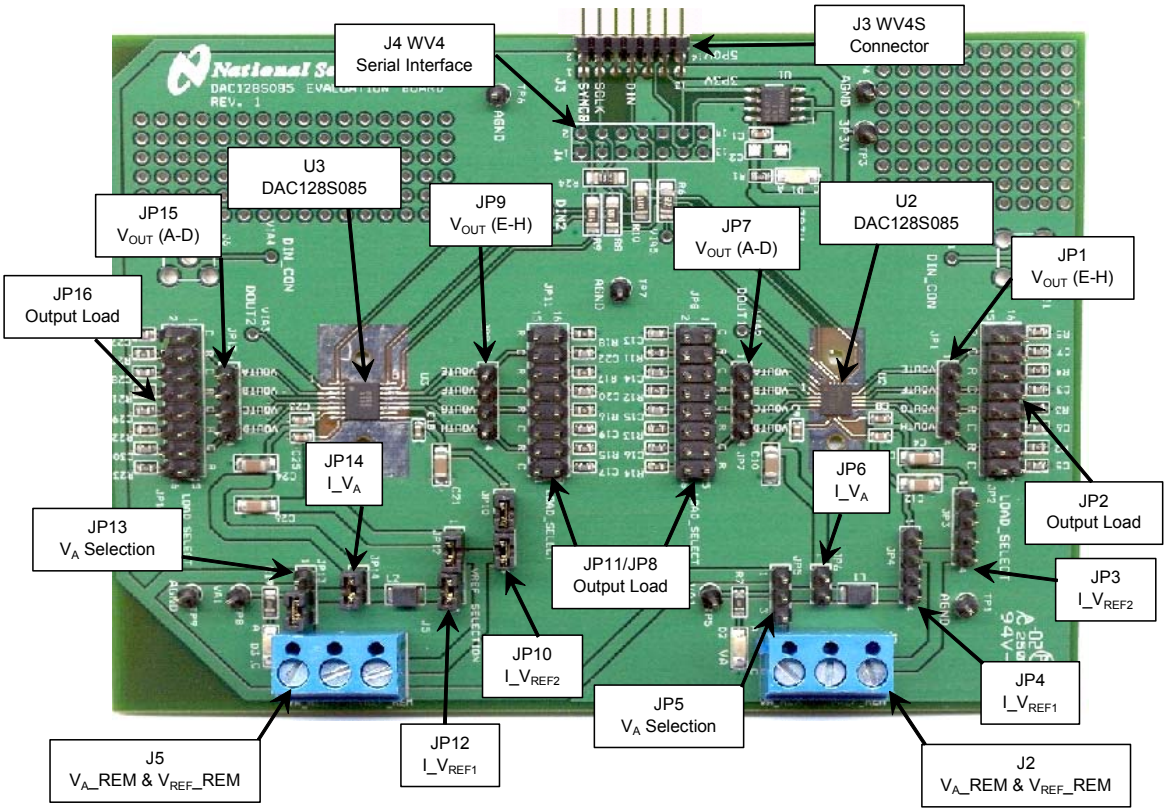


Figure 1: Locations of Test Points and Major Components

2.0 Board Assembly

The DAC128S085 evaluation board comes fully assembled and ready for use with the WV4 (or higher) system. Refer to the Bill of Materials for a description of components, to *Figure 1* for major component placement, and to *Figure 7* for the Evaluation Board schematic.

3.0 Quick Start

The DAC128S085 evaluation board may be used in the Stand-Alone mode or Computer mode. In Stand-Alone mode, a Pattern Generator is used to drive the DAC128S085, and a Signal Analyzer is used to evaluate the analog output signal. In Computer Mode, a WV4 board is used to drive the DAC128S085 and a Signal Analyzer is used to evaluate the analog output signal.

3.1 Stand-Alone Mode

Refer to *Figure 1* or the evaluation board schematic (*Figure 7*) for locations of test points and major components.

1. Connect a clean analog (not switching) +5V power source with a 500mA current limit to pin 3 of header **J2/J5** on the DAC128S085 board, ground pin 2 and turn on the power. Place a jumper across pins 2 & 3 of header **JP5/JP13** to select VA_REM (V_A Remote).
2. Place a jumper across pins 1 & 2 of **JP6/JP14** to power the V_A of the DAC128S085.
3. The default setup is to use the VA_REM to power both V_A and V_{REF}. To do this, place jumpers in the following locations (see *table 1* for details):
   - **JP4/JP12** – pins 1 & 2 and pins 3 & 4
   - **JP3/JP10** – pins 1 & 2 and pins 3 & 4
4. To use separate supplies for V_A and V_{REF}, connect a clean analog (not switching) +5V power source with a 500mA current limit to pin 1 of header **J2/J5** and turn on the power. Place jumpers in the following locations (see *table 1* for details):
   - **JP4/JP12** – pins 1 & 2
   - **JP3/JP10** – pins 1 & 2 and pins 3 & 4
5. Create the digital waveforms seen in *Figure 2* with your Logic Generator. Ensure that SCLK does not exceed 40MHz. Refer to the DAC128S085 Datasheet for further details.

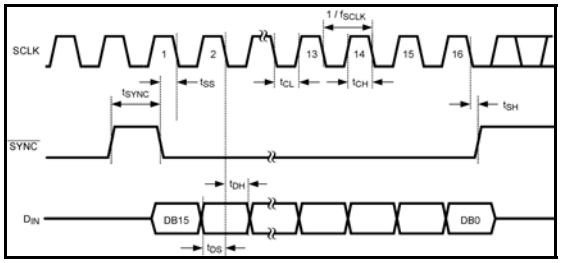


Figure 2: Digital Input Timing Diagram
(*Refer to Appendix 2.0 for an enlarged version*)

6. Connect your Logic Generator to the Serial Interface header J4 (not currently populated). Refer to *Figure 3* below for connection details.

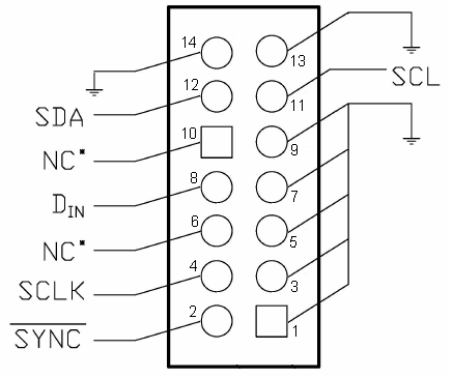


Figure 3: J4 (WV4) Serial Interface Header

7. The Analog Output signals of each channel can be seen DC coupled at header JP1/JP15 for outputs A-D and header JP7/JP9 for outputs E-H.
8. Select the desired output load by adding jumpers to headers JP8/JP16 for outputs A-D and JP2/JP11 for outputs E-H. See *Figure 4* for the configuration of header JP8. Refer to *table 1* in Section 4.0 or the evaluation board schematic (*Figure 7*) for all configurations.

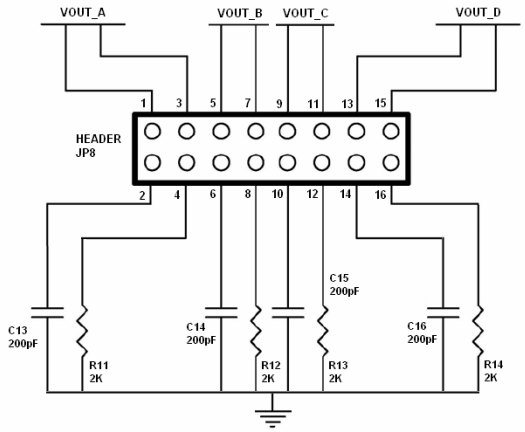


Figure 4: JP8 Load Select Header

3.2 Computer Mode

Refer to *Figure 1* for locations of test points and major components.

1. Run the WaveVision 4 program. While the program is loading continue below.
2. Connect the J3 header on the DAC128S085 Evaluation board to the J7 serial connector on the WV4 board. The Evaluation board can either be powered by an external supply (recommended) through J2/J5 or by the +5.0V and +3.3V supply from the WaveVision. Refer to *Figure 5* for the serial connection and *Figure 6* for specific pin connection details.

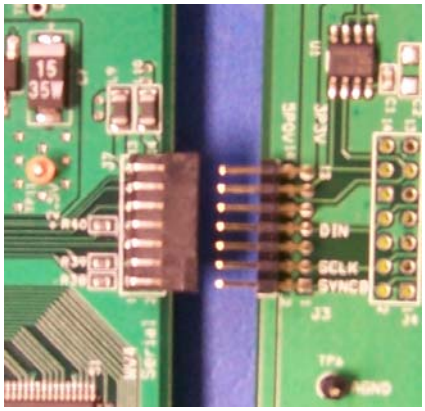


Figure 5: WV4 to DAC128S085 Connection

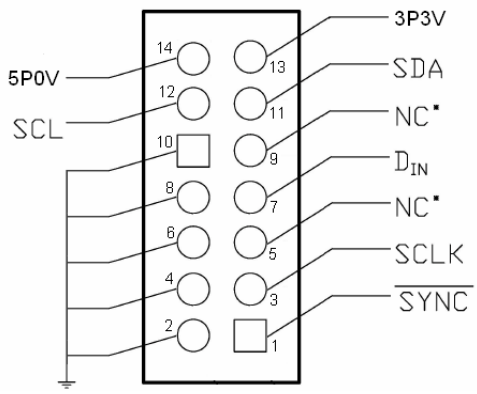


Figure 6: J3 (WV4S) Header Connection

3. Connect a USB cable between the WV4 board and the PC running the WaveVision 4 software.
4. Connect a clean analog (not switching) +5V and 500mA current limit power source to Power Connector J1 on the WV4 board, ground the GND connector and turn on the power.
5. Place a jumper across pins 2 & 3 of **JP5/JP13** on the DAC128S085 board to select VA_REM.
6. V_A and V_{REF} can be supplied either together or separately. The default selection is for V_A and V_{REF} to be supplied from a single source. To accomplish this, place jumpers in the following locations (see *table 1* for further details):
   - **JP6/JP14** - pins 1 & 2
   - **JP3/JP10** - pins 1 & 2 and pins 3 & 4
   - **JP4/JP12** - pins 1 & 2 and pins 3 & 4

   Note: For separate supplies, remove the jumper across pins 3 & 4 of header JP4/JP12.
7. Perform steps 7 and 8 of section 3.1 above.
8. Refer to section 5.0, "Software Operation and Settings."

4.0 Functional Description

Table 1 describes the function of the various jumpers on the DAC128S085 evaluation board. The Evaluation Board schematic is shown in *Figure 7*.

Jumper	Pins 1 & 2	Pins 2 & 3
JP5/ JP13	Select VA=5V from WV4.1 Board	Select VA_REM from J2/J5
JP6/ JP14	Power VA on DAC128S085	NA

Jumper	Pins 1 & 2	Pins 3 & 4
JP3/ JP10	Power VREF2 on DAC128S085	Power VREF2 on DAC128S085
JP4/ JP14	Power VREF1 on DAC128S085	Uses one supply voltage for V_A and V_{REF}, separate supplies if removed

Pin	JP8/ JP16	JP2/ JP11
1 & 2	Select 200pF Output Load Capacitance VOUT_A	Select 200pF Output Load Capacitance VOUT_E
3 & 4	Select 2kΩ Output Load Resistance VOUT_A	Select 2kΩ Output Load Resistance VOUT_E
5 & 6	Select 200pF Output Load Capacitance VOUT_B	Select 200pF Output Load Capacitance VOUT_F
7 & 8	Select 2kΩ Output Load Resistance VOUT_B	Select 2kΩ Output Load Resistance VOUT_F
9 & 10	Select 200pF Output Load Capacitance VOUT_C	Select 200pF Output Load Capacitance VOUT_G
11 & 12	Select 2kΩ Output Load Resistance VOUT_C	Select 2kΩ Output Load Resistance VOUT_G
13 & 14	Select 200pF Output Load Capacitance VOUT_D	Select 200pF Output Load Capacitance VOUT_H
15 & 16	Select 2kΩ Output Load Resistance VOUT_D	Select 2kΩ Output Load Resistance VOUT_H

Table 1: Jumper Configurations

4.1 Serial Interface

In Computer Mode, the serial interface is driven by the WV4 board. The WaveVision 4 software allows the user to drive the DAC128S085 with various digitized signals. Refer to "Software Operation and Settings" for further information.

In Stand-Alone Mode, the serial interface must be driven by an external device. The three-wire interface (SCLK, SYNC, D_{IN}) is compatible with SPI, QSPI and MICROWIRE, as well as most DSPs. See the Timing Diagram (*Figure 2*) for information on a write sequence.

The maximum digital input level of the three-wire interface is independent of the analog supply voltage (V_A). The range of all digital inputs is 0V to 5.25V regardless of V_A.

A write sequence begins by bringing the SYNC line low. Once SYNC is low, the *Binary* data on the D_{IN} line is clocked into the 16-bit serial input register on the falling edges of SCLK. After the 16th falling clock edge, the SYNC is brought high and the programmed function (a change in the mode of operation and/or a change in the DAC register contents) is executed. For a new write sequence to be executed, SYNC must be brought high for the minimum specified time.

Since the D_{IN} buffer draws more current when it is high, it should idle low between write sequences to minimize power consumption.

Please refer to the DAC128S085 datasheet for more information.

4.2 DAC Reference Circuitry

The reference voltage for the DAC128S085 is selected by JP3/JP10 and JP4/JP14, see *table 1* for further details. The reference can either be supplied separatly or using the supply voltage V_A. In both cases, the range of V_{REF} is +0.5V to +5.5V. The analog output range of the DAC128S085 can be set anywhere from 0V to V_{REF}.

4.3 Analog Output

The analog output of this evaluation board is available DC coupled at the header JP7/JP15 and JP1/JP9. For loaded outputs refer to *Figure 4* and *table 1*.

4.4 Power Supply Connections

In Computer mode, the board can be powered by either an external supply or the local WV4 board supply. In Stand-alone mode, the DAC128S085 board must be powered by an external supply.

If you wish to supply V_A externally, connect a DC voltage supply to connector J2/J5 and place a jumper across pins 2 & 3 of JP5/JP13 to select V_A_REM. The supply voltage (V_A) can be set anywhere from 0V to V_{REF}.

If the supply voltage (V_A) serves as the reference for the DAC128S085, ensure a clean power supply is used.

5.0 Software Operation and Settings

The WaveVision software is included with the WV4 board and the latest version can be downloaded from National's web site at http://www.national.com/adc. WaveVision software version 4.4 or later is required to evaluate this device with the WV4 system.

To install this software, follow the procedure in the WAVEVSN BRD 4.1 User's Guide. Once the software is installed, run it and set it up as follows:

Note: Before continuing, ensure that the WaveVision Hardware is setup according to Section 3.2.

1. From the WaveVision main menu, go to Settings, then Capture Settings to open the System Settings window.
2. Under board type, select WaveVision 4 (USB).
3. Turn on the power to both boards, then click on the **"Test"** button and await the firmware download. *After the firmware has downloaded, WaveVision will open up a control panel for the DAC128S085*.
4. Click on the **"Accept"** button to close the System Settings Dialog.
5. From the DAC128S085 Control Panel, configure the digital waveform to be converted by the DAC. *Please see the WV4 User's Manual for detailed instructions. The ability to drive preset waveforms or custom data is provided.*
6. Press the **"Start"** button to begin driving the digital waveform to the DAC.

The WV4 Board will continuously send the waveform out to the DAC128S085 until the **"Stop"** button is pressed. Please refer to S*ection 4.3* for details on measuring the Analog Output of the DAC.

The Digital Waveform is plotted in the main WaveVision window for added convenience. See the WV4 Board User's Guide for details.

If this board is used in conjunction with the WAVEVSN BRD 4.1 Data Capture Board and WaveVision software, a USB cable is needed to connect WAVEVSN BRD 4.1 to the host computer. See the WV4 Board User's Guide for details.

6.0 Evaluation Board Specifications

Board Size:	4.85" x 3.55" (12.3 cm x 9 cm)	
Power Requirements	Min: +2.7V , 3 mA	Max: +5.5V, 5 mA
Max Clock Frequency:	40 MHz	
Analog Output	DC Coupled	
Impedance:	User Selectable: 2KΩ, 200pF, or ∞	

7.0 Hardware Schematic

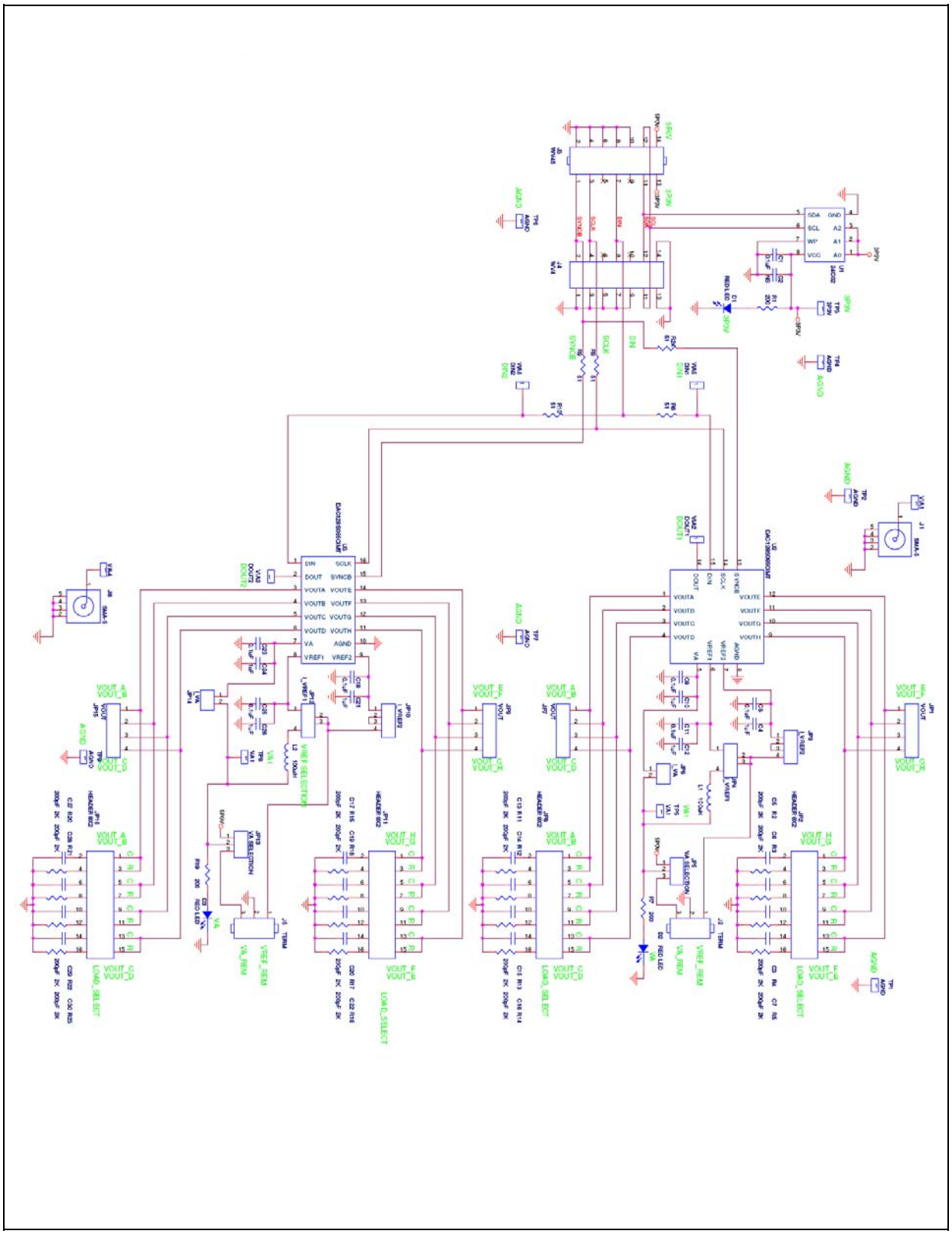


Figure 7: DAC128S085 Evaluation Board Schematic

8.0 Board Layouts

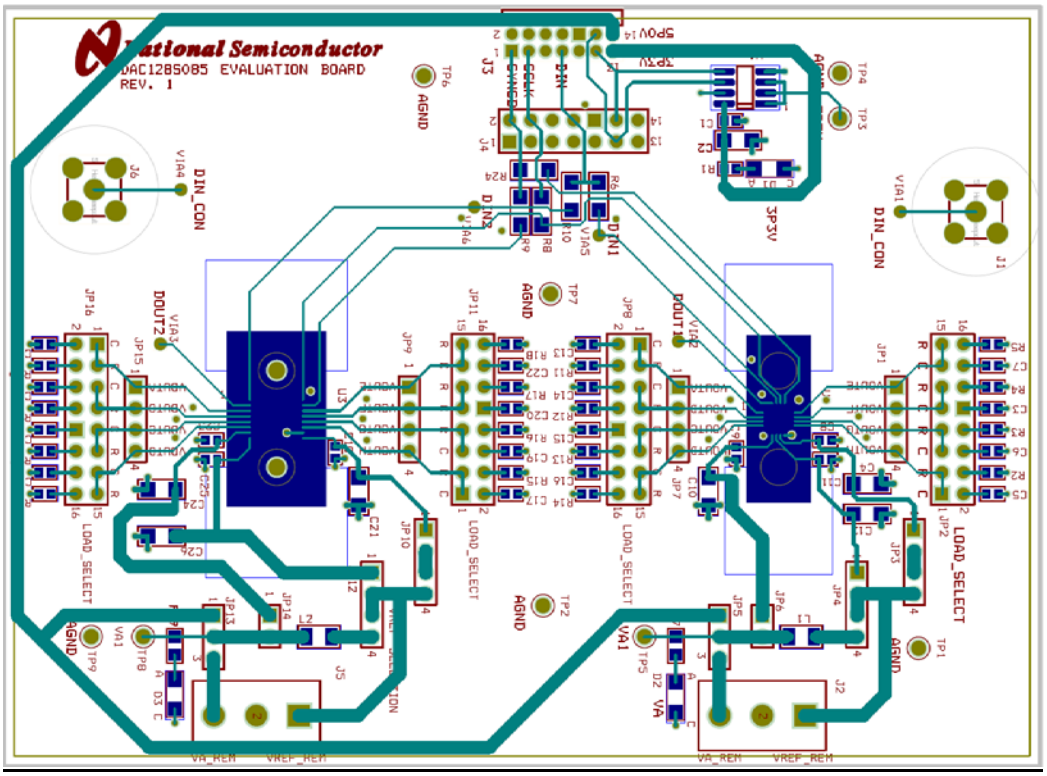


Figure 8: DAC128S085 Evaluation Board Top Layer with Silk Screen

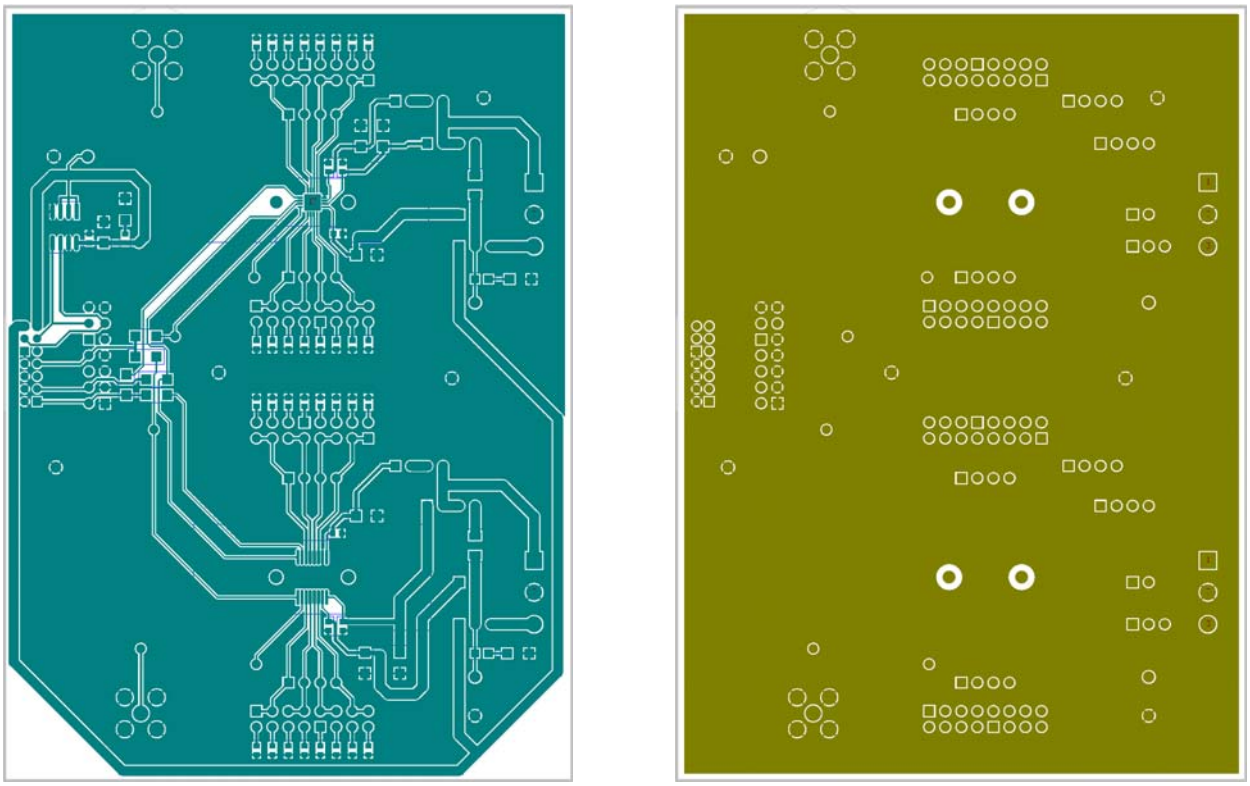


Figure 9: DAC128S085 Evaluation Board Top Layer (left) and Bottom Layer (right)

9.0 Evaluation Board Bill of Materials

Qty.	Reference	PCB Footprint	Source	Source Part #	Rating	Value
7	C1,C8,C9,C11,C18, C23,C25	sm/c_0603			10V	0.1uF
1	C2	sm/c_1206			10V	NS
16	C3,C5,C6,C7,C13,C14, C15,C16,C17,C19,C20, C22,C27,C28,C29,C30	sm/c_0603			10V	200pF
6	C4,C10,C12,C21,C24, C26	sm/c_1206			10V	1uF
3	D1,D2,D3	sm/led_21	Digikey	516-1440-1-ND		RED LED
4	JP1,JP7,JP9,JP15	blkcon.100/vh/tm1sq/w.100/4	Digikey	S1011E-36-ND		VOUT
4	JP2,JP8,JP11,JP16	BLKCON.100/VH/TM2OE/W.200/16/STD	Digikey	S2041E-30-ND		HEADER 8X2
2	JP3,JP10	blkcon.100/vh/tm1sq/w.100/4	Digikey	S1011E-36-ND		I_VREF2
2	JP4,JP12	blkcon.100/vh/tm1sq/w.100/4	Digikey	S1011E-36-ND		I_VREF1
2	JP5,JP13	blkcon.100/vh/tm1sq/w.100/3	Digikey	S1011E-36-ND		VA SELECTION
2	JP6,JP14	blkcon.100/vh/tm1sq/w.100/2	Digikey	S1011E-36-ND		I_VA
2	J1,J6	rf/sma/v_clr		NS		SMA-5
2	J2,J5	term_block/.300/3pos	Digikey	ED1609-ND		TERM
1	J3	blkcon/2mm/ra/tm2oe/w2mm/14	Digikey	S5803-21-ND		WV4S
1	J4	blkcon.100/vh/tm2oe/w.200/14	Digikey	S2041E-30-ND		WV4
2	L1,L2	sm/l_1206	Digikey	445-1543-1-ND		100uH
1	R1	sm/r_0603				200
16	R2,R3,R4,R5,R11,R12, R13,R14,R15,R16,R17, R18,R20,R21,R22,R23	sm/r_0603				2K
5	R6,R8,R9,R10,R24	sm/r_1206				51
2	R7,R19	sm/r_0805				200
6	TP1,TP2,TP4,TP6, TP7,TP9	TP_500X/50/W_CASE	Digikey	S1011E-36-ND		AGND
1	TP3	TP_500X/50/W_CASE	Digikey	S1011E-36-ND		3P3V
2	TP5,TP8	TP_500X/50/W_CASE	Digikey	S1011E-36-ND		VA1
1	U1	sog.050/8/wg.244/l.200				24C02
1	U2	SOCKET_LLP.50M/16/WG4.00/EXP_PAD				DAC128S085CIMT
1	U3	SOCKET_SOG.65M/16/WG6.40/L5.00				DAC128S085CIMT
2	VIA1,VIA4	tp_37/60	Digikey	NS		DIN_CON
1	VIA2	tp_37/60	Digikey	NS		DOUT1
1	VIA3	tp_37/60	Digikey	NS		DOUT2
1	VIA5	tp_37/60	Digikey	NS		DIN1
1	VIA6	tp_37/60	Digikey	NS		DIN2

APPENDIX

A1.0 Summary Tables of Test Points, Jumpers, and Connectors

Test Points on the DAC128S085 Evaluation Board

TP1: AGND	Ground. Located at the upper right of the board.
TP2: AGND	Ground. Located at the upper middle of the board.
TP3: 3P3V	3.3V test point. Located at the lower left of the board.
TP4: AGND	Ground. Located at the lower left of the board.
TP5: VA	V_A Test Point. Located in the upper left of the board.
TP6: AGND	Ground. Located at the lower right of the board.
TP7: AGND	Ground. Located at the middle of the board.
TP8: VA	V_A Test Point. Located in the upper right of the board.
TP9: AGND	Ground. Located in the upper right of the board.

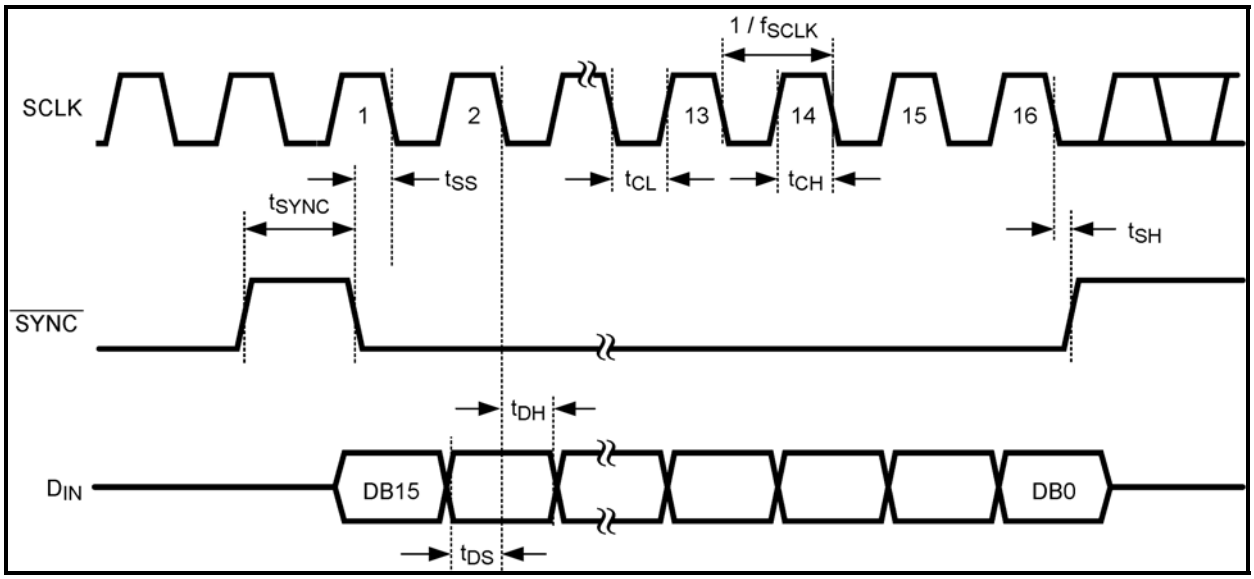
Connectors on the DAC128S085 Evaluation Board

J1: SMA Footprint	Not Used
J2: Terminal Block	VA_REM and VREF_REM. External power supply connector for DAC U2.
J3: WV4.1 Connector	WaveVision 4.1 connector. (Refer to *Figure 6* for a pin-out diagram.)
J4: Serial Interface	Serial Interface connector. (Refer to *Figure 3* for a pin-out diagram.)
J5: Terminal Block	VA_REM and VREF_REM. External power supply connector for DAC U3.
J6: SMA Footprint	Not Used

Selection Jumpers on the DAC128S085 Evaluation Board (Refer to *table 1* in Section 4.0 for configuration details)

JP1: Output Header	DC Coupled output for channels E-H for U2.
JP2: LOAD SELECT	Configures the output load for channels E-H for U2.
JP3: I_VREF2	Powers V_{REF2} and used to measure current going to V_{REF2}.
JP4: I_VREF1	Powers V_{REF1}, measure current going to V_{REF1}, and selection for separate supplies for V_{REF} and V_A.
JP5: VA SELECTION	Selects source of V_A.
JP6: I_VA	Powers V_A and used to measure current going to V_A.
JP7: Output Header	DC Coupled output for channels A-D for U2.
JP8: LOAD SELECT	Configures the output load for channels A-D for U2.
JP9: Output Header	DC Coupled output for channels E-H for U3.
JP10: I_VREF2	Powers V_{REF2} and used to measure current going to V_{REF2}.
JP11: LOAD SELECT	Configures the output load for channels E-H for U3.
JP12: I_VREF1	Powers V_{REF1}, measure current going to V_{REF1}, and selection for separate supplies for V_{REF} and V_A.
JP13: VA SELECTION	Selects source of V_A.
JP14: I_VA	Powers V_A and used to measure current going to V_A.
JP15: Output Header	DC Coupled output for channels A-D for U3.
JP16: LOAD SELECT	Configures the output load for channels A-D for U3.

A2.0 Enlarged Timing Diagram



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