

LMK04610 Evaluation Module

User's Guide



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Preface	3
1 Quick Start Guide	4
1.1 Quick Start Description.....	4
1.2 Device Start-Up Sequence	5
2 Installing the EVM Control Software	6
3 Using the EVM Control Software	7
3.1 Keyboard Shortcuts.....	7
3.2 TICS Pro Overview	7
3.3 TICS Pro with LMK04610 GUI Loaded	8
3.4 GUI: Generic Control	9
3.5 GUI: Operating Modes.....	10
3.6 GUI: OSCin and OSCout.....	11
3.7 GUI: LOS Control.....	11
3.8 GUI: Holdover Control	12
3.9 GUI: Inputs and PLL1.....	13
3.10 GUI: PLL2	14
3.11 GUI: Outputs	15
3.12 GUI: EVM.....	16
4 Configuring the Board	17
4.1 Configuring the Power Supply	17
4.1.1 Supply Plane Source Selection.....	18
4.1.2 Power Distribution	20
4.1.3 VCXO Supply Connection.....	21
4.2 Dip Switch Configuration	22
5 LMK04610 EVM Board Schematics	23
Revision History	30

Overview

Overview

The LMK04610EVM features LMK04610 ultra-low noise and low-power JESD204B compliant Dual Loop Jitter Cleaner. With a power consumption of only typical 880 mW with 10 outputs running, LMK04610 supports typical 65 fs jitter (12 kHz to 20 MHz) using a low noise VCXO module. Integrated LDOs provide high PSRR that enables the use of DC-DC converters.

The dual loop architecture consists of two high-performance phase-locked loops (PLL), a low-noise crystal oscillator circuit, and a high-performance voltage controlled oscillator (VCO). The first PLL (PLL1) provides a low-noise jitter cleaner function while the second PLL (PLL2) performs the clock and SYSREF generation. When used with a very narrow loop bandwidth, PLL1 uses the superior close-in phase noise (offsets below 50 kHz) of the VCXO module or the tunable crystal to clean the input clock. The output of PLL1 is used as the clean input reference to PLL2 where it locks the integrated VCO. The loop bandwidth of PLL2 can be optimized to clean the far-out phase noise (offsets above 50 kHz) where the integrated VCO outperforms the VCXO module.

Features

- Dual Loop Architecture with typical 65 fs rms from 10 kHz to 20 MHz at 122.88-MHz output frequency
- 880 mW typical power consumption for 10 outputs at 122.88 MHz
- JEDEC JESD204B Support
- Jumper configurable supplies with onboard LDOs and DC-DC converters
- GUI platform for full access to device registers

Quick Start Guide

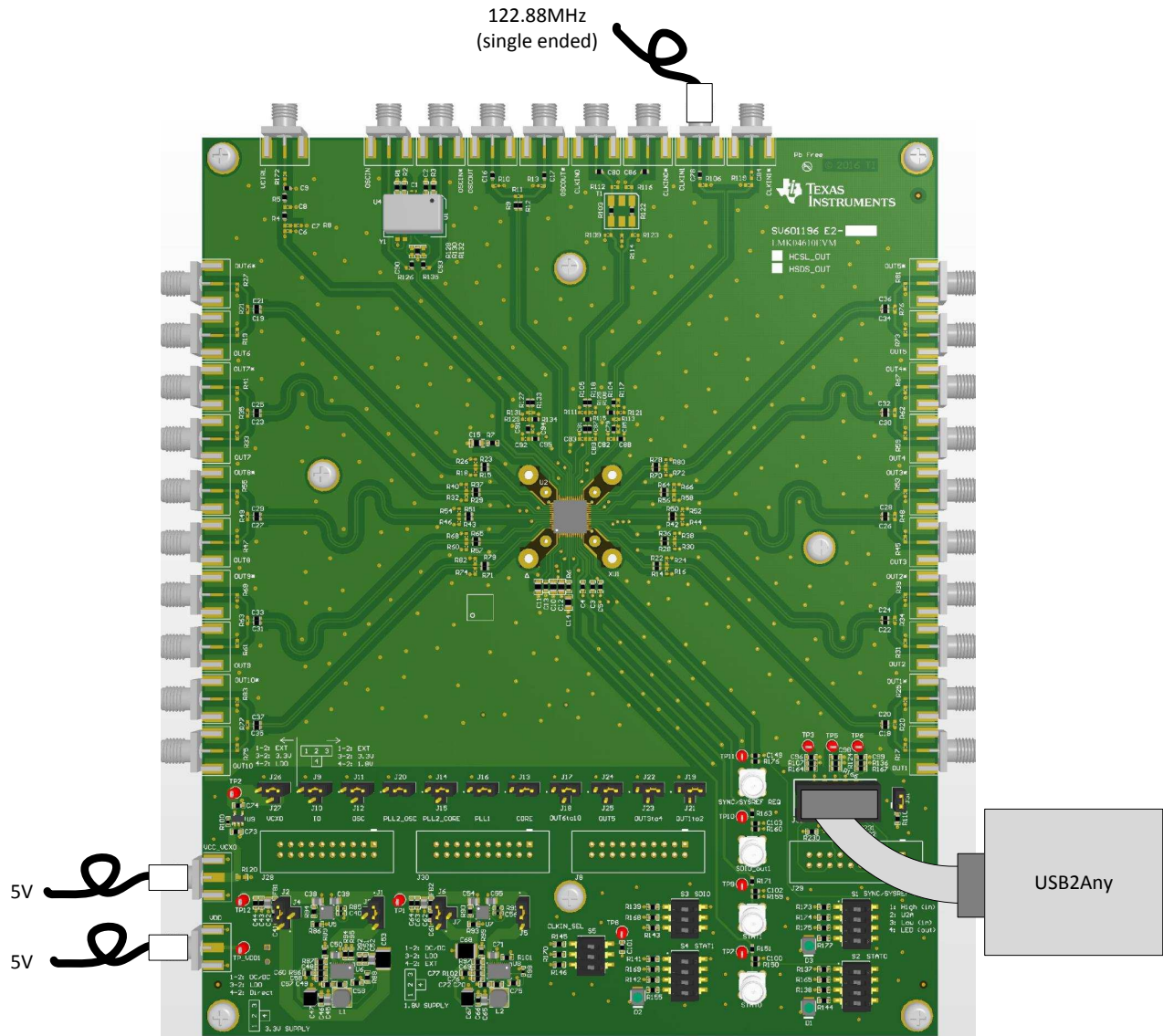


Figure 1-1. LMK04610 EVM Quick Start Connection

1.1 Quick Start Description

The LMK04610 EVM allows full verification of the device functionality and performance specification. To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in [Figure 1-1](#).

1. Place Dip switches S1 to S5 into default position as shown in [Figure 4-6](#)
2. Connect a supply voltage of 5 V to the VCC and VCC_VCXO SMA.
3. Connect a reference clock to the CLKin1 port from a signal generator or other source. Use 122.88 MHz for default.
4. Connect the SPI header to a computer using USB2ANY.
5. Program the device with TICS Pro.
 - (a) Start TICS Pro
 - (b) Select LMK04610 from *Select device* → *Clock Generator/Jitter Cleaner (Dual Loop)* → *LMK0461x Menu*.
 - (c) Select from *USB Communications* → *Interface Menu USB2ANY*.
 - (d) Select default mode from the *Default Configuration Menu*. For the quick start, use *Dual Loop: PLL1 BW= 40Hz REF: CLKin1 (single-ended)*
 - (e) Ctrl-L must be pressed at least once to load all registers. Alternatively click menu *Keyboard Controls* → *Load Device*.
 - (f) Click *Device Start* button in the *Generic* page or use the *Device: DEV_STARTUP* button from the Tool bar.
6. Measurements may be made at an active CLKout port through its SMA connector.

1.2 Device Start-Up Sequence

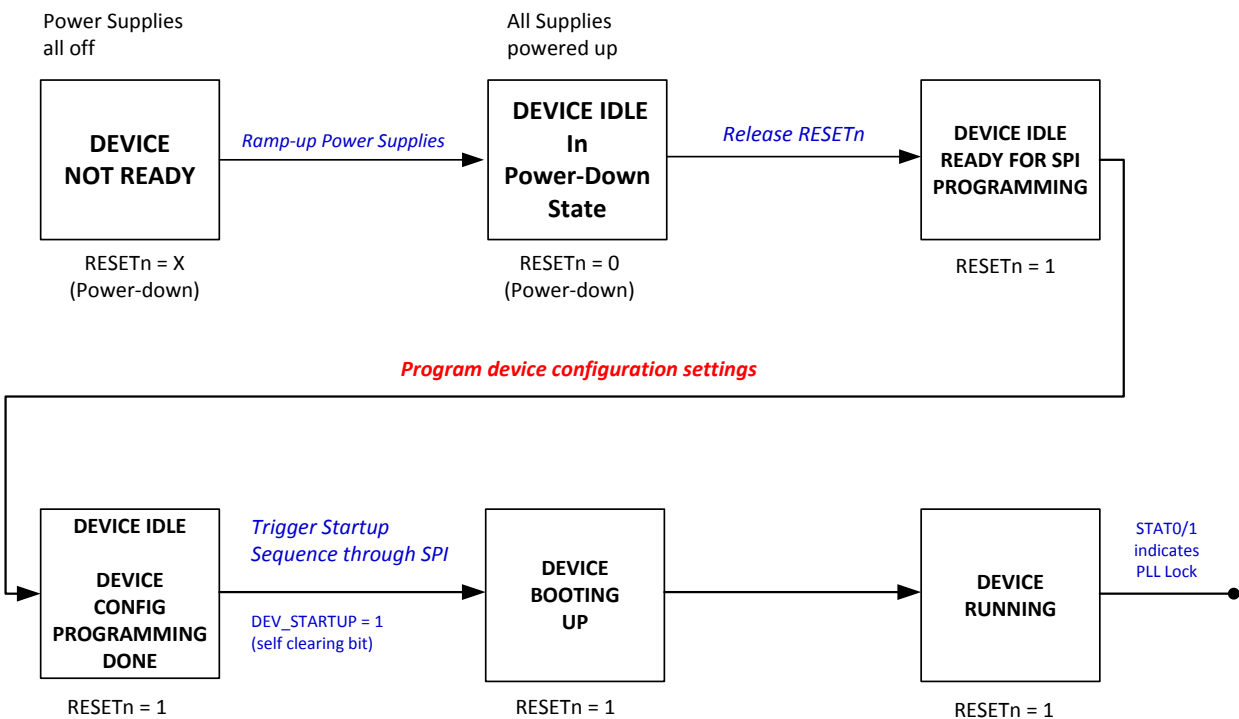


Figure 1-2. Device Start-Up Sequence

Installing the EVM Control Software

1. Install latest TICS Pro software from web: <http://www.ti.com/tool/ticspro-sw>
2. Start TICS Pro.
3. Select *Device* → *Clock Generator/Jitter Cleaner (Dual Loop)* → *LMK0461x* → *LMK04610*

Using the EVM Control Software

3.1 Keyboard Shortcuts

CTRL + L => write all registers

3.2 TICS Pro Overview

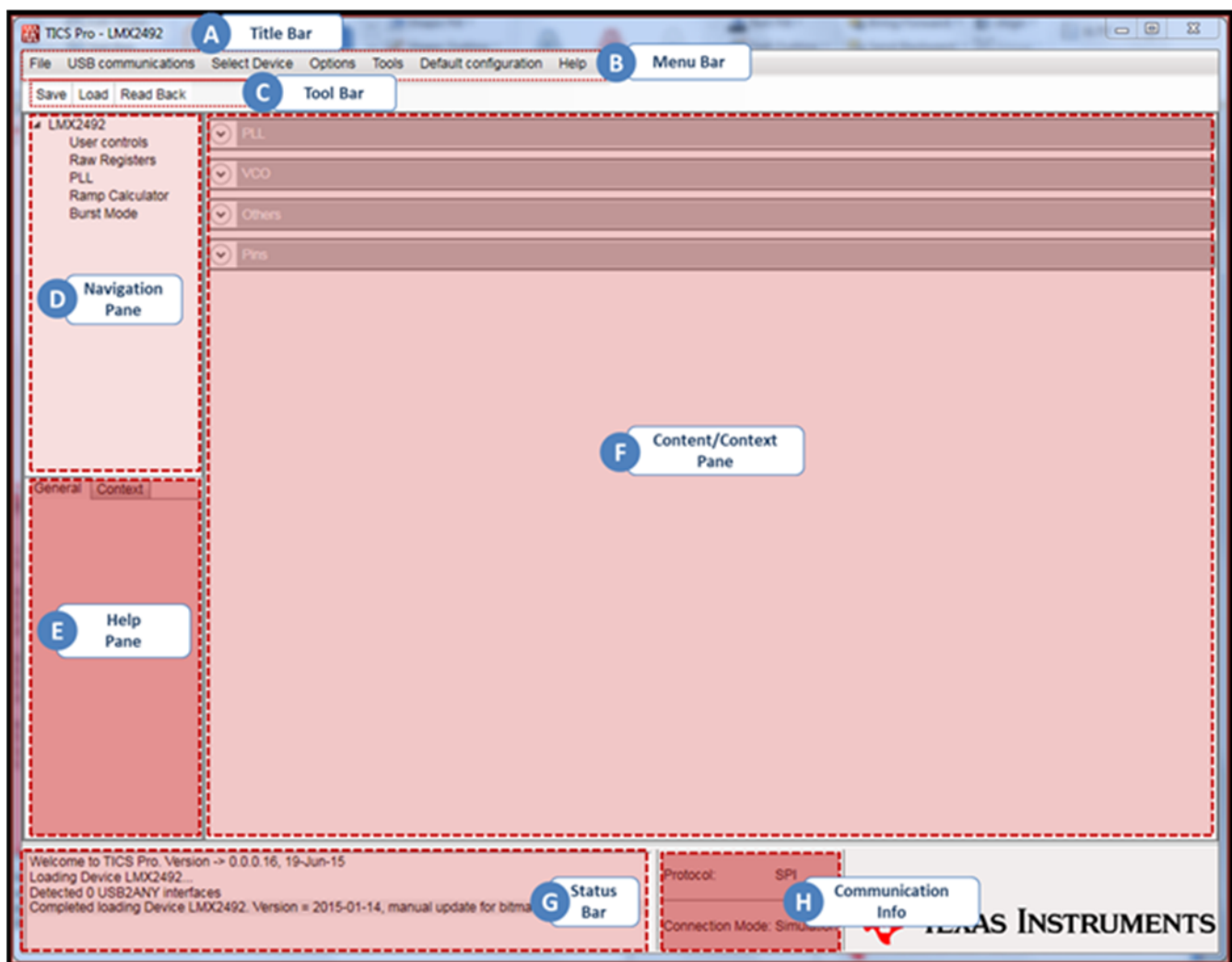


Figure 3-1. TICS Pro Overview

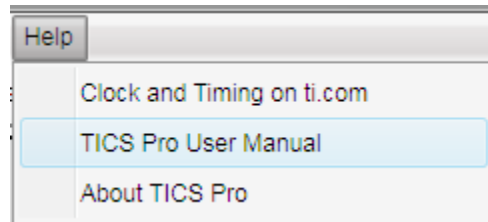


Figure 3-2. TICS Pro User Manual

Further information at *Help* → *TICS Pro User Manual*

3.3 TICS Pro with LMK04610 GUI Loaded

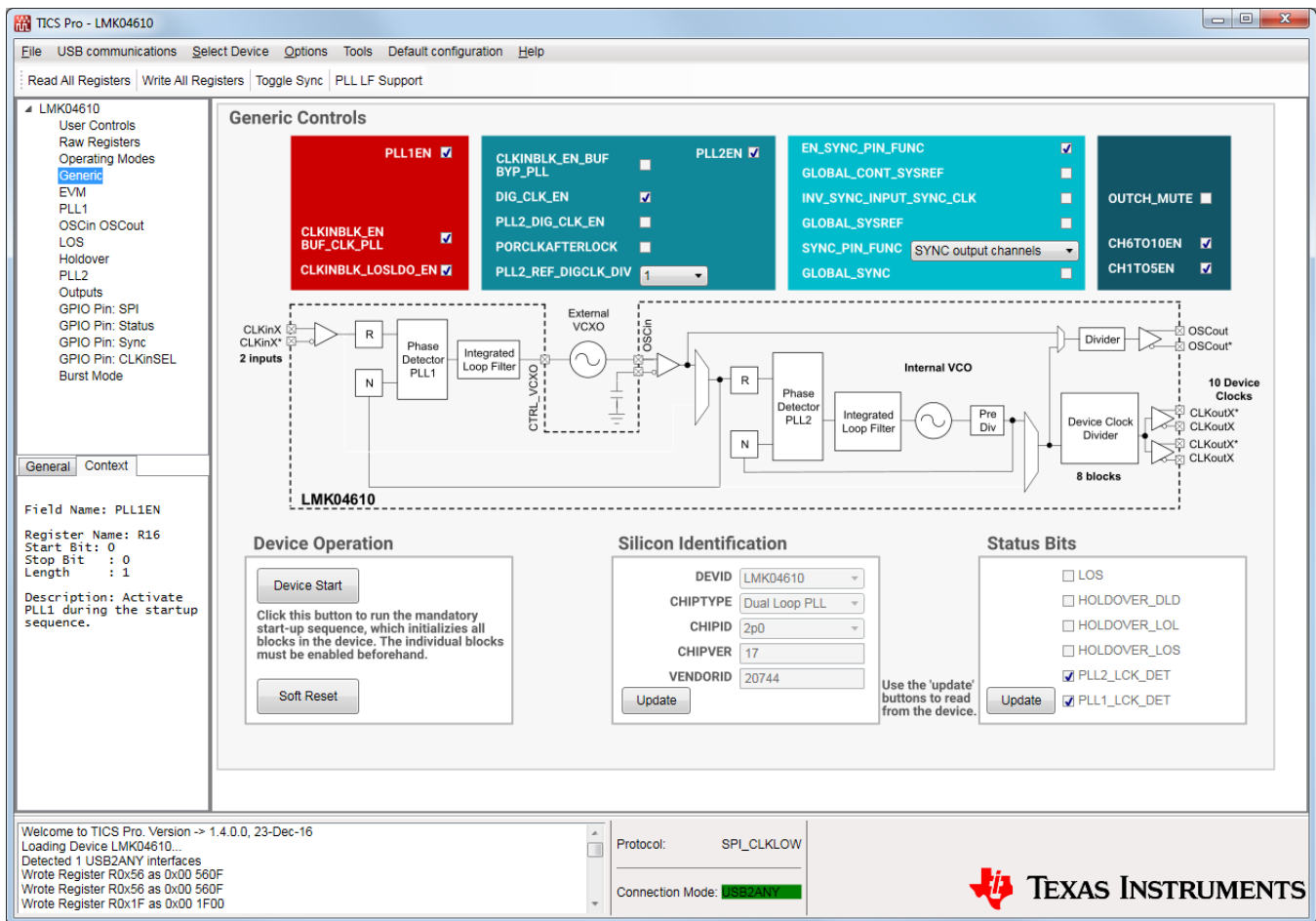


Figure 3-3. TICS Pro With LMK04610 GUI Loaded

3.4 GUI: Generic Control

Generic Controls

PLL1EN <input checked="" type="checkbox"/> CLKINBLK_EN <input checked="" type="checkbox"/> BUF_CLK_PLL <input checked="" type="checkbox"/> CLKINBLK_LOSLDO_EN <input checked="" type="checkbox"/>	CLKINBLK_EN_BUF <input type="checkbox"/> BYP_PLL <input type="checkbox"/> DIG_CLK_EN <input checked="" type="checkbox"/> PLL2_DIG_CLK_EN <input type="checkbox"/> PORCLKAFTERLOCK <input type="checkbox"/> PLL2_REF_DIGCLK_DIV <input type="text" value="1"/>	PLL2EN <input checked="" type="checkbox"/> EN_SYNC_PIN_FUNC <input checked="" type="checkbox"/> GLOBAL_CONT_SYSREF <input type="checkbox"/> INV_SYNC_INPUT_SYNC_CLK <input type="checkbox"/> GLOBAL_SYSREF <input type="checkbox"/> SYNC_PIN_FUNC <input type="text" value="SYNC output channels"/> GLOBAL_SYNC <input type="checkbox"/>	OUTCH_MUTE <input type="checkbox"/> CH6TO10EN <input checked="" type="checkbox"/> CH1TO5EN <input checked="" type="checkbox"/>
--	--	--	--

LMK04610

Device Operation

Device Start

Click this button to run the mandatory start-up sequence, which initializes all blocks in the device. The individual blocks must be enabled beforehand.

Soft Reset

Silicon Identification

DEVID
 CHIPTYPE
 CHIPID
 CHIPVER
 VENDORID

Update

Use the 'update' buttons to read from the device.

Status Bits

LOS
 HOLDOVER_DLD
 HOLDOVER_LOL
 HOLDOVER_LOS
 PLL2_LCK_DET
 PLL1_LCK_DET

Update

Figure 3-4. GUI: Generic Control

3.5 GUI: Operating Modes

Operating Modes Each of the buttons next to a block diagram ensures that the internal paths are enabled as illustrated with the color coding.

Please ensure that the PLL loop can be closed by setting the reference and feedback dividers appropriately on the 'PLL1' and 'PLL2' pages. By default CLKIn1 is selected.

Dual Loop	Dual Loop	
Normal Dual Loop OscOut = OscIn	Normal Dual Loop OscOut = PLL2 Output	
Single Loop PLL1	Single Loop PLL1	
PLL1 Single Loop OscOut = OscIn	PLL1 Single Loop OscOut = PLL1 Output	
Single Loop PLL2	Single Loop PLL2	
PLL2 Single Loop Ref=CLKInX OscOut = OscIn	PLL2 Single Loop Ref=OscIn OscOut = PLL Output	
Single Loop PLL2	Single Loop PLL2	
PLL2 Single Loop Ref=OscIn OscOut = OscIn	PLL2 Single Loop Ref=CLKInX OscOut = PLL Output	
Bypass 2A	Bypass 1	Bypass 2B
Mode 2A Bypass OSCIn- > CLKoutX OscOut = PLL bypass	Mode 1 Bypass CLKInX- > CLKoutX OscOut = PLL bypass	Mode 2B Bypass OSCIn- > CLKoutX OscOut = OscIn

Figure 3-5. GUI: Operating Modes

3.6 GUI: OSCin and OSCout

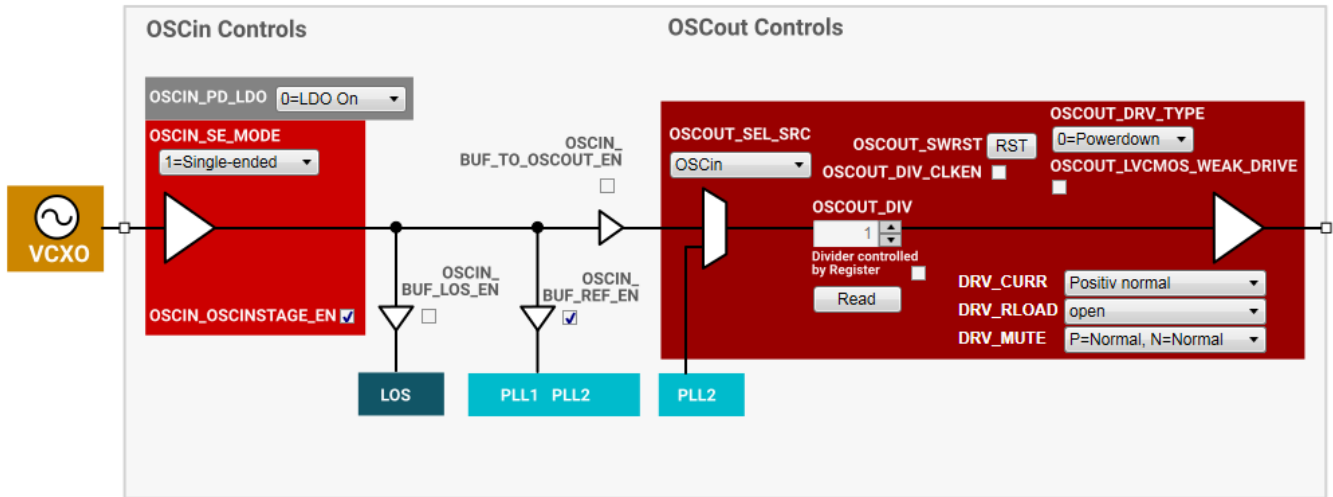


Figure 3-6. GUI: OSCin and OSCout

3.7 GUI: LOS Control

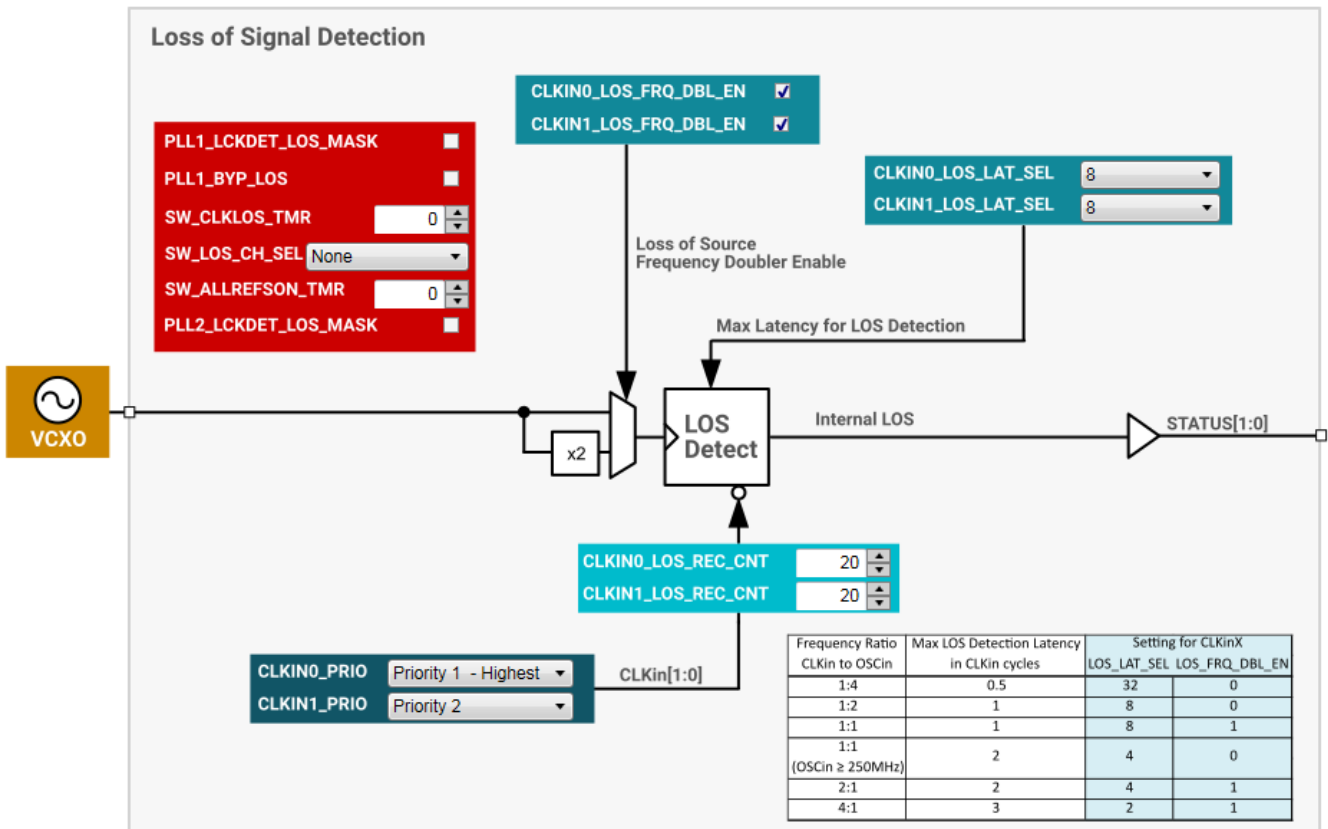


Figure 3-7. GUI: LOS Control

3.8 GUI: Holdover Control

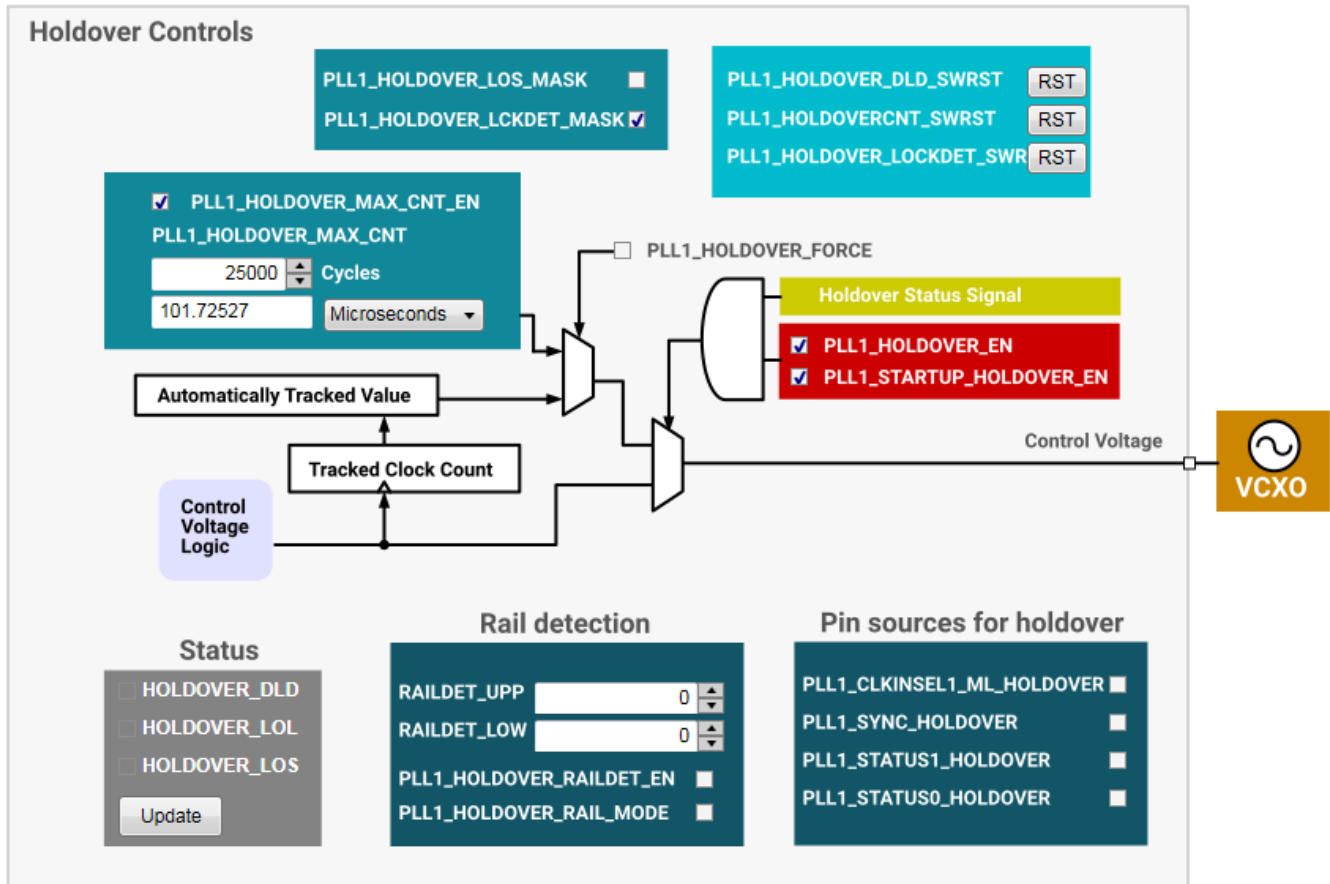


Figure 3-8. GUI: Holdover Control

3.9 GUI: Inputs and PLL1

PLL1 Control

MHz	Input Buffers	Dividers	Inversion	MHz	Reference Mux
122.88	<input type="checkbox"/> CLKIN0_EN 1=Single-ended	CLKIN0_PLL1_RDIV 64	<input type="checkbox"/> CLKIN0_INVERSION	1.024	<input type="checkbox"/> CLKINBLK_ALL_EN 2=Register SW_REFINSEL CLKIN1 <input type="checkbox"/> CLKINSEL1_INV 0=Non-Inverted CLKMUX CLKIN1 <input type="button" value="Read"/>
122.88	<input checked="" type="checkbox"/> CLKIN1_EN 1=Single-ended	CLKIN1_PLL1_RDIV 64	<input type="checkbox"/> CLKIN1_INVERSION	1.024	
<input checked="" type="checkbox"/> PLL1_RDIV_CLKEN <input type="button" value="RST"/> PLL1_RDIV_SWRST					

PLL1_STORAGE_CELL: 9

The read back storage cell value provides an indication of the level of the analog tuning voltage for the external VCXO.

Charge Pumps

Integral Final: 1

Fast Lock: 6

VCXO

122.88 MHz

PFD

PLL1_DIR_POS_GAIN: 1=Negative

Proportional Final: 10

Fast Lock: 2

PLL1_EN_REGULATION:

PLL1_NDIV: 64

FBCLK_INVERSION:

1.024 MHz

PLL1_NDIV_CLKEN: PLL1_NDIV_SWRST

PLL1_SWRST:

F _{IN}	F _{VCXO}	PLL1_RDIV	PLL1_NDIV	PROP MODE	PLL1_PROP	PLL1_INTG	C3
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	2	0	4.7 μF
122.88 MHz	122.88 MHz	100	100	Low Pulse Mode	10	0	4.7 μF
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	2	0	4.7 μF
122.88 MHz	30.72 MHz	100	25	Low Pulse Mode	10	0	4.7 μF

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<input checked="" type="checkbox"/> CLKIN_STAGGER_EN	<input checked="" type="checkbox"/> Disable RDIV/NDIV	<input type="checkbox"/> PLL1_LOL_NORESET
<input type="checkbox"/> CLKIN_SWRST	<input checked="" type="checkbox"/> 50% Duty Cycle CLK Output	<input type="checkbox"/> PLL1_RC_CLK_EN
<input type="checkbox"/> PLL1_LDO_WAIT_TMR: 0		<input type="checkbox"/> PLL1_RC_CLK_DIV: 1
		<input type="checkbox"/> PLL1_F_30: 0=122MHz

Lock Detection

Window Comparator

PLL1_LD_WNDW_SIZE: 63 ns

PLL1_FAST_LOCK:

PLL1_PD_LD:

PLL1_LCKDET_BY_32: /32

PLL1_LOCKDET_CYC_CNT: 16384

Figure 3-9. GUI: Inputs and PLL1

3.10 GUI: PLL2

PLL2 Controls

PLL1 BYPASS
 MHz: 122.88
 OSCin CLK
 PLL2 CLKin

PLL2_REF_CLK_EN
 PLL2_REF_CLK_EN
 x2
 DIV: 1
 Doubler, inv.

PFD + LD
 245.76 MHz
 PLL2_LD WNDW_SIZE: 2 ns
 PLL2_LOCKDET CYC_CNT: 16384
 PFD_DIS SAMPLE
 PROG_PFD_RESET
 PLL2_PD_LD
 PLL2_SWRST RST

Charge Pumps
 PLL2_PROP: 20
 VCO: 5898.24 MHz
 PLL2 INTEGRAL INIT VALUE: 511=Cell 9
 PLL2 INTEGRAL GAIN: 10

Pre-Scaler
 PLL2_PRESCALER_TOP: DIV6
 PLL2_VCO_PRESC LOW_POWER

Other PLL2 Controls:
 PLL2_FB DIV: 2
 PLL2_NDIV: 4
 PLL2_NDIV_SWRST
 PLL2_NDIV_CLKEN
 PLL2_NBYPASS_DIV2_FB

F _{IN} PLL2	F _{VDD}	PLL2_RDIV	PLL2_NDIV	PRESCALER	INPUT MODE	PLL2_PROP	PLL2_INTG	PLL2_CPROP	R3, C3 ⁽¹⁾
122.88 MHz	5898.24 MHz	1	4	6	Doubler Invert	20	0	5.4 pF	disabled, 0 pF
122.88 MHz	5898.24 MHz	1	4	6	Doubler Invert	21	0	5.4 pF	4.7 kΩ, 96 pF
30.72 MHz	5898.24 MHz	1	16	6	Doubler Invert	20	0	5.4 pF	disabled, 0 pF
30.72 MHz	5898.24 MHz	1	16	6	Doubler Invert	7	0	5.4 pF	4.7 kΩ, 96 pF

Charge Pump

PLL2_CFILT_64
 PLL2_CFILT_32
 PLL2_CFILT_16
 PLL2_CFILT_8
 PLL2_CFILT_4
 PLL2_EN_FILTER
 PLL2_CSAMPLE: 4.85 pF
 PLL2_RFILT
 PLL2_CP_EN_SAMPLE_BYP
 PLL2_CPROP: 3.0 pF
 PLL2_AC_REQ RST

PLL2_LD_WNDW_SIZE_INITIAL: 2 ns
 PLL2_LOCKDET_CYC_CNT_INITIAL: 16384
 PLL2_SWRST RST

Enable Bypass Buffer

PLL2 BYPASS
 Enable Buffer
 CLKout
 PLL2 CLKin → CLK to OSCout

PLL2_SYNC_BOTTOM
 Enable Buffer
 PLL2 Sy
 SYNC to OUTCH1...5
 VSS

PLL2_BOTTOM
 Enable Buffer
 CLKout
 PLL2 CLKin → CLK to OUTCH1...5

PLL2_SYNC_TOP
 Enable Buffer
 PLL2 Sy
 SYNC to OUTCH6...10
 VSS

PLL2_TOP
 Enable Buffer
 CLKout
 PLL2 CLKin → CLK to OUTCH6...10

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Figure 3-10. GUI: PLL2

3.11 GUI: Outputs

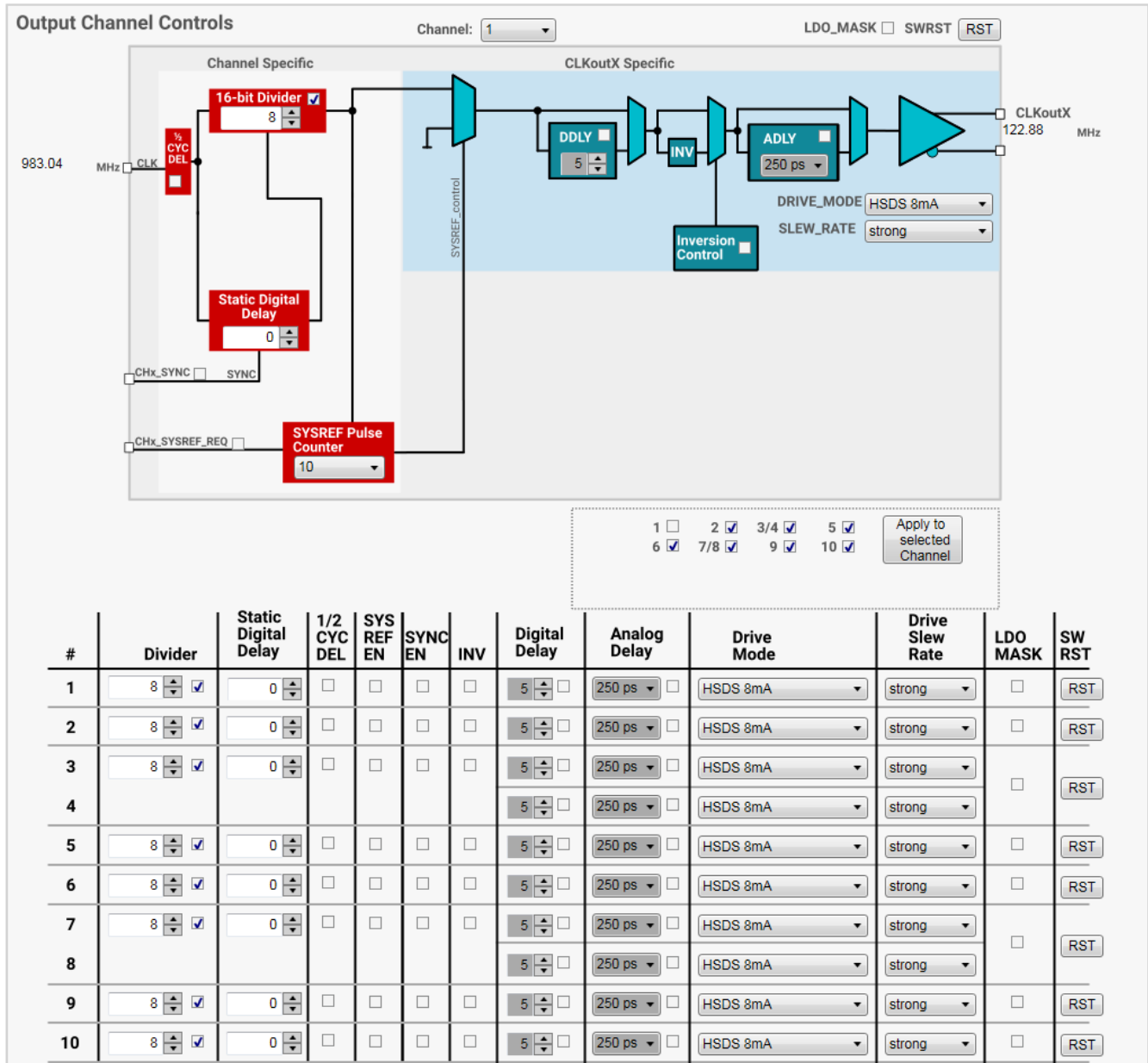


Figure 3-11. GUI: Outputs

3.12 GUI: EVM

LMK04610 Evaluation Module

This page provides an overview of the evaluation module. Use it as guidance to identify input references and output signals.

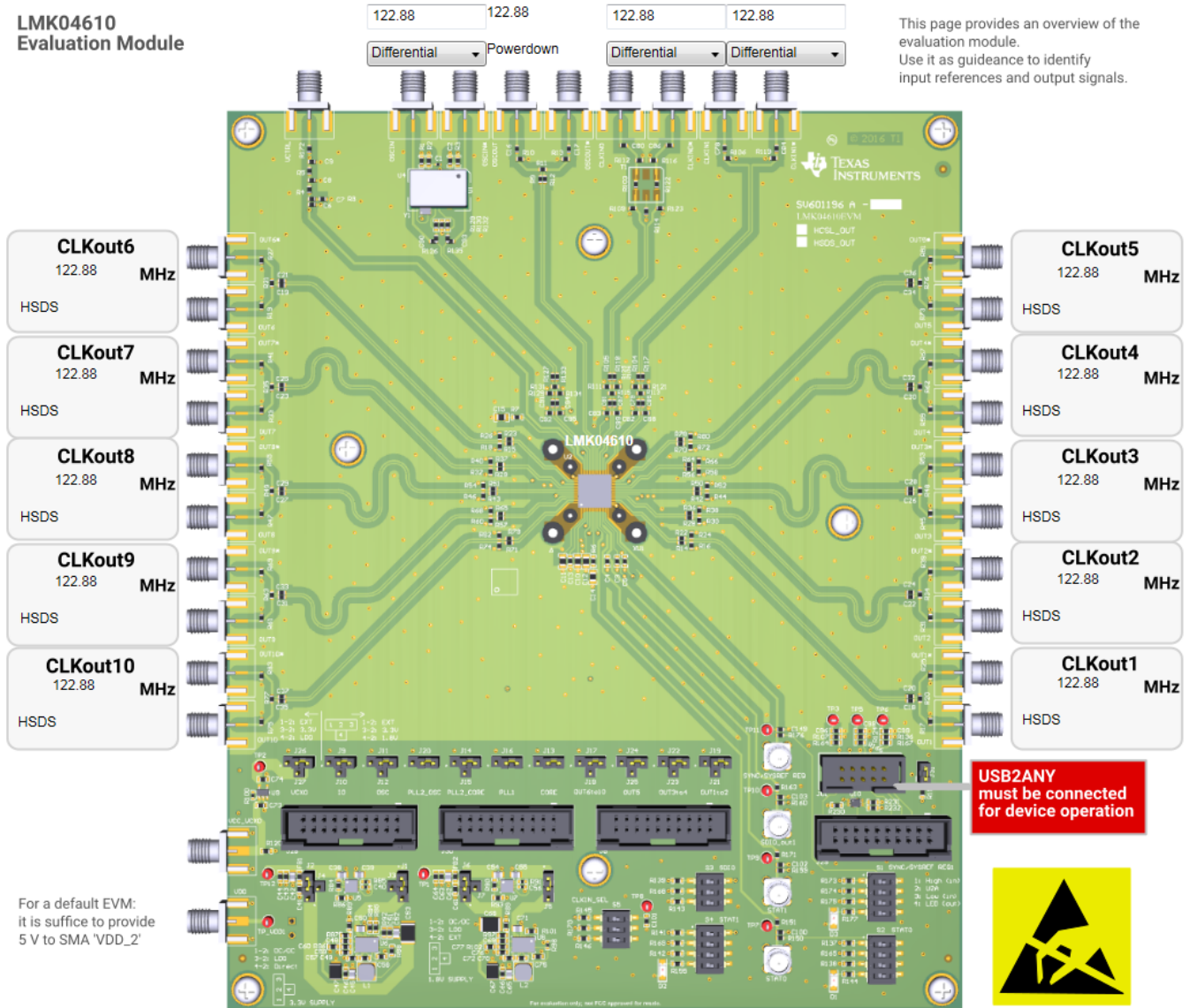


Figure 3-12. GUI: EVM Overview

Configuring the Board

The LMK04610 is a programmable clock jitter cleaner with many options. The EVM was designed with maximum flexibility so engineers can configure the EVM for operation at its desired mode.

Figure 4-1 shows the connection concept of the LMK04610EVM.

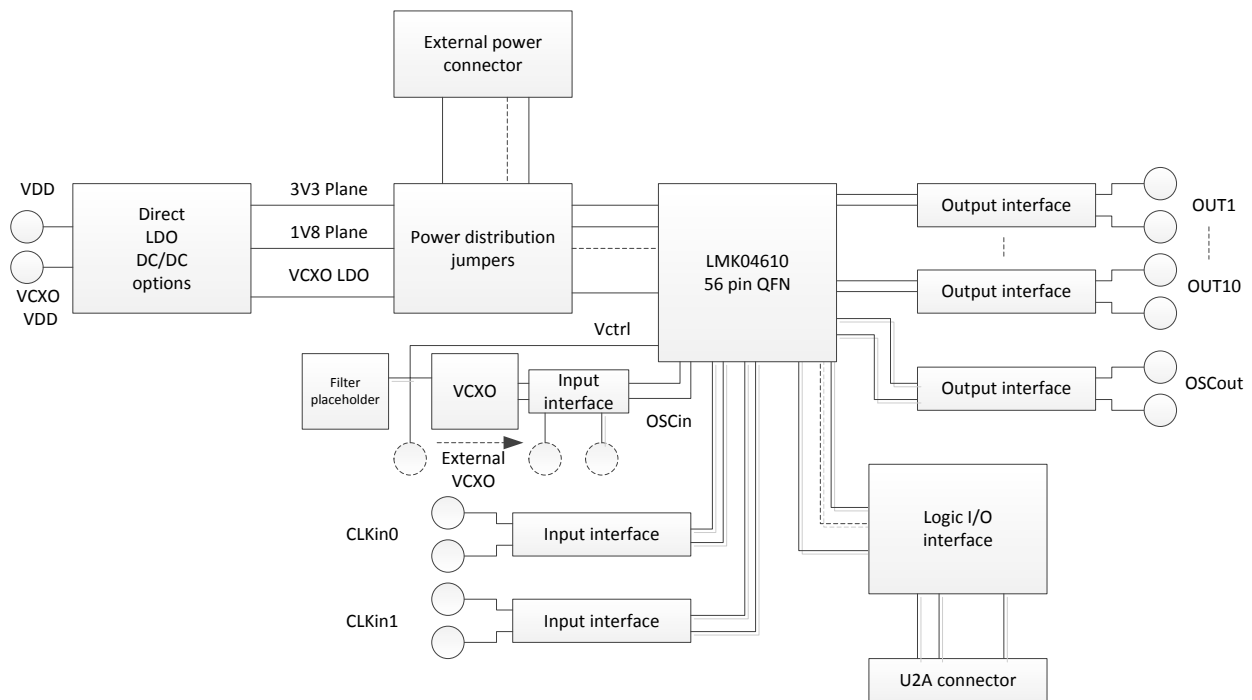


Figure 4-1. EVM Connection Concept

4.1 Configuring the Power Supply

Figure 4-2 shows the default jumper setting to supply 3.3 V and 1.8 V to the device.

The VDD SMA or VDD_2 terminal block (on the back side of the EVM) is connected to J1 and J5 to provide the external supply voltage for the 3.3-V and 1.8-V supply plane. Connect 5-V external power supply if LDO or DCDC converter is used.

The VDD_VCXO SMA is directly connected to the VCXO LDO.

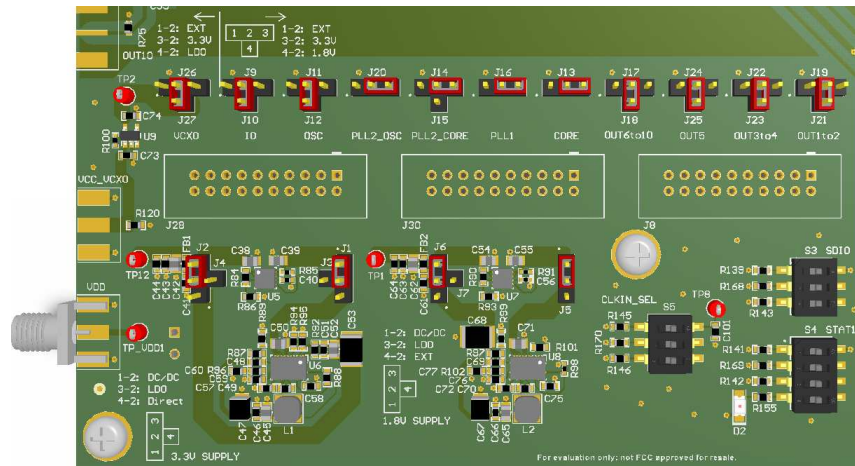


Figure 4-2. Default Power Supply Connection

4.1.1 Supply Plane Source Selection

Jumper J1 and J2 selects the Power connection for the 3.3-V plane from either the LDO, a DC-DC switcher, or direct from VDD SMA Connector. A 5-V supply needs to be connected to VDD SMA Connector.

Table 4-1. 3.3-V Supply Plane Connections

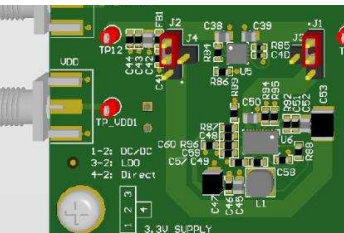
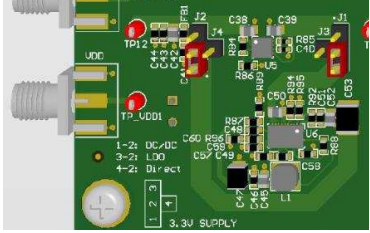
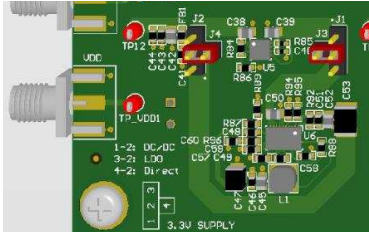
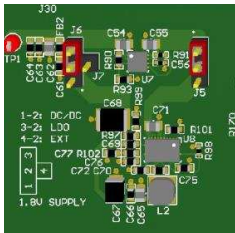
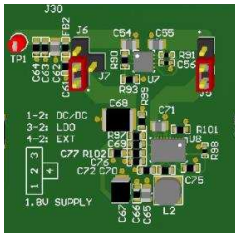
<p>3.3-V LDO (TPS7A8101)</p>	<p>J1: 1-2 J2: 2-3</p>	
<p>3.3-V DC-DC (TPS54120)</p>	<p>J1: 2-3 J2: 1-2</p>	

Table 4-1. 3.3-V Supply Plane Connections (continued)

<p>Direct from VDD SMA NOTE: Apply 3.3 V only</p>	<p>J1: 2-4 J2: 2-4</p>	
--	----------------------------	---

Jumper J6 and J5 selects the Power connection for the 1.8-V plane from either a LDO or a DC-DC switcher.

Table 4-2. 1.8-V Supply Plane Connections

<p>1.8-V LDO (TPS7A8101)</p>	<p>J5: 1-2 J6: 2-3</p>	
<p>1.8-V DC-DC (TPS54120)</p>	<p>J5: 2-3 J6: 1-2</p>	

4.1.2 Power Distribution

The power distribution jumpers (J9, J11, J13, J14, J16, J17, J19, J20, J22, and J24) are connected to the 3.3-V and 1.8-V supply planes and individual external connections.

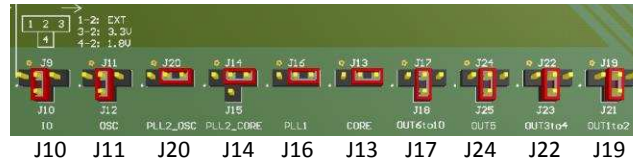


Figure 4-3. Power Distribution Jumpers

J13 (VDD_CORE), J16 (VDD_PLL1), and J20 (VDD_PLL2_OSC) selects between 3.3-V supply plane and external supply connection as shown in [Figure 4-4](#).



Figure 4-4. J13, J16, J20 Connection Description

J9 (VDD_IO), J11 (VDD_OSC), J14 (VDD_PLL2_CORE), J17 (VDD_OUT6to10), J19 (VDD_OUT1to2), J22 (VDD_OUT3to4), and J24 (VDD_OUT5) selects between 3.3-V supply plane, 1.8-V supply plane and external supply connection as shown in [Figure 4-5](#).



Figure 4-5. J9, J11, J14, J17, J19, J22, J24 Connection Description

NOTE: External supply connection is available on Jumpers J8, J28, and J30.

4.1.3 VCXO Supply Connection

The VCXO has its own LDO (LM5907MFX-3.3). A 5-V supply needs to be connected to VCC_VCXO SMA. Jumper J26 selects between this LDO, the LMK04610 3.3-V supply plane and external supply connection as shown in [Table 4-3](#).

Table 4-3. VCXO Supply Connections

<p>3.3-V LDO (LM5907MFX-3.3)</p>	<p>J26: 2-4</p>	
<p>3.3-V supply plane (TPS7A8101 or TPS54120)</p>	<p>J26: 2-3</p>	
<p>External supply connection on Jumper J28 NOTE: Apply 3.3 V only</p>	<p>J26: 1-2</p>	

4.2 Dip Switch Configuration

Default configuration of Dip Switches is shown in [Table 4-4](#) or [Figure 4-6](#).

Table 4-4. Default Dip Switch Configuration

SWITCH POSITION	S1 SYNC/SYSREF REQ	S2 STAT0	S3 SDIO	S4 STAT1	S5 CLKIn_SEL
1 – High	OFF	OFF	OFF	OFF	OFF
2 – U2A	ON	ON	ON	ON	ON
3 – Low	OFF	OFF	OFF	OFF	OFF
4 – LED	ON	ON	n/a	ON	n/a

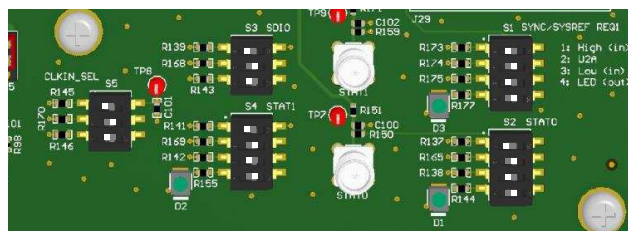
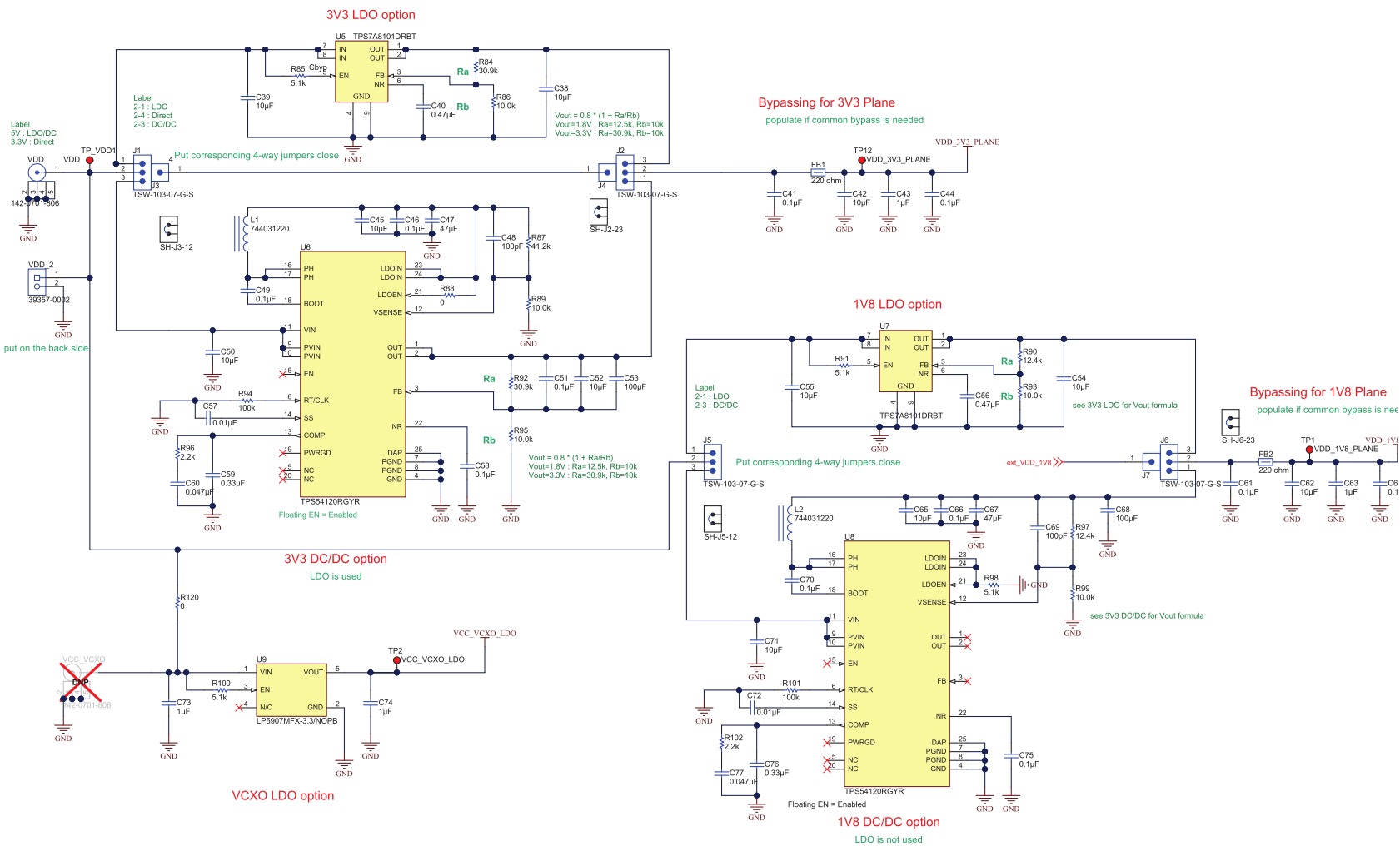


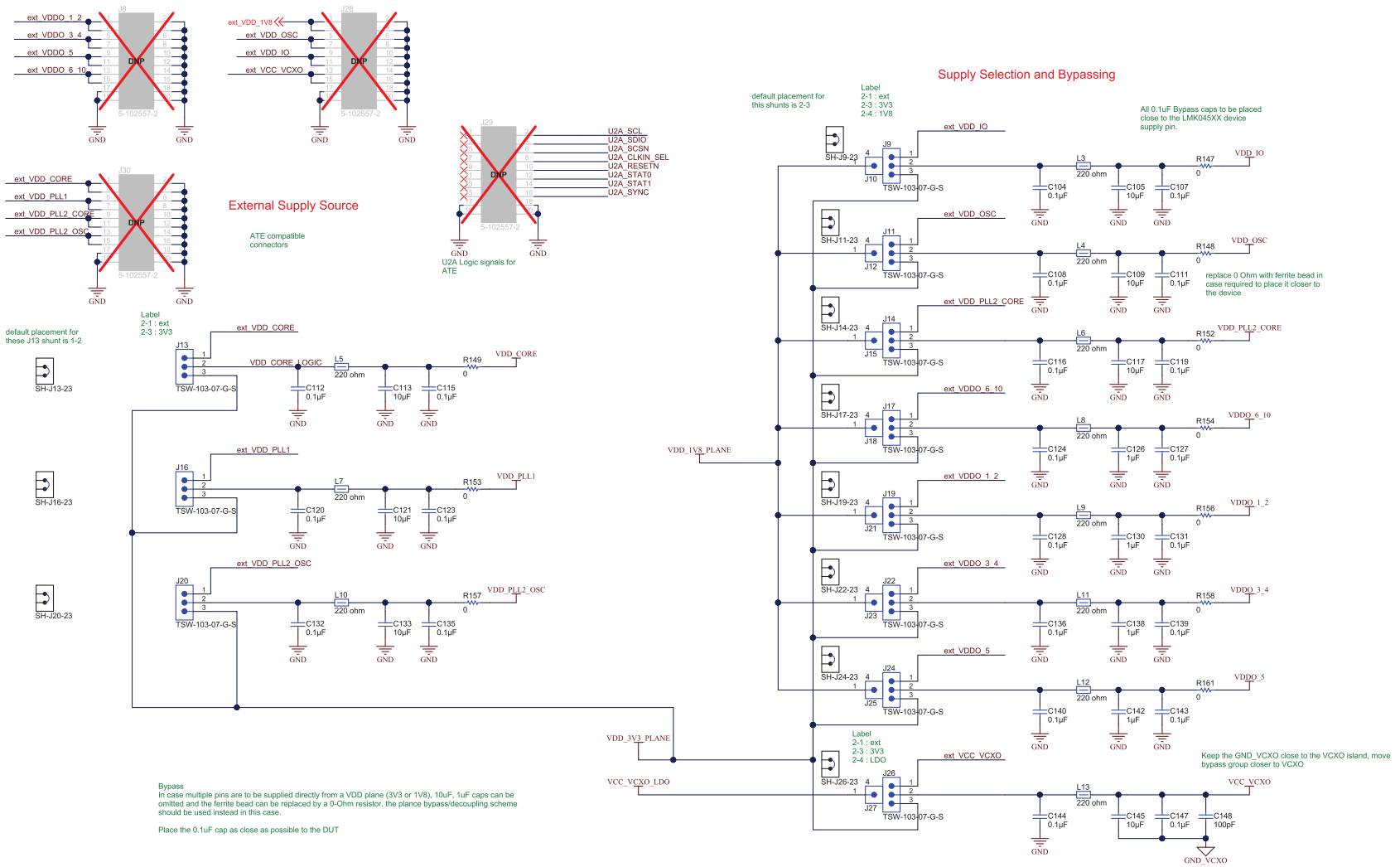
Figure 4-6. Default Dip Switch Setting

LMK04610 EVM Board Schematics



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Figure 5-1. Power Supply Connection



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Figure 5-2. Power Distribution

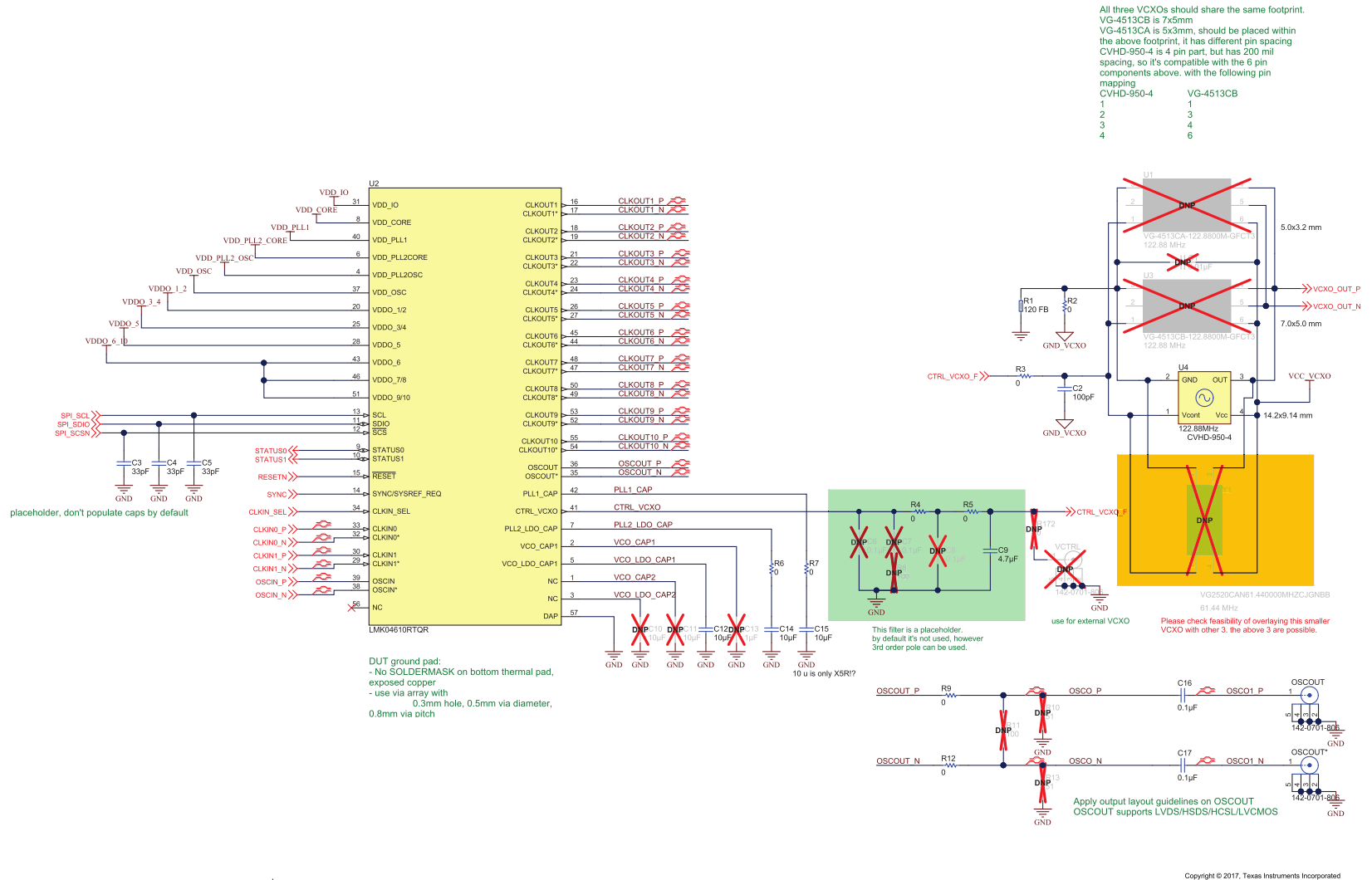
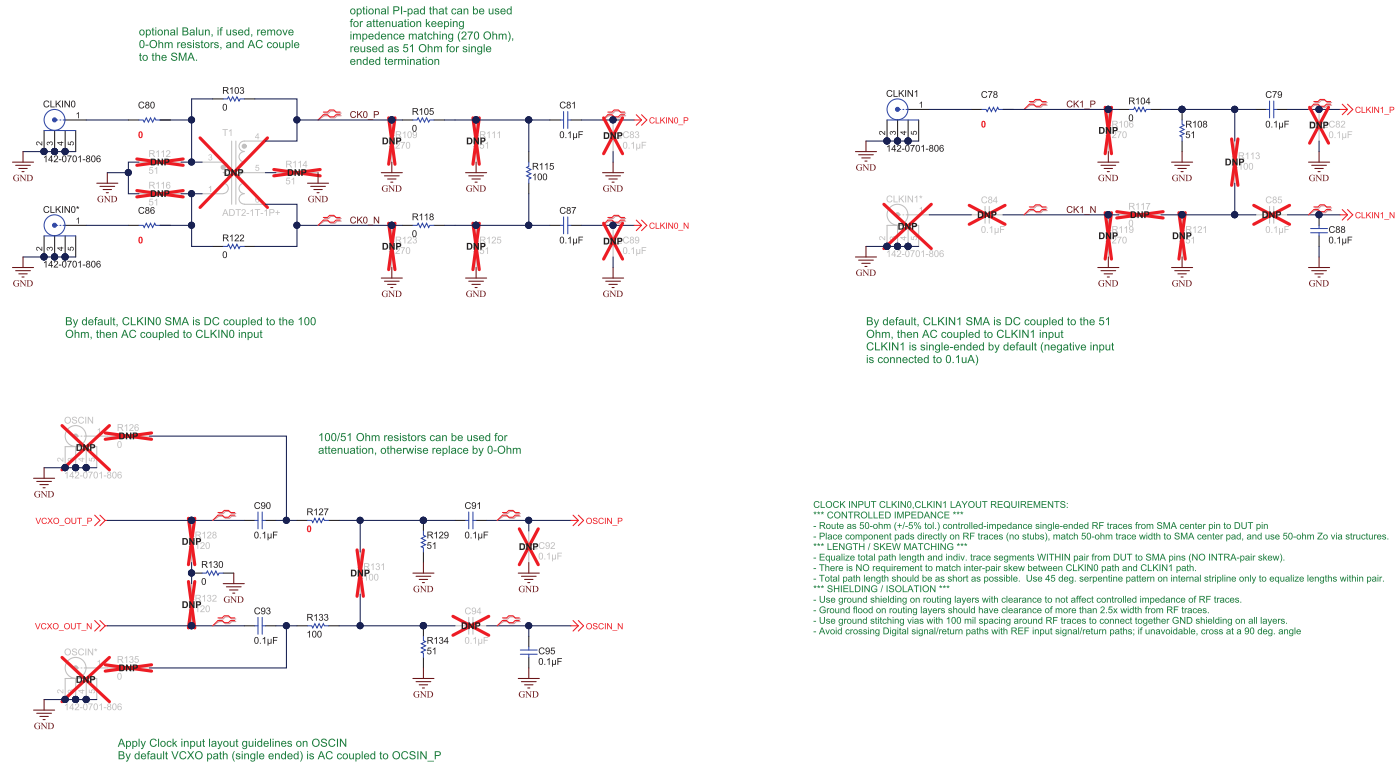
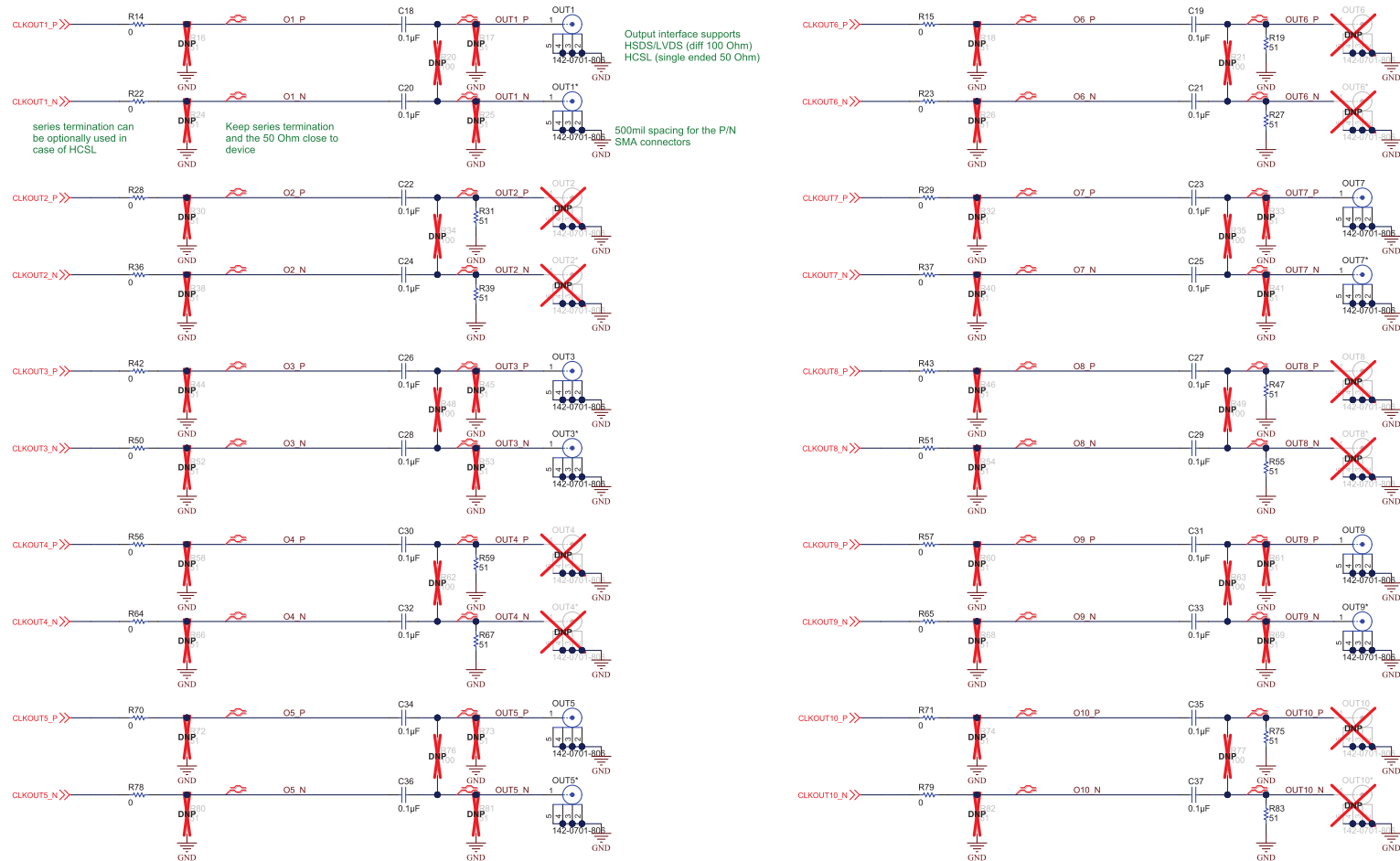


Figure 5-3. LMK04610 Main



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Figure 5-4. Inputs



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Figure 5-5. Outputs

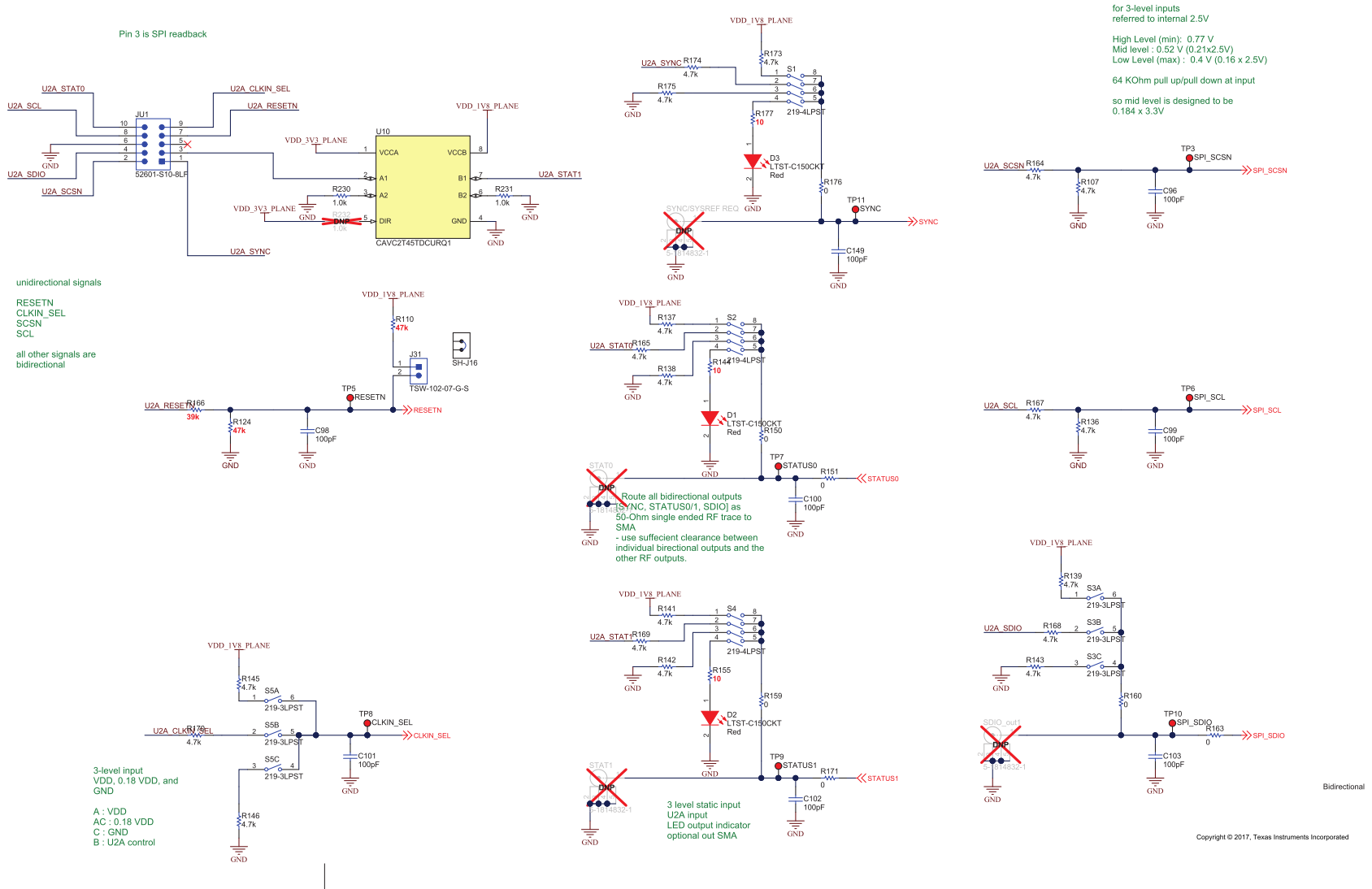


Figure 5-6. Logic/GPIO

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January 2017) to A Revision	Page
• Updated the text in the <i>Overview</i> section	3
• Changed typical rms value from: 60 fs to: 65 fs.....	3
• Changed typical power consumption value from: 0.9 W to: 880 mW	3

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