CDCI6214EVM

User's Guide

Literature Number: SNAU202B
July 2017–Revised October 2018

Contents

Preface **5**

1 Setup Procedure **6**

1.1 Quick Start 6

1.1.1 Default Configuration 7

2 Evaluation Module Configuration **8**

2.1 Device Under Test 8

2.2 Control Pins 8

2.3 Reference Input 9

2.4 Clock Outputs 12

2.5 Power Supplies 13

3 Frequently Asked Questions - FAQ **17**

3.1 Troubleshooting 17

A References **19**

A.1 Software 19

A.2 EVM Schematics 20

A.3 EVM Layout 29

Revision History **36**

Copyright © 2017–2018, Texas Instruments Incorporated

List of Figures

1-1. CDCI6214EVM 6
2-1. Evaluation Module Default, Control Pins 8
2-2. Evaluation Module Default, Control Pin Level Shifters 9
2-3. Evaluation Module Default, Reference Connection 11
2-4. Rework, Input, and Output Termination Options 13
2-5. Evaluation Module Default, Power Distribution 15
2-6. Evaluation Module Default, Device Connection 16
A-1. Schematics, Clock Generator 20
A-2. Schematics, Inputs 21
A-3. Schematics, Outputs 22
A-4. Schematics, Control Pins 23
A-5. Schematics, Power Distribution 24
A-6. Schematics, Power 25
A-7. Schematic, USB Interface 26
A-8. Schematic, EVM Hardware 27
A-9. Schematic, Block Guidance 28
A-10. Layout, Assembly Top 30
A-11. Layout, Assembly Bottom 31
A-12. Layout, Top Layer 32
A-13. Layout, Middle Layer 1 33
A-14. Layout, Middle Layer 2 34
A-15. Layout, Bottom Layer 35

Copyright © 2017–2018, Texas Instruments Incorporated

List of Tables

2-1. Input Connection Options 10
2-2. Output Connection Options, Example for Y1 Channel Soldered Termination 12
2-3. Power Supply Option Examples 14
2-4. Power Distribution 14
A-1. Stack-Up 29

Copyright © 2017–2018, Texas Instruments Incorporated

Introduction

The *CDCI6214EVM* is an evaluation platform for the *CDCI6214 Ultra-Low Power Clock Generator*. This evaluation module provides an USB-based interface to access the I^2C bus to communicate with the CDCI6214 as well as its control pins and the power supply. The edge-launch SMA-connectors enable measurements using 50-Ω equipment while the onboard termination allows to use high impedance probes. The flexible re-work options allow to adapt the evaluation module to many application-specific requirements for rapid prototyping.

Features

- CDCI6214
  - Single high-performance phase-locked-loop
  - Ultra-low power operation
  - Supports mixed power supply operation from 1.8 V to 3.3 V
  - Four differential outputs with multi-mode output buffers
  - One LVCMOS bypass output
  - Crystal oscillator with integrated load capacitance and configurable gain
  - LVCMOS or AC-coupled differential reference input
  - Output divider synchronization and digital delays
  - General-purpose inputs and outputs for individual output enable and status signals
  - I^2C programming interface
  - Integrated EEPROM with two pages
- Evaluation Module
  - Power distribution network to choose from
    - Low-noise LDO
    - High-efficiency DC-DC switcher
  - Level-shifters to adapt programming interface so selected supply voltage
  - Onboard input and output termination options
  - Flexible footprint for four pin SMD crystals

What's Included

- CDCI6214EVM
- Micro-USB cable

What's Required

- Windows-based computer for supplied graphical user interface - TICS Pro
- Measurement equipment
  - Oscilloscope
  - Spectrum analyzer or phase noise analyzer
  - Digital Multi-meter

Copyright © 2017–2018, Texas Instruments Incorporated

Setup Procedure

1.1 Quick Start

The evaluation module is powered either from the USB port or using an external 5-V supply for more flexibility. By default the device operates from USB and is supplied with 1.8 V from the onboard LDO. The control pins of the device can be set using shunts for the respective pullup and pulldown option on the pin headers in the center of the evaluation module. The control signals are alternatively steered using the TICS Pro graphical user interface which is available free of charge on the TI website.

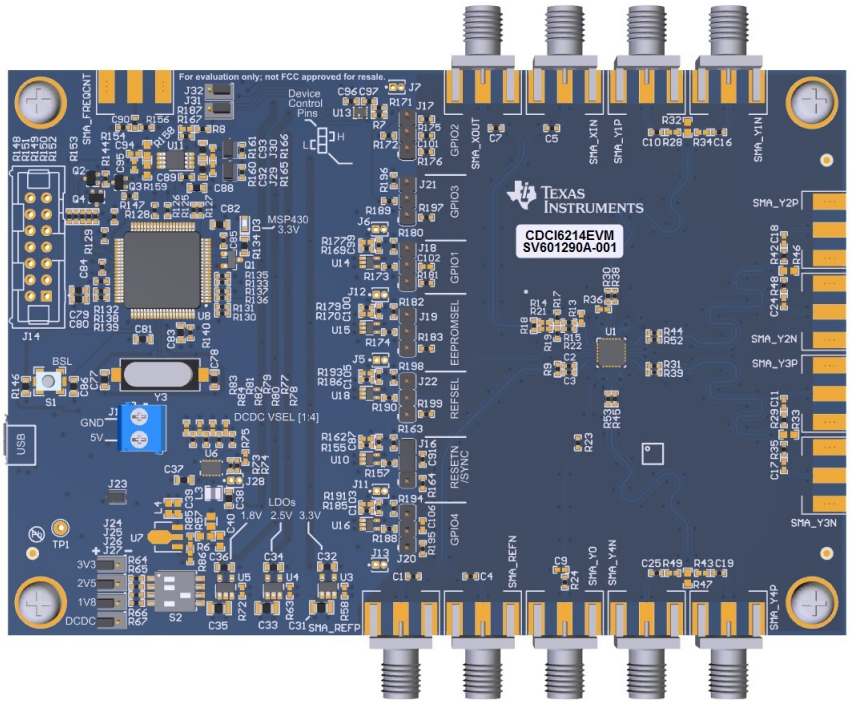


Figure 1-1. CDCI6214EVM

NOTE: The SMA_XOUT connector drives XIN/FB_N (pin 2) and the SMA_XIN connector drives XOUT/FB_P (pin 1).

1. Cross-check the default EVM configuration using Figure 2-1. Ensure the correct position of the control pin signals and the connections to the device and the input reference.
2. Install the newest version of the TICS Pro software from http://www.ti.com/tool/ticspro-sw.
3. Load the CDCI6214 device profile in the *CDC Devices* category using the *Select Device* menu.
4. Connect the USB cable to the EVM and the computer. At the bottom of the screen you will observe a green status indicator with the protocol set to *I2C*.
5. Press the button *Power Off* and observe the button change to *Power On*.
6. Press the button *Find Device*. You are connected to the device and can program its registers.
7. At the top of the screen, choose *Default Configuration* and select *EVM Default*.

Copyright © 2017–2018, Texas Instruments Incorporated

8. Press the button *Lock?* to poll the lock detector status bit. You can also press the toolbar button *Read All Registers* to obtain more detailed information under *User Controls*.
9. The clocks outputs can be observed now, providing 100 MHz generated using the onboard 25-MHz crystal.

1.1.1 Default Configuration

- Input: 25-MHz crystal
- Supplies: all 1.8-V LDO
- Outputs:
  - Soldered on termination: Y2, Y3 AC-coupled LVPECL.
  - Scope with 50-Ω termination: Y1, Y4 DC-connection.

Copyright © 2017–2018, Texas Instruments Incorporated

Evaluation Module Configuration

2.1 Device Under Test

The evaluation module is shipped with a soldered down unit. The position of pin 1 of the 24-pin VQFN package is indicated by a silkscreen symbol as well as the reference designator U1.

2.2 Control Pins

Each control pin is set by two options:

1. MSP430 micro-controller through level shifters controlled by TICS Pro GUI
2. Computer-independent control using pin header shunts with onboard pullup and pulldown resistors.

TICS Pro Control:

For software-based control, the shunts should be removed. Ensure that, when a device GPIO pin is configured as an output, the signal does not collide with the micro-controller signal. The connection to the level-shifter can, therefore, be disconnected using the solder bridges: R157, R173, R174, R188, and R190.

Independent Control:

The connection to the level-shifter should be disconnected using the solder bridges: R157, R173, R174, R188, and R190. Alternatively, the enable pins of the level-shifters can be tied to the *disabled* state using: R162, R177, R179, R191, and R193. The shunts of the pin headers are used to tie each pin to VDDREF or to GND.

The relevant sections of the evaluation module are shown in Figure 2-1 and Figure 2-2.

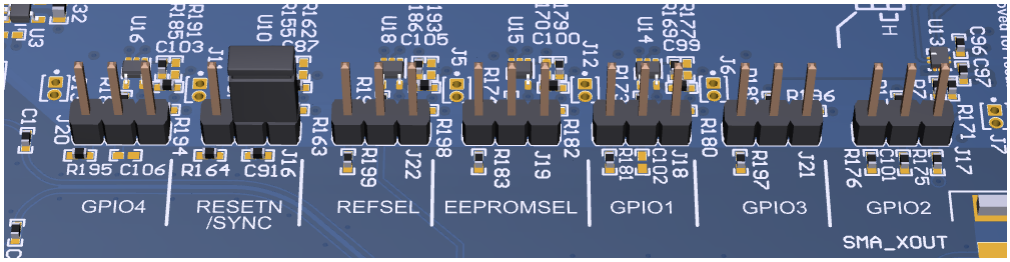


Figure 2-1. Evaluation Module Default, Control Pins

Copyright © 2017–2018, Texas Instruments Incorporated

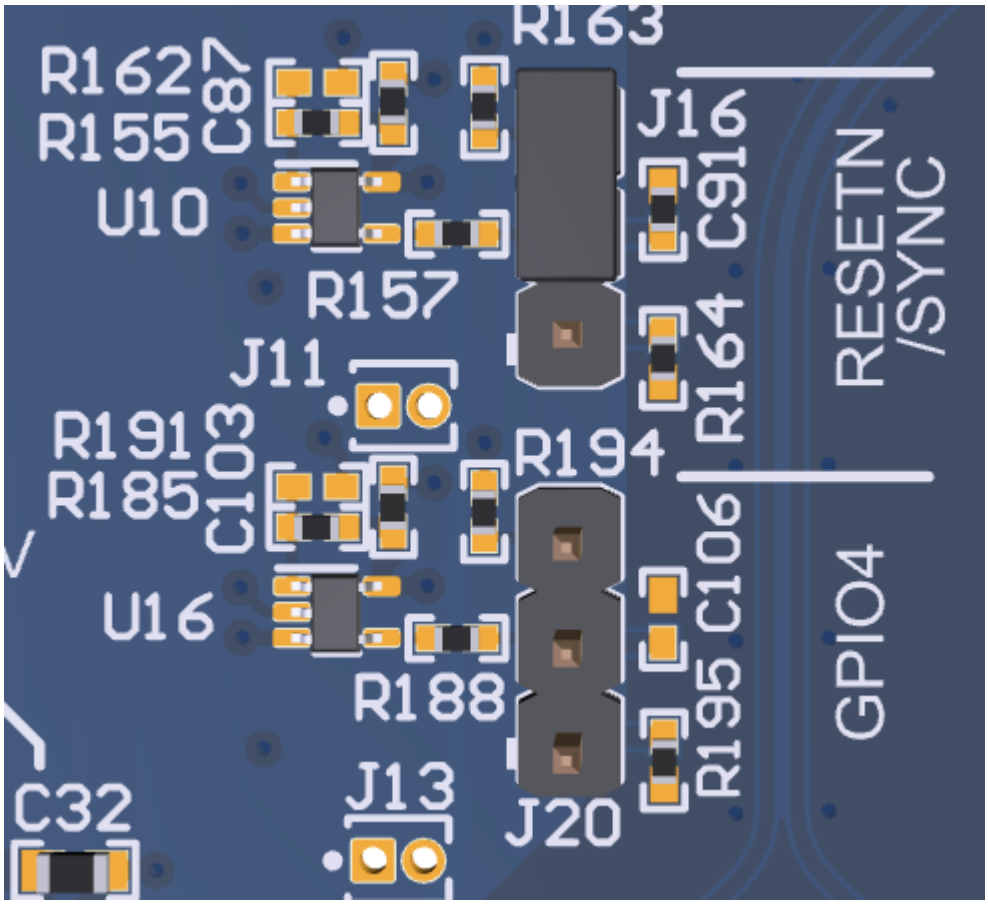


Figure 2-2. Evaluation Module Default, Control Pin Level Shifters

2.3 Reference Input

The device offers multiple-input stages:

1. Crystal Oscillator
2. LVCMOS
3. Differential AC-Coupled

The evaluation module supports all of these options. By default the board is assembled for crystal operation. the crystal is situated on the bottom side of the PCB. It connects to the top layer with R17 and R19. See Table 2-1, Figure 2-3 and Figure 2-4 for more information. Two four-pad SMD footprints are overlaid on the bottom side of the evaluation module that eases to populate 3.2-mm × 2.5-mm as well as 2.0-mm × 1.6-mm crystals.

Copyright © 2017–2018, Texas Instruments Incorporated

Table 2-1. Input Connection Options

INPUT TYPE	POPULATE	DEPOPULATE
Crystal	R15 = 0 Ω	R13, R14, R21
	R17 = 10 Ω[1]	
	R19 = 0 Ω	
	R22 = 0 Ω	
LVCMOS	C5 = 0 Ω[2]	R13, R18, R17, R19
	C7 = 0 Ω	
	R14 = 0 Ω	
	R15 = 0 Ω	
	R21 = 0 Ω	
	R22 = 0 Ω	
Differential AC-Coupled	C5 = 100 nF	R13, R17, R19
	C7 = 100 nF	
	R14 = 0 Ω	
	R15 = 0 Ω	
	R18 = 100 Ω	
	R21 = 0 Ω	
	R22 = 0 Ω	

(1) Depending on the crystal specifications, it may be required to adapt the series resistance R17 to stay within the power limit of the crystal for the set drive current, see bit-field ip_xo_gm..

(2) For very strong LVCMOS drivers it is recommended to use C5 population option for a series resistance to adapt to the trace impedance and reduce reflections at the device input.

Copyright © 2017–2018, Texas Instruments Incorporated

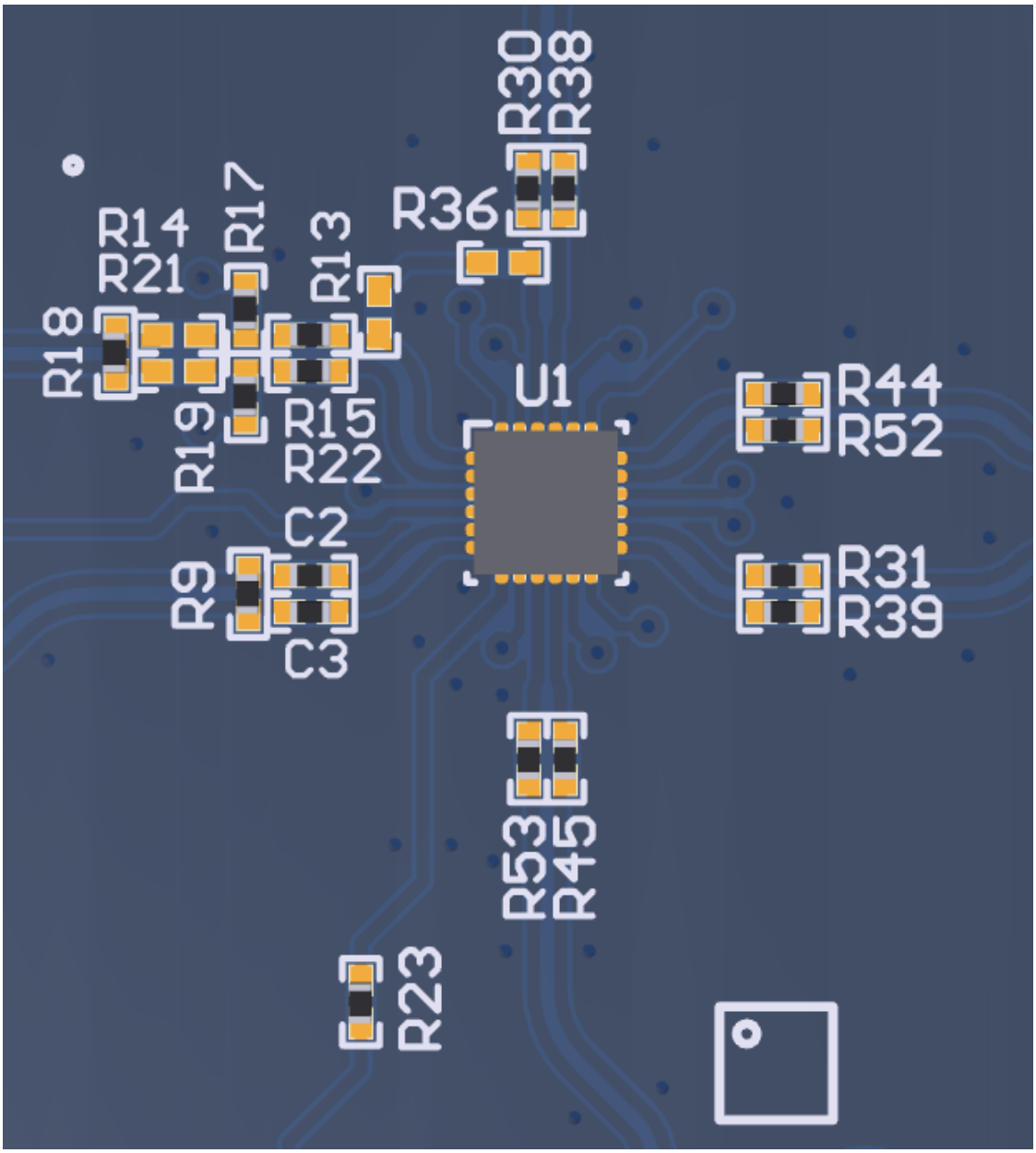


Figure 2-3. Evaluation Module Default, Reference Connection

Copyright © 2017–2018, Texas Instruments Incorporated

2.4 Clock Outputs

The evaluation module is flexible for the various output formats the device supports.

Table 2-2. Output Connection Options, Example for Y1 Channel Soldered Termination

INPUT TYPE	POPULATE	DEPOPULATE
LVDS	R28 = 49.9 Ω	C10, C16, R32, R36
	R30 = 0 Ω	
	R34 = 49.9 Ω	
	R38 = 0 Ω	
LVDS, AC-Coupled	R28 = 49.9 Ω	C10, C16, R32, R36
	R30 = 100 nF	
	R34 = 49.9 Ω	
	R38 = 100 nF	
CML, AC-Coupled	R28 = 49.9 Ω	C10, C16, R32, R36
	R30 = 100 nF	
	R34 = 49.9 Ω	
	R38 = 100 nF	
LVPECL, AC-Coupled	R28 = 49.9 Ω	C10, C16, R32, R36
	R30 = 100 nF	
	R34 = 49.9 Ω	
	R38 = 100 nF	
HCSL	R28 = 49.9 Ω	C10, C16, R36
	R30 = 0 Ω	
	R34 = 49.9 Ω	
	R38 = 0 Ω	
	R32 = 0 Ω	
LVCMOS,	R28 = 2 pF	R34, R38, C16
	R30 = 22 Ω	
	R32 = 0 Ω	
	C10 = 499 Ω with SMA short	

Copyright © 2017–2018, Texas Instruments Incorporated

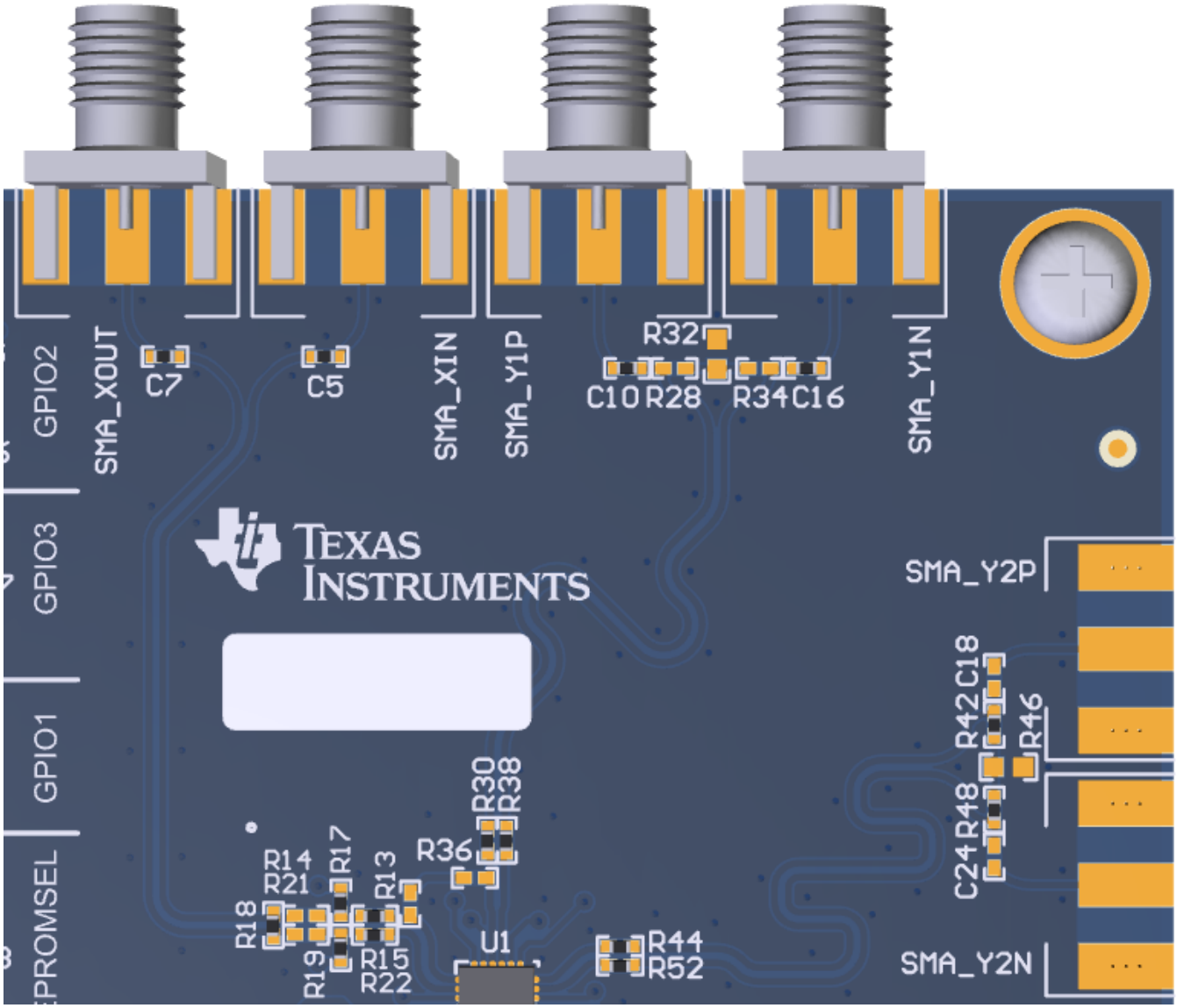


Figure 2-4. Rework, Input, and Output Termination Options

NOTE: The SMA_XOUT connector drives XIN/FB_N (pin 2) and the SMA_XIN connector drives XOUT/FB_P (pin 1).

2.5 Power Supplies

The EVM is supplied using the USB 5-V rail by default. In this configuration only a single LDO or the DC-DC switcher can be used. For mixed power supplies, TI recommends using the external 5-V option using J1 wire connector.

NOTE: The onboard power regulators are alternatively supplied from either USB 5 V or an externally supplied 5 V. Before an external supply is connected to J1, the connection to the USB supply has to be disconnected by removing J23.

Copyright © 2017–2018, Texas Instruments Incorporated

The onboard regulators have enable signals which can be connected to a common micro-controller signal controlled through the TICS Pro software. The regulators can be enabled or disabled by default using a pin-strap option.

Table 2-3. Power Supply Option Examples[1][2]

DESCRIPTION	5 V		DC-DC, ADJUSTABLE[3]			LDO, 1.8 V			LDO, 2.5 V			LDO, 3.3 V		
	J1	J23	SW	EN	DIS	SW	EN	DIS	SW	EN	DIS	SW	EN	DIS
			S2	J27	J27	S2	J26	J26	S2	J25	J25	S2	J24	J24
USB only, 1.8 V, LDO, Default	no connect	close	3-6 on		-		+				-			-
USB only, 1.8 V, DC-DC	no connect	close	4-5 on	+				-			-			-
External supply, 1.8 V, DC-DC	connect	open	4-5 on	+				-			-			-
External supply, 1.8 V, DC-DC, 3.3-V LDO	connect	open	4-5 on	+				-			-	1-8 on	+	
External supply, 1.8 V, DC-DC, 1.8-V to 3.3-V LDO	connect	open	4-5 on	+		3-6 on	+		2-7 on	+		1-8 on	+	

(1) Legend: "blank" = switch set to OFF. "+" = shunt set to EN position. "-" shunt set to disable position.
(2) As there is a shared enable signal: all shunts must have the same setting when connected using the switch. Otherwise they must be disconnected. E.g. only per default enabled signals are connected or only disabled signals.
(3) By default set to 1.8 V.

NOTE: For USB-only operation, only a single power regulator is recommended to be enabled at a time. The other regulators, shall be kept disabled using the pin-strap options.

The clock generator offers four separate supply domains for each block of the device. The supplies can be mixed using 1.8 V, 2.5 V, or 3.3 V. Each supply is selected using a resistor solder option on the bottom side of the evaluation module.

NOTE: For each supply only one resistor may be populated at a time.

Table 2-4. Power Distribution[1]

SUPPLY	VDDREF				VDDVCO				VDDO12				VDDO34			
	DC-DC	LDO, 1.8 V	LDO, 2.5 V	LDO, 3.3 V	DC-DC	LDO, 1.8 V	LDO, 2.5 V	LDO, 3.3 V	DC-DC	LDO, 1.8 V	LDO, 2.5 V	LDO, 3.3 V	DC-DC	LDO, 1.8 V	LDO, 2.5 V	LDO, 3.3 V
	R92	R91	R90	R89	R110	R109	R108	R107	R100	R99	R98	R97	R114	R113	R112	R111
1.8 V, LDO, Default		x				x				x				x		
1.8 V, DC-DC	x				x				x				x			
Voltage Translation 3.3 V → 1.8 V, LDO + DC-DC				x				x	x				x			
Voltage Translation 1.8 V → 2.5 V, LDOs		x				x					x				x	

(1) For mixed configurations, the 5 V is recommended to be supplied externally using J1 connector.

Copyright © 2017–2018, Texas Instruments Incorporated

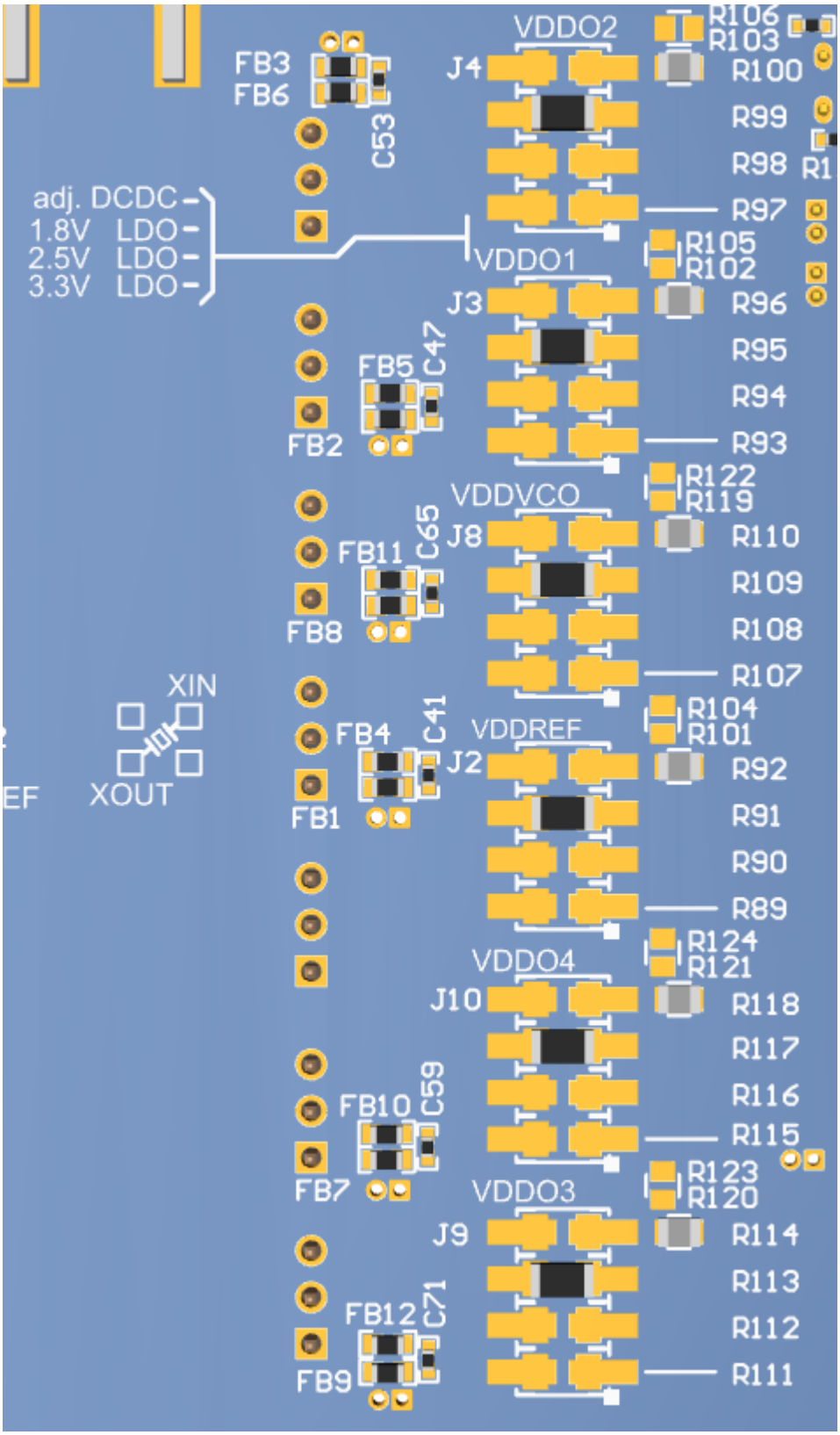


Figure 2-5. Evaluation Module Default, Power Distribution

Copyright © 2017–2018, Texas Instruments Incorporated

Each supply has multiple options for local decoupling and noise reduction using ferrite beads which can be optimized for custom frequency plans.

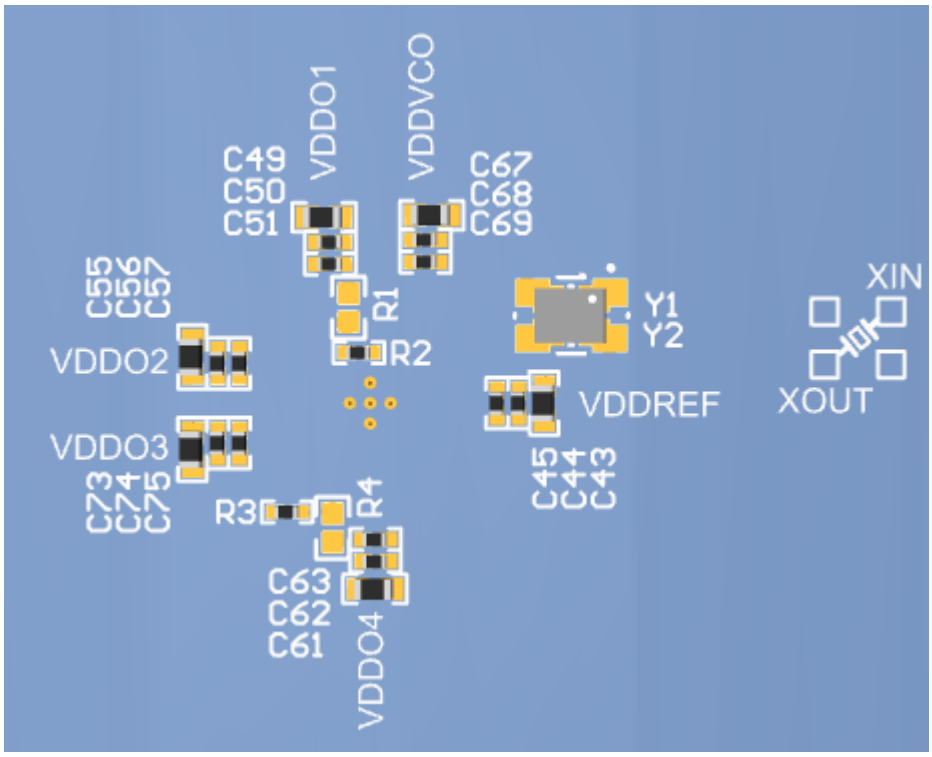


Figure 2-6. Evaluation Module Default, Device Connection

Copyright © 2017–2018, Texas Instruments Incorporated

Frequently Asked Questions - FAQ

3.1 Troubleshooting

Question:	Suggestion:
I want to measure the current consumption of the device. Where can I do that?	For a first-order estimate, the best option is to use an external 5-V supply with current measurement option. Remove J23 before you connect to J1. The individual supplies have ferrite beads for better noise isolation. Next to each ferrite are two full-through VIAs which can be used to solder in a current probe with the ferrite bead removed. Alternatively, a shunt resistor can be populated here on resistors like R100.
I programmed the unit and I see that the PLL lock detector status bit shows a locked PLL, but I do not get any outputs from the device.	Check if you configured one of the GPIOs as a output enable pin. Maybe the signal is set to GND or TICS Pro still drives low level to the pin.
I click in the software or I set the RESETN/SYNC pin to low, but the device keeps active.	GPIO0 might be configured as status output. Thus the only way to reset the device is a power-cycle on VDDREF.
I tried different slave addresses and power cycled the device. Nothing makes the serial interface work! Is the unit broken?	The EEPROM of the unit may contain a configuration which disables the serial interface and instead uses the pins as output enable pins. Does the unit start reacting when you set EEPROMSEL to GND or VDDREF, followed by a power-cycle with RESETN at VDDREF level? REFSEL must always be tied to GND when doing this. When the unit does not react, both EEPROM pages seem to have disabled the interface. Enter *Fallback-Mode* to force the serial interface active. Remove any shunts from J19 and J22 and configure the pins in TICS Pro to *Hi-Z* state. When you do not use the software, disconnect the level shifters by removing R174 and R190. This leaves EEPROMSEL and REFSEL pin floating. Power-cycle the unit and ensure that RESETN/SYNC pin (J16) sees a VDDREF level. Either by using TICS Pro to drive the level or using a shunt on J16-2-3. You should see that the device responds on slave address 0x74.
The device does not draw current any current. Also the regulators seem not to be operating.	Cross-check Table 2-3 for the switch and shunt settings. The enable signal might be blocked by a wrong setting.

Copyright © 2017–2018, Texas Instruments Incorporated

I want to test the zero delay mode to minimize the phase delay between input clock and output clocks. Can I do this on this EVM?	Yes, you can evaluate zero delay mode on this EVM. You are going to need a set of very well flight-time matched 50 Ω SMA cables with at least six pieces. • Connect REF inputs to the clock source. • It can be advantageous to buffer in the clock source using a dedicated buffer part, to generate another clock copy for viewing on a scope. • Connect Y2P to FB_P and Y2N to FB_N and rework the EVM with AC-coupling on C5, C7 and with R14=R21= 0 Ω and R17, R19 depopulated. • Connect Y3 to the scope. • Enable the input clock source. • Configure the device for your frequency plan and ensure the input and output buffers match. • Ensure that the reference divider to the PLL is set to division "/1". • Ensure that the Y2 output frequency matches the input frequency at REF. • Set zdm_clocksel = 1 (external feedback), zdm_auto = 1, ref_mux_src = 1, ref_mux = 1 and then zdm_mode = 1. Re-calibrate the PLL using recal = 1. • You will see that the device operates in zero delay mode. In zero delay mode the least delay is achieved using each output channels own integer divider. When you test the zero delay mode with internal feedback: this happens using Y2. Any inherent delay from the PLL setup and input path can be minimized using the digital delay in the output channels. You will have to introduce an offset between feedback output Y2 and the Y1,Y3,Y4 which drive actual receivers.
I tried the divider synchronization and now all the outputs are muted. What did I do?	Cross-check the following: The input muxes of the integer dividers in each of the output channels must have a valid (=active) pre-scaler clock selected. Moreover the ch[4:1]_sync_en bits must be set. Moreover check the actual block power down bits if the required pre-scaler clock tree and the output channel are active.
I evaluated the CDCI6214 clock generator and I am designing my own application board. Until I've finished my production program, how do you recommend to program first samples for my application prototypes?	For few units you could use the EVM and wire it into your application. To wire the serial interface from the EVM to your application board. Replace R176, R197 using 0 Ω. Then you can wire J17, J21 to your application. Should you need a power supply as well, you can insert J28 to access an additional output port of the DC/DC-switcher. For larger amounts we recommend to design your application board including an in-system programming option, when your system allows it. This evaluation module can be used as reference for the control pin pin-strap options. When you want to omit any in-system programming and take advantage of the factory-pre-programmed devices, please contact your TI representative for options.

Copyright © 2017–2018, Texas Instruments Incorporated

References

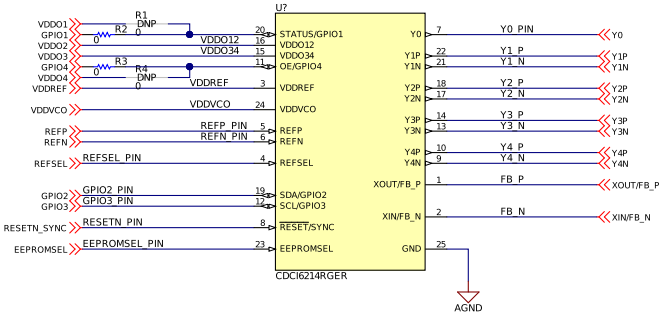
A.1 Software

To download the latest newest version of the TICS Pro software, go to http://www.ti.com/tool/ticspro-sw.

The device profile for the EVM is available in the "Clock Generator-Jitter Cleaner (Single Loop)" category for the clock generator "CDCI6214".

Copyright © 2017–2018, Texas Instruments Incorporated

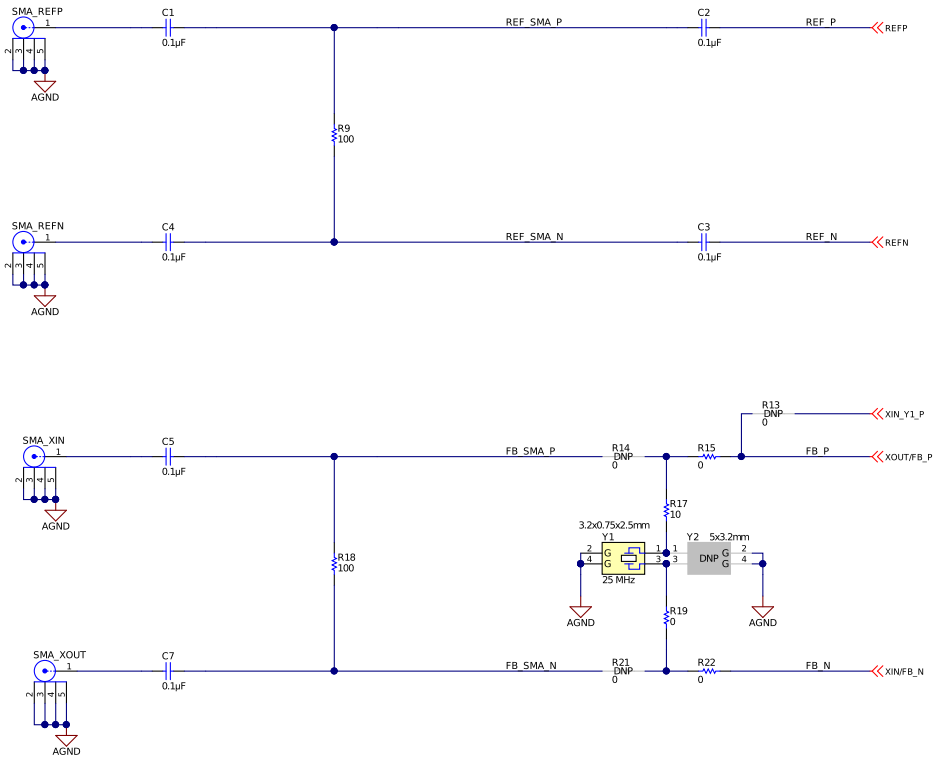
A.2 EVM Schematics



Copyright © 2018, Texas Instruments Incorporated

Figure A-1. Schematics, Clock Generator

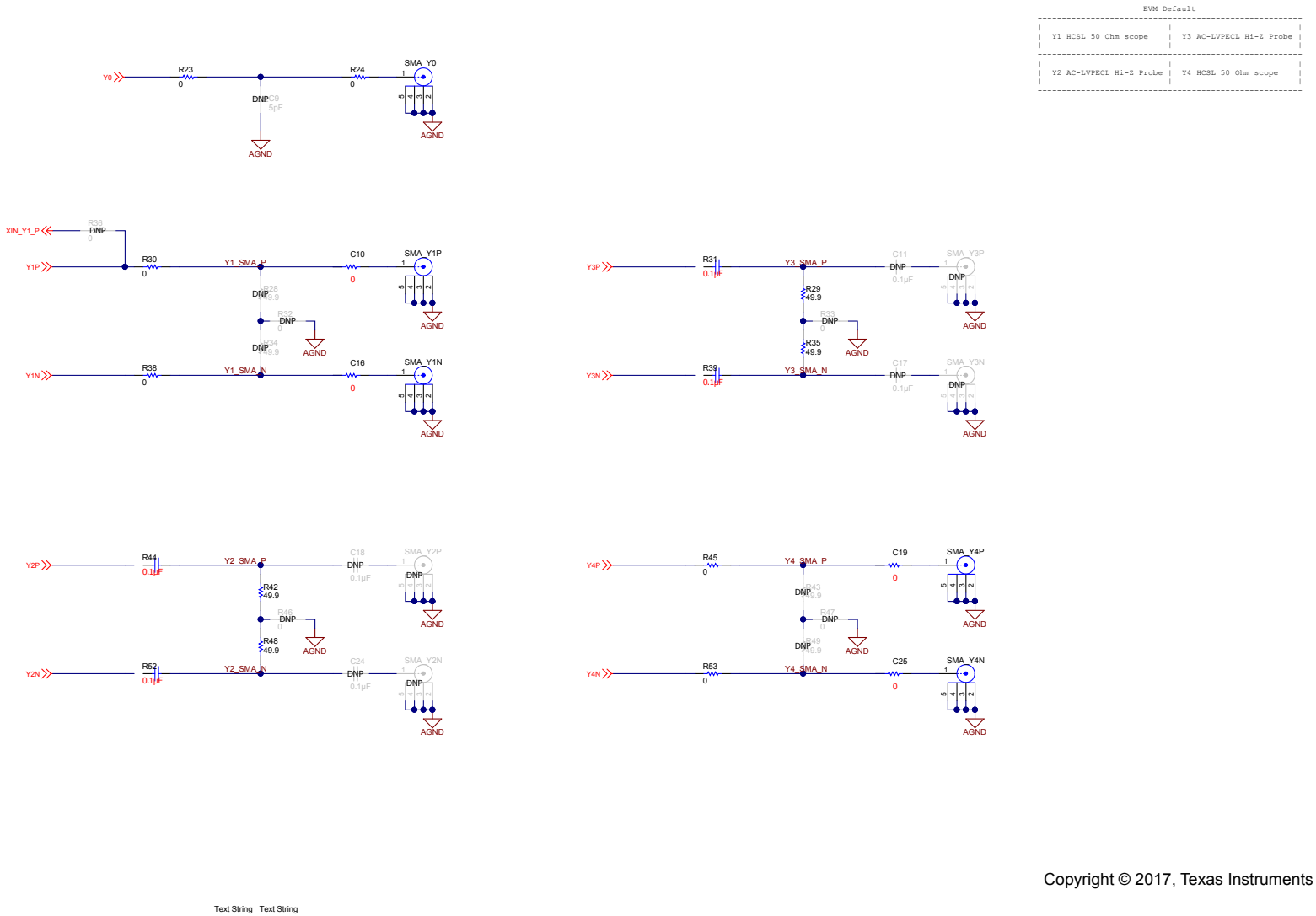
Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2018, Texas Instruments Incorporated

Figure A-2. Schematics, Inputs

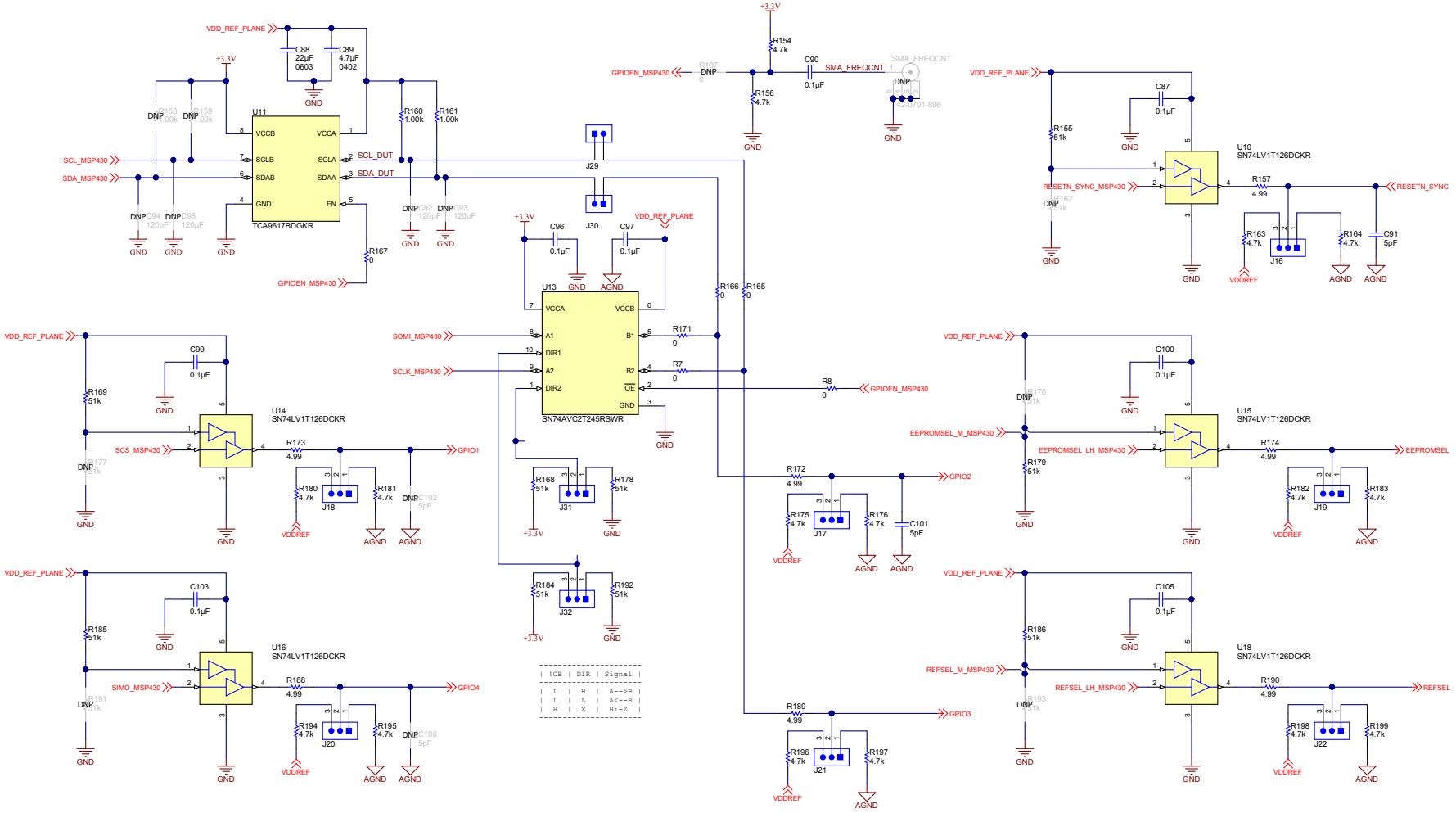
Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2017, Texas Instruments Incorporated

Figure A-3. Schematics, Outputs

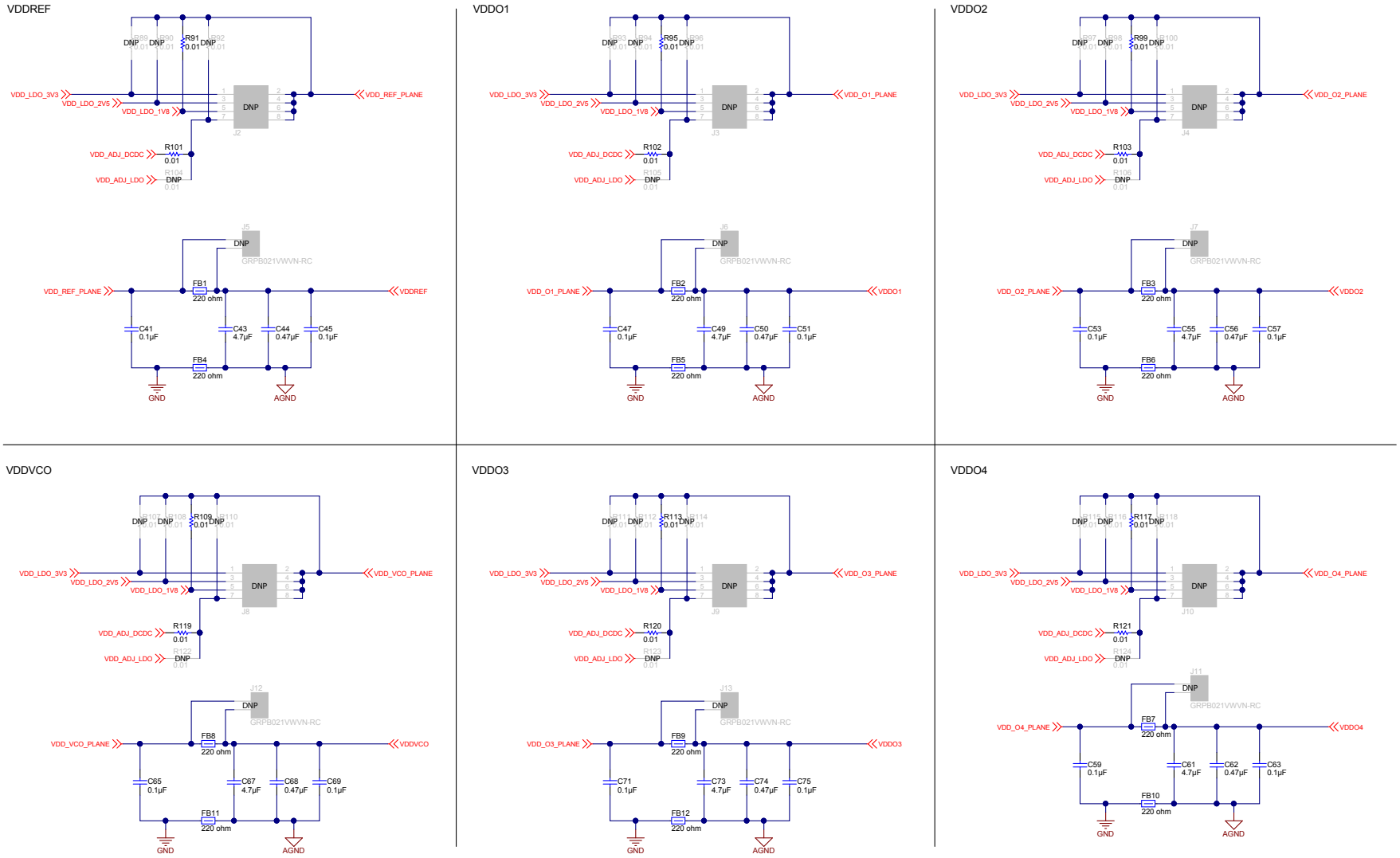
Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2017, Texas Instruments Incorporated

Figure A-4. Schematics, Control Pins

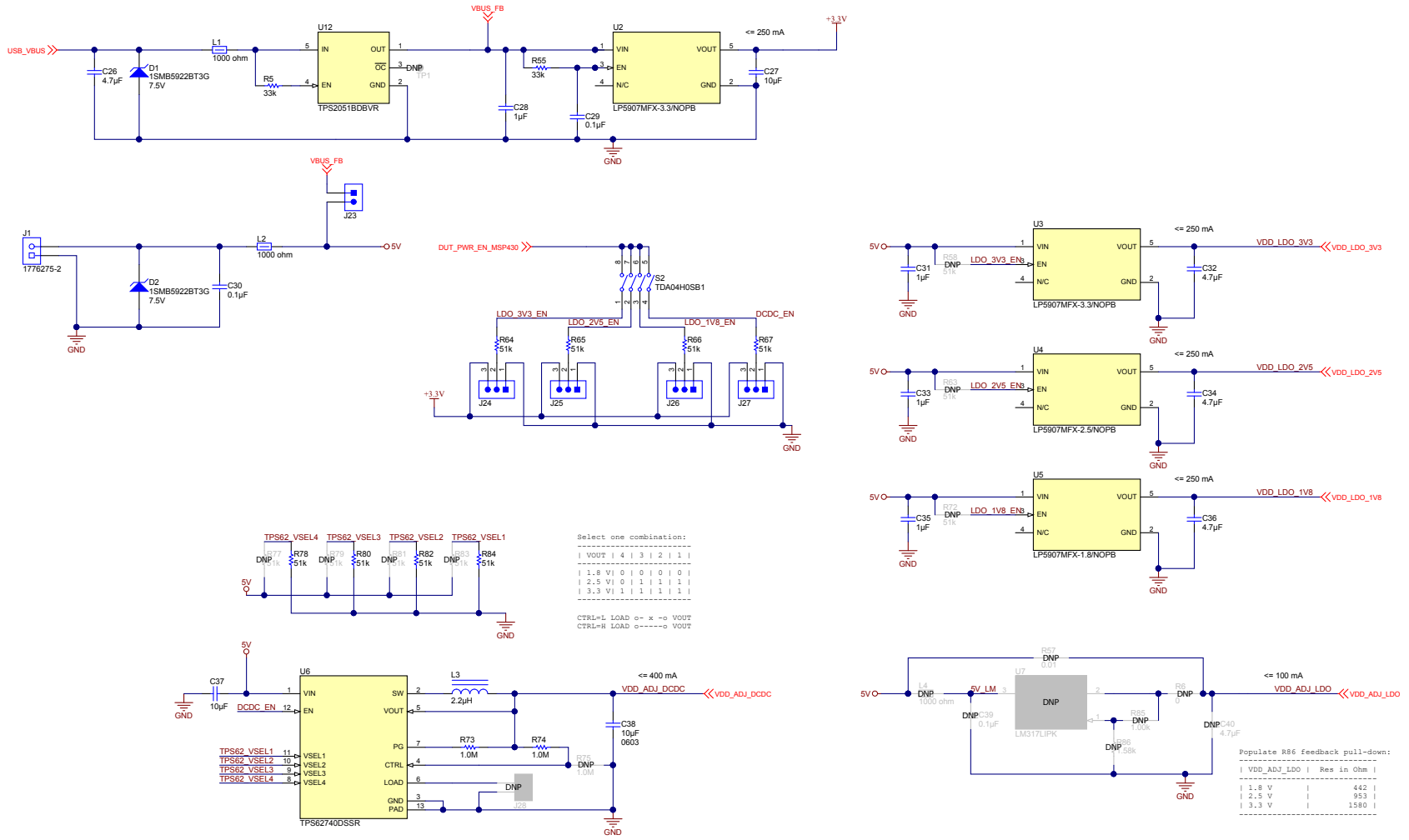
Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2017, Texas Instruments Incorporated

Figure A-5. Schematics, Power Distribution

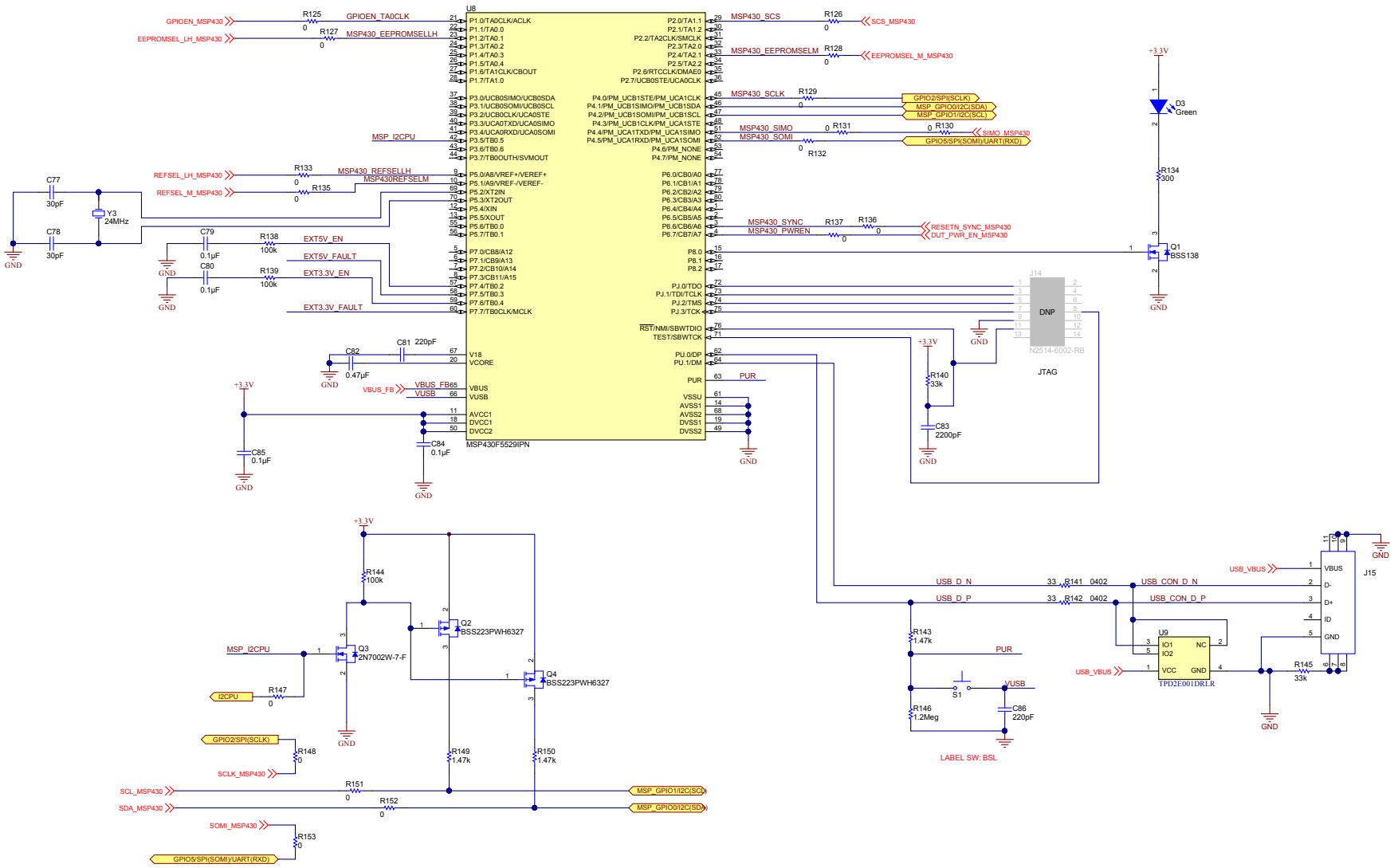
Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2017, Texas Instruments Incorporated

Figure A-6. Schematics, Power

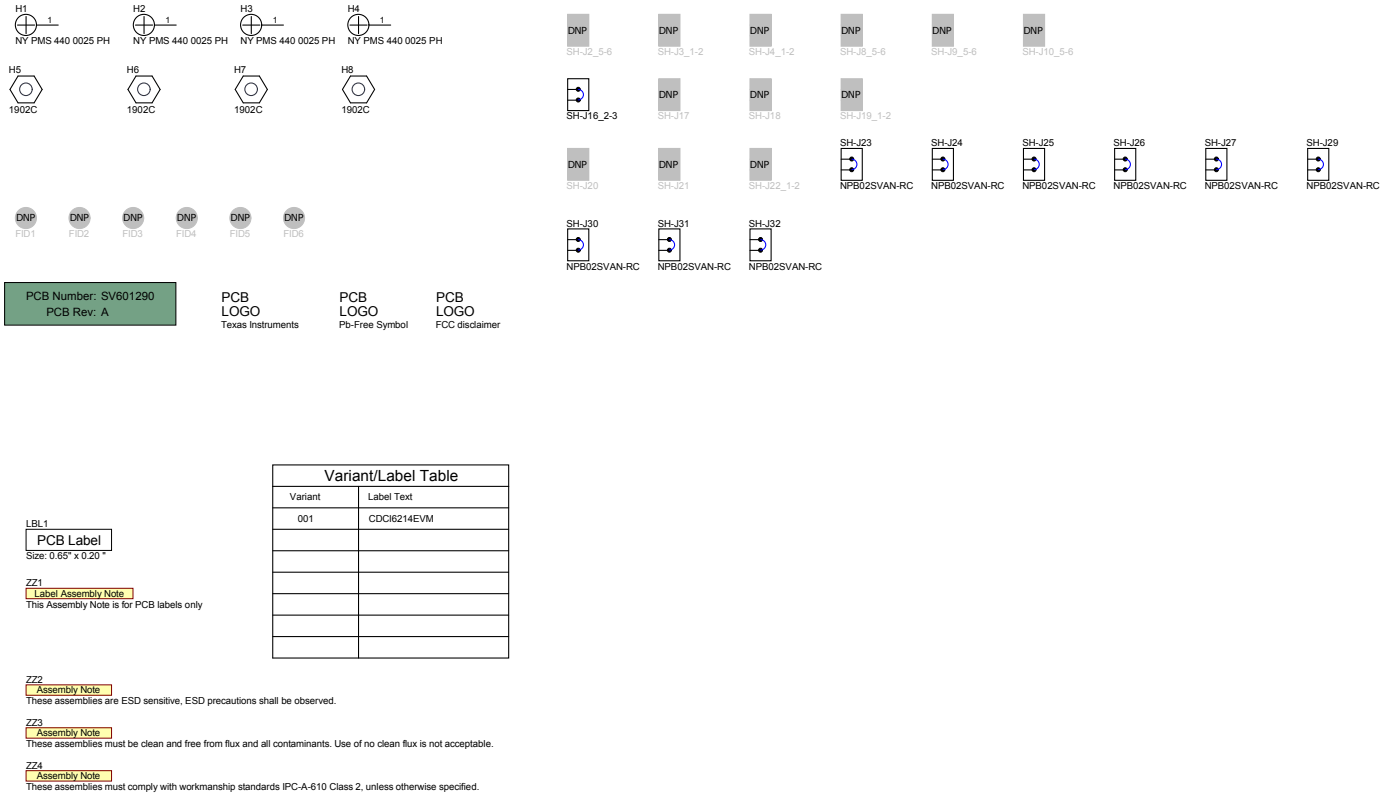
Copyright © 2017–2018, Texas Instruments Incorporated



Copyright © 2017, Texas Instruments Incorporated

Figure A-7. Schematic, USB Interface

Copyright © 2017–2018, Texas Instruments Incorporated



Variant/Label Table	
Variant	Label Text
001	CDCI6214EVM

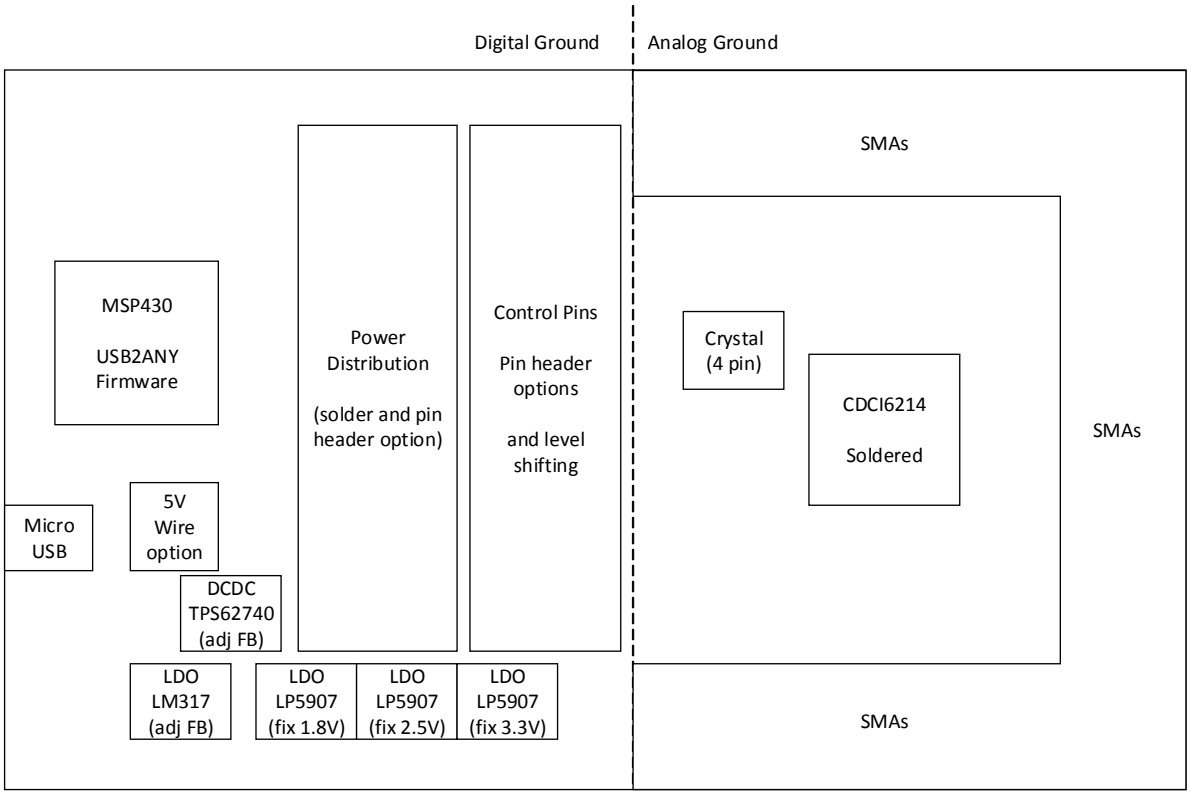
Copyright © 2017, Texas Instruments Incorporated

Figure A-8. Schematic, EVM Hardware

Copyright © 2017–2018, Texas Instruments Incorporated

CDCI6214EVM

Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



Copyright © 2017, Texas Instruments Incorporated

Figure A-9. Schematic, Block Guidance

Copyright © 2017–2018, Texas Instruments Incorporated

A.3 EVM Layout

Table A-1. Stack-Up

NO.	LAYER	NAME	MATERIAL	THICKNESS IN m	DIELECTRIC CONSTANT	DESCRIPTION
1		Top Solder	solder resist	0.79	3.5	
2	1	Top Layer	copper	0.67		RF signals
3		Dielectric 1	FR-4	12.21	4.2	
4	2	Middle Layer 1	copper	1.38		Ground
5		Dielectric 2	FR-4	31.50	4.8	
6	3	Middle Layer 2	copper	1.38		Ground, power routing, control signals
7		Dielectric 3	FR-4	12.21	4.2	
8	4	Bottom Layer	copper	0.67		Power routing, control signals
9		Bottom Solder	solder resist	0.79	3.5	

Copyright © 2017–2018, Texas Instruments Incorporated

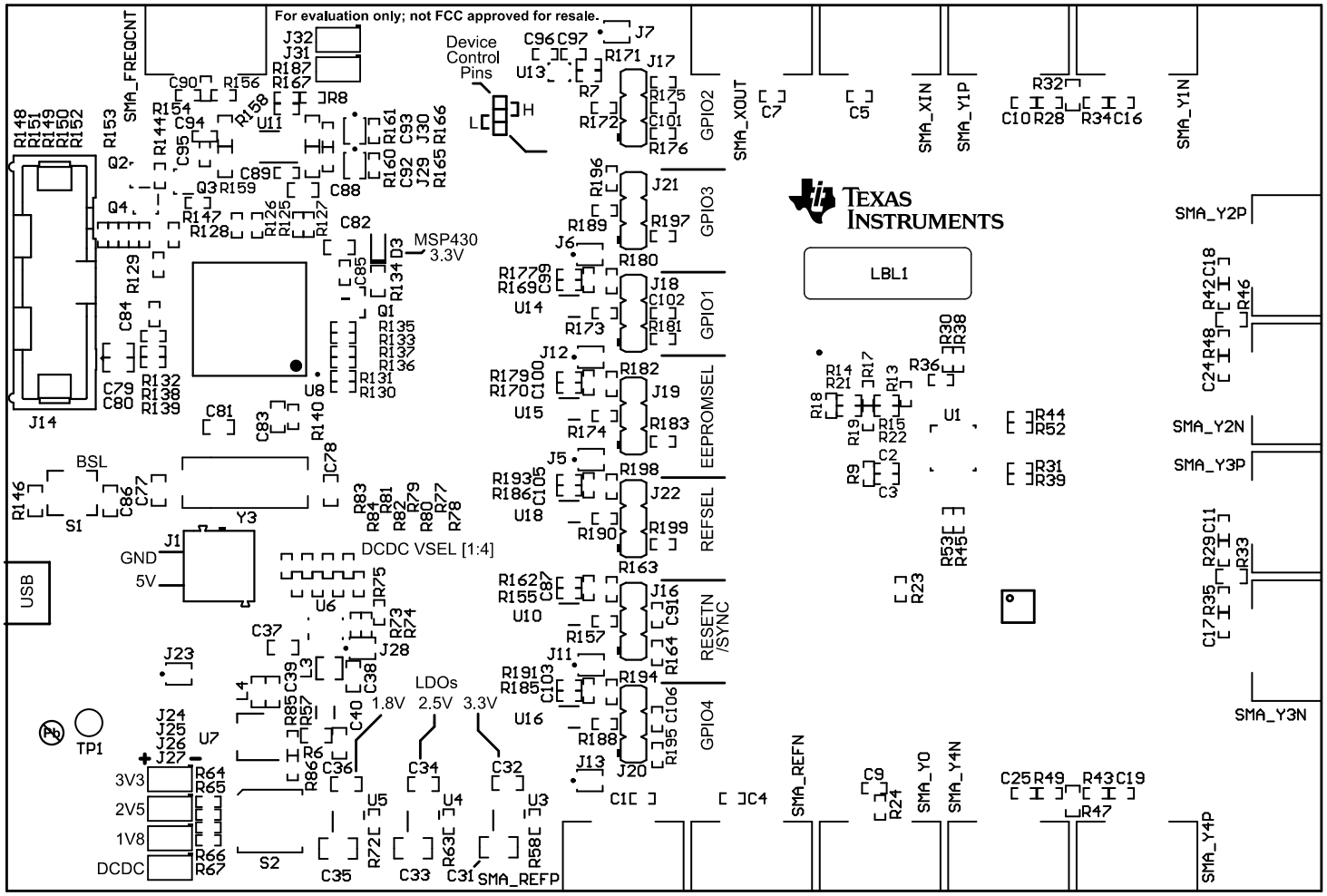


Figure A-10. Layout, Assembly Top

Copyright © 2017–2018, Texas Instruments Incorporated

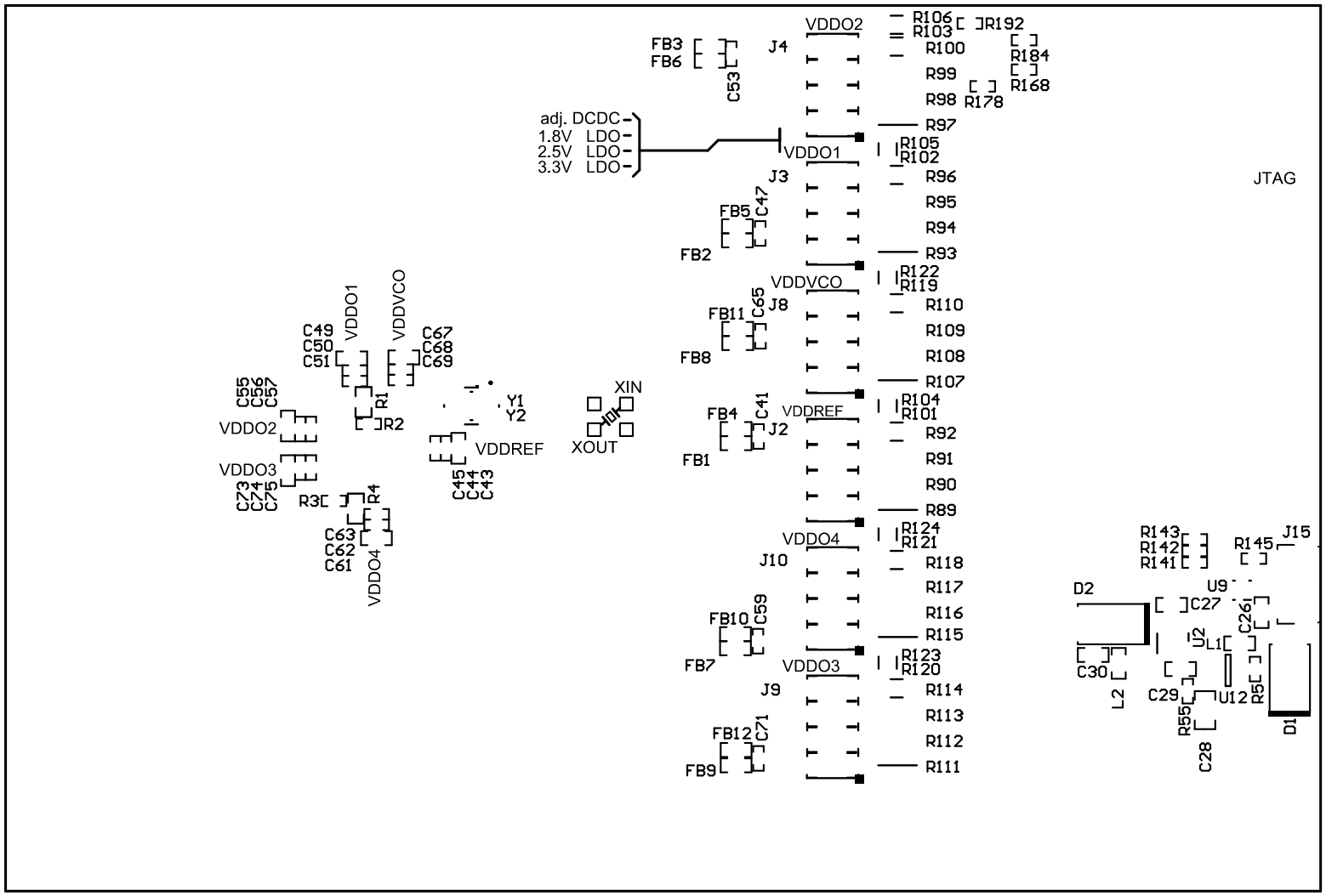


Figure A-11. Layout, Assembly Bottom

Copyright © 2017–2018, Texas Instruments Incorporated

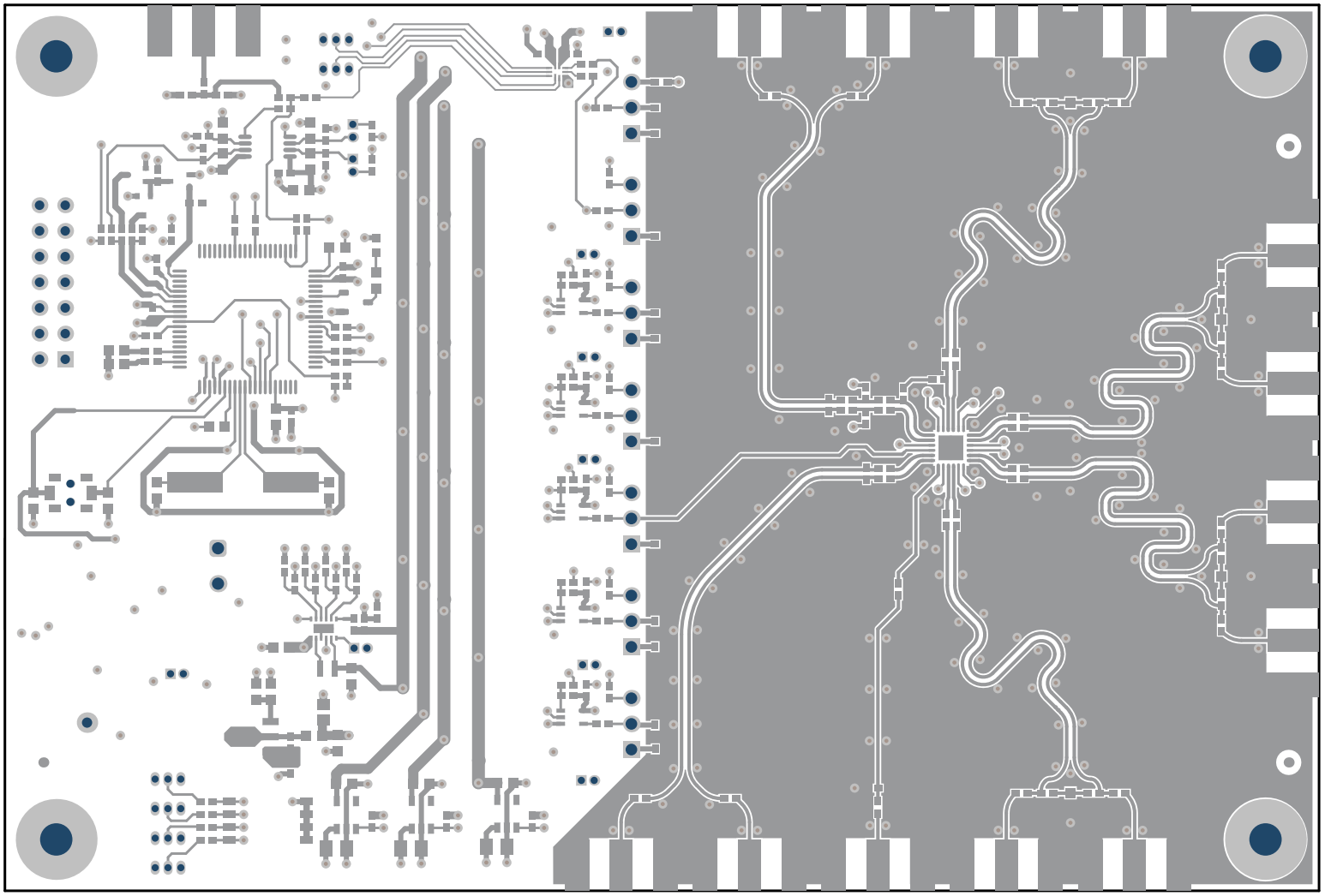


Figure A-12. Layout, Top Layer

Copyright © 2017–2018, Texas Instruments Incorporated

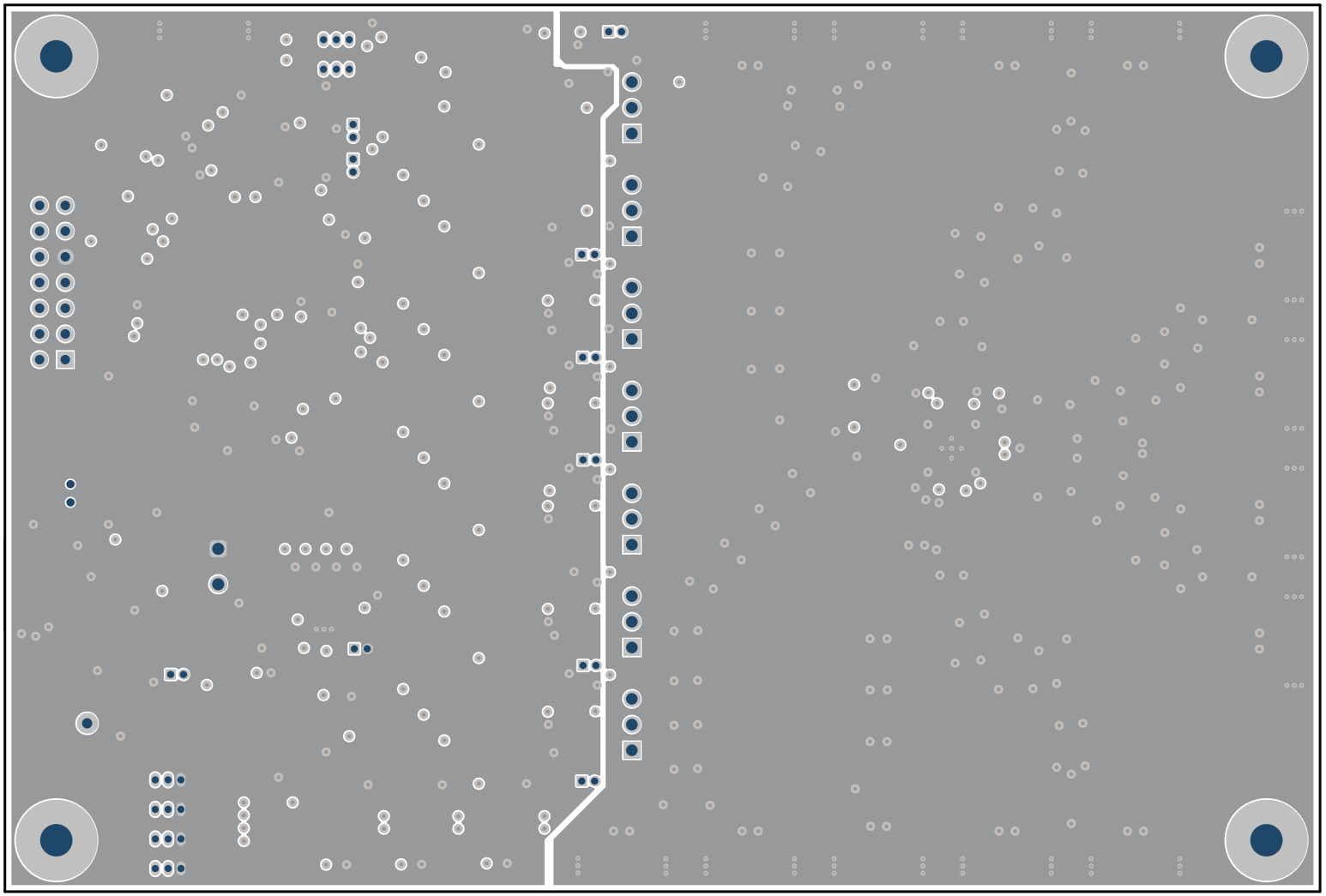


Figure A-13. Layout, Middle Layer 1

Copyright © 2017–2018, Texas Instruments Incorporated

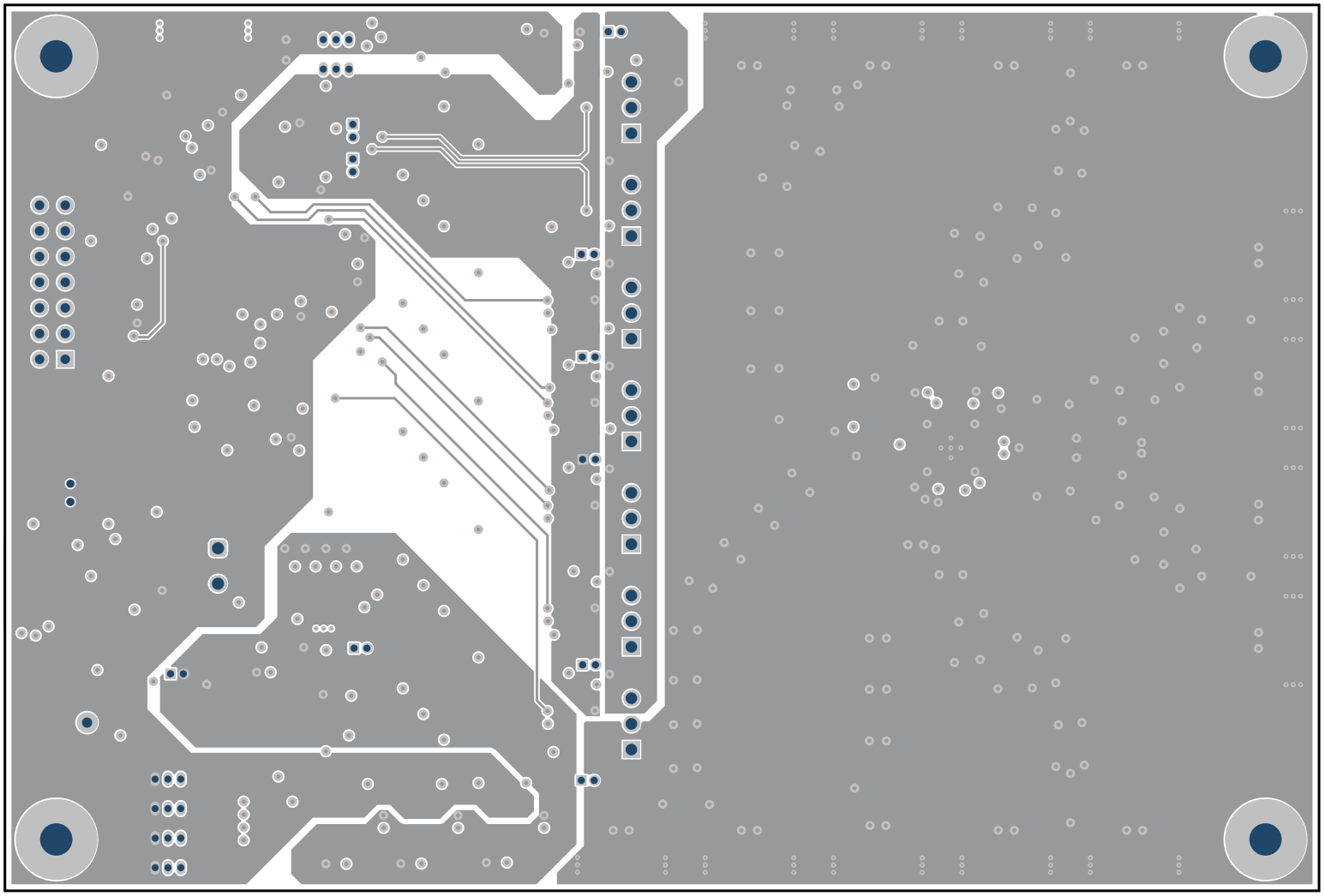


Figure A-14. Layout, Middle Layer 2

Copyright © 2017–2018, Texas Instruments Incorporated

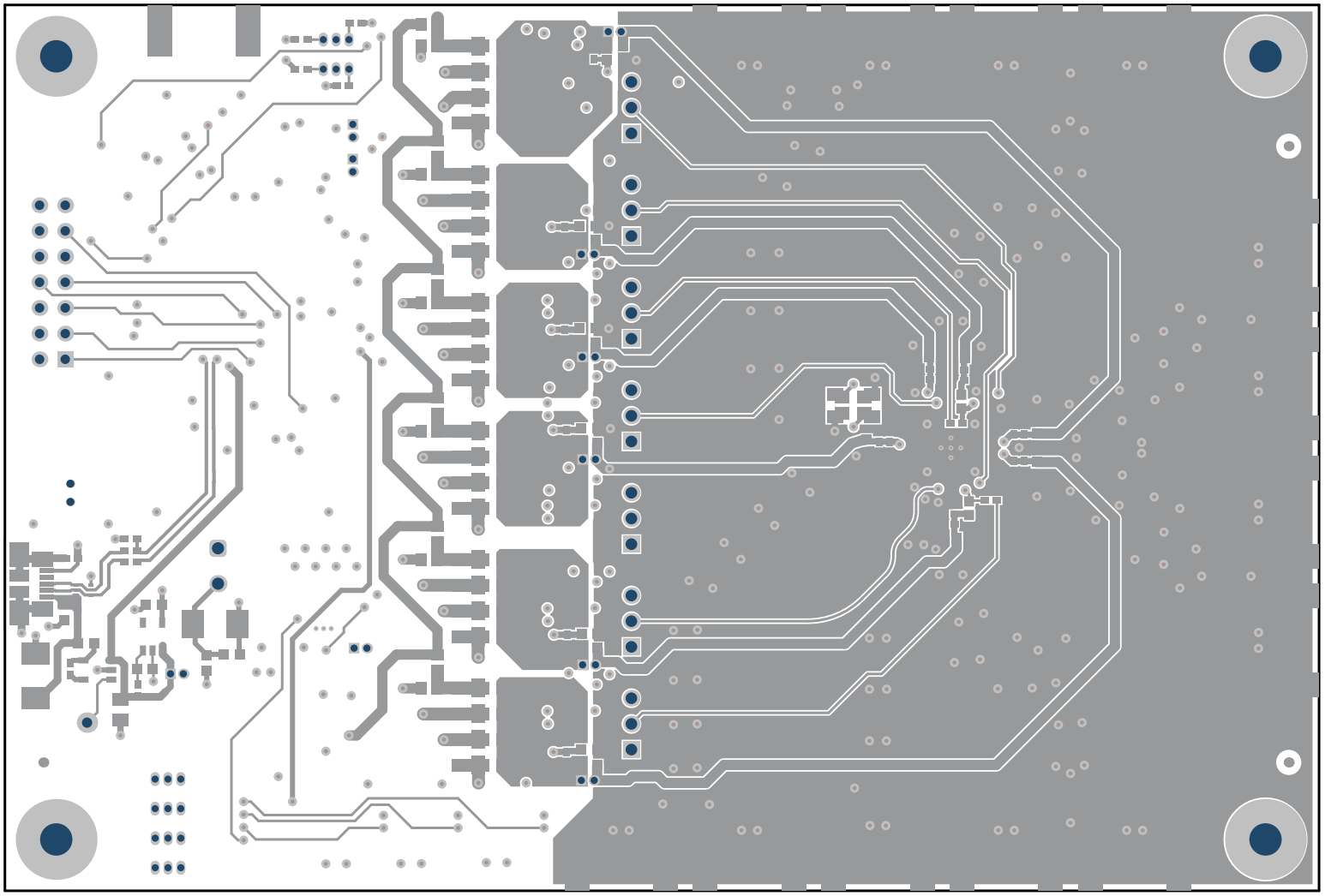


Figure A-15. Layout, Bottom Layer

Copyright © 2017–2018, Texas Instruments Incorporated

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (September 2017) to B Revision **Page**

- Added notice for silkscreen typo to Figure 1-1 6
- Added notice for silkscreen typo to Figure 2-4 13
- Changed "must" to "is recommended to" 14
- Updated U7 symbol in Figure A-1 20
- Updated the off sheet connectors on pins 1 and 2 in Figure A-1 20
- Updated the off sheet connectors on pins 1 and 2 in Figure A-2 21

Changes from Original (July 2017) to A Revision **Page**

- Changed EVM image from APL to production data release 6
- Removed reference to socket option 8
- Added "device" for clarification. 8
- Updated power supply options table to reflect switch and jumper name updates 14
- Changed USB-only operation note from "required" to "recommended". 14
- Added more FAQ answers. 17
- Added Figure A-8 and Figure A-9 27

Copyright © 2017–2018, Texas Instruments Incorporated

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。 技術適合証明を受けていないもののご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

東京都新宿区西新宿６丁目２４番１号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

   6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.

7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

   8.1 *General Limitations*. IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

   8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated