

LMX2624-SP Evaluation Module With 26GHz Space Grade Synthesizer



Description

LMX2624SPEVM is used to evaluate the performance of the LMX2624-SP device. This device is a space grade RF synthesizer in 10mm x 10mm 64-pin plastic package. LMX2624-SP is able to generate continuous wave signal up to 26GHz. LMX2624SPEVM evaluation module provides all the hardware interface to enable users to quickly evaluate and develop with the LMX2624-SP RF synthesizer.

Get Started

1. Order the EVM, [LMX2624SPEVM](#).
2. Download the latest programming GUI, [TICS Pro](#).
3. Download the PLL simulation tool, [PLLatinum Sim](#).
4. Learn more about VCO calibration, [SNA4336](#).
5. Ping-pong architecture overview, [SNA4357](#).

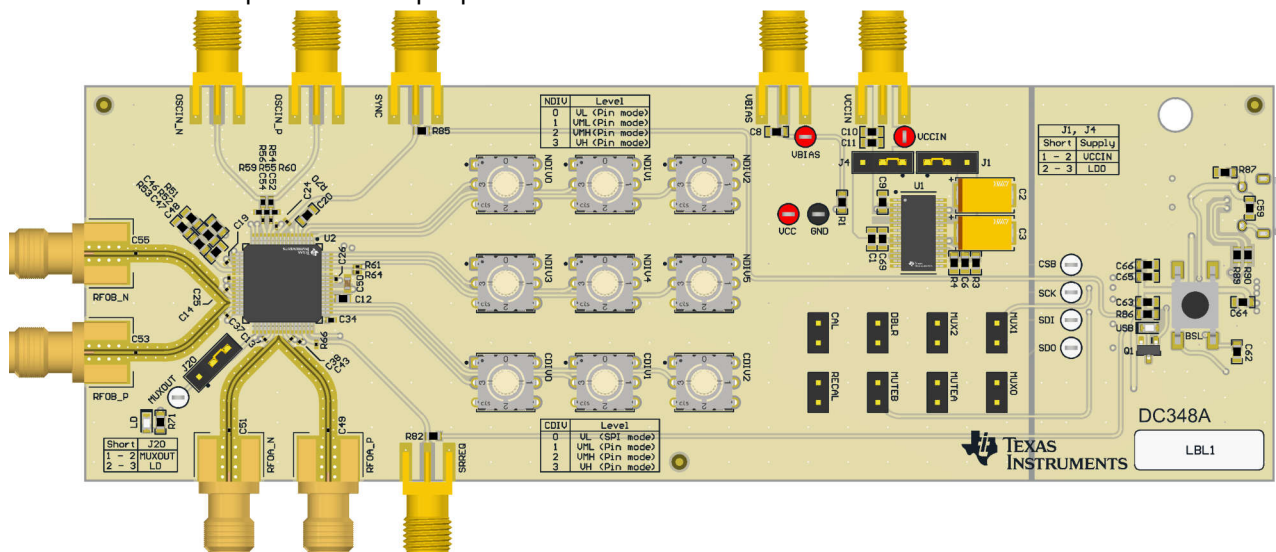
Features

- Up to 15.24GHz direct VCO output and 26GHz VCO doubler output at both output ports

- JESD204 SYSREF clock generation and repeater mode operation
- Support synchronization of output phase across multiple devices
- Onboard USB interface for SPI control
- Support pin control operation without SPI programming

Applications

- [Space communications](#)
- [Space radar systems](#)
- Phased array antennas and beam forming
- High-speed data converter clocking (supports JESD204B)



1 Evaluation Module Overview

1.1 Introduction

LMX2624SPEVM board contains a LMX2624-SP space grade (Engineering mode) RF synthesizer, a very low noise LDO and a microcontroller (also referred to as *USB2ANY*). The board has two RF outputs, RFOUTA and RFOUTB. The RF outputs can output divided down, direct VCO or VCO doubler output up to 26GHz. RFOUTB also support low frequency SYSREF clock output. SYSREF operation includes continuous SYSREF clock generation and SYSREF pulser mode. SYSREF repeater mode is also supported by feeding external SYSREF signal to the EVM.

Configuration to the LMX2624-SP device is made through the onboard USB2ANY to a PC. [TICS Pro](#) is used to configure and program the LMX2624-SP device.

LMX2624-SP can operate in pin mode, in this case, no register programming is required. Onboard rotary switches and 2-pin headers are used to set up the configuration of the LMX2624-SP device.

1.2 Kit Contents

Included within each evaluation kit is:

- One LMX2624-SP EVM board (DC348-001) with integrated USB2ANY controller
- One USB cable

1.3 Specification

Table 1-1. LMX2624-SP EVM Specification

| Parameter | Value | Conditions |
|-----------------------|---|----------------------------|
| Supply voltage | VCCIN: 3.3V | Onboard LDO is bypassed |
| | VCCIN: 3.6 to 4.0V VBIAS: 5.0V | Onboard LDO output is 3.3V |
| Supply current | 1.1A maximum. | Configuration dependent |
| OSCIN input frequency | 5MHz to 1GHz | 10dBm |
| RF output frequency | 4.96MHz to 26GHz | RFOUTA, RFOUTB |
| SYSREF | Continuous clock generation Pulser generation Repeater mode | RFOUTB |

1.4 Device Information

The LMX2624-SP is a high performance, space grade, wideband phase-locked loop (PLL) with integrated voltage controlled oscillator (VCO) that can generate any frequency from 4.96MHz and 26GHz. The device runs from a single 3.3V supply and has integrated LDOs that eliminate the need for onboard low noise LDOs.

LMX2624-SP has two output channels, the channels can support direct VCO output, divided down output and VCO doubler output. Output channel B can also support SYSREF clock output. Output can be quickly muted through pin control, response time is as short as 10ns. This feature is especially useful for ping-pong switching application. See [SNAA357](#) for details.

Multiple LMX2624-SP devices can be synchronized so that the output phases are aligned. Output phase with respect to the input reference clock is also adjustable.

With a new Full Assist operation, LMX2624-SP VCO lock time is greatly reduced to within 20 μ s.

Configuration of LMX2624-SP is made through SPI programming. LMX2624-SP can operate without SPI programming via pin strapping in Pin mode.

This device is fabricated in Texas Instruments' advanced BiCMOS process and is available in a 64-lead 10mm x 10mm QFP plastic package.

2 Hardware

2.1 Setup

2.1.1 Evaluation Setup Requirement

At a minimum, evaluation of the EVM requires:

- A DC power supply capable of at least 5V, 2A
- A high quality signal source, such as an SMA100B
- A spectrum analyzer or phase noise analyzer up to 26GHz
- A PC running Windows 7 or a more recent version with [TICS Pro](#) software installed

Full evaluation requires the following additional hardware:

- A high speed 4-channel oscilloscope capable of resolving 5ps step size for phase adjustment and SYSREF delay evaluation
- An arbitrary function generator or a pulse source capable of outputting square wave continuous clock or pulses for phase synchronization and SYSREF evaluation

2.1.2 Connection Diagram

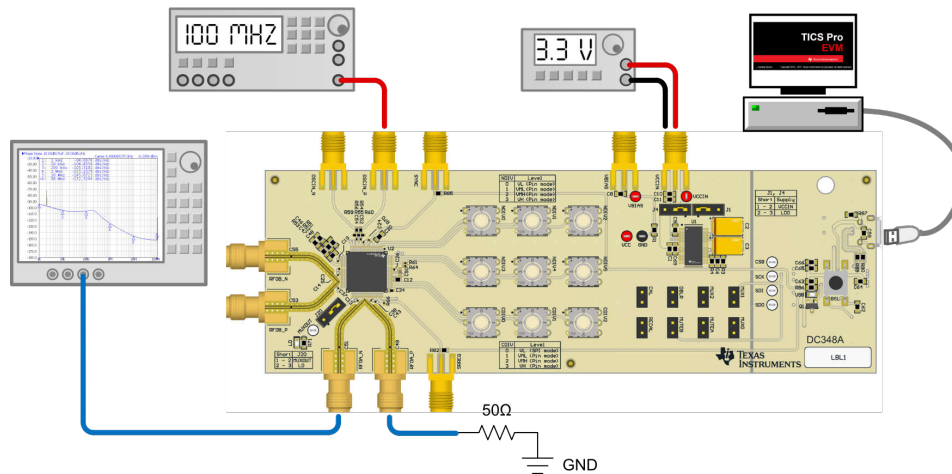


Figure 2-1. Connection Diagram

2.2 Jumper Information

Jumper J1 and J4 determines the supply voltage to the board.

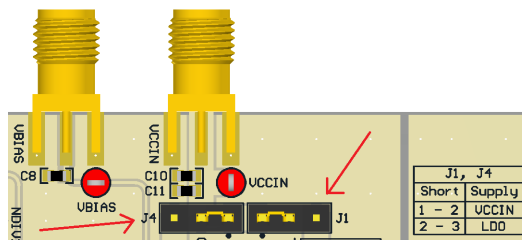


Figure 2-2. Power Supply Jumpers

To bypass the LDO, set these jumpers to the 1-2 position. This is the EVM default configuration.

To use the LDO, set these jumpers to the 2-3 position.

2.3 Power Requirements

When LDO is bypassed (EVM default configuration). Apply 3.3V to VCCIN SMA connector. Acceptable supply voltage range is 3.2V to 3.4V.

When using the LDO, apply 3.6V to 4V to VCCIN SMA connector. Apply 5V to VBIAS SMA connector.

The board can draw up to 1A during operation, so the resistance of the power cable is matter.

2.4 Reference Clock

Connect OSCIN_P SMA connector to a high quality signal source such as an SMA100B signal generator. Set the output power of the signal generator to 10dBm.

Input can be driven differentially. Populate R56, connect both OSCIN_P and OSCIN_N SMA connectors to a balun or a differential clock source. Populate R55, R59 or R60 properly to match the input signal termination requirement.

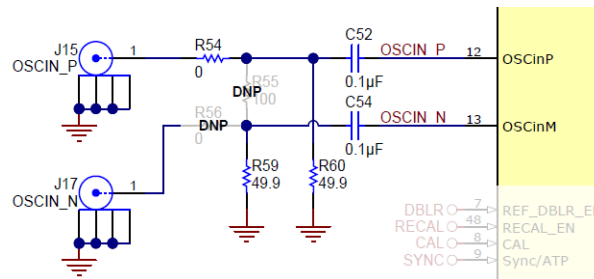


Figure 2-3. Reference Clock

2.5 Output Connections

Connect either RFOA_P or RFOA_N 2.92mm connector to a signal analyzer. The unused connector must be terminated with a 50Ω resistor or a SMA load. Default TICS Pro evaluation software configuration has RFOA output 6GHz signal and RFOB powered down. RFOB 2.92mm connectors can be left open.

2.6 Test Points

Table 2-1. SPI Test Points

| Test point | Designator | Property |
|------------|------------|--|
| TP9 | SDO | Serial data output (Register read back) |
| TP6 | CSB | SPI chip select input |
| TP7 | SCK | SPI clock input |
| TP8 | SDI | SPI data input |

Table 2-2. MUXOUT Test Point

| Test point | Designator | Property |
|------------|------------|---|
| TP5 | MUXOUT | Serial data output, phase detector clock or state machine clock output |

Table 2-3. Power Supply Test Point

| Test point | Designator | Property |
|------------|------------|---|
| TP4 | VCCIN | 3.3V (LDO bypassed) 3.6V to 4V (use onboard LDO) |
| TP2 | VBIAS | 5V (use onboard LDO) |
| TP1 | VCC | 3.3V |
| TP3 | GND | 0V |

3 Software

3.1 Software Description

Texas Instruments Clocks and Synthesizers (TICS) Pro software is used to program this evaluation module (EVM) through the on-board USB2ANY interface.

3.2 Software Installation

Download and install TICS Pro software from www.ti.com/tool/ticspro-sw.

3.3 USB2ANY Interface

The on-board USB2ANY interface provides a bridge between TICS Pro software and the LMX2624-SP device. When the on-board USB2ANY controller is first connected to a PC, or if the firmware revision for the controller does not match with the version used by TICS Pro, a firmware update to the controller is required.

1. Connect the USB cable from the PC to the EVM. The USB interface provides the necessary power to enable the on-board USB2ANY controller.
2. After Windows has set up a USB device, run TICS Pro in the PC.
3. The next screen looks like the image below.

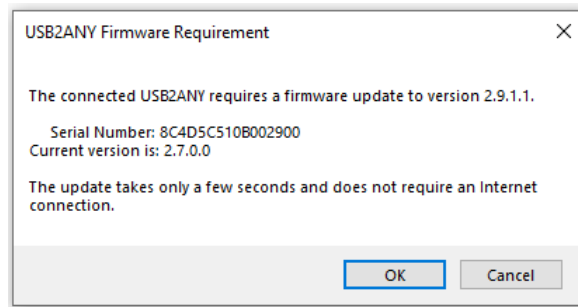


Figure 3-1. Firmware Update Request

4. Click *OK*, then the screen looks like the image below. Click *Update Firmware*.

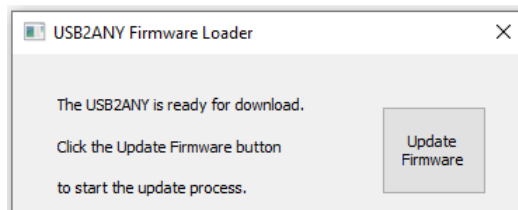


Figure 3-2. Firmware Loader

5. Then the screen below appears.

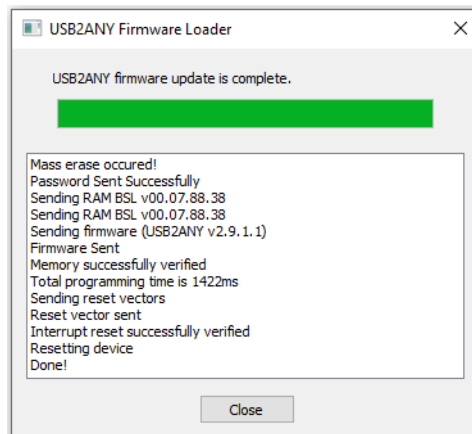


Figure 3-3. Firmware Update Complete

6. Click the *Close* button to close the window.

7. A TICS Pro default device pops up. Check to make sure that we get a green light on Connection Mode at the bottom of the GUI.

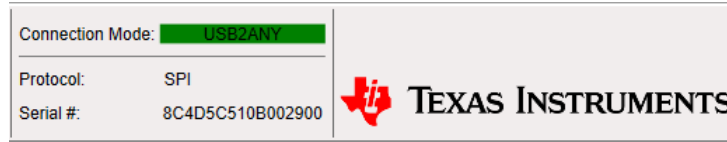


Figure 3-4. Connection Mode

8. Go to the menu bar, click *USB Communications*, then select *Interface*.

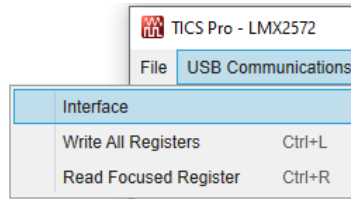


Figure 3-5. USB Communications

9. Click the *Identify* button, the LED in the USB2ANY interface flashes.

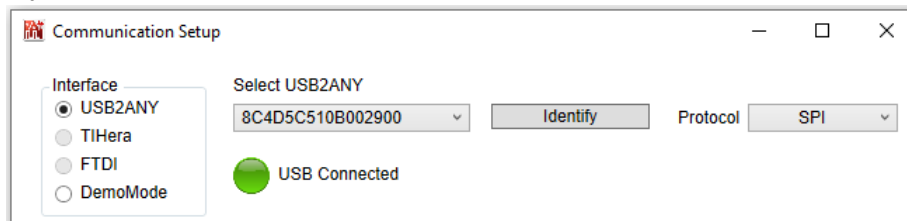


Figure 3-6. Identify USB2ANY Controller

10. Now, the USB2ANY is ready to use. Click the *Close* button to close the window.

4 Implementation Results

4.1 Evaluation Setup

Default EVM configuration is operated in SPI mode with LDO bypassed. Setup the connection as shown in Figure 2-1. Run TICS Pro evaluation software and follow these steps to start the program.

1. Go to **Select Device** → **PLL + VCO** → **LMX2624-SP**.

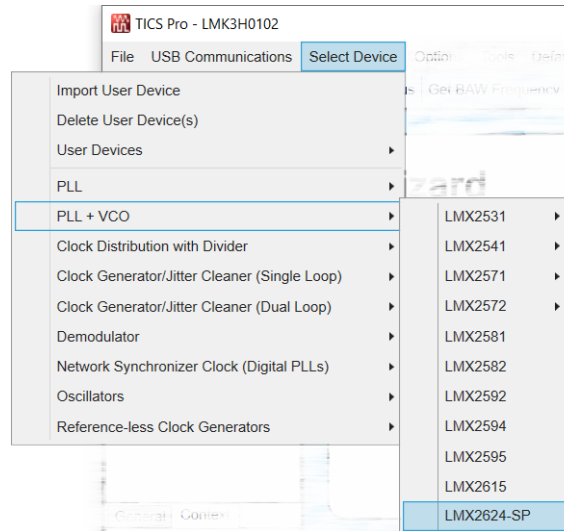


Figure 4-1. Select Device in TICS Pro

2. The "ReadMe" page loads. Please take a minute to read the content to have an overview of the GUI.
3. Go to **Default Configuration** → **EVM Default Mode**.

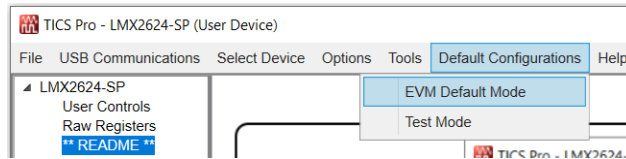


Figure 4-2. Default Mode

4. Go to **USB Communications** → **Write All Registers** to write all the registers to LMX2624-SP.

4.2 Performance Data and Results

4.2.1 RF Output

With EVM Default Mode configuration, VCO frequency is 12GHz, RFoutA output is 6GHz.

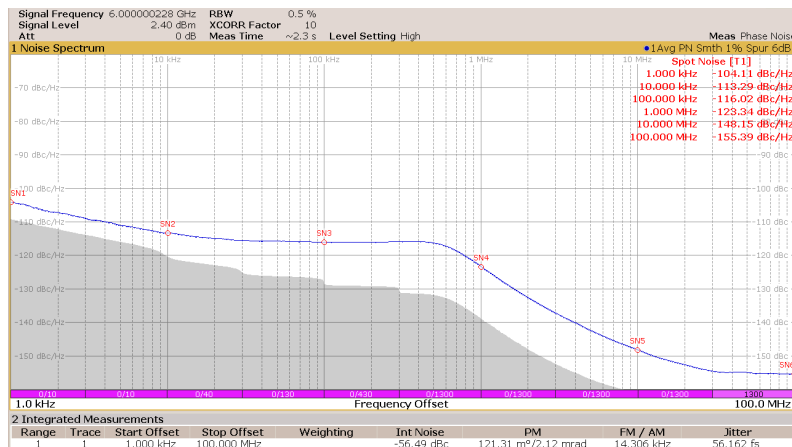


Figure 4-3. Divided Down Output

Click on **Output MUX** and select VCO, RFoutA output becomes 12GHz.



Figure 4-4. Output MUX Options

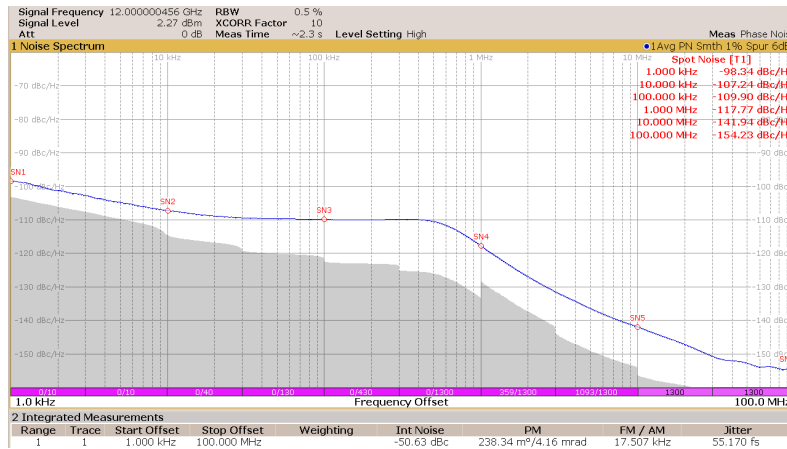


Figure 4-5. Direct VCO Output

To get VCO doubler output, click on **Output MUX** and select **Doubler**. A VCO doubler calibration is required to configure the internal tracking filter so that the 2x signal passes through while the sub-harmonics are suppressed. To complete the doubler calibration, set **FCAL_DBLR_EN** = 1 and click the **Calibrate VCO** button once (this programs R0).

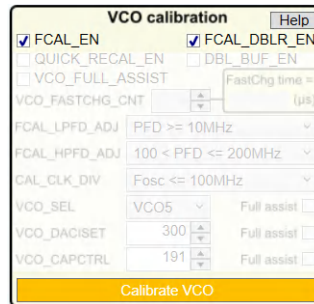


Figure 4-6. VCO Doubler Calibration

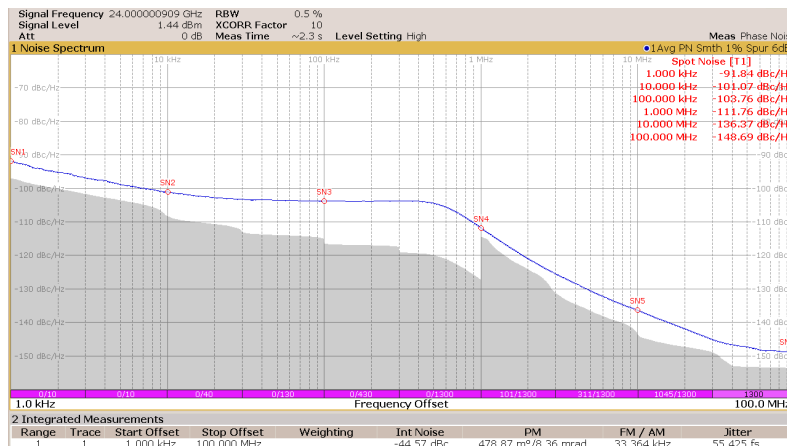


Figure 4-7. VCO Doubler Output

Sub-harmonic suppression is about -52dBc at 24GHz output and -42dBc at 15.24GHz output.

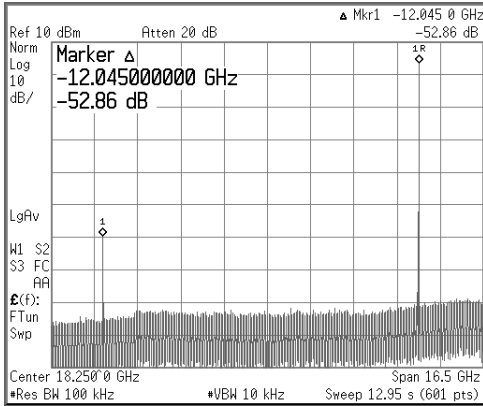


Figure 4-8. 24GHz Output

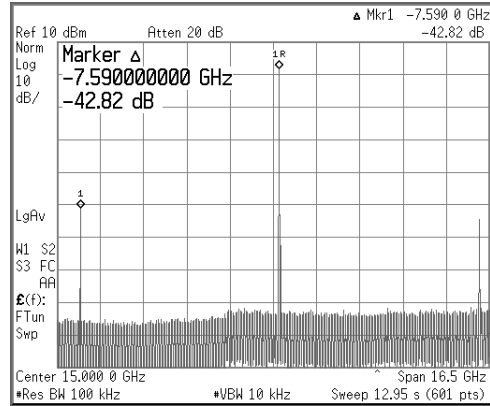


Figure 4-9. 15.24GHz Output

If RFOUTA or RFOUTB is not used, output driver can be shut down by setting **OUTx_PD** = 1. Unused output pins can be left floating or AC-shunt to ground. Output can also be muted without shutting down the driver. Output mute is controlled by the **MUTEA** and **MUTEB** pin or configurable via SPI programming.

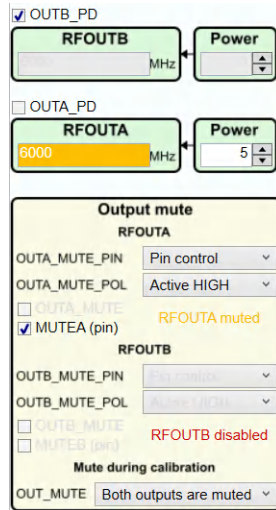


Figure 4-10. Output Mute Control

The response time of mute control using the hardware pin is very fast, typical value is 10ns.

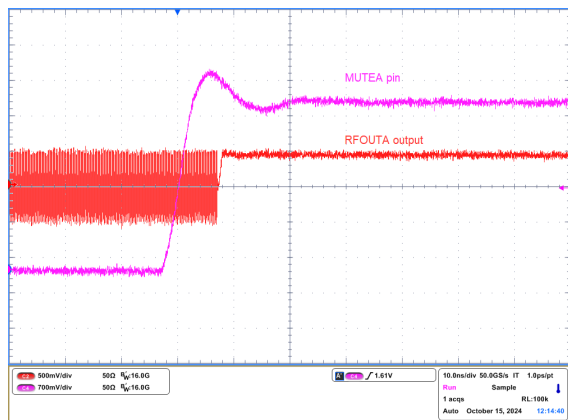


Figure 4-11. Pin Control Mute Response Time

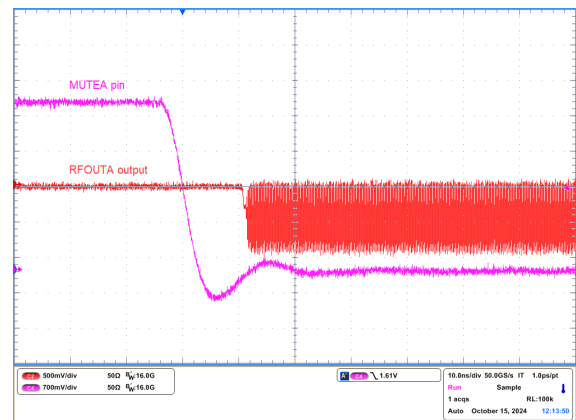


Figure 4-12. Pin Control Unmute Response Time

4.2.2 VCO Calibration

Whenever the VCO frequency is change, a VCO calibration is required to select the right VCO core and band for the PLL to lock. In LMX2624-SP, there are 7 VCO cores and each core has 192 bands. Selection of the VCO core and band is done automatically whenever register R0 is programmed with **FCAL_EN** = 1. This is called No Assist operation. TICS Pro EVM default mode is setup for No Assist operation. If there is no requirement to the VCO switching time, using No Assist operation is recommended. However, if your application requires very fast VCO switching, the LMX2624-SP can be placed in Full Assist operation mode. In this case, VCO calibration is bypassed. See application note [SNA336](#) for VCO calibration details.

4.2.2.1 No Assist Operation

With No Assist operation, the time taken to switch VCO frequency is equal to the sum of (1) register programming time, (2) VCO calibration time and (3) PLL lock time. VCO calibration time depends on whether the frequency change is upward or downward as well as register **VCO_SEL**, **VCO_DACISSET** and **VCO_CAPCTRL** setting. PLL lock time depends on the loop filter bandwidth. In general, wider loop bandwidth returns shorter lock time. For example, using default EVM configuration to switch VCO frequency between 7642MHz (VCO1) and 15.24GHz (VCO7) with No Assist operation, the lock time (excluding register programming time) is approximately 300 μ s to 500 μ s. (Output is divide by 4 due to limitation of test equipment)

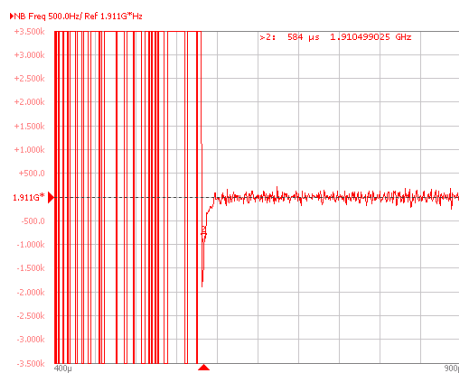


Figure 4-13. No Assist Jump Down

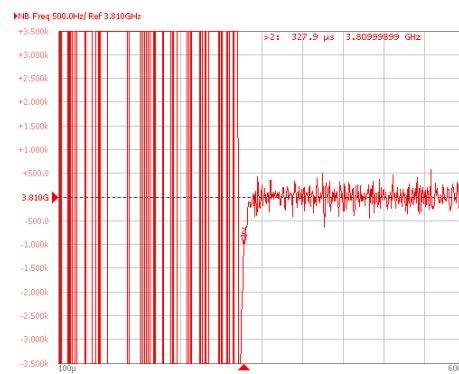


Figure 4-14. No Assist Jump Up

Programming information:

1. Set **DBL_BUF_EN** = 1 to enable register double buffering. Writing to the double-buffered registers do not change the configuration of the PLL until register R0 is programmed.
2. Set **Channel divider** = 4.
3. Program **PFD_DLY**, **PLL_N**, **PLL_NUM** for VCO = 7642MHz.
4. Click **Calibrate VCO** button once to initiate VCO calibration. (Use the CSB pin to trigger test equipment)
5. Repeat step 3 for VCO = 15240MHz.
6. Click **Calibrate VCO** button once to initiate VCO calibration. (Use the CSB pin to trigger test equipment)

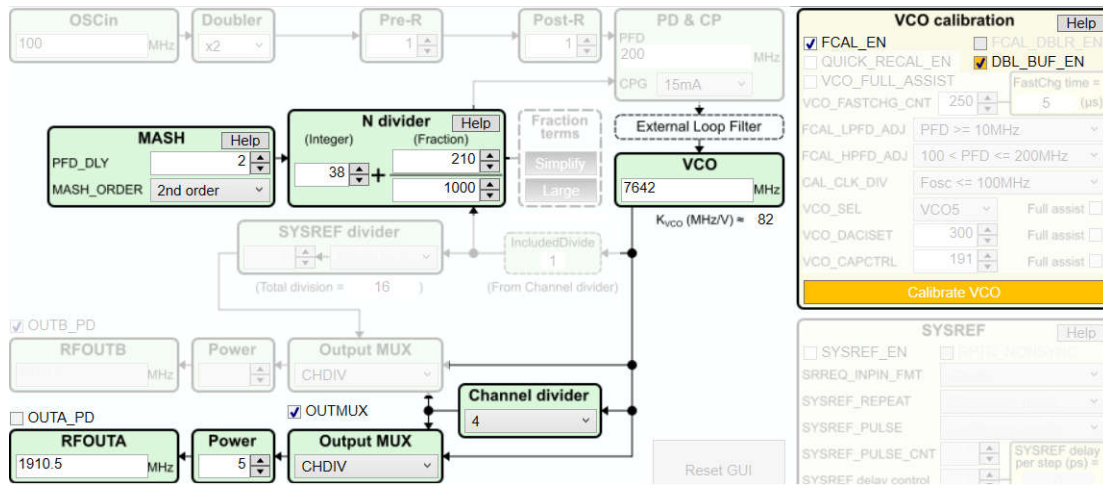


Figure 4-15. No Assist VCO Switching Configuration

4.2.2.2 Full Assist Operation

Every time the VCO frequency is changed, instead of performing a VCO calibration, Full Assist operation specifies the VCO core and band for the PLL to lock. As a result, there is no VCO calibration time involved. The total time taken to switch VCO frequency is equal to register programming time plus PLL lock time.

To be able to know which VCO core and band to use for a specific VCO frequency, a one-time VCO calibration needs to be performed, a register read back needs to be performed to collect this information, and the information needs to be stored in a look up table (LUT). In addition to the VCO parameters, if VCO doubler is used, VCO doubler parameters can be obtained in the similar fashion. For example, again switching the VCO frequency between 7642MHz and 15.24GHz. RFOUTA is divide by 4 output. With Full Assist operation, the lock time (excluding register programming time) is less than 20µs.

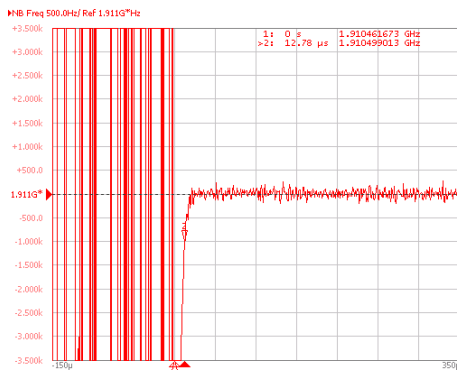


Figure 4-16. Full Assist Jump Down

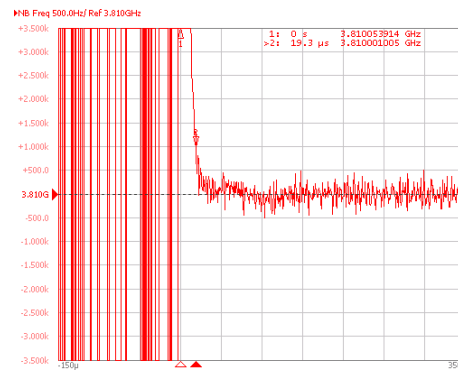


Figure 4-17. Full Assist Jump Up

Programming information:

A. LUT creation

1. Set **MUXOUT** = Register read back.
2. Set **READBACK** = Read state machine value.
3. Program the LMX2624-SP to lock to 7642MHz with No Assist operation.
4. Click the **Register read back** button once to read back the register values as shown in the **Full assist read back** column. Record these values in a text file.
5. Repeat step 3 to 4 for 15.24GHz.

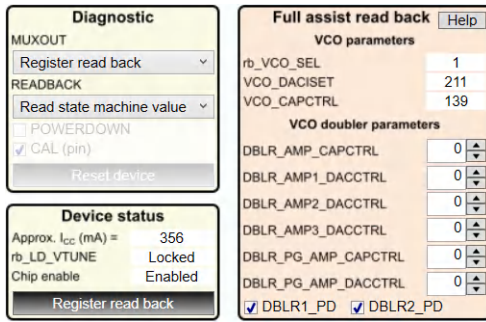


Figure 4-18. LUT Creation

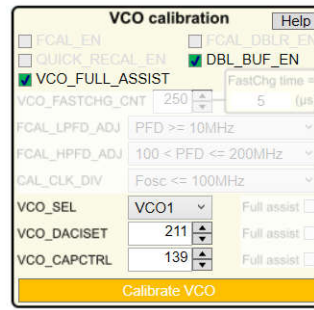


Figure 4-19. Full Assist Programming

B. Apply LUT data

1. Set **VCO_FULL_ASSIST** = 1.
2. Set **DBL_BUF_EN** = 1.
3. Program **PFD_DLY**, **PLL_N**, **PLL_NUM** for VCO = 7642MHz.
4. Program **VCO_SEL**, **VCO_DACISSET** and **VCO_CAPCTRL** with the values from LUT.
5. Click **Calibrate VCO** button once to kick start VCO switching. (Use the CSB pin to trigger test equipment)
6. Repeat step 3 to 4 for VCO = 15240MHz.
7. Click **Calibrate VCO** button once to kick start VCO switching. (Use the CSB pin to trigger test equipment)

4.2.3 SYSREF

LMX2624-SP supports generation of SYSREF continuous clock and a train of pulses. SYSREF clocks are output from RFOUTB. The phase between SYSREF clock and RF clock (from RFOUTA) is adjustable. LMX2624-SP also support SYSREF repeater mode. Incoming SYSREF clocks can pass through to RFOUTB asynchronously or being re-clocked so as to phase align with RF clock.

4.2.3.1 SYSREF Clock Generation

To enable SYSREF function, set **SYSREF_EN** = 1. SYSREF operation requires some of the phase synchronization building blocks, so **VCO_PHASE_SYNC** must also be set to =1. When this bit is set, phase detector frequency must be equal to or less than 50MHz. Set **Output MUX** to **SYSREF** so that RFOUTB output is SYSREF clock. To generate continuous SYSREF clock, set **SYSREF_REPEAT** = *Generation mode*; set **SYSREF_PULSE** = *Continuous mode*. Clocks are coming out from RFOUTB in 20ns after the SysRefReq pin is pulled HIGH. This can be done by checking the **SRREQ (pin)** box. Use **SYSREF divider** to adjust the output SYSREF clock frequency.

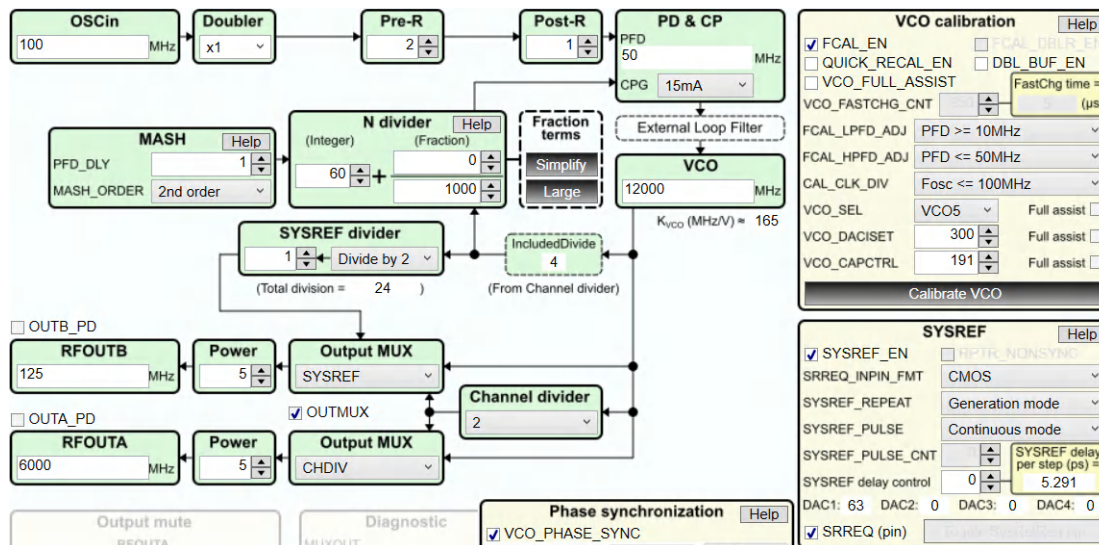


Figure 4-20. SYSREF Continuous Clock Generation

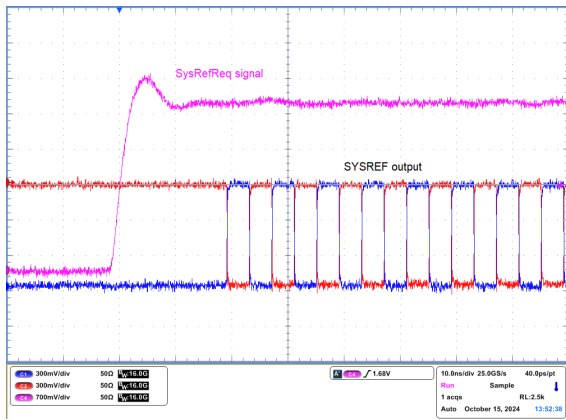


Figure 4-21. Continuous SYSREF Clock Generation

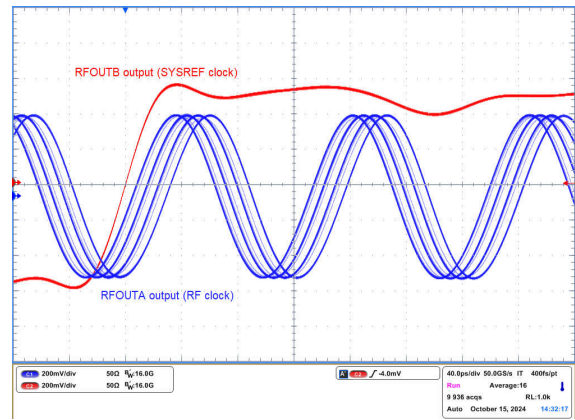


Figure 4-22. SYSREF Delay

The phase between SYSREF clock (RFOUTB) and RF clock (RFOUTA) is adjustable using registers JESD_DACx.

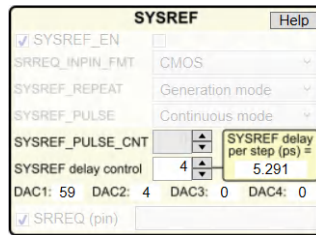


Figure 4-23. SYSREF Delay Control

If DC-couple of the SYSREF clock is desired, care must be taken on the output common mode voltage, which is not a constant but varied with the output voltage swing setting. Set **Power** to a different value changes both the SYSREF clock output voltage swing as well as the common mode voltage.

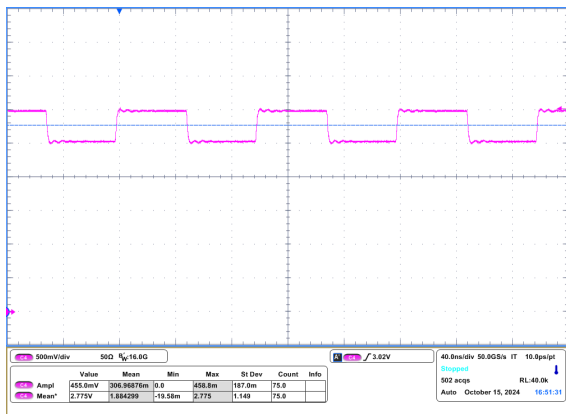


Figure 4-24. SYSREF Output With Power = 2

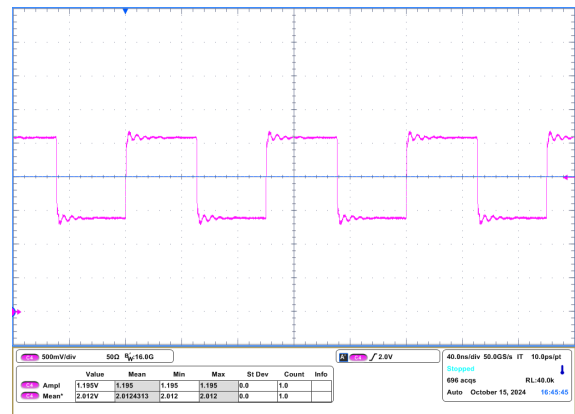


Figure 4-25. SYSREF Output With Power = 7

4.2.3.2 SYSREF Pulse Generation

To generate SYSREF pulses, change **SYSREF_PULSE** to *Pulsed mode* and set the desired number of pulse with the **SYSREF_PULSE_CNT** register field. SYSREF delay control is supported in pulse generation mode. Use the JESD_DACx registers to change the delay.

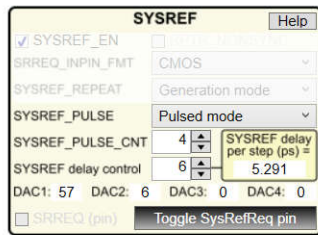


Figure 4-26. SYSREF Pulsed Mode Configuration

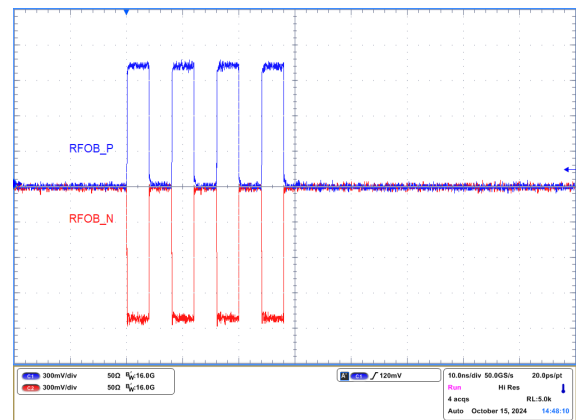


Figure 4-27. SYSREF Pulses Generation

4.2.3.3 SYSREF Repeater Mode

There are two type of SYSREF repeater mode operations, synchronous and asynchronous repeater mode. With synchronous repeater mode, incoming SYSREF clock is re-clocking to align with the VCO, SYSREF delay control is supported. With asynchronous repeater mode, incoming SYSREF clock passes through the device and output at RFOUTB. SYSREF delay control does not apply in this mode. To put LMX2624-SP in this mode, set **RPTR_NONSYNC** = 1.

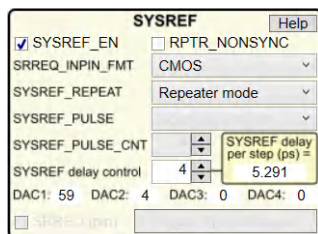


Figure 4-28. Synchronous Mode Configuration

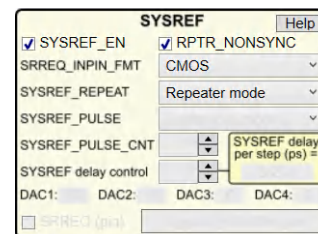


Figure 4-29. Asynchronous Mode Configuration

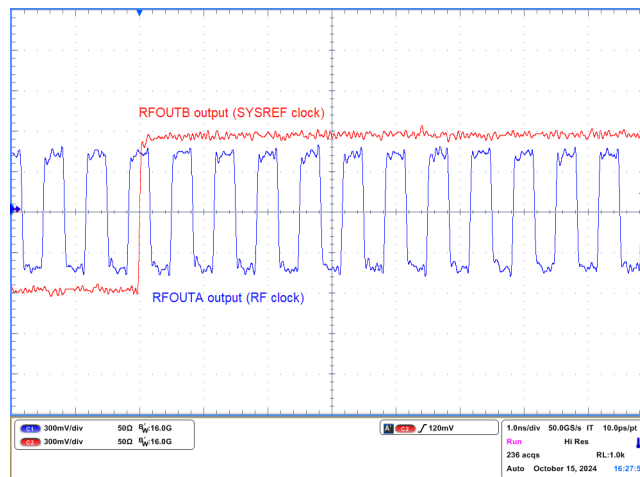


Figure 4-30. SYSREF Synchronous Repeater Mode

4.2.4 Phase Adjustment

The **MASH_SEED** word can use the sigma-delta modulator of the PLL to shift output signal phase with respect to the input reference clock. To enable phase adjustment, set **MASH_SEED_EN** = 1 and then program a value to **MASH_SEED**. Alternatively, a desired phase shift value can be used with TICS Pro calculating the

MASH_SEED value. There are some restrictions in using phase adjustment, click the **Help** button to see the details.

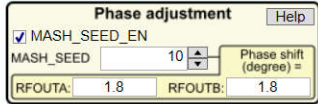


Figure 4-31. Phase Adjustment Configuration

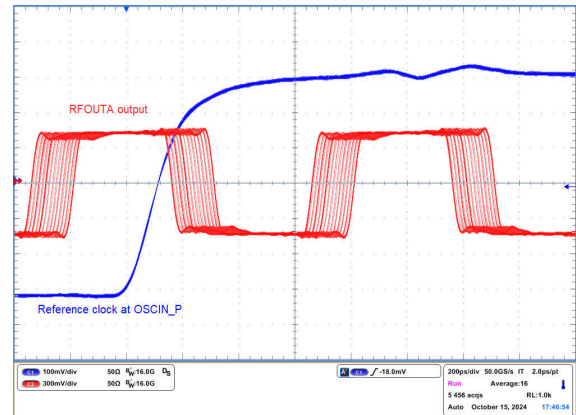


Figure 4-32. Phase Adjustment

In the example above, if **MASH_SEED** = 10 is programmed one hundred times, the result is a 180 degrees flip.

4.2.5 Phase Synchronization

Phase synchronization is useful if there are multiple LMX2624-SP devices in a system and having all the RF clocks aligned in phase is desirable. There are four different categories of synchronization.

- Category 4: Synchronization is not possible.
- Category 3: Synchronization is possible with a time-critical SYNC pulse and the devices are in SYNC mode.
- Category 2: Synchronization is possible with a non time-critical SYNC pulse and the devices are in SYNC mode.
- Category 1b: Requires the devices are in SYNC mode.
- Category 1a: Nothing is required to setup, the devices phase align by nature.

4.2.5.1 Category 1b and Category 2 SYNC

Category 1b and Category 2 SYNC requires putting LMX2624-SP in SYNC mode. That means, **VCO_PHASE_SYNC** = 1. Please note, in SYNC mode, the maximum f_{PD} is 50MHz.

For Category 1b SYNC, enabling SYNC mode is sufficient. After programming the devices, the output phases are all be aligned.

For Category 2 SYNC, in addition to putting the devices in SYNC mode, a non-time-critical SYNC pulse is required to trigger all devices to synchronize. The SYNC pulse can be given by an external source or by toggling the SYNC pin LOW-HIGH-LOW. Click the **Toggle Sync pin** button toggles the SYNC pin L-H-L once.

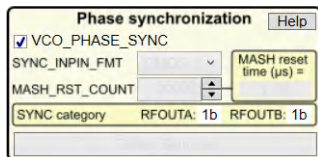


Figure 4-33. Category 1b SYNC

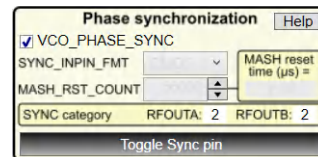


Figure 4-34. Category 2 SYNC

4.2.5.2 Category 3 SYNC

The SYNC pulse being used for Category 3 synchronization requires a certain setup and hold time with respect to the input reference clock. This requirement is to verify that all the devices use the same input clock edge to start synchronization. **MASH_RST_COUNT** must be set to provide sufficient time for the synchronization to complete.

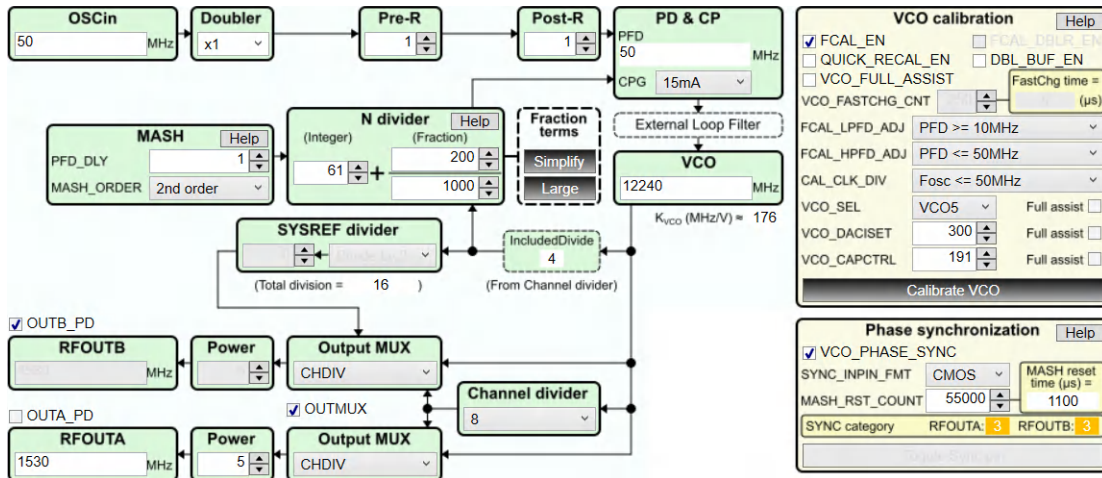


Figure 4-35. Category 3 SYNC Configuration

If a non time-critical SYNC pulse is used for Category 3 SYNC, or after a VCO calibration, the phase between devices is not identical.

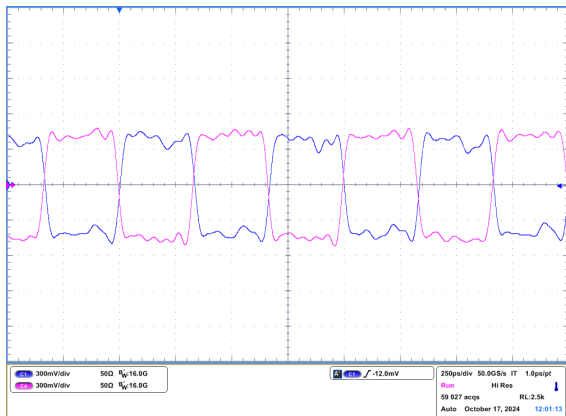


Figure 4-36. Not Synchronous Example 1

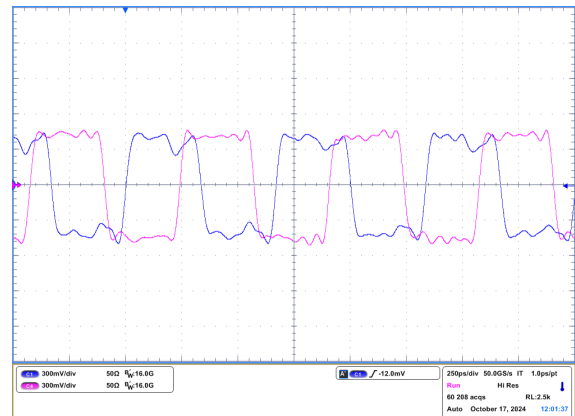


Figure 4-37. Not Synchronous Example 2

With a time-critical SYNC pulse, the output phase is aligned. Please note that the output phase of each device can not be exactly the same, but the difference remain unchanged after synchronization.

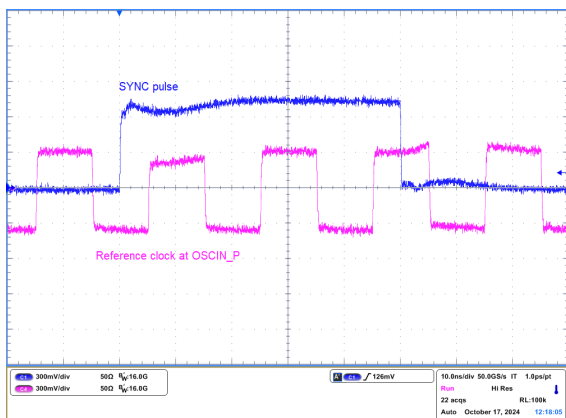


Figure 4-38. Time Critical SYNC Pulse

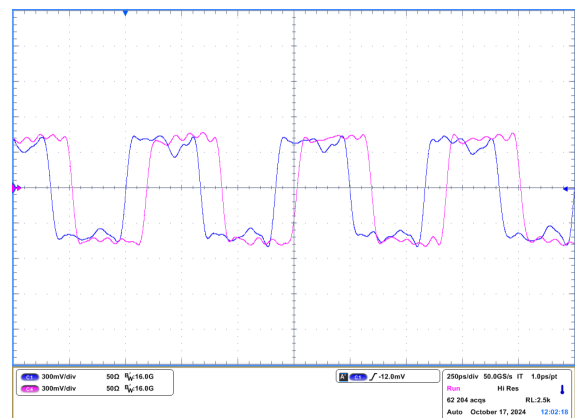


Figure 4-39. Category 3 SYNC

4.2.6 Pin Mode

LMX2624-SP supports pin configuration operation without the need of register programming. The setup for pin mode operation is same as the diagram shown in Figure 2-1, except that the connection to a PC is not necessary. In the EVM, the configuration of LMX2624-SP is determined by the rotary DIP switches and the 2-pin headers.

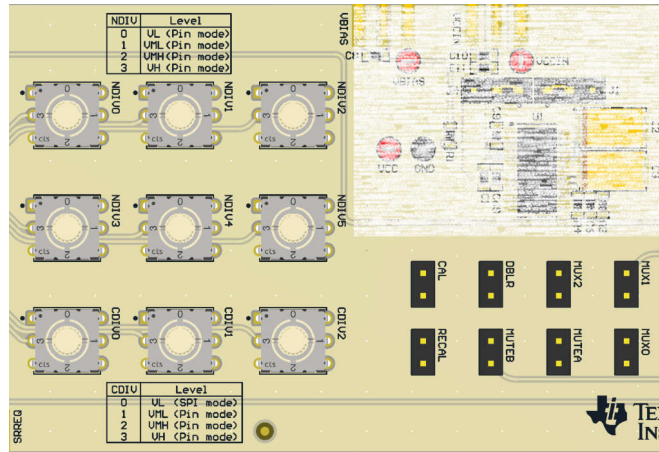


Figure 4-40. Pin Control Elements

N-divider value is configured by the NDIVx rotary DIP switches, the CDIVx rotary DIP switches are used to set the channel divider value. NDIVx and CDIVx pins are 4-level input pins. The position of the rotary DIP switch (0, 1, 2, or 3) sets the pin to one of the levels: VL (0V); VML; VMH and VH (3.3V).

Table 4-1. CDIVx Channel Divider Truth Table

| CDIV2 | CDIV1 | CDIV0 | Divider Value |
|-------|-------|-------|---------------|
| 0 | 0 | 0 | SPI mode |
| 0 | 1 | 0 | 2 |
| 0 | 2 | 0 | 4 |
| 0 | 2 | 3 | 6 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 3 | 12 |
| 1 | 1 | 0 | 16 |
| 1 | 1 | 3 | 24 |
| 1 | 2 | 0 | 32 |
| 1 | 2 | 3 | 48 |
| 1 | 3 | 0 | 64 |
| 1 | 3 | 3 | 96 |
| 2 | 0 | 0 | 128 |
| 2 | 0 | 3 | 192 |
| 2 | 1 | 0 | 256 |
| 2 | 1 | 3 | 384 |
| 2 | 2 | 0 | 512 |
| 2 | 2 | 3 | 768 |
| 2 | 3 | 0 | 1024 |
| 2 | 3 | 3 | 1536 |

Table 4-2. NDIVx N-Divider Truth Table

| Decimal | NDIV5 | NDIV4 | NDIV3 | NDIV2 | NDIV1 | NDIV0 |
|---------|-------|-------|-------|-------|-------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 0 | 0 | 0 | 2 |
| 3 | 0 | 0 | 0 | 0 | 0 | 3 |
| 4 | 0 | 0 | 0 | 0 | 1 | 0 |
| 5 | 0 | 0 | 0 | 0 | 1 | 1 |
| 6 | 0 | 0 | 0 | 0 | 1 | 2 |
| 7 | 0 | 0 | 0 | 0 | 1 | 3 |
| 8 | 0 | 0 | 0 | 0 | 2 | 0 |
| ... | ... | ... | | | | ... |
| 59 | 0 | 0 | 0 | 3 | 2 | 3 |
| 60 | 0 | 0 | 0 | 3 | 3 | 0 |
| 61 | 0 | 0 | 0 | 3 | 3 | 1 |
| 62 | 0 | 0 | 0 | 3 | 3 | 2 |
| ... | ... | ... | | | | ... |
| 4092 | 3 | 3 | 3 | 3 | 3 | 0 |
| 4093 | 3 | 3 | 3 | 3 | 3 | 1 |
| 4094 | 3 | 3 | 3 | 3 | 3 | 2 |
| 4095 | 3 | 3 | 3 | 3 | 3 | 3 |

2-pin headers MUX0, MUX1 and MUX2 determine RFOUTA and RFOUTB output.

Table 4-3. Output MUX Setting

| MUX2 | MUX1 | MUX0 | RFOUTA | RFOUTB |
|------|------|------|-----------------|-----------------|
| 0 | 0 | 0 | Channel divider | Channel divider |
| 0 | 0 | 1 | Channel divider | VCO |
| 0 | 1 | 0 | VCO | Channel divider |
| 0 | 1 | 1 | VCO | VCO |
| 1 | 0 | 0 | Doubler | Channel divider |
| 1 | 0 | 1 | VCO | Doubler |
| 1 | 1 | 0 | Doubler | VCO |
| 1 | 1 | 1 | Doubler | Doubler |

The definition of the others 2-pin headers are as follows:

Table 4-4. 2-pin Headers Definition

| Designator | Function |
|--------------|---|
| MUTEA, MUTEB | Output mute control. |
| RECAL | If RECAL is HIGH, when the device loses lock, the device automatically re-calibrates to re-gain lock. EVM default has this pin tied HIGH. |
| DBLR | Enables OSCin doubler. |
| CAL | Tie HIGH to enable the device. A Low-to-High transition triggers VCO calibration. |

As an example, to configure LMX2624-SP for the following configuration in pin mode:

- $f_{OSC} = 100\text{MHz}$; $f_{PD} = 200\text{MHz}$; $f_{VCO} = 12\text{GHz}$
- $RFOUTA = 24\text{GHz}$ output; $RFOUTB = 3\text{GHz}$

Hardware configuration is:

- N-divider = $12\text{G} / 200\text{M} = 60 \rightarrow \text{NDIV}[5:0] = (000330)_4$
- $RFOUTA = 24\text{GHz}$ and $RFOUTB = 3\text{GHz} \rightarrow \text{MUX}[2:0] = (100)_2$
- Channel divider = $12\text{G} / 3\text{G} = 4 \rightarrow \text{CDIV}[2:0] = (020)_4$
- $f_{PD} = 200\text{MHz} \rightarrow \text{DBLR} = \text{HIGH}$

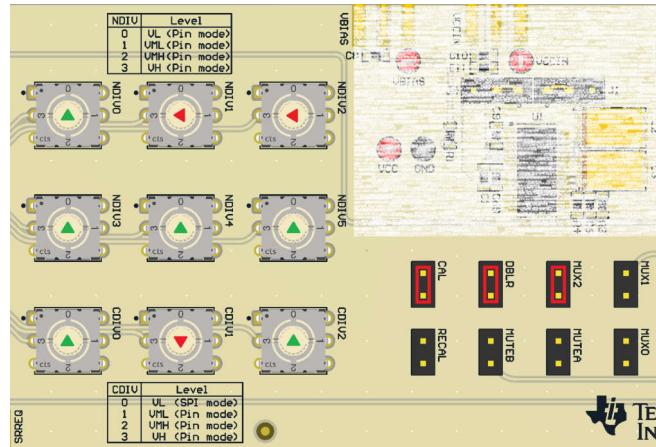


Figure 4-41. Pin Mode Hardware Configuration

5 Hardware Design Files

5.1 Schematics

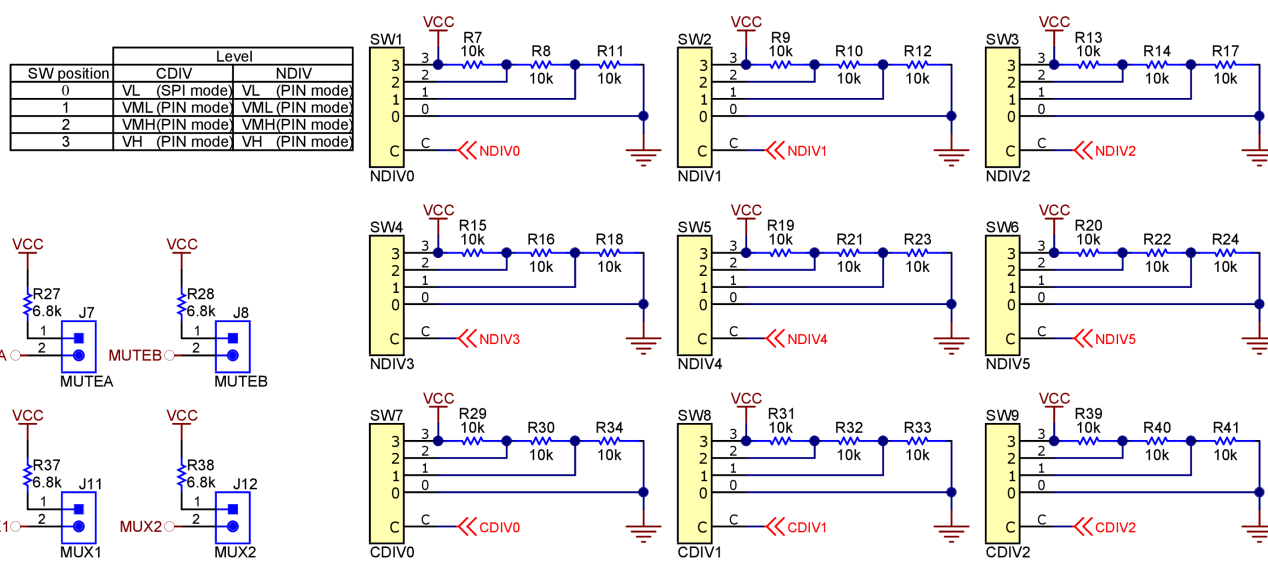
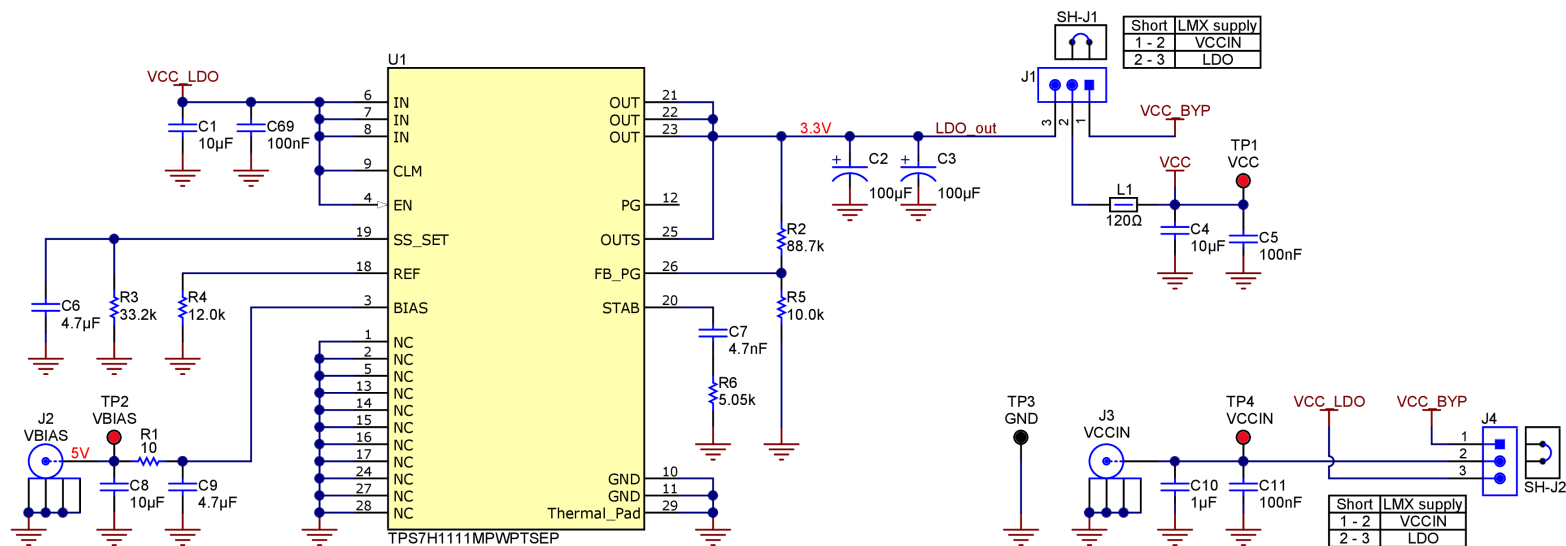


Figure 5-1. Power and Control

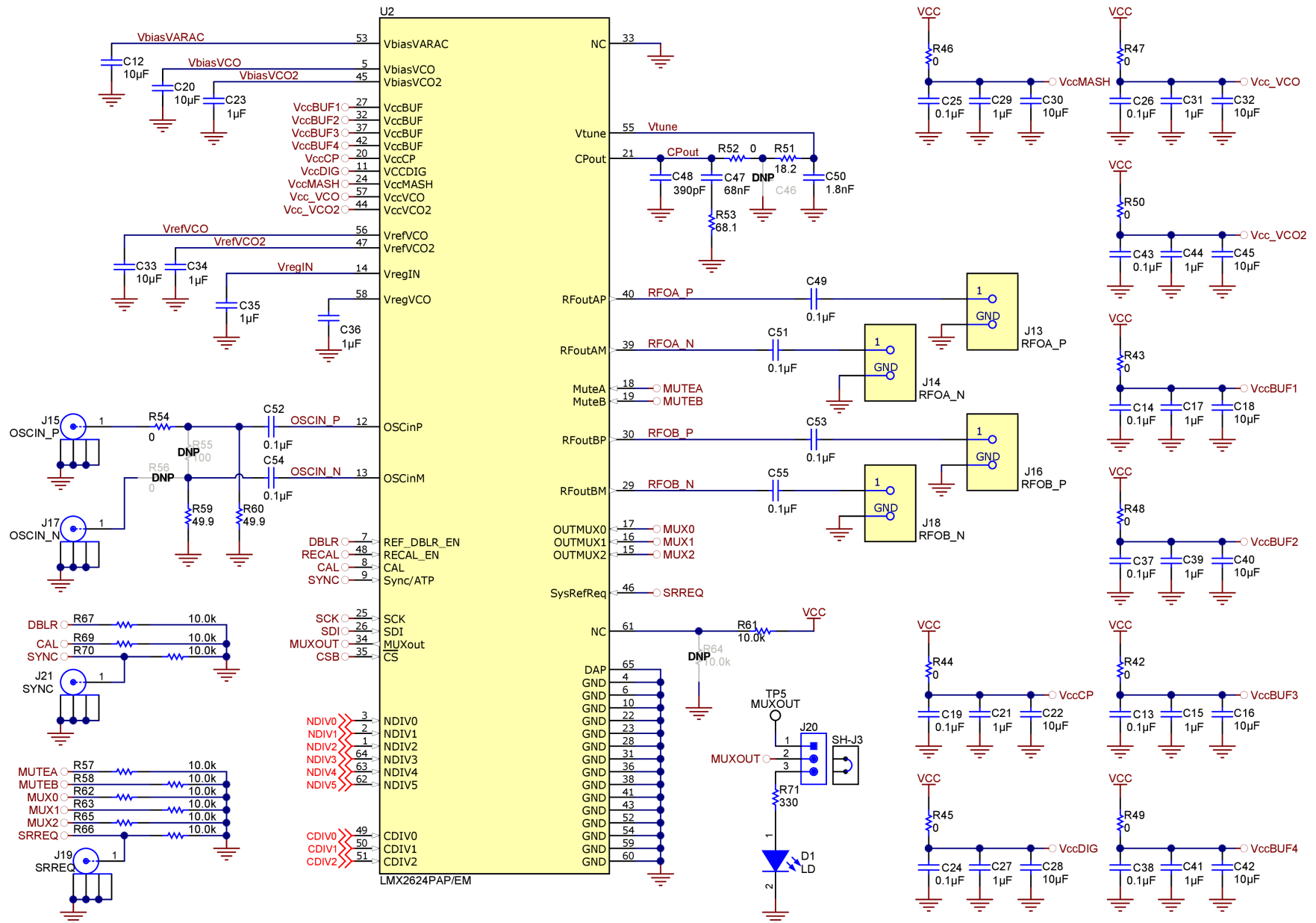


Figure 5-2. LM2624-SP

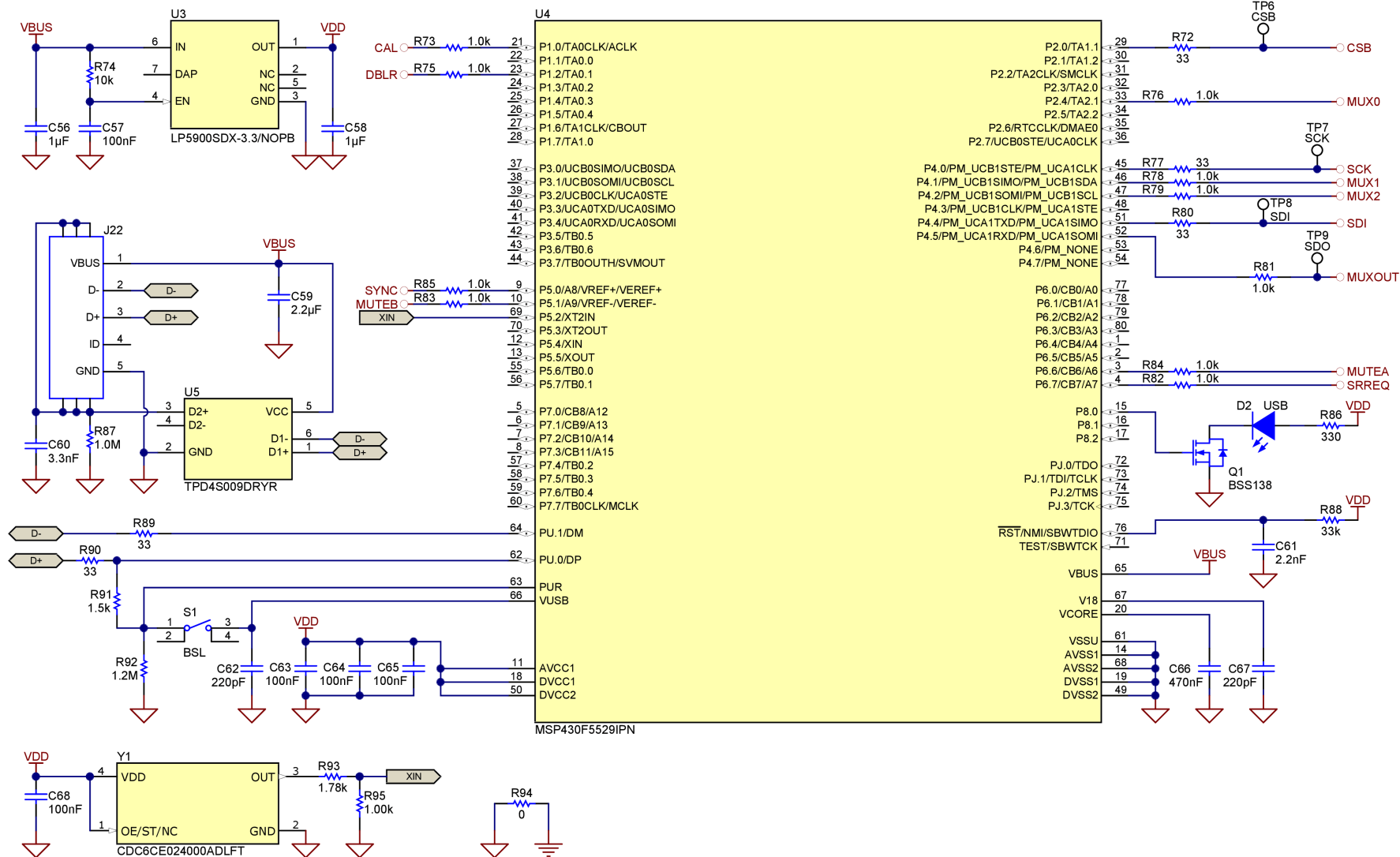


Figure 5-3. USB2ANY

5.2 PCB Layouts

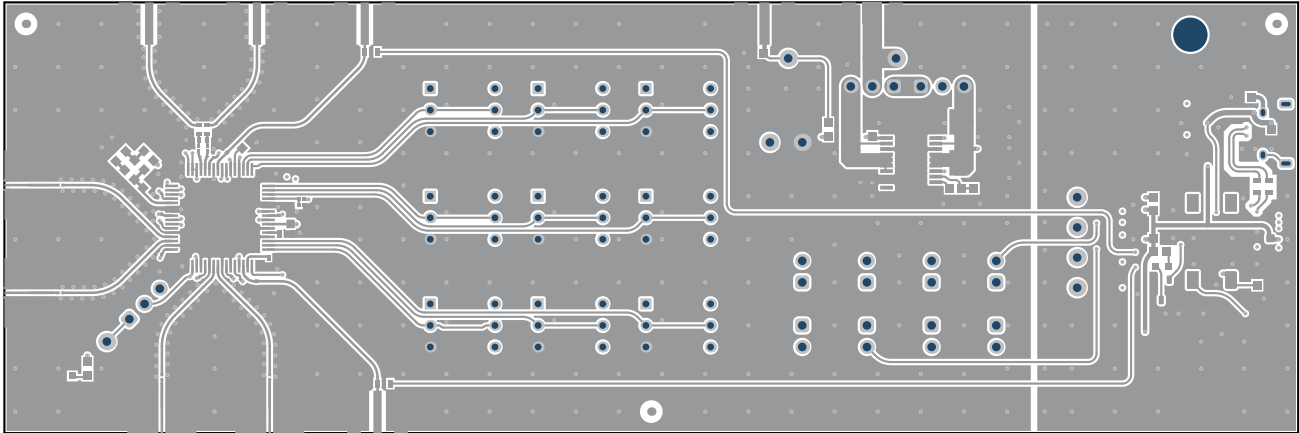


Figure 5-4. Top Layer

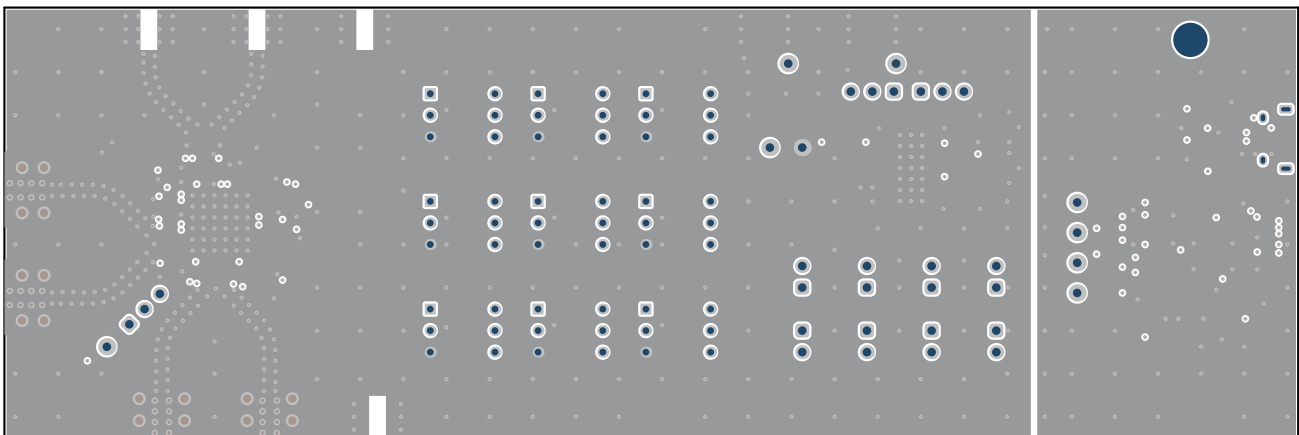


Figure 5-5. 2nd Layer

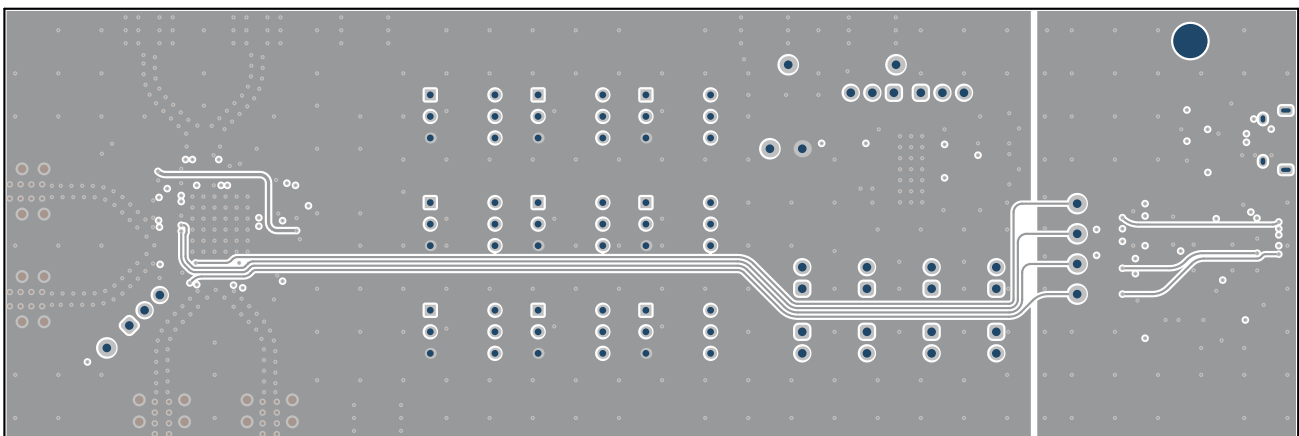


Figure 5-6. 3rd Layer

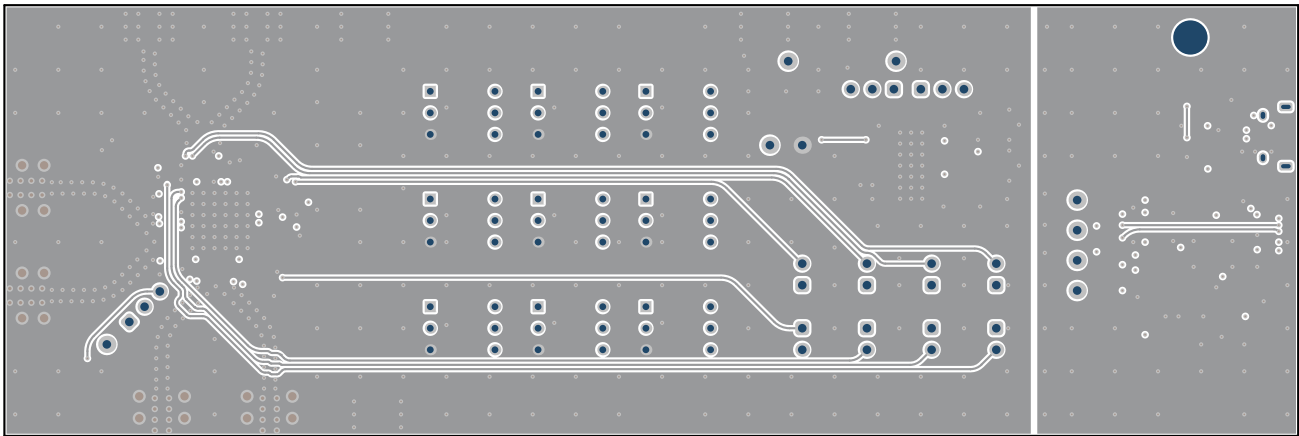


Figure 5-7. 4th Layer

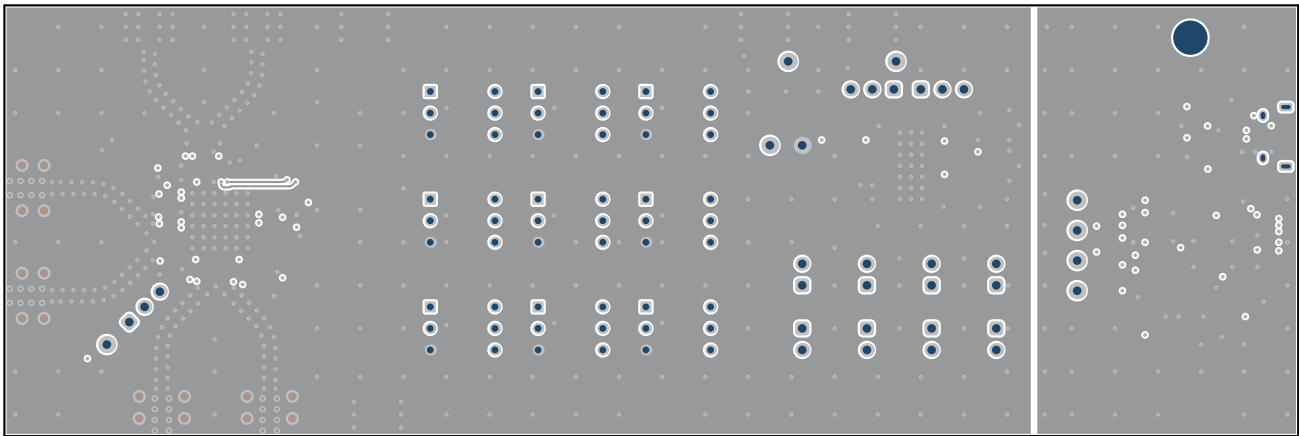


Figure 5-8. 5th Layer

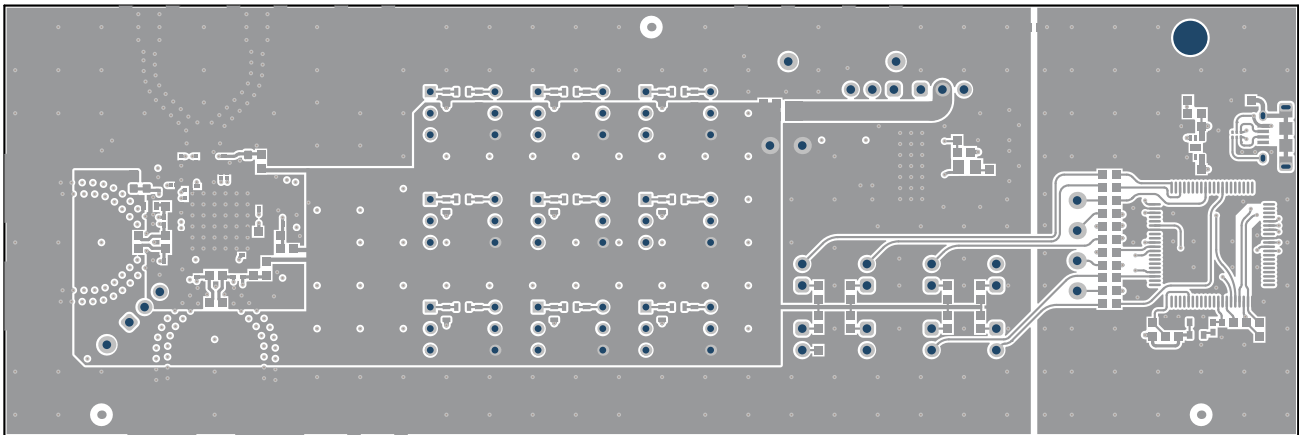


Figure 5-9. Bottom Layer

Table 5-1. PCB Stackup

| Layer | Material | Thickness (mil) | Constant |
|------------|----------|-----------------|----------|
| Top | Copper | 2.8 | |
| Dielectric | RO4350 | 6.6 | 3.48 |
| 2nd | Copper | 1.4 | |
| Dielectric | FR4 | 14 | 4.2 |
| 3rd | Copper | 1.4 | |
| Dielectric | FR4 | 9 | 4.2 |
| 4th | Copper | 1.4 | |
| Dielectric | FR4 | 14 | 4.2 |
| 5th | Copper | 1.4 | |
| Dielectric | FR4 | 6.6 | 4.2 |
| Bottom | Copper | 2.8 | |

5.3 Bill of Materials (BOM)

| Designator | Description | PartNumber | Manufacturer |
|--|---|--------------------|-------------------|
| C1, C4, C8, C12, C16, C18, C20, C22, C28, C30, C32, C33, C40, C42, C45 | CAP, CERM, 10 μ F, 10V, 10%, X5R, 0603 | GRM188R61A106KAALD | MuRata |
| C2, C3 | Cap Tant Solid 100 μ F 20V E CASE 10% | TPME107K020R0035 | KYOCERA AVX |
| C5, C11, C57, C63, C64, C65, C68, C69 | CAP, CERM, 0.1 μ F, 16V, 10%, X7R, 0603 | 885012206046 | Wurth Elektronik |
| C6, C9 | CAP, CERM, 4.7 μ F, 16V, 10%, X7R, 0603 | GRM188Z71C475KE21D | MuRata |
| C7 | CAP, CERM, 4.7nF, 50V, 5%, C0G, 0805 | GRM2165C1H472JA01D | MuRata |
| C10, C56, C58 | CAP, CERM, 1 μ F, 16V, 10%, X7R, 0603 | 885012206052 | Wurth Elektronik |
| C13, C14, C19, C24, C25, C26, C37, C38, C43, C49, C51, C52, C53, C54, C55 | CAP, CERM, 0.1 μ F, 10V, 10%, X5R, 0201 | ATC530Z104KT10T | AT Ceramics |
| C15, C17, C21, C23, C27, C29, C31, C34, C35, C36, C39, C41, C44 | CAP, CERM, 1 μ F, 25V, 10%, X5R, 0402 | GRM155R61E105KA12D | MuRata |
| C47 | CAP, CERM, 68nF, 25V, 10%, X7R, 0603 | 885012206070 | Wurth Elektronik |
| C48 | CAP, CERM, 390pF, 50V, 5%, C0G, 0603 | C0603C391J5GACTU | Kemet |
| C50 | CAP, CERM, 1.8nF, 10%, X7R 0603 | C0603C182K5RACTU | Kemet |
| C59 | CAP, CERM, 2.2 μ F, 16V, 20%, X5R, 0603 | 885012106018 | Wurth Elektronik |
| C60 | CAP, CERM, 3.3nF, 50V, 10%, X7R, 0603 | 885012206086 | Wurth Elektronik |
| C61 | CAP, CERM, 2.2nF, 16V, 10%, X7R, 0603 | 885012206036 | Wurth Elektronik |
| C62, C67 | CAP, CERM, 220pF, 50V, 5%, C0G, 0603 | C0603C221J5GACTU | Kemet |
| C66 | CAP, CERM, 0.47 μ F, 16V, 10%, X7R, 0603 | GRM188R71C474KA88D | MuRata |
| D1, D2 | LED, Green, SMD, 0603 | LTST-C190GKT | Lite-On |
| H1, H2, H3, H4, H5 | BUMPER CYLIN 0.312" DIA | SJ61A6 | 3M |
| J1, J4, J20 | Header, 100mil, 3x1, Gold, TH | TSW-103-07-G-S | Samtec |
| J2, J3, J15, J17, J19, J21 | CONN SMA JACK STR EDGE MNT | CON-SMA-EDGE-S | RF Solutions Ltd. |
| J5, J6, J7, J8, J9, J10, J11, J12 | Header, 100mil, 2x1, Gold, TH | TSW-102-07-G-S | Samtec |
| J13, J14, J16, J18 | 2.92mm Connector, 50Ohm Board Edge | 1521-00002 | SV Microwave |
| J22 | USB 2.0, Micro-USB Type B, R/A, SMT | 10118194-0001LF | FCI |
| L1 | Ferrite Bead, 120 Ω @ 100MHz, 3A, 0603 | BLM18SG121TN1D | MuRata |
| Q1 | MOSFET, N-CH, 50V, 0.22A, SOT-23 | BSS138 | Fairchild |
| R1 | RES, 10, 5%, 0.1W, 0603 | CRCW060310R0JNEA | Vishay-Dale |
| R2 | RES, 88.7k, 1%, 0.1W, 0603 | CRCW060388K7FKEA | Vishay-Dale |
| R3 | RES, 33.2k, 0.1%, 0.1W, 0603 | RT0603BRD0733K2L | Yageo America |
| R4 | RES, 12.0k, 0.1%, 0.1W, 0603 | RT0603BRD0712KL | Yageo America |
| R5 | RES, 10.0k, 1%, 0.1W, 0603 | CRCW060310K0FKEA | Vishay-Dale |
| R6 | RES, 5.05k, 0.5%, 0.1W, 0603 | RT0603DRE075K05L | Yageo America |
| R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R29, R30, R31, R32, R33, R34, R39, R40, R41 | RES 10k, 5%, 0.1W, 0603 | CRCW060310K0JNEBC | Vishay |
| R25, R74 | RES, 10k, 5%, 0.1W, 0603 | CRCW060310K0JNEA | Vishay-Dale |

| Designator | Description | PartNumber | Manufacturer |
|---|--|--------------------|-------------------|
| R26, R27, R28, R35, R36, R37, R38 | RES, 6.8k, 5%, 0.1W, 0603 | CRCW06036K80JNEA | Vishay-Dale |
| R42, R43, R44, R45, R46, R47, R48, R49, R50, R52, R94 | RES, 0, 5%, 0.1W, 0603 | CRCW06030000Z0EA | Vishay-Dale |
| R51 | RES, 18.2, 1%, 0.1W, 0603 | CRCW060318R2FKEA | Vishay-Dale |
| R53 | RES, 68.1, 1%, 0.1W, 0603 | CRCW060368R1FKEA | Vishay-Dale |
| R54 | RES, 0, 5%, 0.063W, 0402 | CRCW04020000Z0ED | Vishay-Dale |
| R57, R58, R61, R62, R63, R65, R66, R67, R69, R70 | RES, 10.0k, 1%, 0.05W, 0201 | CRCW020110K0FKED | Vishay-Dale |
| R59, R60 | RES, 49.9, 1%, 0.063W, 0402 | CRCW040249R9FKED | Vishay-Dale |
| R68, R73, R75, R76, R78, R79, R81, R82, R83, R84, R85 | RES, 1.0k, 5%, 0.1W, 0603 | CRCW06031K00JNEA | Vishay-Dale |
| R71, R86 | RES, 330, 5%, 0.1W, 0603 | CRCW0603330RJNEA | Vishay-Dale |
| R72, R77, R80, R89, R90 | RES, 33, 5%, 0.1W, 0603 | CRCW060333R0JNEA | Vishay-Dale |
| R87 | RES, 1.0 M, 5%, 0.1W, 0603 | CRCW06031M00JNEA | Vishay-Dale |
| R88 | RES, 33k, 5%, 0.1W, 0603 | CRCW060333K0JNEA | Vishay-Dale |
| R91 | RES, 1.5k, 5%, 0.1W, 0603 | CRCW06031K50JNEA | Vishay-Dale |
| R92 | RES, 1.2M, 5%, 0.1W, 0603 | CRCW06031M20JNEA | Vishay-Dale |
| R93 | RES, 1.78k, 1%, 0.063W, 0402 | CRCW04021K78FKED | Vishay-Dale |
| R95 | RES, 1.00k, 1%, 0.063W, 0402 | CRCW04021K00FKED | Vishay-Dale |
| S1 | Switch, Tactile, SPST, 0.05A, 12V, SMT | FSM4JSMA | TE Connectivity |
| SH-J1, SH-J2, SH-J3 | Shunt, 100mil, Gold plated, Black | SNT-100-BK-G | Samtec |
| SW1, SW2, SW3, SW4, SW5, SW6, SW7, SW8, SW9 | Switch Rotary DIP SP4T 100MA 50V | 220ADB04 | CTS |
| TP1, TP2, TP4 | Test Point, Miniature, Red, TH | 5000 | Keystone |
| TP3 | Test Point, Miniature, Black, TH | 5001 | Keystone |
| TP5, TP6, TP7, TP8, TP9 | Test Point, Miniature, White, TH | 5002 | Keystone |
| U1 | 1.5A, Radiation Hardened LDO | TPS7H1111MPWPTSEP | Texas Instruments |
| U2 | Space Grade Wideband RF Synthesizer | LMX2624PAP/EM | Texas Instruments |
| U3 | Ultra Low Noise, 150mA LDO | LP5900SDX-3.3/NOPB | Texas Instruments |
| U4 | 25MHz Microcontroller | MSP430F5529IPN | Texas Instruments |
| U5 | 4-Channel ESD Diode | TPD4S009DRYR | Texas Instruments |
| Y1 | High-Performance BAW Oscillator | CDC6CE024000ADLFT | Texas Instruments |

6 Additional Information

6.1 Debug Information

If the EVM does not work as expected, consider the following:

Verify hardware setup:

- Do not make modifications to the EVM or change the default settings until AFTER the EVM is verified to be working.
- Validate power supply is connected, is turned on, and current limit is appropriate for the device.
- Validate OSCIN signal is supplied, is turned on with appropriate output level.
- Verify that the spectrum analyzer center frequency matches target frequency. Choose wide span so that the carrier can be seen if the frequency is off from center.
- Verify that the device is not powered down by the CAL pin in Pin Mode.
- When the EVM is in Pin Mode,
 - Power up current of the EVM is approximately 240mA if CAL header is strapped.
 - Power up current of the EVM is approximately 16mA if CAL header is open.
- When the EVM is connected to a PC,
 - Power up current of the EVM is approximately 240mA if TICS Pro with EVM Default Mode configuration is loaded.
 - Power up current of the EVM is approximately 16mA, otherwise.
- If onboard LDO is used, there is an additional 20mA current drawn due to the LDO.
- If onboard LDO is used, both VBIAS and VCCIN supplies are required.

Verify software setup:

- If your configuration is not working, revert back to EVM Default Mode configuration, validate the device is locked and then modify the device again to your configuration.
- Validate that no red warning is prompted. If so, mouse over to the warning element, read the tool tips or check the message in the bottom left status window.
- Click the **Reset device button** once to reset the device, then load all the registers.
- With No Assist operation, after changing the VCO frequency or enabling VCO doubler output, a VCO calibration is required. Click the **Calibrate VCO** button to initiate VCO calibration.
- Register read back requires the correct configuration, see [Figure 4-18](#) for details.

Verify PC communications:

- In the menu bar, click *USB Communications* → *Interface*. Verify that the USB2ANY button is turned green. Click *Identify* to validate the USB LED on the EVM blinks.
- Program **POWERDOWN** = 1 to validate there is significant current change.

6.2 Trademarks

All trademarks are the property of their respective owners.

STANDARD TERMS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, and/or documentation which may be provided together or separately (collectively, an "EVM" or "EVMs") to the User ("User") in accordance with the terms set forth herein. User's acceptance of the EVM is expressly subject to the following terms.
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 - 1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.
2. *Limited Warranty and Related Remedies/Disclaimers:*
 - 2.1 These terms do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.
 - 2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.
 - 2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

WARNING

Evaluation Kits are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems.

User shall operate the Evaluation Kit within TI's recommended guidelines and any applicable legal or environmental requirements as well as reasonable and customary safeguards. Failure to set up and/or operate the Evaluation Kit within TI's recommended guidelines may result in personal injury or death or property damage. Proper set up entails following TI's instructions for electrical ratings of interface circuits such as input, output and electrical loads.

NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGRADATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

3 Regulatory Notices:

3.1 United States

3.1.1 Notice applicable to EVMs not FCC-Approved:

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

3.3 Japan

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

<https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html>

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

【無線電波を送信する製品の開発キットをお使いになる際の注意事項】 開発キットの中には技術基準適合証明を受けていないものがあります。技術適合証明を受けていないものご使用に際しては、電波法遵守のため、以下のいずれかの措置を取っていただく必要がありますのでご注意ください。

1. 電波法施行規則第6条第1項第1号に基づく平成18年3月28日総務省告示第173号で定められた電波暗室等の試験設備でご使用いただく。
2. 実験局の免許を取得後ご使用いただく。
3. 技術基準適合証明を取得後ご使用いただく。

なお、本製品は、上記の「ご使用にあたっての注意」を譲渡先、移転先に通知しない限り、譲渡、移転できないものとします。

上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。日本テキサス・イ

ンスツルメンツ株式会社

東京都新宿区西新宿 6 丁目 2 4 番 1 号

西新宿三井ビル

3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lstds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。 <https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html>

3.4 European Union

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive):*

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

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4. *EVM Use Restrictions and Warnings:*
 - 4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.
 - 4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.
 - 4.3 *Safety-Related Warnings and Restrictions:*
 - 4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.
 - 4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.
 - 4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.
 5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.
 6. *Disclaimers:*
 - 6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.
 - 6.2 EXCEPT FOR THE LIMITED RIGHT TO USE THE EVM SET FORTH HEREIN, NOTHING IN THESE TERMS SHALL BE CONSTRUED AS GRANTING OR CONFERRING ANY RIGHTS BY LICENSE, PATENT, OR ANY OTHER INDUSTRIAL OR INTELLECTUAL PROPERTY RIGHT OF TI, ITS SUPPLIERS/LICENSORS OR ANY OTHER THIRD PARTY, TO USE THE EVM IN ANY FINISHED END-USER OR READY-TO-USE FINAL PRODUCT, OR FOR ANY INVENTION, DISCOVERY OR IMPROVEMENT, REGARDLESS OF WHEN MADE, CONCEIVED OR ACQUIRED.
 7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

8.1 *General Limitations.* IN NO EVENT SHALL TI BE LIABLE FOR ANY SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL, OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THESE TERMS OR THE USE OF THE EVMS , REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO, COST OF REMOVAL OR REINSTALLATION, ANCILLARY COSTS TO THE PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES, RETESTING, OUTSIDE COMPUTER TIME, LABOR COSTS, LOSS OF GOODWILL, LOSS OF PROFITS, LOSS OF SAVINGS, LOSS OF USE, LOSS OF DATA, OR BUSINESS INTERRUPTION. NO CLAIM, SUIT OR ACTION SHALL BE BROUGHT AGAINST TI MORE THAN TWELVE (12) MONTHS AFTER THE EVENT THAT GAVE RISE TO THE CAUSE OF ACTION HAS OCCURRED.

8.2 *Specific Limitations.* IN NO EVENT SHALL TI'S AGGREGATE LIABILITY FROM ANY USE OF AN EVM PROVIDED HEREUNDER, INCLUDING FROM ANY WARRANTY, INDEMNITY OR OTHER OBLIGATION ARISING OUT OF OR IN CONNECTION WITH THESE TERMS, , EXCEED THE TOTAL AMOUNT PAID TO TI BY USER FOR THE PARTICULAR EVM(S) AT ISSUE DURING THE PRIOR TWELVE (12) MONTHS WITH RESPECT TO WHICH LOSSES OR DAMAGES ARE CLAIMED. THE EXISTENCE OF MORE THAN ONE CLAIM SHALL NOT ENLARGE OR EXTEND THIS LIMIT.

9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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