Application Report

How to Tune DS160PR410 for Best Signal Integrity

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ABSTRACT

PCI-Express (or PCIe) 4.0 links provide overall loss budget of 28 dB at 8 GHz. Unsurprisingly, many system have PCIe links that exceed the loss budget, or have imperfect implementations that reduce the available loss budget, or both. The DS160PR410, a quad-channel PCI-Express 4.0 PCI-SIG compliant linear redriver with integrated signal conditioning, reduces deterministic jitter caused by channel losses, increases the loss budget, and ultimately increases the reach of the PCIe 4.0 links by up to 50%. This application reports provides guidance on using the DS160PR410 for best signal integrity and maximum extension of the PCIe 4.0 links.

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1 Introduction

Redriver tuning is one of the few required tasks when designing with the DS160PR410 PCIe 4.0 linear redriver. Using information in this application report makes redriver tuning easy to understand and implement. This application report provides a quick overview of the DS160PR410 key signal conditioning features, it describes components of PCIe links relevant to redriver tuning, shares useful DS160PR410 validation and system level results, suggests optimal redriver placement based on these results, outlines possible PCIe link extensions, and provides redriver step-by-step tuning instructions using real system examples. With a complete understanding of the redriver capabilities, limitations, and redriver tuning steps, system designers are better equipped to extend the reach of PCIe 4.0 links using linear redrivers.

2 Device Overview

The DS160PR410 is a quad-channel PCI-Express 4.0, PCI-SIG compliant, linear redriver with integrated signal conditioning. As illustrated in Figure 2-1, each channel includes a continuous-time linear equalizer (CTLE) and a linear driver that together enable significant extension of PCIe links.

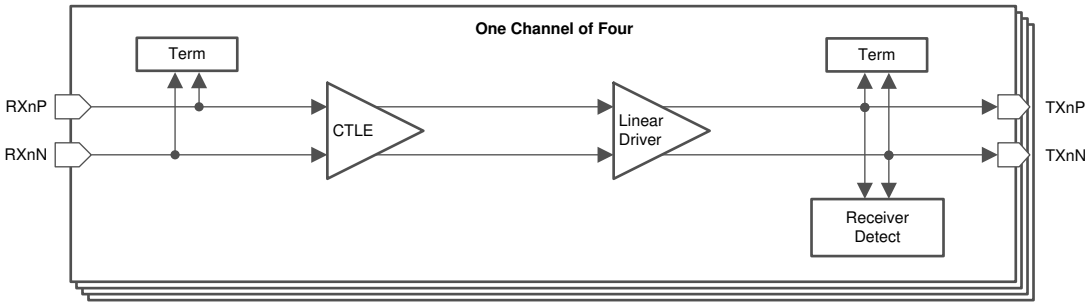

Figure 2-1. DS160PR410 Simplified Block Diagram

With very low additive random jitter (60 fs rms), latency (70 ps), and power consumption, the DS160PR410 is suitable for many PCIe 3.0 and 4.0 systems requiring link extension devices.

2.1 Receiver Equalization

The DS160PR410 CTLE boosts 8 GHz frequency components of a PCIe 4.0 data stream by up to 18 dB. There are 16 programmable equalization steps (EQ Indexes), as shown in Table 2-1, that enable setting equalization boost to a level that closely matches the insertion loss of a transmission channel. Setting of the equalization boost can be done with the device pins when operating in pin mode, or programmatically when operating in one of the SMBus / I2C modes (See DS160PR410 Programming Guide for more details).

Table 2-1. DS160PR410 Equalization Settings

EQ INDEX	TYPICAL CTLE BOOST (dB)	
	@ 4 GHz	@ 8 GHz
0	–0.3	–0.8
1	0.4	1.3
2	3.3	5.7
3	3.8	7.1
4	4.9	8.4
5	5.2	9.1
6	5.4	9.8
7	6.5	10.7
8	6.7	11.3
9	7.7	12.6
10	8.7	13.6
11	9.1	14.4
12	9.4	15.0
13	10.3	15.9
14	10.6	16.5
15	11.8	17.8

2.2 Redriver Linearity

The linearity of the data path is specifically designed to preserve any transmit equalization while keeping receiver equalization effective. It allows unobstructed PCIe 3.0 and 4.0 link training for automatic optimization of the PCIe TX and RX equalization functions on both the root complex and the endpoint sides of the link. Table 2-2 shows typical PCIe TX preset values (pre-shoot and de-emphasis levels) before the presets are passed through the DS160PR410 redriver and after the PCIe TX presets are re-driven. This data was measured with adherence to the PCI-Express 4.0 Base specification, section 8.3.3.5. Note that the preset values after the redriver deviate from the initial values by less than one dB.

Table 2-2. DS160PR410 Performance with PCIe TX Presets

PCIe TX Preset	PCIe Preset Limits		Typical PCIe Presets Before Redriver		Typical PCIe Presets After Redriver	
	Ideal Pre-shoot	Ideal De-emphasis	Pre-shoot (dB)	De-emphasis (dB)	Pre-shoot (dB)	De-emphasis (dB)
P0	0	–6.0 ±1.5 dB	0	-6.7	0	-5.9
P1	0	–3.5 ±1.0 dB	0	-3.9	0	-3.3
P2	0	–4.4 ±1.5 dB	0	-4.8	0	-4.2
P3	0	–2.5 ±1.0 dB	0	-2.9	0	-2.4
P4	0	0	0	0	0	0
P5	1.9 ±1.0 dB	0	2.0	0	1.7	0
P6	2.5 ±1.5 dB	0	2.9	0	2.4	0
P7	3.5 ±1.0 dB	–6.0 ±1.5 dB	3.9	-6.7	3.6	-6.1
P8	3.5 ±1.0 dB	-3.5 ±1.0 dB	3.9	-4.0	3.6	-3.6
P9	3.5 ±1.0 dB	0	3.9	0	3.3	0
P10	0	-9.5 ±1.5 dB	0	-10.6	0	-9.8

The eye diagrams in Figure 2-2 through Figure 2-13 further illustrate the redriver's linearity and its ability to pass through the PCIe transmitter equalization (pre-shoot and de-emphasis wave shapes or TX presets) at the PCIe 4.0 rates when the redriver is placed very close to a PCIe transmitter (< -3 dB). For brevity, only the PCIe TX presets P0, P1, P4, P8, and P9 pre are shown. All eye diagrams shown below were captured using a 50 GHz oscilloscope with the 200 mV / division vertical scale and the 10 ps / division horizontal scale.

Note that this test case is a pathological case and is unlikely to be encountered in any real system. The redriver placement of at least -8 dB or more from a PCIe transmitter is a more typical use case.

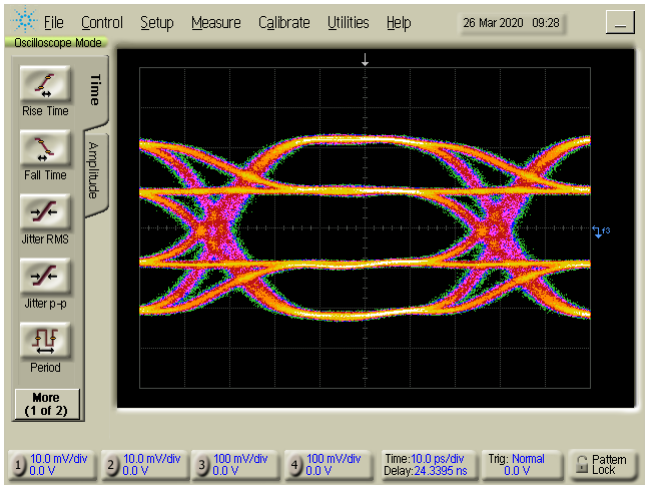

Figure 2-2. PCIe TX Preset P0 (-6 dB De-emphasis) Before Redriver

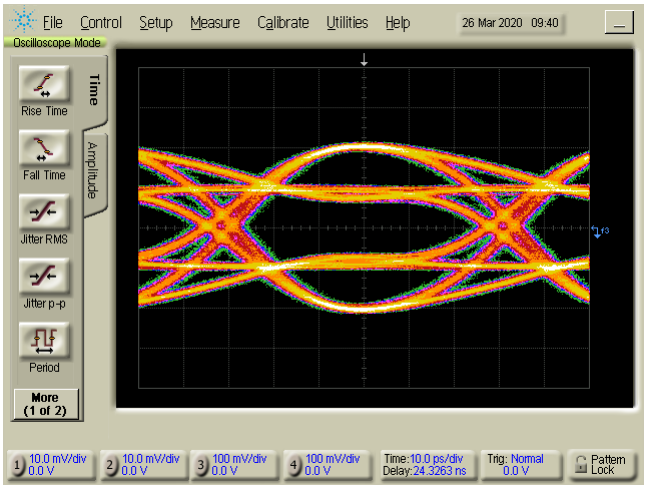

Figure 2-3. PCIe TX Preset P0 (-6 dB De-emphasis) After Redriver (EQ Index 1 = 1.3 dB)

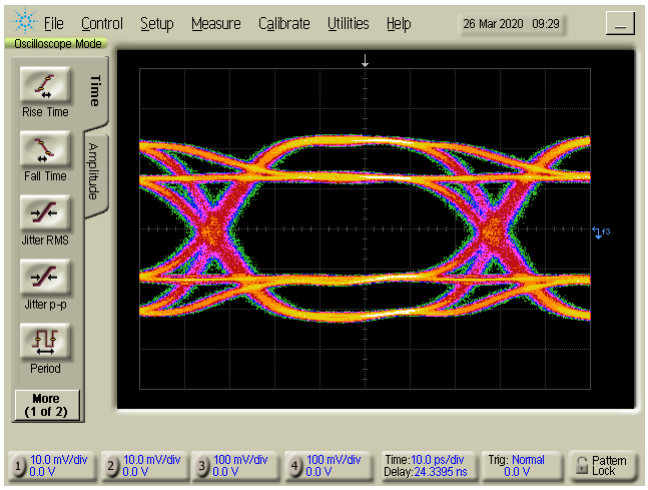

Figure 2-4. PCIe TX Preset P1 (-3.5 dB De-emphasis) Before Redriver

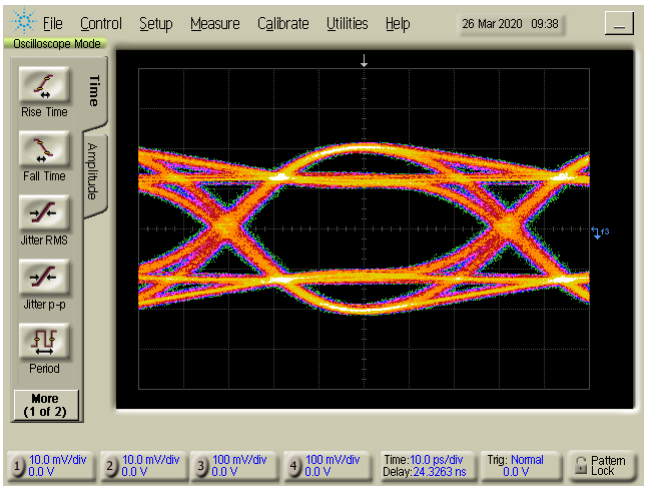

Figure 2-5. PCIe TX Preset P1 (-3.5 dB De-emphasis) After Redriver (EQ Index 1 = 1.3 dB)

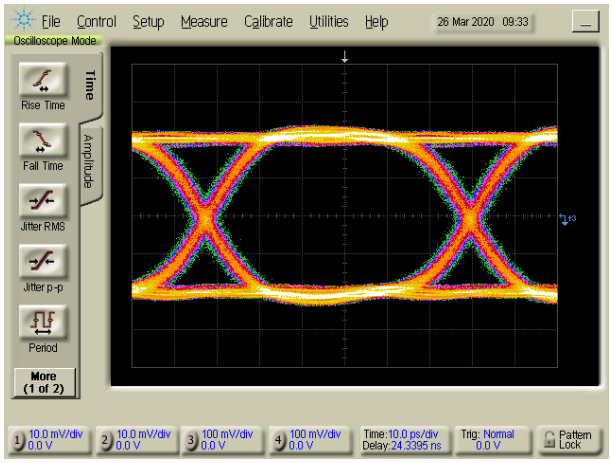

Figure 2-6. PCIe TX Preset P4 (0 dB Preset) Before Redriver

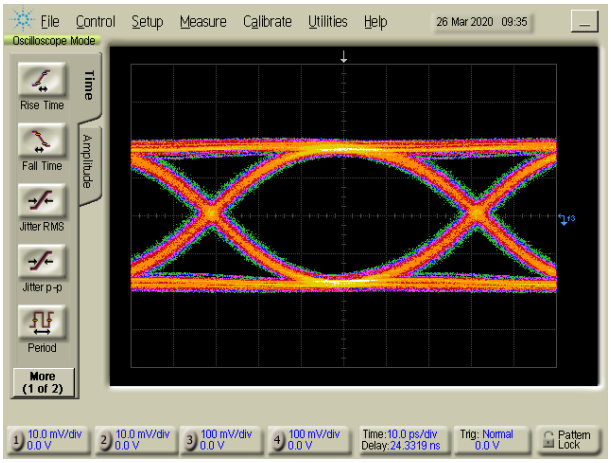

Figure 2-7. PCIe TX Preset P4 (0 dB Preset) After Redriver (EQ Index 1 = 1.3 dB)

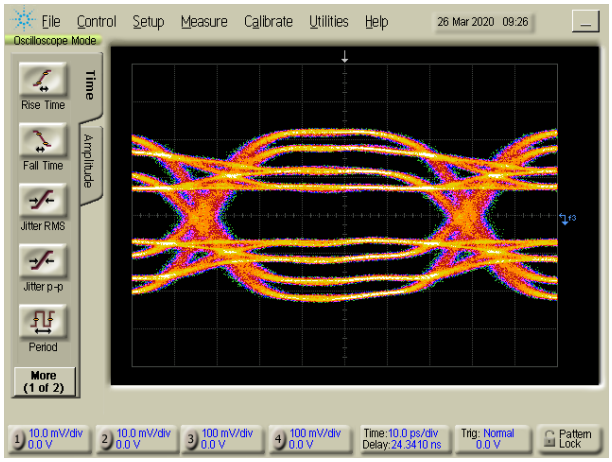

Figure 2-8. PCIe TX Preset P7 (3.5 dB Pre-shoot, -6 dB De-emphasis) Before Redriver

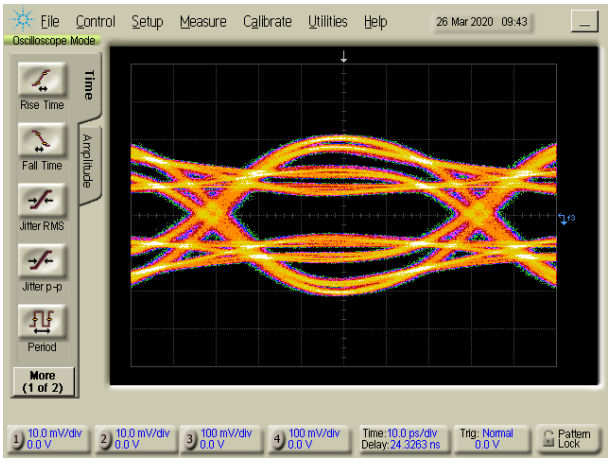

Figure 2-9. PCIe TX Preset P7 (3.5 dB Pre-shoot, -6 dB De-emphasis) After Redriver (EQ Index 1 = 1.3 dB)

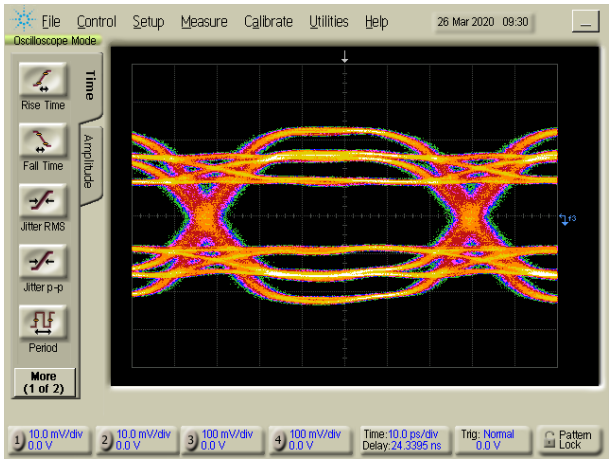

Figure 2-10. PCIe TX Preset P8 (3.5 dB Pre-shoot, -3.5 dB De-emphasis) Before Redriver

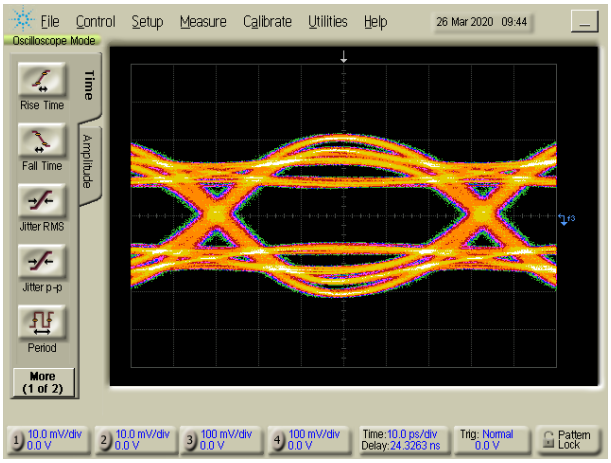

Figure 2-11. PCIe TX Preset P8 (3.5 dB Pre-shoot, -3.5 dB De-emphasis) After Redriver (EQ Index 1 = 1.3 dB)

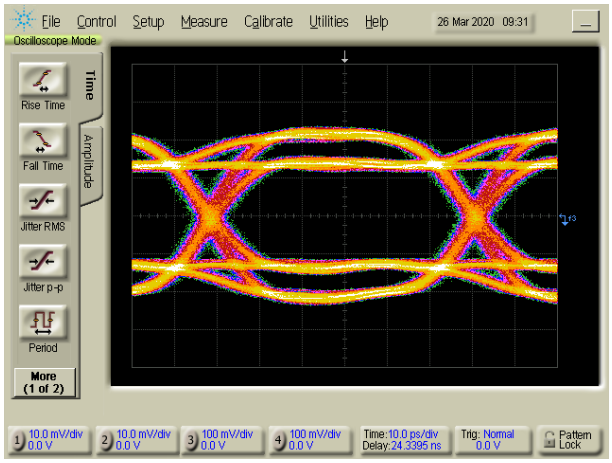

Figure 2-12. PCIe TX Preset P9 (3.5 dB Pre-shoot) Before Redriver

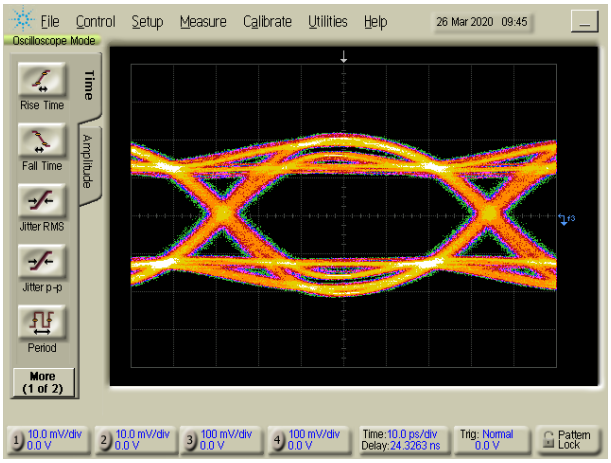

Figure 2-13. PCIe TX Preset P9 (3.5 dB Pre-shoot) After Redriver (EQ Index 1 = 1.3 dB)

Based on the eye diagrams in Figure 2-2 through Figure 2-13, it is evident that the PCIe presets P0, P1, and P4 wave shapes are well retained after they are re-driven by the DS160PR410 while the TX presets such as P7 show some wave shape degradation, but retain most of the PCIe equalization boost after they are passed through the redriver. This degradation should be considered when placing redrivers too close to the PCIe transmitters.

3 PCIe Links with Linear Redrivers

PCI-Express (PCIe) links are typically implemented with 4-lane (x4), 8-lane (x8), and 16-lane (x16) widths. For the purpose of redriver tuning, it is useful to become familiar with components of a PCIe lane that incorporates linear redrivers. As shown in Figure 3-1, bidirectional communication between a PCIe root complex (RC) and a PCIe endpoint (EP) is carried over downstream (from RC to EP) and upstream (from EP to RC) channels.

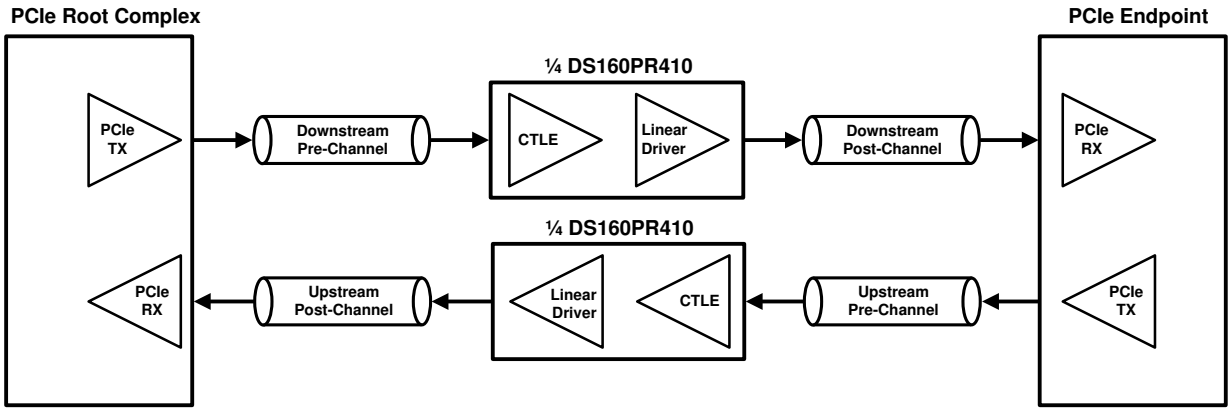

Figure 3-1. Single PCIe Lane with Linear Redrivers

A channel between a PCIe transmitter (TX) and a redriver is a pre-channel, while a channel between a redriver and a PCIe receiver (RX) is a post-channel indicating channels' positions relative to the redriver.

It is important to note that the pre-channel loss compensation is handled by both PCIe TX equalization (for example, finite impulse response (FIR) function) and the redriver CTLE. As shown in Figure 3-2, the DS160PR410 CTLE alone with the 18 dB boost at 8 GHz compensates the losses of a -20 dB transmission channel and opens a fully closed eye diagram with a wide margin. With the help of a PCIe TX with a preset P7 (~ 8 dB added boost), a -30 dB channel is handled with a sufficient margin as well.

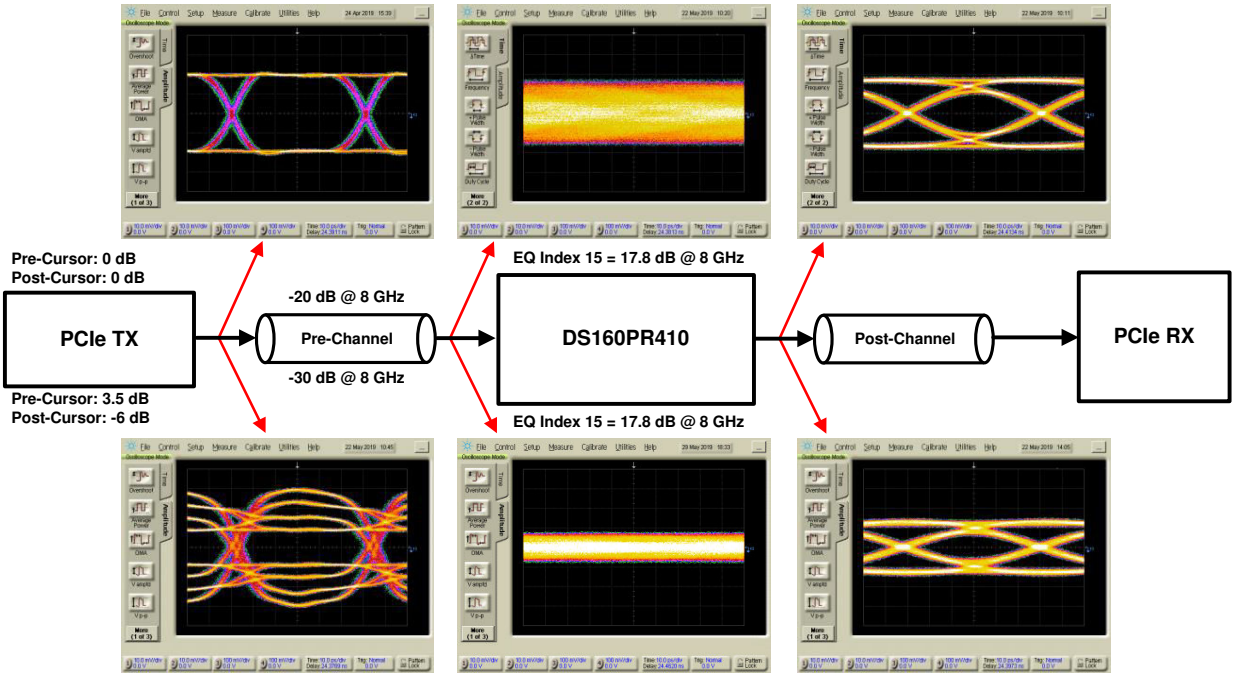

Figure 3-2. PCIe TX Equalization and DS160PR410 CTLE Sharing Pre-Channel Loss Compensation Duty

The post-channel loss compensation is handled by the PCIe receiver equalization functions such as adaptive CTLE and DFE (decision feedback equalizer), and any excess PCIe TX equalization that is passed through the linear redriver. As shown in Figure 3-3, a relatively short channel with -10 dB of insertion loss at 8 GHz is handled with a PCIe TX alone with the DS160PR410 redriving the signal with minimal CTLE gain. In this scenario, the post-channel loss must be handled by the PCIe RX alone. Alternatively, the DS160PR410 CTLE can be configured to fully compensate for the pre-channel loss, as also shown in Figure 3-3, and the PCIe TX equalization wave shape is passed through the redriver for handling the post-channel loss together with the PCIe RX equalization functions.

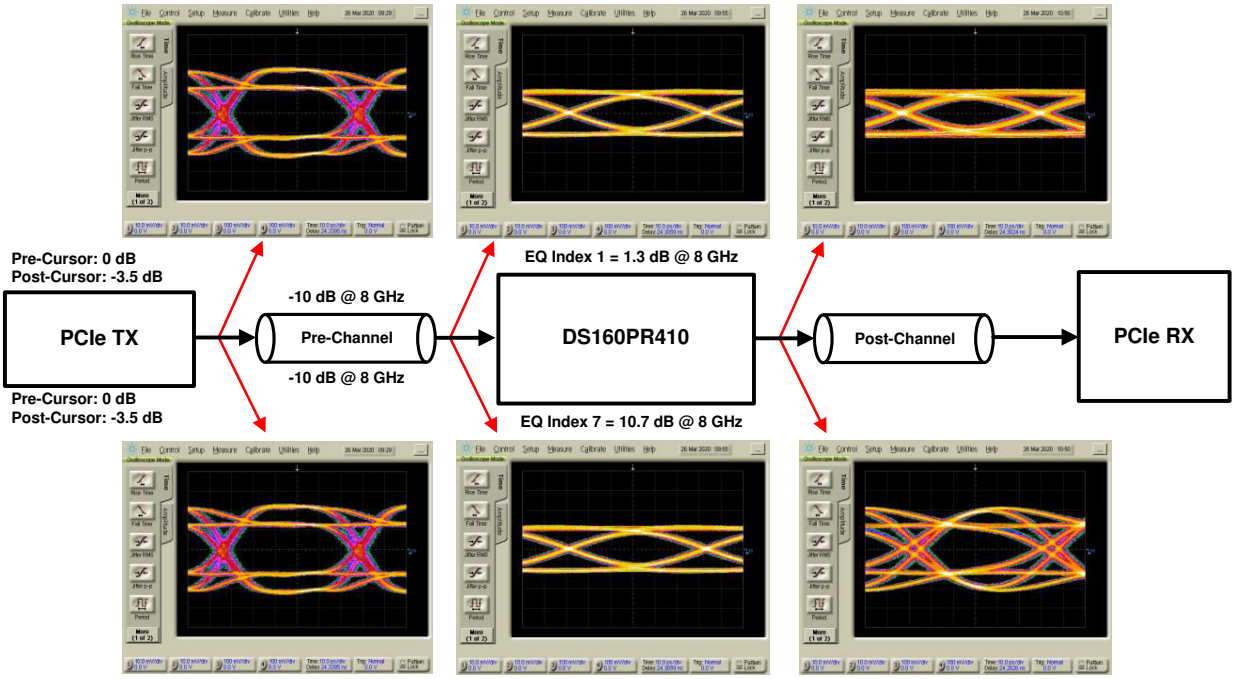

Figure 3-3. DS160PR410 Passing PCIe TX Equalization Wave Shapes to the Post-Channel

4 Redriver Tuning

For the DS160PR410, tuning its CTLE settings is all that is necessary for its optimal operation in a PCIe link. Other redriver settings such as VOD and DC Gain settings should be kept at the default values for most applications.

Tuning a CTLE typically means adjusting its gain curve to match the inverse of a given channel loss curve. However, for PCIe redrivers such as the DS160PR410, CTLE tuning means selecting a CTLE setting that works with most PCIe TX presets to ensure robust PCIe link training with sufficient timing and noise margins. As shown in Figure 4-1 and Figure 4-2, there are multiple redriver CTLE settings and PCIe TX pre-sets that help produce an acceptable eye opening after it had also been conditioned with PCIe compliant receiver equalization techniques. These figures show the measured eye height (EH) and eye width (EW) of a PCIe compliance pattern captured with the oscilloscope and then post-processed by the PCI-SIG's SigTest v4.0.48 software that is modeling the PCIe receiver's adaptive CTLE and DFE functions as defined in the PCIe 4.0 Base specification.

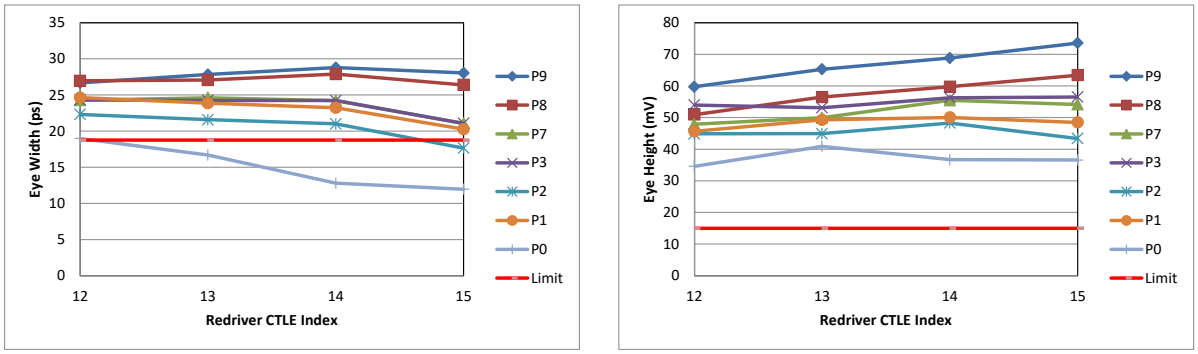

Figure 4-1. Eye Width and Eye Height as a Function of PCIe TX Preset and Redriver CTLE Setting for a 18-dB Pre-Channel and a 18-dB Post-Channel

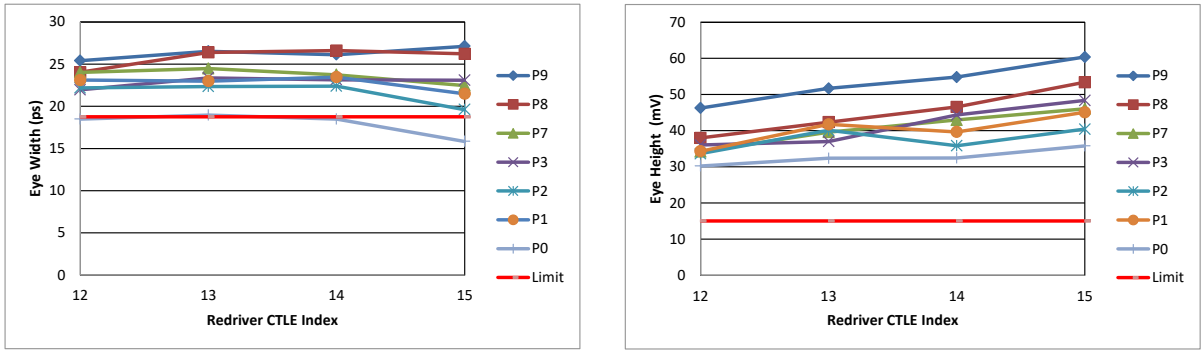

Figure 4-2. Eye Width and Eye Height as a Function of PCIe TX Preset and Redriver CTLE Setting for a 24-dB Pre-Channel and a 18-dB Post-Channel

As previously noted, the pre-channel loss compensation is handled by both the PCIe TX equalization and the redriver CTLE while the post-channel loss is handled by the PCIe RX equalization and any excess PCIe TX equalization that is passed through by the redriver. In theory, the range of the redriver CTLE settings that is acceptable for a given pre-channel loss is at least as wide as the PCIe TX EQ boost range (0 - 9.5 dB). This is illustrated in Figure 4-3 for the 18-dB and 22-dB pre-channels. For example, for the 18-dB pre-channel, the maximum PCIe TX EQ of 9.5 dB (preset P10) and the redriver CTLE boost of 8.4 dB (CTLE Index 4) provide a combined equalization boost of 17.9 dB, a close match to the -18 dB pre-channel loss. Similarly, if the redriver CTLE boost of 17.8 dB is selected (CTLE Index 15), there is enough equalization boost for the 18-dB pre-channel even if it is combined with the PCIe TX preset P4 (0 dB of the TX EQ boost). The advantage of selecting the redriver CTLE index 15 is that it can be combined with any PCIe preset to compensate for the 18-dB pre-channel losses. Any excess PCIe TX EQ boost would be passed through the redriver to help with the post-channel losses. This is illustrated in Figure 4-3 by highlighting the cells with the acceptable values of the combined (PCIe TX EQ + Redriver CTLE) equalization boost.

PCIe TX Presets		PCIe TX EQ Boost (dB)							
		P4	P5	P3 P6	P1 P9	P2	P0 P8	P7	P10
Redriver CTLE Index	Redriver CTLE Boost (dB)	0.00	1.90	2.50	3.50	4.40	6.00	8.00	9.50
0	**-0.8**	-0.8	1.1	1.7	2.7	3.6	5.2	7.2	8.7
1	**1.3**	1.3	3.2	3.8	4.8	5.7	7.3	9.3	10.8
2	**5.7**	5.7	7.6	8.2	9.2	10.1	11.7	13.7	15.2
3	**7.1**	7.1	9.0	9.6	10.6	11.5	13.1	15.1	16.6
4	**8.4**	8.4	10.3	10.9	11.9	12.8	14.4	16.4	17.9
5	**9.1**	9.1	11.0	11.6	12.6	13.5	15.1	17.1	18.6
6	**9.8**	9.8	11.7	12.3	13.3	14.2	15.8	17.8	19.3
7	**10.7**	10.7	12.6	13.2	14.2	15.1	16.7	18.7	20.2
8	**11.3**	11.3	13.2	13.8	14.8	15.7	17.3	19.3	20.8
9	**12.6**	12.6	14.5	15.1	16.1	17.0	18.6	20.6	22.1
10	**13.6**	13.6	15.5	16.1	17.1	18.0	19.6	21.6	23.1
11	**14.4**	14.4	16.3	16.9	17.9	18.8	20.4	22.4	23.9
12	**15.0**	15.0	16.9	17.5	18.5	19.4	21.0	23.0	24.5
13	**15.9**	15.9	17.8	18.4	19.4	20.3	21.9	23.9	25.4
14	**16.5**	16.5	18.4	19.0	20.0	20.9	22.5	24.5	26.0
15	**17.8**	17.8	19.7	20.3	21.3	22.2	23.8	25.8	27.3

Pre-Channel Loss: -18 dB

PCIe TX Presets		PCIe TX EQ Boost (dB)							
		P4	P5	P3 P6	P1 P9	P2	P0 P8	P7	P10
Redriver CTLE Index	Redriver CTLE Boost (dB)	0.00	1.90	2.50	3.50	4.40	6.00	8.00	9.50
0	**-0.8**	-0.8	1.1	1.7	2.7	3.6	5.2	7.2	8.7
1	**1.3**	1.3	3.2	3.8	4.8	5.7	7.3	9.3	10.8
2	**5.7**	5.7	7.6	8.2	9.2	10.1	11.7	13.7	15.2
3	**7.1**	7.1	9.0	9.6	10.6	11.5	13.1	15.1	16.6
4	**8.4**	8.4	10.3	10.9	11.9	12.8	14.4	16.4	17.9
5	**9.1**	9.1	11.0	11.6	12.6	13.5	15.1	17.1	18.6
6	**9.8**	9.8	11.7	12.3	13.3	14.2	15.8	17.8	19.3
7	**10.7**	10.7	12.6	13.2	14.2	15.1	16.7	18.7	20.2
8	**11.3**	11.3	13.2	13.8	14.8	15.7	17.3	19.3	20.8
9	**12.6**	12.6	14.5	15.1	16.1	17.0	18.6	20.6	22.1
10	**13.6**	13.6	15.5	16.1	17.1	18.0	19.6	21.6	23.1
11	**14.4**	14.4	16.3	16.9	17.9	18.8	20.4	22.4	23.9
12	**15.0**	15.0	16.9	17.5	18.5	19.4	21.0	23.0	24.5
13	**15.9**	15.9	17.8	18.4	19.4	20.3	21.9	23.9	25.4
14	**16.5**	16.5	18.4	19.0	20.0	20.9	22.5	24.5	26.0
15	**17.8**	17.8	19.7	20.3	21.3	22.2	23.8	25.8	27.3

Pre-Channel Loss: -22 dB

Figure 4-3. Possible Redriver CTLE Settings for 18-dB and 22-dB Pre-Channels

The type of visualization exemplified in Figure 4-3 can help with the redriver tuning, or more precisely, with selecting a redriver CTLE setting that works best with most PCIe TX presets. For example, for the 18-dB pre-channel, the redriver CTLE Indexes 10-15 work well with seven or more PCIe TX presets. The empirical data, later shown in Table 5-1, indicates that the DS160PR410 best performs with the PCIe TX presets with the EQ boost that is within the 1.9 dB - 4.4 dB range. If the PCIe TX presets outside of this range are excluded, the redriver CTLE settings that work well with most PCIE TX presets can be narrowed down to the redriver CTLE Indexes 12 to 15. This is highlighted with a red frame in Figure 4-3. If the post-channel loss can fully be compensated for by the PCIE TX receiver equalization, the lower redriver setting from the range (for example, CTLE Index 12 or 13) should be selected. However, if the post-channel loss is significant and the PCIe TX equalization is needed to help with the post-channel compensation, then a higher redriver CTLE setting from the range should be selected (for example, CTLE Index 14 or 15).

The following steps provide general guidance for selecting optimal redriver CTLE settings:

1. Understand signal conditioning capabilities of the companion PCIe transmitters and receivers in the link. While all PCIe transmitters and receiver should meet the minimum requirements defined in the PCIe. 4.0 Base specification, there may be vast differences in performance between various endpoints and CPUs.
2. Determine or estimate the pre-channel, post-channel, and total channel losses of all downstream and upstream channels.
3. Determine the optimal CTLE setting for each redriver. Based on the pre-channel loss estimates, share the loss compensation duty between the PCIe transmitter and the DS160PR410 CTLE. Use a table exemplified in Figure 4-3 to select optimal CTLE index that works best with most PCIe TX presets. This step should be repeated for each redriver provided each redriver has a significantly different pre-channel loss profile. Typically, the pre-channel loss profiles differ between downstream and upstream redrivers.
4. Verify the optimal CTLE settings for the downstream redrivers. Sweep the CTLE settings of the downstream redrivers up and down from the initially selected CTLE setting (while keeping the initially selected CTLE setting of the upstream redrivers) to determine the range of CTLE settings that allow a successful system link up, if testing an actual system, or meet the minimum predefined eye mask if performing system simulations or measuring eye diagrams.
5. Verify the optimal CTLE settings for the upstream redrivers. Sweep the CTLE settings of the upstream redrivers up and down from the initially selected CTLE setting (while keeping the optimal CTLE setting of the downstream redrivers) to determine the range of CTLE setting that allow a successful system link up or meet the minimum predefined eye mask.

5 Performance Matrix

The DS160PR410 performance matrix in Table 5-1 shows the device performance with various pre-channel and post-channel combinations using Intel's widely accepted PCI Express 4.0 linear redriver characterization methodology.

Table 5-1. DS160PR410 Performance Matrix

Pre-Channel	Post-Channel Loss				
Loss	-10 dB	-14 dB	-18 dB	-22 dB	-26 dB
-10 dB	EH = 145.93 mV EW = 33.08 ps TX EQ = P5 **(1.9 dB)** ReDrv EQ Index = 8, **9**, 10 ReDrv EQ = **12.6 dB** RX CTLE Index = 1 RX DFE: Tap1 = 14.2 mV Tap2 = -10.7 mV	EH = 113.98 mV EW = 32.84 ps TX EQ = P5 **(1.9 dB)** ReDrv EQ Index = 8, **9**, 10 ReDrv EQ = **12.6 dB** RX CTLE Index = 1 RX DFE: Tap1 = 28.8 mV Tap2 = -5.4 mV	EH = 79.8 mV EW = 31.38 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 11, **12**, 13 ReDrv EQ = **15 dB** RX CTLE Index = 1 RX DFE: Tap1 = 27.8 mV Tap2 = -3.4 mV	EH = 53.92 mV EW = 30.6 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 10, **11**, 12 ReDrv EQ = **14.4 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = 2.9 mV	EH = 33.9 mV EW = 25.0 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 11, **12**, 13 ReDrv EQ = **15 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 5.4 mV
-14 dB	EH = 139.58 mV EW = 31.0 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 11, **12**, 13 ReDrv EQ = **15 dB** RX CTLE Index = 1 RX DFE: Tap1 = 8.8 mV Tap2 = -13.2 mV	EH = 103.56 mV EW = 30.5 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 11, **12**, 13 ReDrv EQ = **15 dB** RX CTLE Index = 1 RX DFE: Tap1 = 22.9 mV Tap2 = -8.3 mV	EH = 76.4 mV EW = 29.33 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 13, **14**, 15 ReDrv EQ = **16.5 dB** RX CTLE Index = 1 RX DFE: DFE Tap1 = 30 mV DFE Tap2 = -5.4 mV	EH = 51.39 mV EW = 28.15 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = -1.5 mV	EH = 31.04 mV EW = 24.65 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 2 mV
-18 dB	EH = 129.15 mV EW = 30.4 ps TX EQ = P5 **(1.9 dB)** ReDrv EQ Index = 12, **13**, 14 ReDrv EQ = **15.9 dB** RX CTLE Index = 1 RX DFE: Tap1 = 25.4 mV Tap2 = -11.2 mV	EH = 95.87 mV EW = 29.5 ps TX EQ = P5 **(1.9 dB)** ReDrv EQ Index = 13, **14**, 15 ReDrv EQ = **16.5 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = -6.3 mV	EH = 67.51 mV EW = 27.22 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = -3.4 mV	EH = 44.48 mV EW = 26.09 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 13, **14**, 15 ReDrv EQ = **16.5 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 2 mV	EH = 22.48 mV EW = 20.04 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 5.4 mV

Table 5-1. DS160PR410 Performance Matrix (continued)

Pre-Channel	Post-Channel Loss				
-22 dB	EH = 110.76 mV EW = 30.9 ps TX EQ = P5 **(1.9 dB)** ReDrv EQ Index = 13, **14**, 15 ReDrv EQ = **16.5 dB** RX CTLE Index = 1 RX DFE Tap1 = 30 mV RX DFE Tap2 = -6.3 mV	EH = 74.42 mV EW = 29.68 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 13, **14**, 15 ReDrv EQ = **16.5 dB** RX CTLE Index = 1 RX DFE Tap1 = 30 mV RX DFE Tap2 = -0.5 mV	EH = 53.47 mV EW = 27.9 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 1 RX DFE Tap1 = 30 mV RX DFE Tap2 = 1.5 mV	EH = 37.65 mV EW = 25.74 ps TX EQ = P9 **(2.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 2 RX DFE Tap1 = 30 mV RX DFE Tap2 = 3.4 mV	
-26 dB	EH = 81.77 mV EW = 29.19 ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = -4.4 mV	EH = 57.47 mV EW = 27.39 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = 0.5 mV	EH = 40.59 mV EW = 23.81 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 2 mV		
-30 dB	EH = 48.66 mV EW = 26.84 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDRV EQ = **17.8 dB** RX CTLE Index = 1 RX DFE: Tap1 = 30 mV Tap2 = 1 mV	EH = 33.45 mV EW = 23.82 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 2.9 mV			
-32 dB	EH = 33.49 mV EW = 24.84ps TX EQ = P6 **(2.5 dB)** ReDrv EQ Index = 13, **14**, 15 ReDrv EQ = **16.5 dB** RX CTLE Index = 3 RX DFE: Tap1 = 30 mV Tap2 = 2.9 mV	EH = 23.37 mV EW = 21.21 ps TX EQ = P9 **(3.5 dB)** ReDrv EQ Index = 14, **15** ReDrv EQ = **17.8 dB** RX CTLE Index = 2 RX DFE: Tap1 = 30 mV Tap2 = 5.9 mV			

A test setup equivalent to the setup shown in Figure 3-2 was used for collecting the data in the performance matrix. In this test setup, a pattern generator modeled a PCIe TX while an oscilloscope with the PCI-SIG's SigTest v4.0.48 software modeled a PCIe RX, all connected to a single DS160PR410 channel with the worst case crosstalk presented on the adjacent channels. The device voltage, ambient temperature, and process variation was considered for this data set.

Each Figure 4-1 entry shows the measured eye height (EH) and eye width (EW) of a PCIe compliance pattern captured with the oscilloscope and then post-processed by the PCI-SIG's SigTest v4.0.48 software that is modeling the PCIe receiver's adaptive CTLE and DFE functions as defined in the PCIe 4.0 Base specification. It also shows the selected optimal PCIe TX preset (as defined in Table 2-2), the DS160PR410 redriver CTLE setting or EQ Index (as defined in Table 2-1), and PCIe RX equalization (CTLE and DFE) settings for given pre-channel and post-channel losses.

The entries with the green background show the pre-channel and post-channel combinations that meet the minimum eye opening requirements for a PCIe 4.0 receiver (EH ≥ 15 mV and EW ≥ 18.75 ps) while the orange entries show the pre-channel and post channel combinations that do not meet the minimum eye opening requirements. The pre-channel and post-post channel combinations resulting in the total channel loss of -40 dB or more are shown with the entries with the dark green background.

5.1 Redriver Placement

The performance matrix also suggests possible reach of PCIe 4.0 links as a function of the redriver placement. A detailed examination of the performance matrix leads to the following conclusions about the redriver placement:

- Redrivers placed in the middle of a PCIe link allow for the maximum link extension as suggested in the first block diagram of Figure 5-1.
- When the pre-channel losses for both the upstream and downstream redrivers are at least -14 dB, the total channel loss (pre-channel + post channel) can be -40 dB or more (Figure 4-1). In other words, extending a PCIe link to -40 dB or more requires placing the DS160PR410 redrivers at least -14 dB from the PCIe transmitter.
- Placing redrivers closer than -14 dB to either upstream or downstream PCIe transmitters linearly reduces the maximum reach of the link. As shown in the 2nd and 3rd block diagrams of Figure 5-1, a -40 dB reach is possible with the redrivers placed at -14 dB from either a PCIe root complex or an endpoint. However, placing the redrivers, for example, within -8 dB of a PCIe root complex or an endpoint, limits the maximum link reach to -34 dB.
- Placing upstream and downstream redrivers in different locations is also possible, as shown in Figure 5-2, however, it may be impractical for most systems.

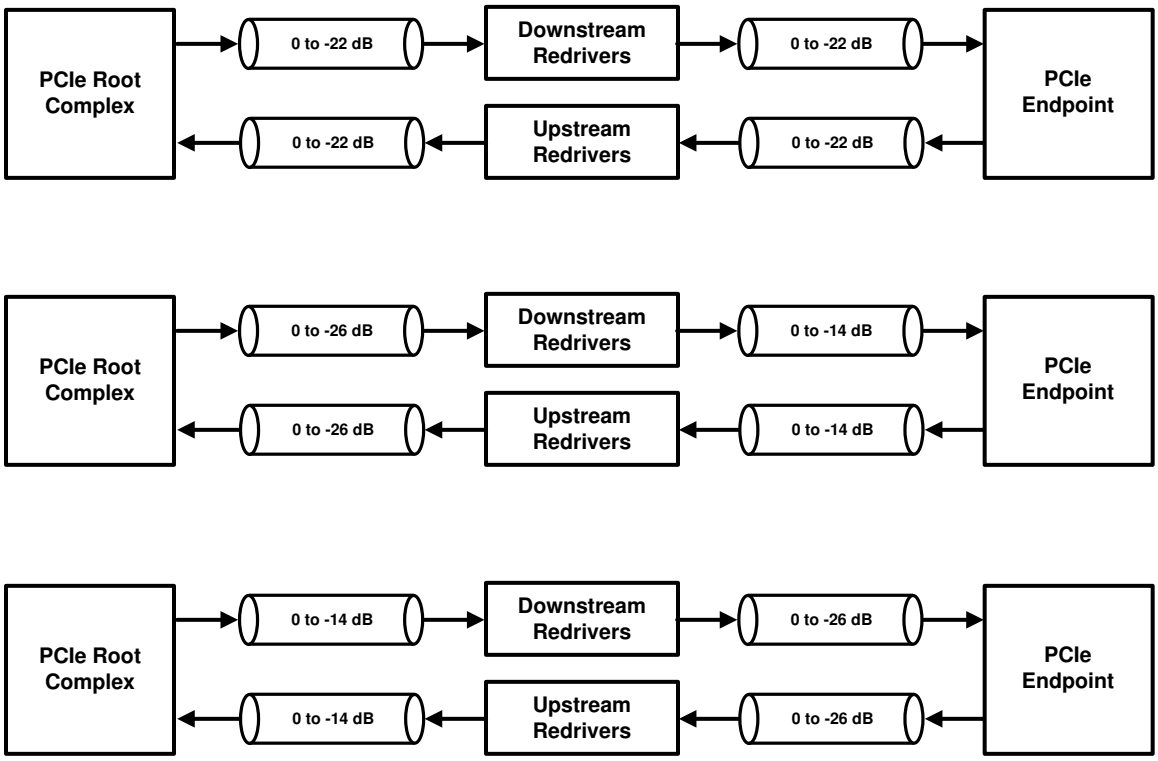

Figure 5-1. Redriver Placement Options: Upstream and Downstream Redrivers at Same Location

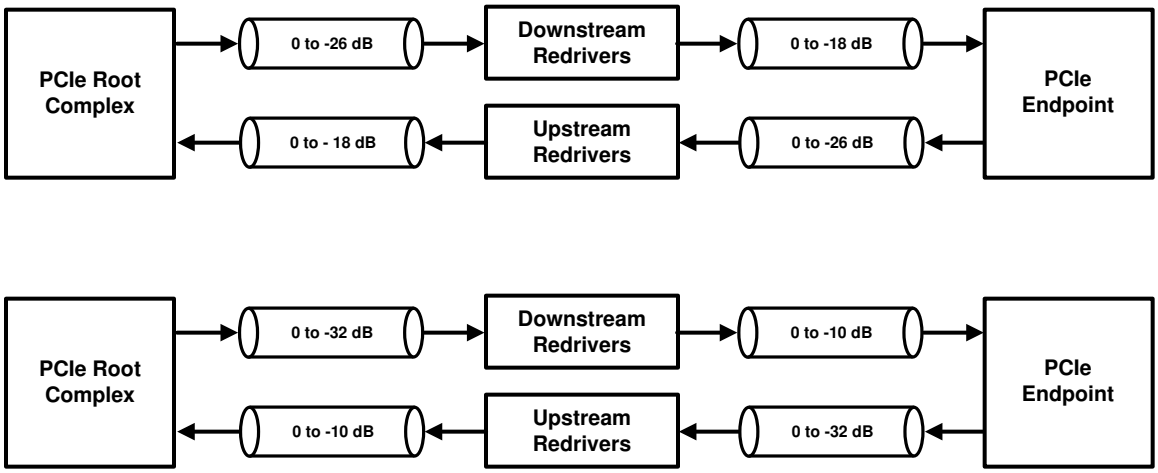

Figure 5-2. Redriver Placement Options: Upstream and Downstream Redrivers at Different Locations

6 Tuning Example

Consider a system shown in Figure 6-1. A DS160PR410EVM-RSC, a riser card style TI evaluation module featuring eight DS160PR410 devices and capable of extending a x16 PCIe 4.0 link, is placed between a CPU on a server motherboard and an PCIe end point (Network Interface Card or NIC). Additional "Extender" cards (Intel PCIe Link Extension Cards or PLECs) are inserted to increase the channel loss and demonstrate the redriver's ability to extend the link reach.

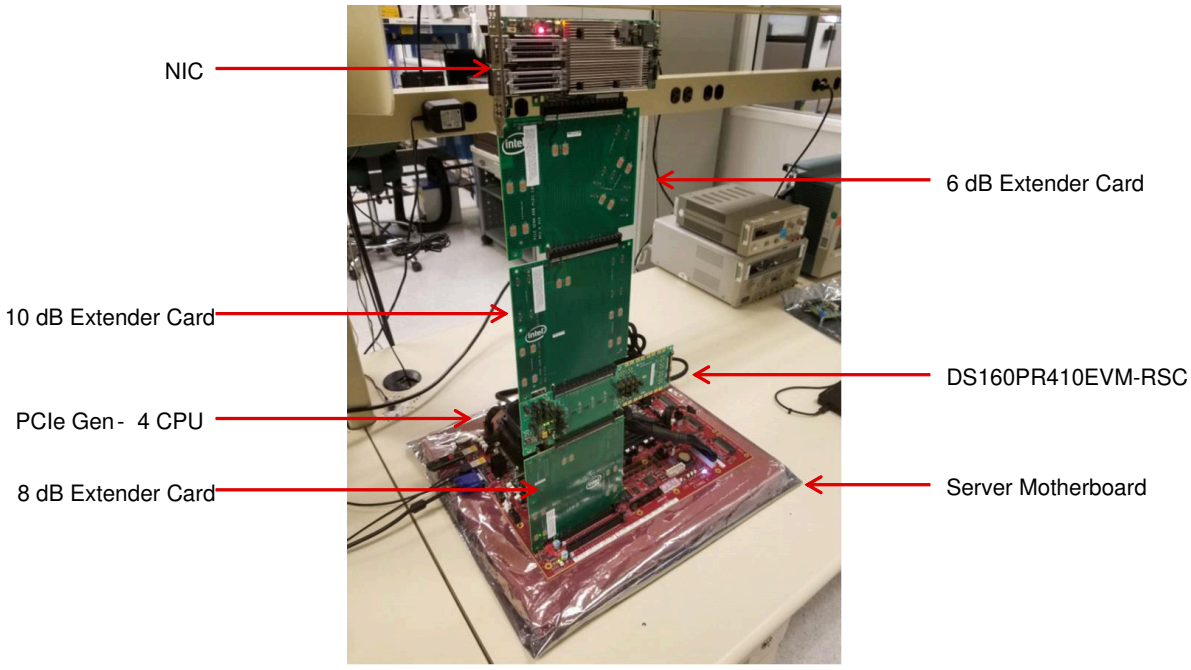

Figure 6-1. System Level Test Setup Example

Redriver tuning steps for this example are outlined as follows:

1. Understand capabilities of the companion PCIe TXs and RXs: Both the CPU and the network interface card (NIC) feature PCIe 4.0 I/Os and have been confirmed to handle at least a -28 dB channel loss without redrivers.
2. Determine or estimate channel losses:
   - Downstream pre-channel and upstream post-channel (the channels between the CPU and the redrivers): CPU package (~5 dB), motherboard differential trace (~10 dB), 8 dB extender card (8 dB), DS160PR410EVM-RSC differential trace (~0.5 dB), two CEM connectors (2 x 0.5 dB), totaling 24.5 dB.
   - Downstream post-channel and upstream pre-channel (the channels between the redrivers and the endpoint): DS160PR410EVM-RSC differential trace (~0.5 dB), 10 dB and 6 dB extender cards (16 dB), NIC including the SoC package (~2.5 dB), and three CEM connectors (3 x 0.5 dB), totaling 20.5 dB.
3. Determine the optimal redriver CTLE settings:
   - Downstream redrivers: With the -24.5 dB of the downstream pre-channel loss and using the two-dimensional array exemplified in Figure 6-2, the CTLE index 15 looks as an optimal setting that should work well with most PCIe TX presets.
   - Upstream redrivers: With the -20.5 dB of the upstream pre-channel loss and using the two-dimensional array exemplified in Figure 6-2, the CTLE index 15 also looks as an optimal setting that should work best with most PCIe TX presets.

PCIe TX Presets		PCIe TX EQ Boost (dB)							
		P4	P5	P3 P6	P1 P9	P2	P0 P8	P7	P10
Redriver CTLE Index	Redriver CTLE Boost (dB)	0.00	1.90	2.50	3.50	4.40	6.00	8.00	9.50
0	**-0.8**	-0.8	1.1	1.7	2.7	3.6	5.2	7.2	8.7
1	**1.3**	1.3	3.2	3.8	4.8	5.7	7.3	9.3	10.8
2	**5.7**	5.7	7.6	8.2	9.2	10.1	11.7	13.7	15.2
3	**7.1**	7.1	9.0	9.6	10.6	11.5	13.1	15.1	16.6
4	**8.4**	8.4	10.3	10.9	11.9	12.8	14.4	16.4	17.9
5	**9.1**	9.1	11.0	11.6	12.6	13.5	15.1	17.1	18.6
6	**9.8**	9.8	11.7	12.3	13.3	14.2	15.8	17.8	19.3
7	**10.7**	10.7	12.6	13.2	14.2	15.1	16.7	18.7	20.2
8	**11.3**	11.3	13.2	13.8	14.8	15.7	17.3	19.3	20.8
9	**12.6**	12.6	14.5	15.1	16.1	17.0	18.6	20.6	22.1
10	**13.6**	13.6	15.5	16.1	17.1	18.0	19.6	21.6	23.1
11	**14.4**	14.4	16.3	16.9	17.9	18.8	20.4	22.4	23.9
12	**15.0**	15.0	16.9	17.5	18.5	19.4	21.0	23.0	24.5
13	**15.9**	15.9	17.8	18.4	19.4	20.3	21.9	23.9	25.4
14	**16.5**	16.5	18.4	19.0	20.0	20.9	22.5	24.5	26.0
15	**17.8**	17.8	19.7	20.3	21.3	22.2	23.8	25.8	27.3

Downstream Pre-Channel Loss: -24.5 dB

PCIe TX Presets		PCIe TX EQ Boost (dB)							
		P4	P5	P3 P6	P1 P9	P2	P0 P8	P7	P10
Redriver CTLE Index	Redriver CTLE Boost (dB)	0.00	1.90	2.50	3.50	4.40	6.00	8.00	9.50
0	**-0.8**	-0.8	1.1	1.7	2.7	3.6	5.2	7.2	8.7
1	**1.3**	1.3	3.2	3.8	4.8	5.7	7.3	9.3	10.8
2	**5.7**	5.7	7.6	8.2	9.2	10.1	11.7	13.7	15.2
3	**7.1**	7.1	9.0	9.6	10.6	11.5	13.1	15.1	16.6
4	**8.4**	8.4	10.3	10.9	11.9	12.8	14.4	16.4	17.9
5	**9.1**	9.1	11.0	11.6	12.6	13.5	15.1	17.1	18.6
6	**9.8**	9.8	11.7	12.3	13.3	14.2	15.8	17.8	19.3
7	**10.7**	10.7	12.6	13.2	14.2	15.1	16.7	18.7	20.2
8	**11.3**	11.3	13.2	13.8	14.8	15.7	17.3	19.3	20.8
9	**12.6**	12.6	14.5	15.1	16.1	17.0	18.6	20.6	22.1
10	**13.6**	13.6	15.5	16.1	17.1	18.0	19.6	21.6	23.1
11	**14.4**	14.4	16.3	16.9	17.9	18.8	20.4	22.4	23.9
12	**15.0**	15.0	16.9	17.5	18.5	19.4	21.0	23.0	24.5
13	**15.9**	15.9	17.8	18.4	19.4	20.3	21.9	23.9	25.4
14	**16.5**	16.5	18.4	19.0	20.0	20.9	22.5	24.5	26.0
15	**17.8**	17.8	19.7	20.3	21.3	22.2	23.8	25.8	27.3

Upstream Pre-Channel Loss: -20.5 dB

Figure 6-2. Possible Redriver CTLE Settings for the Downstream and Upstream Pre-Channels

4. Verify the optimal CTLE settings for the downstream redrivers. Sweep the CTLE settings of the downstream redrivers while keeping the upstream redrivers with the CTLE Index 15 setting. The downstream redriver settings are stepped down from the starting setting of Index 15. At each step, the link training was restarted and then the system checked if a successful PCIe 4.0 x16 link up was established. For this example, it was determined that the CTLE settings ranging from Index 10 to Index 15 yielded successful PCIe 4.0 x16 link ups. The wide range of the downstream redriver CTLE settings that allow a successful link up indicate a strong performance of the endpoint PCIe receivers.
5. Verify the optimal CTLE settings for the upstream redrivers. Sweep the CTLE settings of the upstream redrivers while keeping the downstream redrivers with the optimal CTLE Index 15. The upstream redriver settings are stepped up and down from the starting setting of Index 15. At each step, the link training was restarted and then the system checked if a successful PCIe 4.0 x16 link up was established. For this example, it was determined that the CTLE settings ranging from Index 13 to Index 15 yielded successful PCIe 4.0 x16 link ups.

7 Summary

In this application report, key signal conditioning features of the DS160PR410 PCIe 4.0 linear redriver are reviewed in detail. In addition, relevant validation and system level test results are reviewed and used for mapping the maximum reach of PCIe links with redrivers and suggesting optimal redriver placement. Step-by-step redriver tuning instructions using a real system example are also provided. With a complete understanding of the redriver capabilities, limitations, and redriver tuning steps, system designers are better equipped to extend the reach of PCIe 4.0 links using linear redrivers.

8 References

1. Texas Instruments, *DS160PR410 Quad Channel PCI Express 4.0 Linear Redriver Data Sheet*
2. Texas Instruments, *DS160PR410 Programming Guide*
3. Texas Instruments, *Understanding EEPROM Programming for DS160PR410 PCI-Express Gen-4 Redriver Application Report*
4. Intel, *PCI Express 4.0 Linear Re-Driver Characterization Methodology*, Revision 1.0, January 2019
5. PCI-SIG, *PCI Express Base Specification*, Revision 4.0 Version 1.0, September 27, 2017

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2020) to Revision A (July 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	2

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