Application Note

DP83TC81x, DP83TG72x Software Implementation Guide

Gerome Cacho *High-Speed Data - Ethernet*

ABSTRACT

Texas Instruments' 100Base-T1 (DP83TC811, DP83TC812) and 1000Base-T1 (DP83TG720) Automotive Ethernet physical layers (PHYs) are designed such that same PCB board can be used for either transceiver. While the hardware changes needed to make the swap are listed in the *DP83TC811, DP83TG720 Rollover Document* application note, there are also necessarily changes to be accounted for in software. This application note acts as a reference guide to point out the appropriate timing flowchart for these devices and distinguish between the necessary timing specifications of each device.

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Trademarks

1 Introduction

Ethernet PHYs have their own timing requirements as dictated in their respective data sheets. It is important that these requirements are met from a power supply standpoint to be able to supply the PHY appropriately as well as from a microcontroller standpoint to know exactly when a PHY is available for normal communication as well as register access for any programming needs for the system. Also, each PHY has an optimized register configuration which is loaded after the power-up sequence is complete.

Even after the PHY is configured and linked-up with the remote link partner, systems can choose to continue with status or health checks of the link using various PHY registers. Details of the required sequence to control and poll the PHY is described in this document.

2 PHY Link-up Sequence

The flowchart in Figure 2-1 shows a high-level summary of the steps needed for a PHY to link up from power-up. The 'A' reference in Figure 2-1 comes from Figure 2-6.

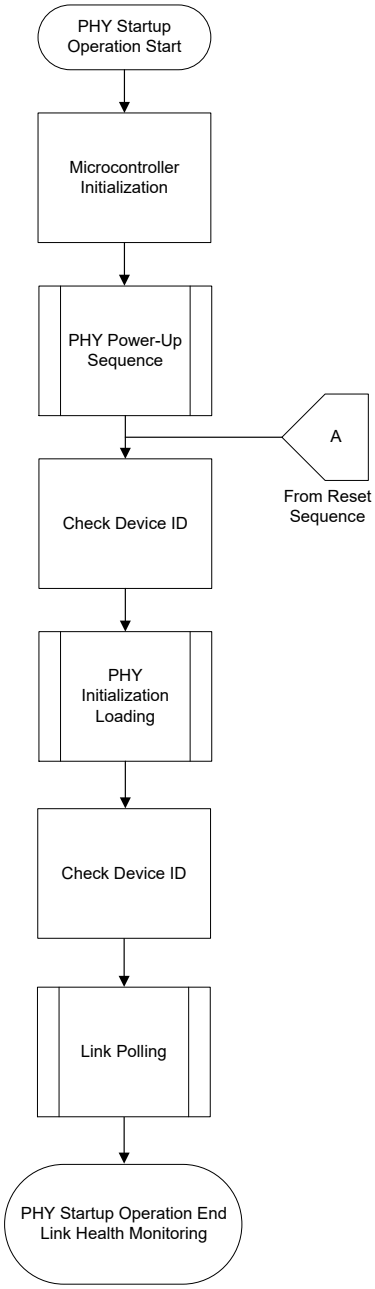

Figure 2-1. Overall Flowchart

2.1 Microcontroller Initialization

The microcontroller assists in initializing itself with regards to the PHY system by configuring:

- MDC and MDIO pins for register access
- Any pins that control PHY states (Wake, Reset, EN) according to the application
- Any shared PHY pins also controlled by the MCU (that is, strapping pins) to Hi-Z to avoid the PHY sampling unintended strap voltages

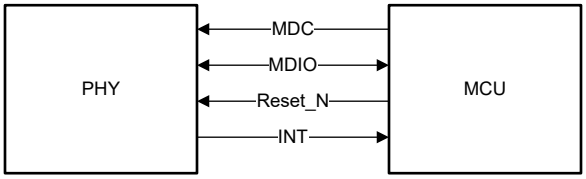

Figure 2-2. Connections Between MCU and PHY

2.2 Power-up Sequence

The PHY begins to go through the power-up sequence. The MCU should still hold control and strap pins in the same states as during initialization.

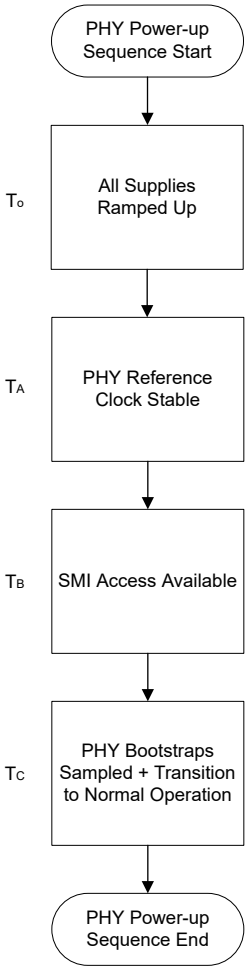

Figure 2-3. Power-up Sequence Flowchart

2.2.1 All Supplies Ramped

All pertinent supplies pertaining to the PHY should be high at this point. Keep in mind the ramp rates and times as specified in data sheet. The point in time where all supplies are at desired voltages is known as T_0.

2.2.2 PHY Clock Required Good

At T_A (relative to T_0), the PHY should have a stable clock signal. The clock signal is either supplied by a crystal, for which XI and XO pins are used, or through an oscillator where XI is only used. If using an oscillator, the amplitude follows the VDDIO rail.

	811	720	812
T_A (ms)	40	20	10

2.2.3 SMI Access Available

At T_B (relative to T_0), the PHY is able to be accessible via SMI access. MDC and MDIO are used for this communication.

	811	720	812
T_B (ms)	60	60	60

Figure 2-4 shows the MDC and MDIO timing diagram. The pairs are separated as the write timing diagram is above the read diagram. Within the pairs, MDC is above MDIO. Please be aware that some PHYs can require 32 bits of preamble for the synchronization purposes.

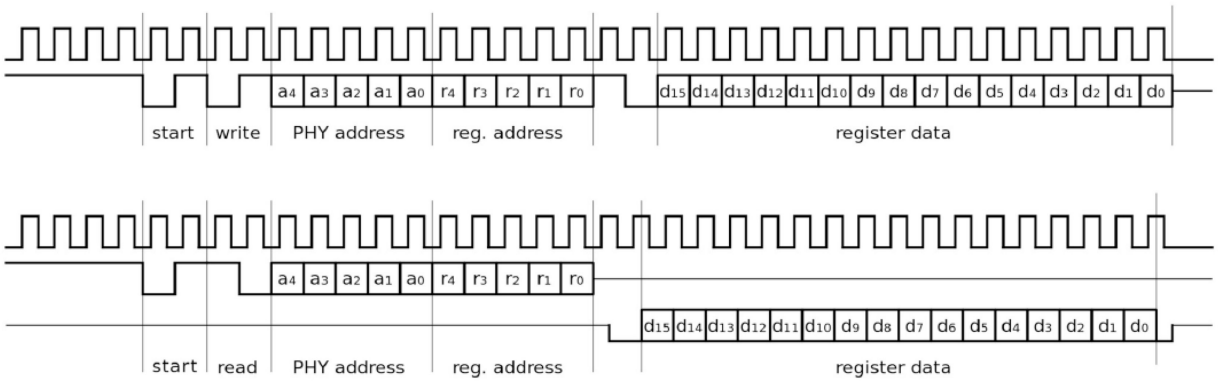

Figure 2-4. SMI Timing

2.2.4 PHY Bootstraps Sampled

At T_C (relative to T_0), the PHY samples the bootstraps to determine initial modes in which to power up. Since a number of the PHY pins are bootstrap pins, it is important that MCUs do not alter the voltages at these pins at this time or else the PHY does not sample properly. The desired voltages are set in hardware through a series of voltage divider circuits or internal pullup or pulldown resistors.

	811	720	812
T_C (ms)	60	60	10

An example is a MII pin which also functions as a strap pin. If the Media Access Control (MAC) were to begin sending packets during strapping, the pin can be driven by the MCU instead of by the strap network and therefore the PHY can sample an unintended voltage depending on where in the waveform the PHY begins to

sample. This is more consequential in multilevel straps where the voltage ranges per mode are smaller. After sampling, the pins transition to their normal operation shortly after. MAC and MCU proper functions for these pins can occur after this transition.

2.3 Check Device ID

The microcontroller checks the PHY ID to confirm the MCU is communicating with the appropriate device. This is done by reading registers 0x2 and 0x3 to check the vendor and specific PHY ID. Reading correct values can indicate the PHY has been powered up correctly and communication via SMI has been established.

2.4 PHY Initialization

At this point, the PHY has been powered up and functions properly. The next step is to load any needed application-specific initial configurations of the PHY. Examples of how to initialize TI's automotive PHYs are found in the sections on *software configuration* in the *DP83TG720: Configuring for Open Alliance Specification Compliance*, *DP83TC812, DP83TC813, and DP83TC814: Configuring for Open Alliance Specification Compliance*, and DP83TC811: Configuring for Open Alliance Specification Compliance. See the flowchart in Figure 2-5 for the proper method to initialize a PHY.

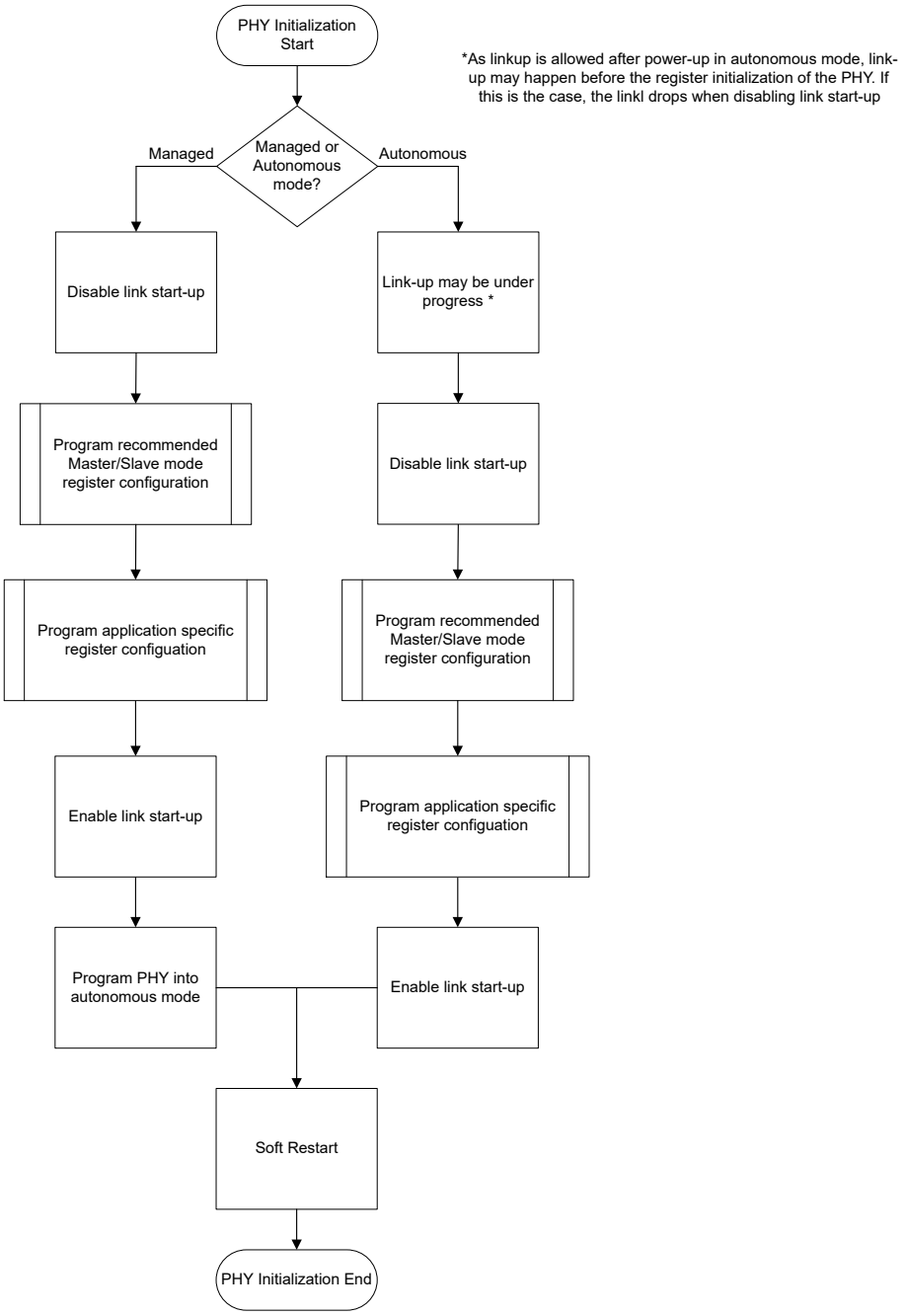

Figure 2-5. PHY Initialization Flowchart

2.4.1 Managed or Autonomous Mode?

Depending on the strapping settings, the PHY is either in autonomous or managed mode upon power up. Compared to managed mode, if a PHY is in autonomous mode, it is possible that the PHY links up with the link partner. To configure the PHY appropriately, the linkup must be disabled.

2.4.2 Program PHY Configuration Settings, Enable Link Start-up

Configure any application-specific settings required of the PHY. This can be as simple as modifying RGMII clock delays to an entire recipe of MDI modifications. After these instructions have been programmed into the PHY, the final step in initialization is enabling link start-up.

2.4.3 Program PHY Into Autonomous Mode

If the PHY was strapped into managed mode, configure the PHY to be in autonomous mode. If autonomous mode is strapped, no action is needed here.

2.4.4 Soft Restart or Polling for Link

Command the PHY to soft restart (0x1F = 0x4000) once initialization settings are loaded. This makes sure that the PHY restarts while not wiping register settings. Once the restart is complete, the MCU checks for PHY linkup by reading register 0x1[2].

2.4.5 Results of Link Polling

Make sure the automotive Ethernet cable is connected accordingly between the PHY system and Link Partner system. If the PHY is properly linked up, then the MAC can begin sending packets through. If not, the MCU continues to poll the PHY for the link status until a proper link is established. If this polling continues for 100ms and the link is still not established, the MCU commands the PHY to soft restart once more and repeat the polling process.

2.5 Post Start-up Operation

At this point in the sequence, the PHY should be configured and linked up with the link partner. Therefore, the PHY is ready to complete data transmission. However, periodically poll the link bit to verify that the link is still established. This bit is a latch low bit, indicating that if the PHY lost link at any point between polls, the lost link result is kept for a single register read.

Another periodic action the MCU takes post start-up is to check the quality of the link via the Signal Quality Indicator (SQI). Section 6 in the respective Open Alliance Configuration application note of the PHY has details on registers to read to extract the link health. If the SQI begins to drop from *excellent* to *bad* or *good*, corrective action can be taken depending on the application.

2.6 Reset Sequence

The PHY begins to go through the reset sequence once the reset command is issued via pulling the Reset pin low for some time and releasing, or via register access (0x1F = 0x8000). The MCU should still hold control and strap pins in same states as during MCU initialization.

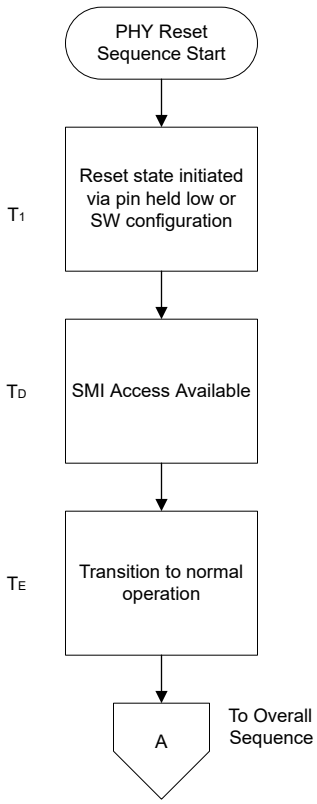

Figure 2-6. Reset Sequence Flowchart

2.6.1 Reset Initiated

The PHY is sent into the reset state. This can be done in two ways, via hardware where the Reset pin is held low for F duration, or via software where register 0x1F[15] = '1'. The point in time when either the Reset pin is released, or the write command has been delivered to the PHY is known as T_1. While these procedures do initiate a reset of the PHY, issuing the reset via pin toggling causes the PHY to sample the bootstraps while issuing a via register write does not cause resampling.

	811	720	812
Reset pin held low to initiate (µs)	1	65	0.72

2.6.2 SMI Access Available

At T_D (relative to T_1), the PHY is able to be accessible via Station Management Tool (SMI) access. MDC and MDIO are used for this communication.

	811	720	812
T_D (µs)	2.5	1000	1000

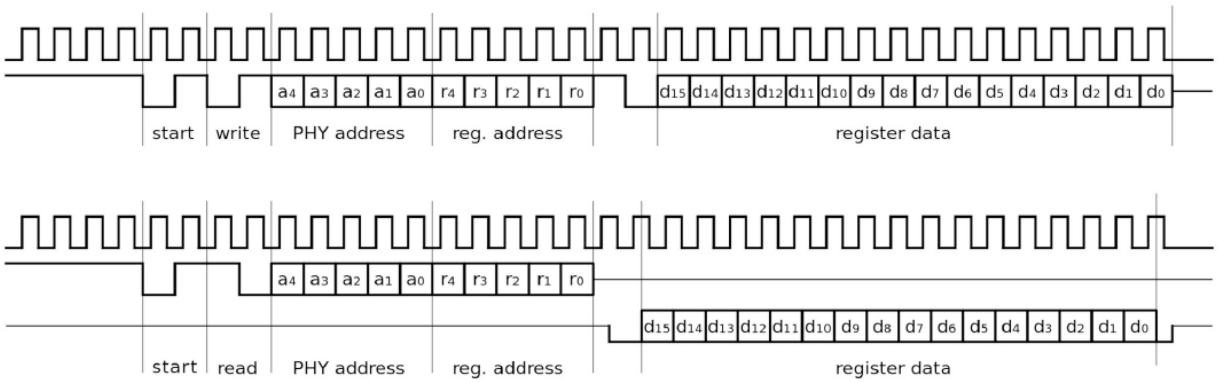

Figure 2-7. SMI Timing

2.6.3 Transition to Normal Operation

The PHY transitions to normal operation from the reset state. Depending on the method used to initiate reset, the PHY can sample the bootstraps. If this is the case, at T_E (relative to T_1), the PHY samples the bootstraps to determine initial modes in which to power up. Since a number of pins of the PHY are bootstrap pins, it is important that MCUs do not alter the voltages at this time or else the PHY does not sample properly. The desired voltages are set in hardware through a series of voltage divider circuits or internal pullup or pulldown resistors.

	811	720	812
T_E (µs)	0.7	2	40

An example is a MII pin which also functions as a strap pin. If the MAC were to begin sending packets during strapping, the pin is driven by the MCU instead of by the strap network; therefore, the PHY can sample an unintended voltage depending on where in the waveform the PHY begins to sample. This is more consequential in multilevel straps where the voltage ranges per mode are smaller. After sampling, the pins transition to their normal operation shortly after. MAC and MCU proper functions for these pins can occur after this transition.

3 Summary

This application note discussed the differences between the Ethernet PHYs catalogs. Details were presented how these differences can be accommodated by slightly modifying timing parameters to meet the appropriate timing power up and reset requirements of the device.

A Appendix

Figure A-1 shows the main flowchart. The 'A' reference in Figure 2-1 comes from Figure 2-6.

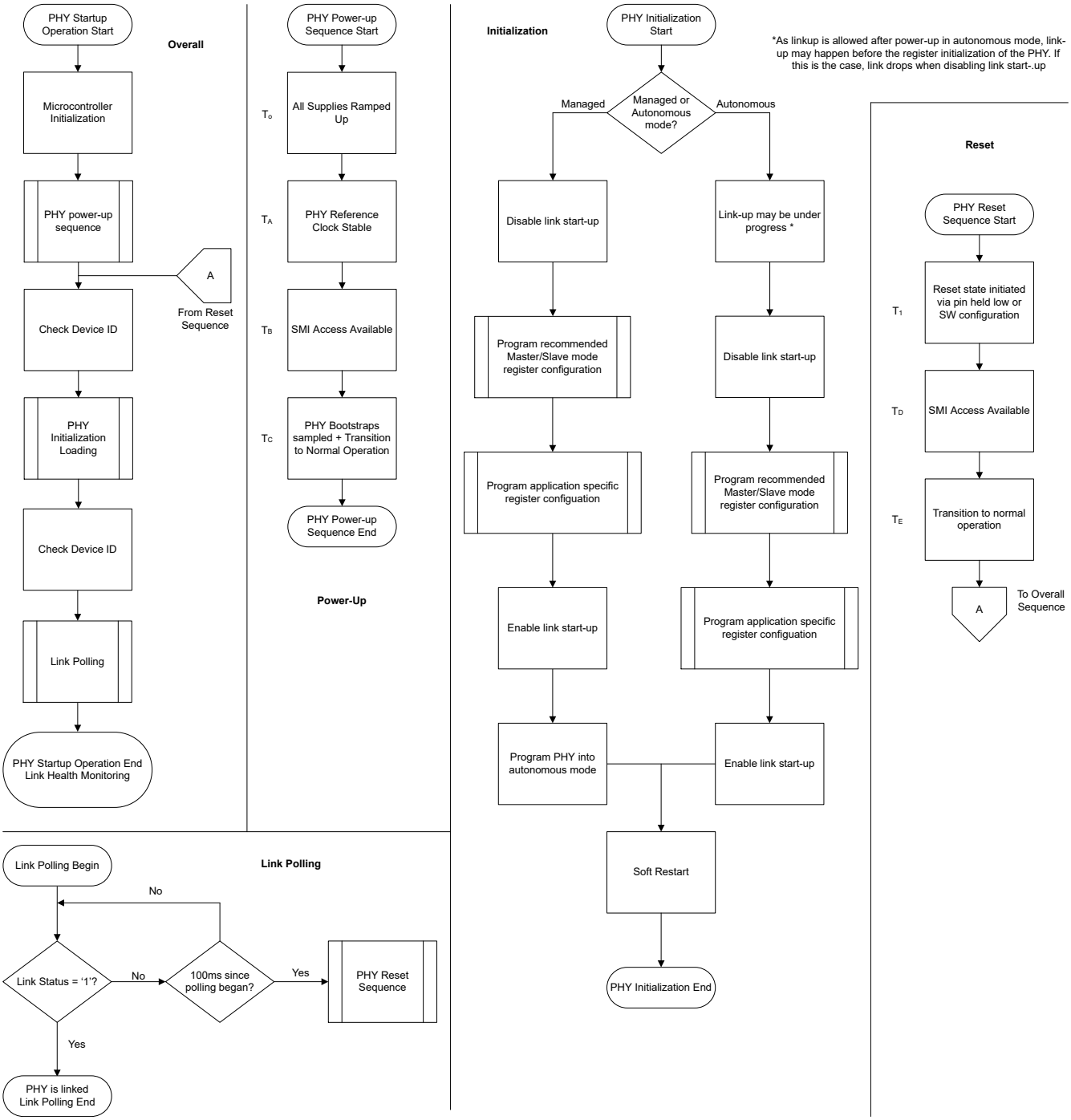

Figure A-1. Main Flowchart

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