Application Note

How and When to Use Ethernet PHYs in PROFINET Systems

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ABSTRACT

This document describes how to select and use TI's Ethernet PHYs in a PROFINET® system. Example PHYs mentioned in this document are the: DP83822, DP83826, DP83867, and DP83869.

Using our PHYs provide a cost effective and reliable option for real-time Ethernet use in an industrial automation system using PROFINET®.

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1 Introduction

PROFINET® is an open real-time communication protocol designed to exchange data between controllers and devices in an automation setting using industrial Ethernet. More detailed information about PROFINET® can be found in PROFINET® System Description. This document goes over the Ethernet PHY requirements and provides a few options, with their configurations, for immediate use in a PROFINET® system. Ethernet PHYs are only one component in a PROFINET® system, Texas Instruments also provides processors that function with PROFINET® , please refer to *PROFINET® on TI's Sitara™ Processors*.

2 PROFINET Specification Requirements

An Ethernet PHY which supports PROFINET® requirements must be compliant to the IEEE802.3 standard and must fulfill all the required functionality.

The standard functionality are listed in Table 2-1.

Table 2-1. PROFINET Requirements

Feature	Description
MAC Interface	MII (mandatory)
	RGMII/RMII (optional)
Speed	100Base-TX (mandatory)
	1000Base-T (optional)
	100Base-FX (optional)
	1000Base-X (optional)
MDI/MDIX	Auto-Negotiation
	Manual Setting
Serial Management Interface (MDIO) as defined by IEEE 802.3 Clause 45	Power Down Mode with MDIO interface running is required
LED indication support	Manual control (by software) is required

Note

- For PROFINET® Isochronous real-time applications, auto-negotiation might need to be disabled and speed, MDI/X, and Full Duplex operation to be configured manually.
- Items marked as optional are application specific.

3 Ethernet PHY Setup

Our Ethernet PHYs can be set up through software register reads or hardware bootstraps. The following sections describe how to configure the PHYs using both methods.

3.1 DP83822

The DP83822 is an ultra-robust, low-power single-port 10/100 Mbps Ethernet PHY. Both 100Base-TX and 100Base-FX are supported. DP83822 has gone through *Cable Break Tests* to validate how link loss is indicated in a timely manner. More information can be found in *DP83822 Cable Break Test for Profinet Compliance*.

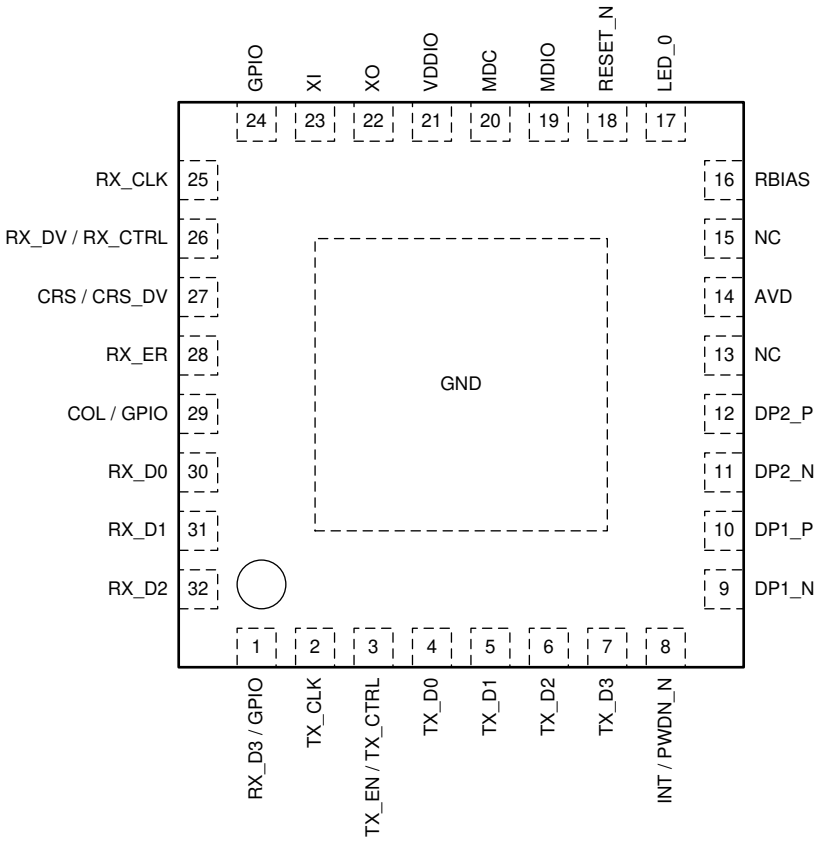

Figure 3-1. DP83822 RHB Package 32-Pin VQFN Top View

3.1.1 DP83822 Hardware Bootstrap Configurations

The DP83822 uses certain pins as bootstrap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hardware reset, providing a way to configure the device into a desired mode without the need for software configuration.

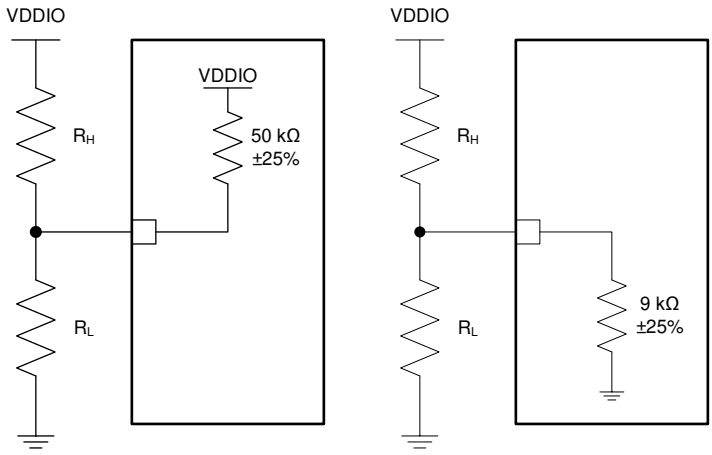

Figure 3-2. Bootstrap Circuit

Note

The 50 kΩ and 9 kΩ resistors are internal pull-up and pull-down resistors, respectively.

Table 3-1. DP83822 100Base-TX Strapping

DP83822 100Base-TX Strapping	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
PHY Address: 1, MAC Interface: MII, 10/100 Mbps Full Duplex Advertised, Copper, Auto-negotiation Enabled, Auto-MDIX Enabled, FLD Enabled,	COL	Open	Open	Copper PHY_ADD0[1]
	RX_D0	Open	Open	PHY_ADD1[0]
	RX_D1	Open	Open	EEE disable PHY_ADD2[0]
	RX_D2	10	2.49	FLD Enabled PHY_ADD3[0]
	RX_D3	Open	Open	Auto-Negotiation Enabled
	LED_0	Open	Open	Advertised Full Duplex 10Base-Te/100Base-TX
	LED_1	Open	Open	No Added Functionality Do not use Mode 2 & 3
	RX_ER	Open	Open	MII Auto-MDIX Enable
	RX_DV	Open	Open	MII

Table 3-2. DP83822 100Base-FX Strapping

DP83822 100Base-FX Strapping	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
PHY Address: 1, MAC Interface: MII, 10/100 Mbps Full Duplex Advertised, Fiber, Auto-negotiation Enabled, Auto-MDIX Enabled, FLD Enabled,	COL	13	1.96	Fiber Enabled PHY_ADD0[1]
	RX_D0	Open	Open	PHY_ADD1[0]
	RX_D1	Open	Open	EEE disable PHY_ADD2[0]
	RX_D2	10	2.49	FLD Enabled PHY_ADD3[0]
	RX_D3	Open	Open	Auto-Negotiation Enabled
	LED_0	Open	Open	Advertised Full Duplex 10Base-Te/100Base-FX
	LED_1	Open	Open	No Added Functionality Do not use Mode 2 & 3
	RX_ER	Open	Open	MII Auto-MDIX Enable
	RX_DV	Open	Open	MII

Note

PHY_ADD[0..3] determine the PHY's Address. In Table 3-1 and Table 3-2, PHY Address is set to 0b0001.

3.1.2 DP83822 Register Configuration

If hardware bootstraps are not sufficient, our Ethernet PHYs can be configured through Register Writes, which can change the PHYs mode, regardless of how the Bootstraps are configured.

Table 3-3. DP83822 Software Configuration

Register Address	Write Value	Remarks
0000	3100	Auto-Negotiation and Full Duplex Enabled. For 100Mbps Forced Mode write '2100'
0004	0101	De-advertise 10BaseTe and Half Duplex modes of operation
000A	See Remark	For Copper, write '0080' For Fiber write '4080'
000B	100F	FLD Enabled Last nibble 'F' sets Fast Link Drop Functionality Details can be found in Data Sheet, search for '0x000B'
001F	4000	Soft Reset PHY

3.2 DP83826

The DP83826 offers low and deterministic latency, low power, and supports 10BASE-Te/100BASE-TX Ethernet protocols to meet stringent requirements in real-time industrial Ethernet systems.

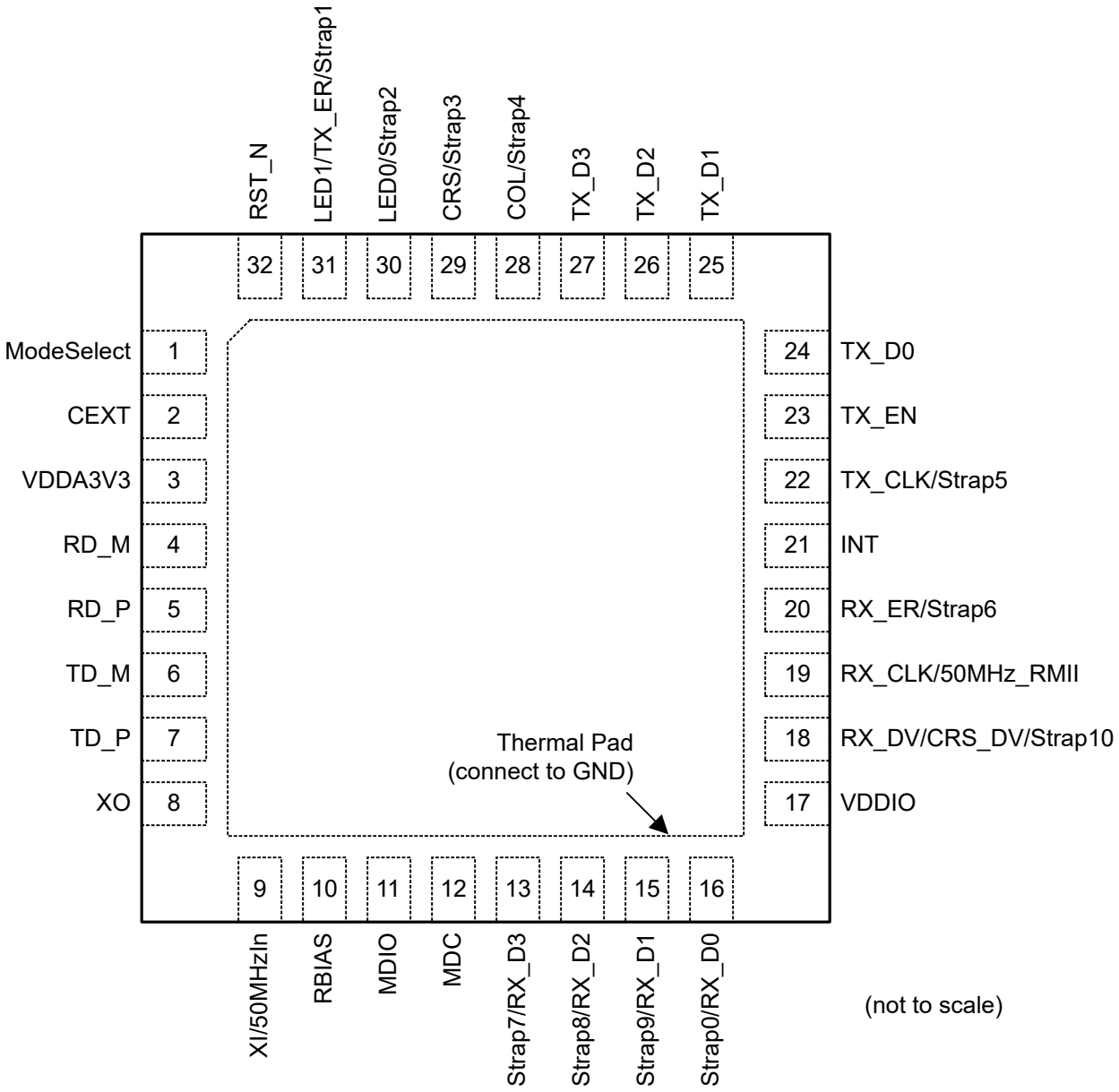

Figure 3-3. DP83826 RHB Package 32-Pin QFN (Top View)

3.2.1 DP83826 Hardware Bootstrap Configuration

DP83826 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset.

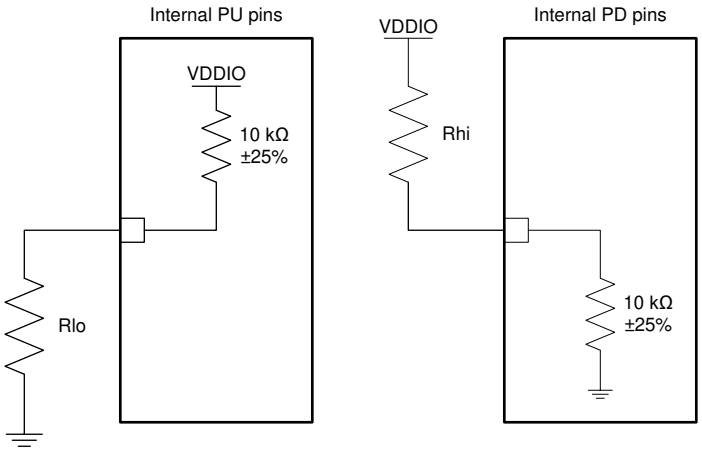

Figure 3-4. Strap Circuit

Table 3-4. DP83826 100Base-TX

DP83826 100Base-TX Strapping	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
Enhanced Mode, MAC Inteface: MII, 10/100 Full Duplex, Auto-Negotiation Enabled, Auto-MDIX Enabled, FLD Enabled,	Mode Select	2.49	Open	Enhanced Mode
	RX_D0	Open	Open	Auto-negotiation Enabled
	RX_D1	Open	Open	Auto MDI-X Enable
	RX_D2	Open	Open	MII
	RX_D3	2.49	Open	FLD Enable

3.2.2 DP83826 Register Configuration

If hardware bootstraps are not sufficient, our Ethernet PHYs can be configured via Register Writes, which can change the PHYs mode, regardless of how the Bootstraps are configured.

Table 3-5. DP83826 Software Configuration

Register Address	Write Value	Remarks
0000	3100	Auto-negotiation enabled, Full Duplex Mode. For Forced 100Mbps write 2100
0004	0101	De-advertise 10Base-T and Half Duplex modes
000B	000F	FLD Enabled Last nibble F sets Fast Link Drop Functionality Details can be found in Data Sheet, search for "Offset = Bh"
0017	0041	This is the default state, Enable MII mode of Operation. For RMII, write 0061
0019	8000	This is the default state, Auto MDI/X enable. For forced MDI or MDIX, write 0000 or 4000 respectively
001F	4000	Soft Reset PHY

3.3 DP83867

The DP83867 device is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols.

Note

MII Interface is not supported

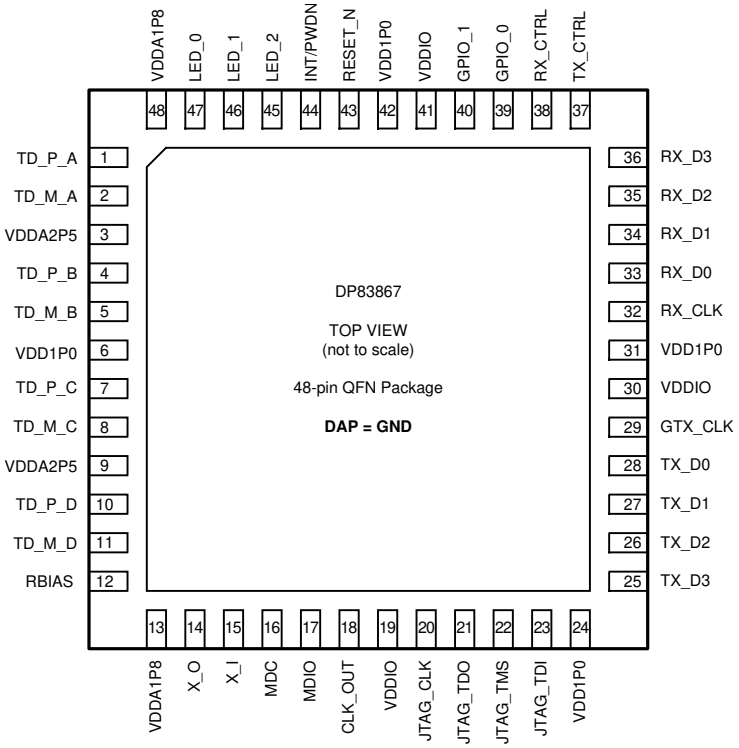

Figure 3-5. RGZ Package 48-Pin VQFN Top View

3.3.1 DP83867 Hardware Bootstrap Configurations

The DP83867 uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset. During software resets, the strap options are internally reloaded from the values sampled at power up or hard reset.

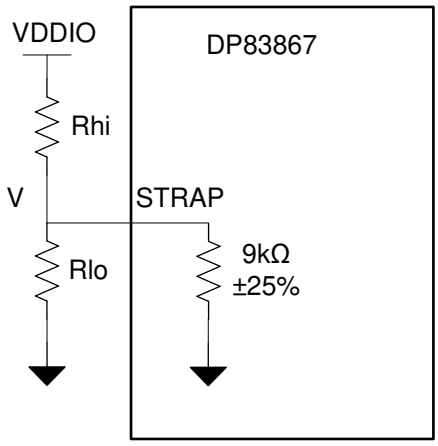

Figure 3-6. Strap Circuit

Table 3-6. DP83867 100Base-TX Strapping

DP83867 100Base-TX/ 1000Base-T	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
MAC Interface: RGMII, 100Base-TX/1000Base-X, Auto-Negotiation Enabled	RX_CTRL	5.76	2.49	Autoneg enable
	GPIO_0	Open	Open	RGMII TX/RX Clock Skew set to default value (2.0 ns) Advertise 100/1000 speed only
	GPIO_1	Open	Open	
	LED_2	Open	Open	
	LED_1	2.49	Open	
	LED_0	Open	Open	SGMII Disable Mirror Mode Disable

3.3.2 DP83867 Register Configuration

If hardware bootstraps are not sufficient, our Ethernet PHYs can be configured via Register Writes, which can change the PHYs mode, regardless of how the Bootstraps are configured.

Table 3-7. DP83867 Software Configuration

Register Address	Write Value	Remarks
0000	1140	Auto-negotiation enabled, Full Duplex Mode, For Forced 100Mbps write 2100 For Forced 1000Mbps write 2140, Note: Not recommended
0004	0181	De-advertise 10Base-Te
0009	0200	De-advertise Half-Duplex for 1000Base-T
0010	5048	SGMII disabled Auto MDI-X enable
002D	401F	FLD Enable Last nibble F sets Fast Link Drop Functionality Details can be found in Data Sheet, search for 0x002D
0032	00D3	RGMII Enable
001F	4000	Soft Reset PHY

3.4 DP83869

The DP83869HM device is a robust, fully-featured gigabit physical layer (PHY) transceiver with integrated PMD sublayers that supports 10BASE-Te, 100BASE-TX and 1000BASE-T Ethernet protocols. The DP83869 also supports 1000BASE-X and 100BASE-FX fiber protocols. More information about the functional modes offered by the DP83869, and how to configure them, can be found in *Understanding Different Modes of Operation in DP83869*.

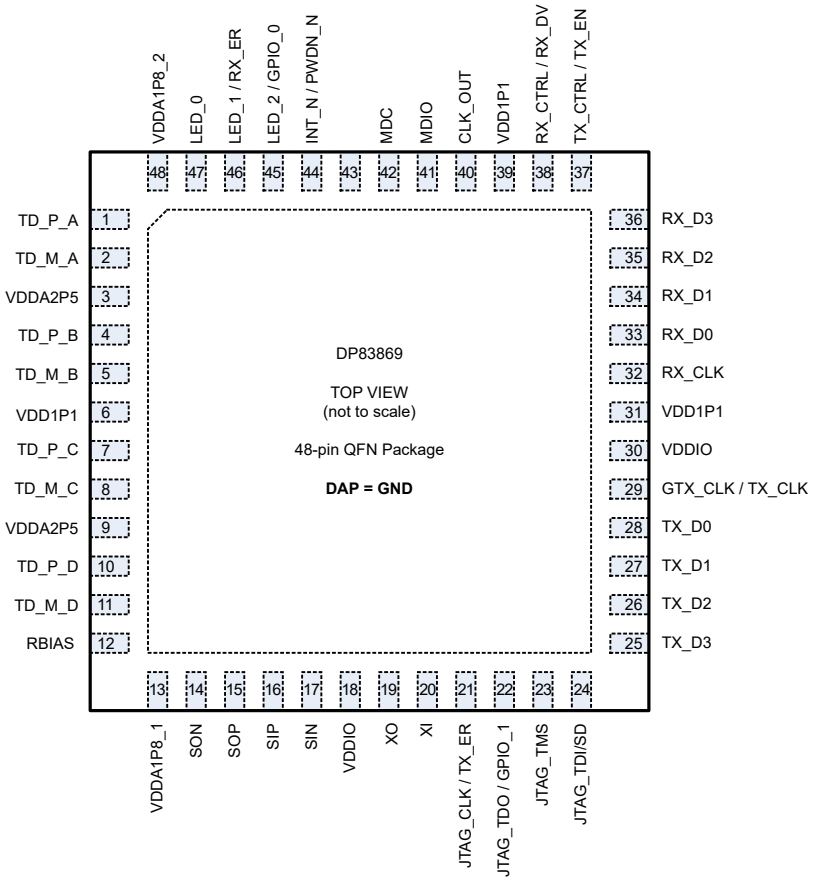

Figure 3-7. RGZ Package (48-Pin VQFN) Top View

3.4.1 DP83869 Hardware Bootstrap Configurations

The DP83869HM uses many of the functional pins as strap options to place the device into specific modes of operation. The values of these pins are sampled at power up or hard reset.

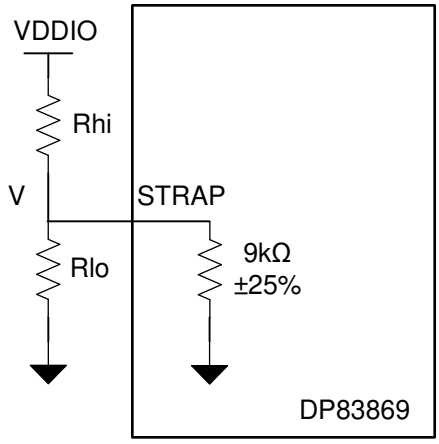

Figure 3-8. Strap Circuit

The bootstrap selection for the DP83869 is mainly controlled by three pins: JTAG_TDO/GPIO_1, RX_D3, and RX_D2. These pins represent bits for OPMODE[0..2], the table below summarizes the different functional modes that can be selected using these pins.

Note

DP83869 cannot be strapped into MII Mode.

MII Mode only works for 100Base-TX/100Base-FX and must be configured via Register Writes by de-advertising gigabit capabilities.

Table 3-8. Functional Mode Strap Table

PIN NAME	STRAP NAME	PIN #	DEFAULT	OPMODE[2]	OPMODE[1]	OPMODE[0]	FUNCTIONAL MODES
JTAG_TDO/ GPIO_1	OPMODE[0]	22	0	0	0	0	RGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				0	0	1	RGMII to 1000Base-X
RX_D3	OPMODE[1]	36	0	0	1	0	RGMII to 100Base-FX
				0	1	1	RGMII-SGMII Bridge Mode
RX_D2	OPMODE[2]	35	0	1	0	0	1000Base-T to 1000Base-X
				1	0	1	100Base-T to 100Base-FX
				1	1	0	SGMII to Copper (1000Base-T/ 100Base-TX/10Base-Te)
				1	1	1	JTAG for boundary scan

Table 3-9. DP83869 100/1000 Copper Bootstrap Selection

DP83869 100Base-TX/ 1000Base-T	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
MAC Interface: RGMII, 100Base-TX/1000Base-T, Full Duplex, Auto_MDIX, Auto-Negotiation,	JTAG_TDO	Open	2.49	OPMODE: 000 RGMII to Copper, 1000Base-T/100Base-TX/ 10base-Te
	RX_D3	Open	2.49	
	RX_D2	Open	2.49	
	LED_0	Open	2.49	Auto-negotiation, 10M speed disable, Auto MDI-X
	LED_1	2.49	Open	
	LED_2	Open	2.49	
	RX_CTRL	Open	2.49	Port Mirroring Disabled

Table 3-10. DP83869 1000Base-X Fiber Bootstrap Selection

DP83869 1000Base-X	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
MAC Interface: RGMII, 1000Base-X, Full Duplex, Auto_MDIX, Auto-Negotiation,	JTAG_TDO	2.49	Open	OPMODE: 001 RGMII to 1000Base-X
	RX_D3	Open	2.49	
	RX_D2	Open	2.49	
	LED_0	Open	2.49	Fiber Auto-negotiation enabled
	LED_1	2.49	Open	Signal Detect Pin enabled

Table 3-11. DP83869 100Base-FX Fiber Bootstrap Selection

DP83869 100Base-FX	Pin	$R_{H(k\Omega)}$	$R_{L(k\Omega)}$	Remarks
MAC Interface: RGMII, 100Base-FX, Full Duplex,	JTAG_TDO	Open	2.49	OPMODE: 010 RGMII to 100Base-FX
	RX_D3	2.49	Open	
	RX_D2	Open	2.49	
	LED_1	2.49	Open	Signal Detect Pin enabled

3.4.2 DP83869 Register Configuration

If hardware bootstraps are not sufficient, our Ethernet PHYs can be configured via Register Writes, which can change the PHYs mode, regardless of how the Bootstraps are configured.

As mentioned in the bootstrap section, the DP83869 cannot be configured into MII mode with Bootstraps alone, register writes are required.

Table 3-12. DP83869 RGMII Software Configuration

Register Address	Write Value	Remarks
01DF	See Remark	OP_MODE_DECODE: RGMII to Copper write: 0000 RGMII to 1000Base-X: 0001 RGMII to 100Base-FX: 0002
0000	1140	Auto-negotiation enabled, Full Duplex Mode, For Forced 100Mbps write 2100 For Forced 1000Mbps write 2140, Note: Not recommended
0004	0101	De-advertise 10Base-T and Half Duplex 100Base-Tx
0009	0200	De-advertise Half-Duplex for 1000Base-T
0010	5048	Auto MDI-X enable
002D	801F	FLD Enable Last nibble 'F' sets Fast Link Drop Functionality Details can be found in Data Sheet, search for "Offset = 2Dh"
001F	4000	Soft Reset PHY

Table 3-13. DP83869 MII Software Configuration

Register Address	Write Value	Remarks
01DF	See Remark	OP_MODE_DECODE: MII to Copper write: 0060 MII to Fiber write: 0062
0000	1140	Auto-negotiation enabled, Full Duplex Mode, For Forced 100Mbps write 2100
0004	0101	De-advertise 10Base-T and Half Duplex 100Base-Tx
0009	0000	De-advertise 1000Base-T
0010	5048	Auto MDI-X enable
0018	000E	Required for MII Operation.
001F	4000	Soft Reset PHY

4 Summary

This application note serves as a guide to help determine if an Ethernet PHY is compliant with PROFINET's system requirements. Furthermore, this application note provides examples of Ethernet PHYs currently offered by Texas Instruments and how to configure them. These has low latency Ethernet PHYs that meet the requirements needed for use in a PROFINET system and have the ability to be configured through hardware bootstraps or software register writes.

5 References

1. *PROFINET System Description*
2. Texas Instruments, *PROFINET® on TI's ® processors*, user's guide
3. Texas Instruments, *DP83826 Deterministic, Low-Latency, Low-Power, 10/100 Mbps, Industrial Ethernet PHY*, data sheet.
4. Texas Instruments, *DP83822 Robust, Low Power 10/100 Mbps Ethernet Physical Layer Transceiver*, data sheet.
5. Texas Instruments, *DP83867E/IS/CS Robust, High Immunity, Small Form Factor 10/100/1000 Ethernet Physical Layer Transceiver*, data sheet.
6. Texas Instruments, *DP83869HM High Immunity 10/100/1000 Ethernet Physical Layer Transceiver With Copper and Fiber Interface*, data sheet.
7. Texas Instruments, *Understanding Different Modes of Operation in DP83869*, application note.
8. Texas Instruments, *DP83822 Cable Break Test for Profinet Compliance*, application note.

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