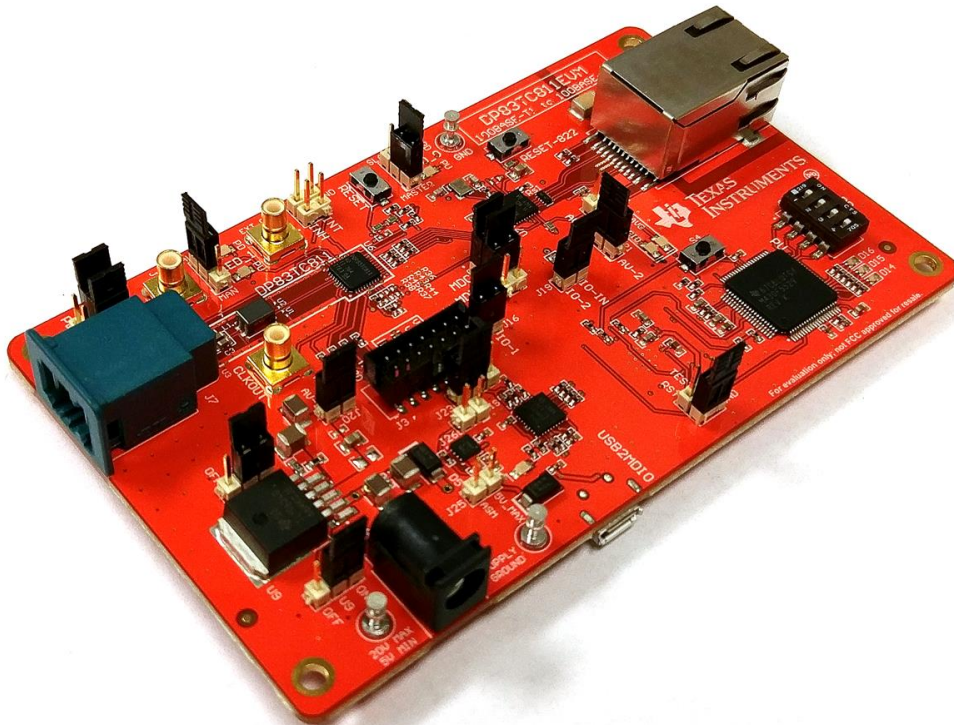


## ***DP83TC811EVM User's Guide***

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This User's Guide discusses how to properly operate and configure the DP83TC811EVM. For best layout practices, schematic files, and Bill of Materials, see the associated support documents.



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## Trademarks

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## 1 Definitions

**Table 1. Terminology**

ACRONYM	DEFINITION
PHY	Physical Layer Transceiver
MAC	Media Access Controller
SMI	Serial Management Interface
MDIO	Management Data I/O
MDC	Management Data Clock
RGMII	Reduced Gigabit Media Independent Interface
SFD	Start-of-Frame Detection
VDDA	Analog Core Supply Rail
VDDIO	Digital Supply Rail
PD	Pulldown
PU	Pullup

## 2 Introduction

The DP83TC811EVM supports 100-Mbps speed and is IEEE 802.3bw compliant. This evaluation board is a media converter to enable bit-error rate testing, interoperability testing and PMA compliance. There is an onboard MSP430F5529 for use with the USB-2-MDIO graphical user interface tool. A DP83822HF is provided for copper (100BASE-TX) support.

### 2.1 Key Features

- Media Converter: 100BASE-T1 to 100BASE-TX
- IEEE802.3bw Compliant
- IEEE802.3u Compliant
- RGMII Back-to-Back Configuration
- Onboard MSP430F5529
  - eZ-FET Debugger
  - USB-2-MDIO Support
  - 4-Pin Dip Switch
- Autonomous and Managed Mode Operation
- Status LEDs
  - DP83TC811
    - Link
    - Link + Activity
  - DP83822
    - Link
    - Multi-LED
  - Power
  - SMI Command
- Variable I/O Voltage Range: 1.8-V, 2.5-V, and 3.3-V
- 4-Level Bootstraps for Hardware Configuration
- 100BASE-T1 Error Free Data transfer Over 60 Meters
- 100BASE-TX Error Free Data Transfer Over 150 Meters on CAT5 Cable



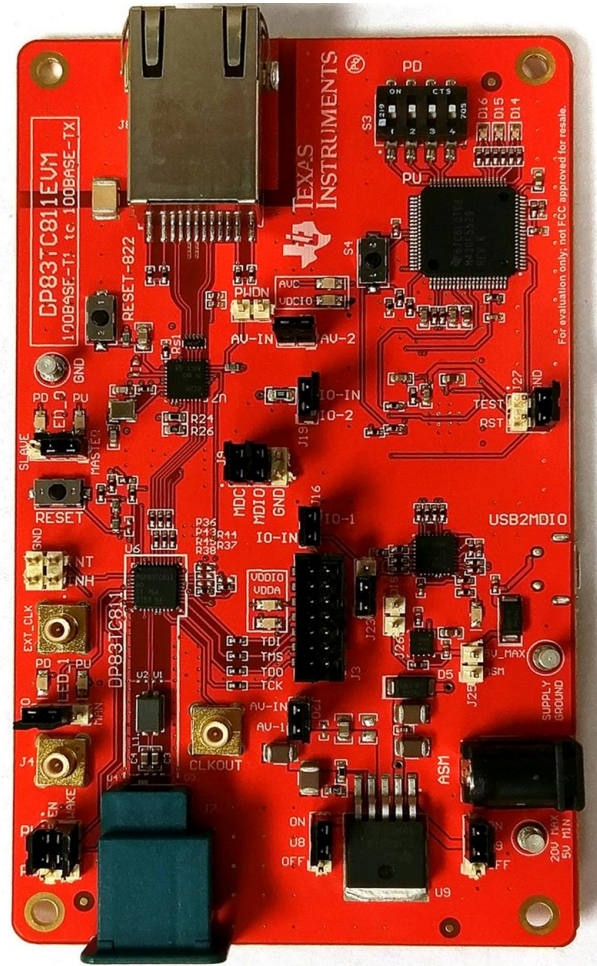


Figure 1. DP83TC811EVM – Top Side

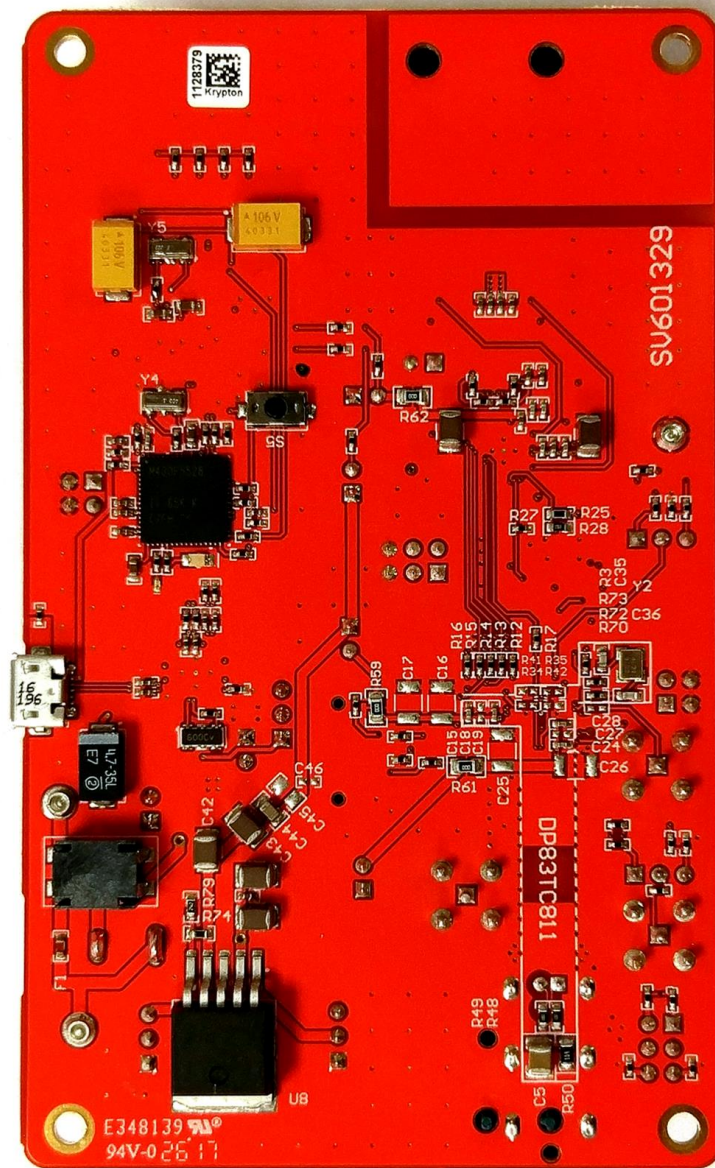
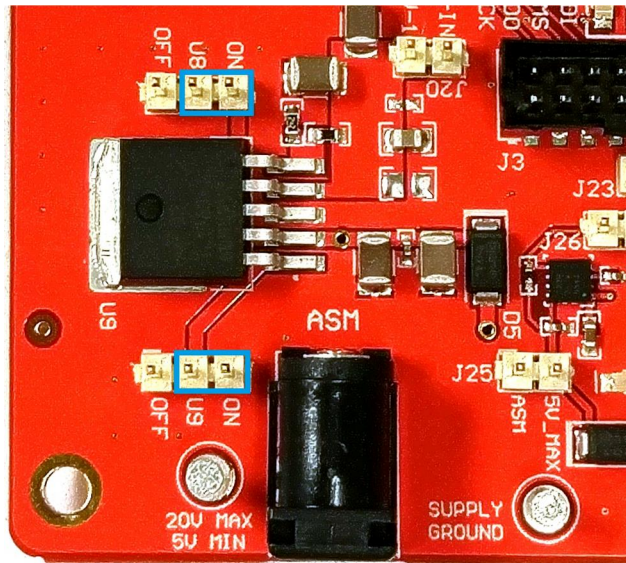


Figure 2. DP83TC811EVM – Bottom Side

## 2.2 Operation – Quick Setup

### 2.2.1 Onboard Power Supply Operation

- EVM can operate from a single DC supply connected to either turret or barrel jack connector
  - Wide  $V_{in}$ : 20-V to 5-V
- Place shunt at U8 header in ON position to enable U8 LDO
- Place shunt at U9 header in ON position to enable U9 LDO



**Figure 3. Onboard Supply Connection and Jumpers**

- DP83TC811 Onboard Power
  - Place shunt at J20 to enable onboard VDDA
  - Place shunt at J16 to enable onboard VDDIO
  - When power is properly supplied, the LED's for VDDA and VDDIO will light up
- DP83822 Onboard Power
  - Place shunt at J21 to enable onboard AVD
  - Place shunt at J19 to enable onboard VDDIO
  - When power is properly supplied, the LEDs for AVD and VDDIO will light up

#### Notes:

- **Only populate J25 when powering over USB**
- **This header has a 5-V maximum limit**

### 2.2.2 External Power Supply Operation

- Place shunt at U8 header in OFF position to disable U8 LDO
- Place shunt at U9 header in OFF position to disable U9 LDO
- DP83TC811 External Power
  - Remove shunt at J20 to disable onboard VDDA
  - Remove shunt at J16 to disable onboard VDDIO
  - Connect 3.3-V to AV-IN on J20
  - Connect 1.8-V, 2.5-V, or 3.3-V to IO-IN on J16
  - Connect ground to GND turret

- DP83822 External Power
  - Remove shunt at J21 to disable onboard AVD
  - Remove shunt at J19 to disable onboard VDDIO
  - Connect 3.3-V to AV-IN on J21
  - Connect 1.8-V, 2.5-V, or 3.3-V to IO-IN on J19
  - Connect ground to GND turret

### 2.2.3 Master and Slave Mode Selection – DP83TC811

- Master Mode
  - Place shunt across pins 1 and 2 at LED\_0
- Slave Mode
  - Place shunt across pins 2 and 3 at LED\_0

### 2.2.4 Managed and Autonomous Mode Selection – DP83TC811

- Managed Mode
  - Place shunt across pins 1 and 2 at LED\_1
- Autonomous Mode
  - Place shunt across pins 2 and 3 at LED\_1

Notes:

- J4 is connected to LED\_1. This SMB can be used for any GPIO features supported by LED\_1
- Remove Shunt on LED\_1 to use SMB connector

### 2.2.5 SMI Connection

- To connect DP83TC811 and DP83822 to the MSP430
  - Place shunt across pins 1 and 2 for MDC on J9
  - Place shunt across pins 3 and 4 for MDIO on J9

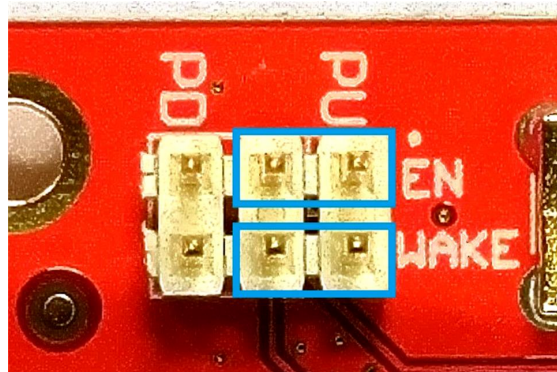
### 2.2.6 Enable Mode – DP83TC811

- PHY Enabled
  - Place shunt in 'PU' position at EN header shown in [Figure 4](#)
  - [Figure 4](#) shows the shunt position for the PHY in ENABLED mode
- PHY Disabled
  - Place shunt in 'PD' position at EN header shown in [Figure 4](#)

### 2.2.7 Sleep Mode – DP83TC811

- PHY Awake
  - Place shunt in 'PU' position at WAKE header shown in [Figure 4](#)
  - [Figure 4](#) shows the shunt position for the PHY in WAKE mode
- PHY Asleep
  - Place shunt in 'PD' position at WAKE header shown in [Figure 4](#)





**Figure 4. Enable and Wake Control**

### 2.2.8 Cable Assembly

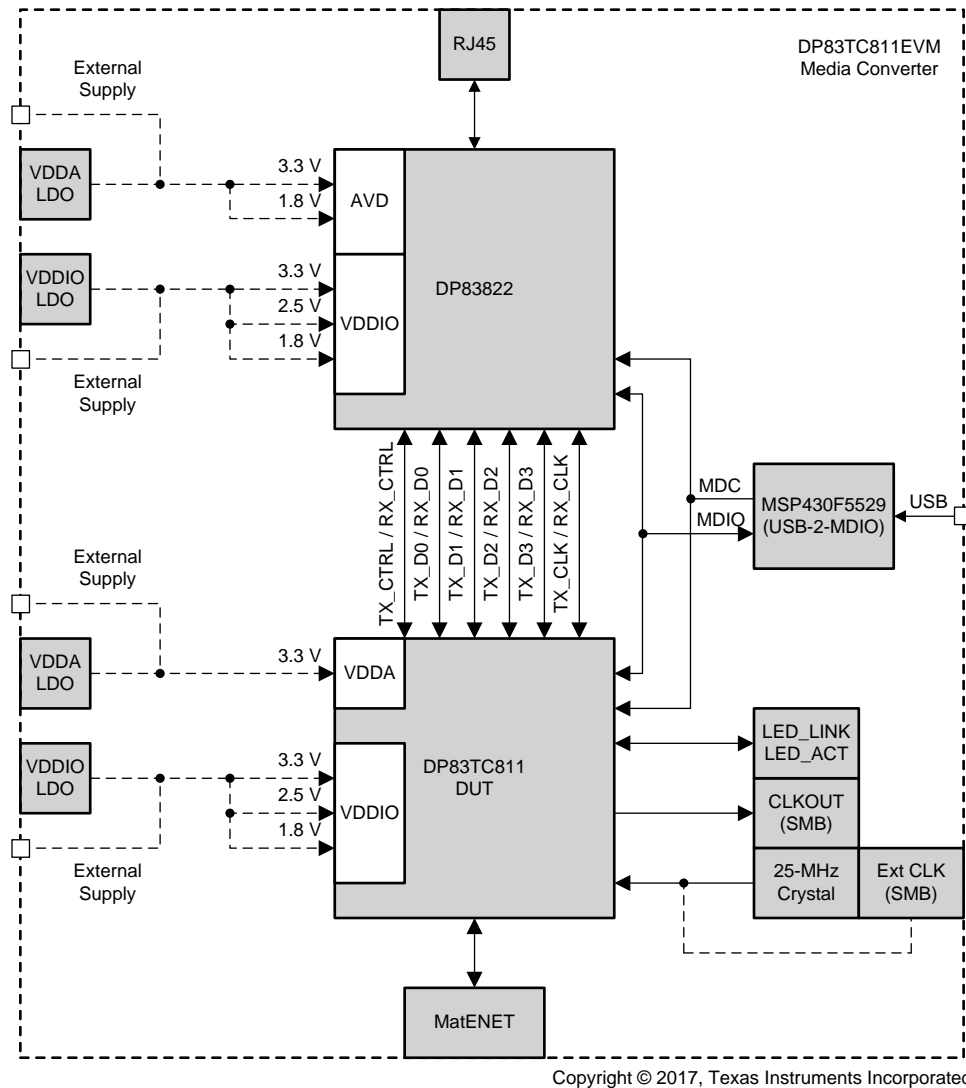
- Plug a CAT5, CAT5E, or CAT6 cable into the RJ45 connector (J8)
  - Connect the far-end of the Ethernet cable to a 100BASE-TX capable PHY
- Plug a MatENET cable assembly into the B-type automotive connector (J7)
  - Connect the far-end of the automotive cable to a 100BASE-T1 capable PHY

### 2.2.9 LED Indication

- Look for LED\_0 and LED\_1 to illuminate when a link is successfully established
- Look for Green LED to illuminate on the RJ45 (J8) when a link is successfully established
- Look for Yellow LED to illuminate on the RJ45 (J8) when speed is at 100 Mbps
- LED\_1 will blink for TX/RX activity

## 3 Board Setup Details

### 3.1 Block Diagram



**Figure 5. DP83TC811EVM Block Diagram**

### 3.2 Serial Management Interface

The DP83TC811EVM supports SMI (MDIO/MDC) through J9 and includes an onboard MSP430F5529 for USB-2-MDIO control.

**Notes:**

- DP83TC811 default PHY\_ID is 0
- DP83822 default PHY\_ID is 1
- PHY IDs can be changed through bootstrap options found in the data sheet

### 3.3 Configuration Options

#### 3.3.1 Bootstrap Options

Some DP83TC811 and DP83822 configurations can be done through bootstrap options. Options can be selected with jumpers or resistor population. Refer to the data sheets for bootstrap options and the schematic and layout sections of this User's Guide for resistor locations.

**Table 2. DP83822 Bootstrap Resistor Designation and Suggested Bootstrap Resistor Values**

PIN NAME	PIN NUMBER	STRAP MODE	PU RESISTOR (KΩ)	PU RESISTOR DESIGNATION	PD RESISTOR (KΩ)	PD RESISTOR DESIGNATION
RX_ER	28	1	OPEN	R24	1.96	R26
		2	13		1.96	
		3	6.20		1.96	
		4	OPEN		OPEN	
CRS	27	1	OPEN	R25	1.96	R28
		2	13		1.96	
		3	6.20		1.96	
		4	OPEN		OPEN	

**Table 3. DP83TC811 Bootstrap Resistor Designation and Suggested Bootstrap Resistor Values**

PIN NAME	PIN NUMBER	STRAP MODE	PU RESISTOR (KΩ)	PU RESISTOR DESIGNATION	PD RESISTOR (KΩ)	PD RESISTOR DESIGNATION
RX_D0	26	1	OPEN	R36	OPEN	R43
		2	10.20		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_D1	25	1	OPEN	R37	OPEN	R44
		2	10.20		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_D2	24	1	OPEN	R38	OPEN	R45
		2	10.20		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_ER	14	1	OPEN	R35	OPEN	R42
		2	10.20		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
RX_DV	15	1	OPEN	R34	OPEN	R41
		2	10.20		2.49	
		3	5.76		2.49	
		4	2.49		OPEN	
LED_0	35	1	OPEN	R30	2.49	R39
4		2.49	OPEN			
LED_1	6	1	OPEN	R31	2.49	R40
		4	2.49		OPEN	

### 3.3.2 Clock Configuration

- Onboard Clock
  - The onboard clock is enabled by default
  - If disabled:
    - Populate Y2, R72, R73, C35, and C36 with their respective values from the schematic
    - Remove R70 if populated
  - By default, a 25-MHz clock output can be viewed using the CLKOUT SMA
- External Clock
  - Remove R72 and R73
  - Populate R70 with a 0- $\Omega$  resistor
  - Use the SMA labeled EXT\_CLK to input the external clock source
  - By default, a 25-MHz clock output can be viewed using the CLKOUT SMA

### 3.3.3 JTAG

- Use J3 for JTAG access to the DP83TC811



## 4 Firmware Configuration

### 4.1 eZ-FET Firmware

- MSP430F5529 Launchpad Configuration
  - Remove all shunts from the Isolation Jumper Block interfacing with the eZ-FET section
  - On the eZ-FET side of the Isolation Jumper Block, place Spy-Bi-Wire on the pins for RST, TST, and GND, as highlighted in [Figure 6](#)
  - Power up the MSP430 Launchpad

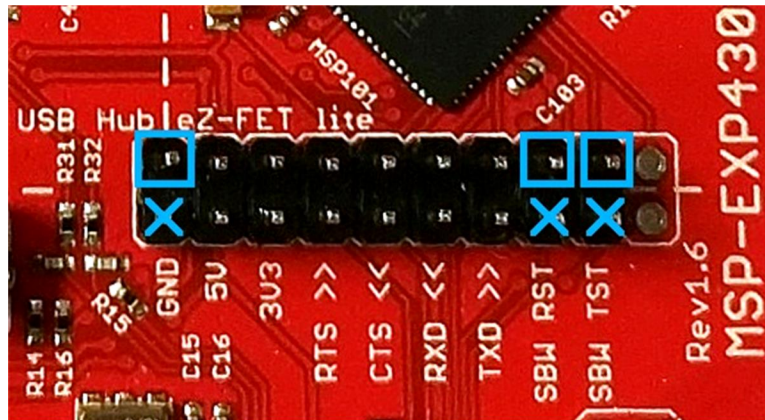


Figure 6. MSP430 Launchpad Spy-Bi-Wire Connection Points

- DP83TC811EVM Configuration
  - Jumper Positions
    - Place shunt across pins 1 and 2 on J23
    - Remove shunt from J26
    - Place shunt on J25

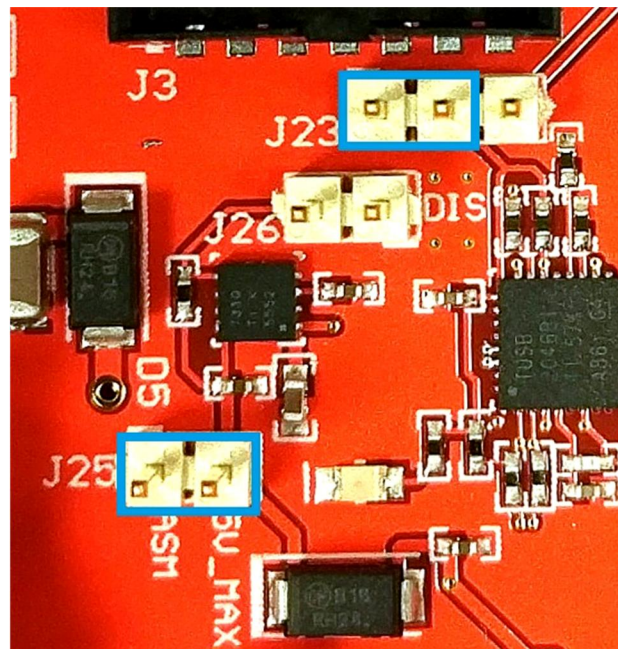
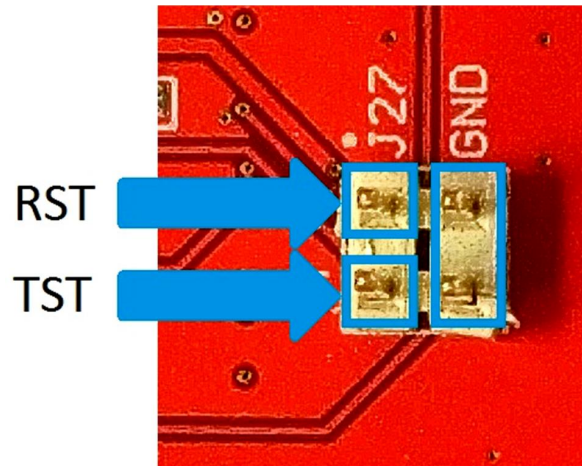


Figure 7. Jumper Positions

- Power up the DP83TC811EVM to no more than 5 V
- To connect the Spy-Bi-Wire from the MSP430 Launchpad:
  - Make sure the MSP430 Launchpad is powered on
  - Connect RST to pin 1 on J27
  - Connect TST to pin 3 on J27
  - Connect GND to either pin 2 or pin 4 on J27



**Figure 8. DP83TC811EVM Spy-Bi-Wire Connection Points**

- Flash the eZ-FET firmware by running the file *Flash\_eZ-FET\_DP83TC811EVM.bat*
- Remove the Spy-Bi-Wire from the DP83TC811EVM
- Remove power from the DP83TC811EVM (and the MSP430 Launchpad if desired)

#### 4.2 **MSP430F5529 Firmware**

- Remove shunt from J25 and store across GND terminals on J27 (pins 2 and 4)
- Plug a USB cable into the DP83TC811EVM
- Check for the correct LED indication
  - One green LED on the top of the board, as in [Figure 9](#)
  - One green LED on the bottom of the board, as in [Figure 9](#)
  - If either LED is not turned on or is the wrong color
    - Power down the DP83TC811EVM
    - Remove shunt from J27
    - Place shunt on J25
    - Repeat steps for eZ-FET Firmware and then try MSP430 Firmware again.

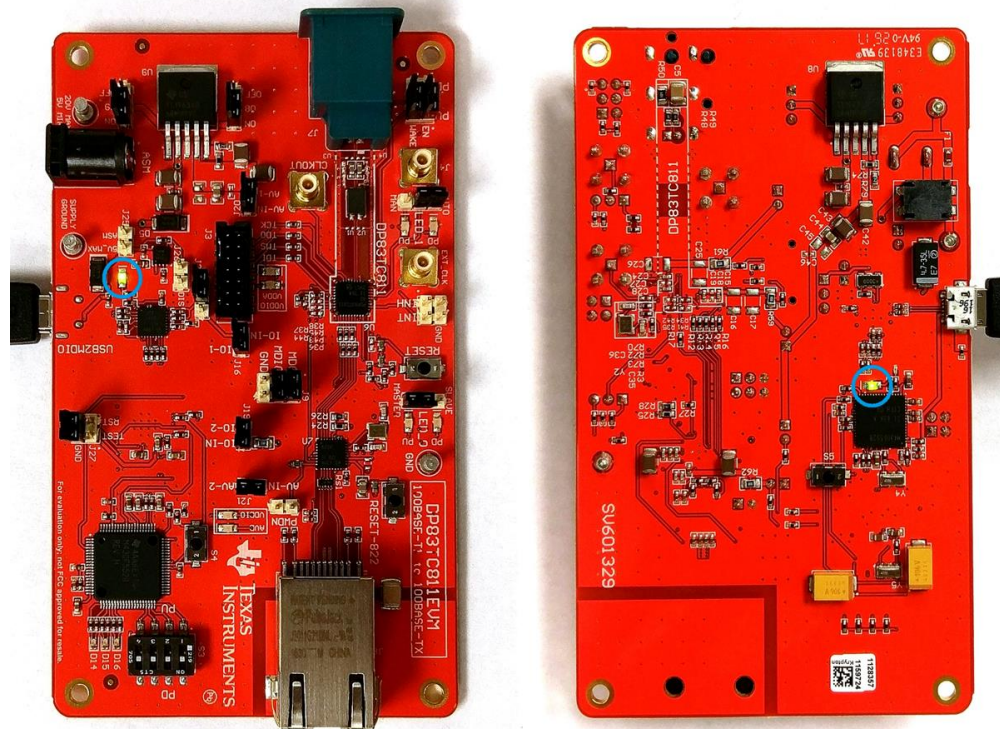


Figure 9. LED on Both Top and Bottom of DP83TC811EVM

- Flash the MSP430 firmware by running the file *Flash\_MSP430\_DP83TC811EVM.bat*
- Remove power from the DP83TC811EVM
- Firmware flash is successful if LED D14 is both red and green after reboot, as in [Figure 10](#)

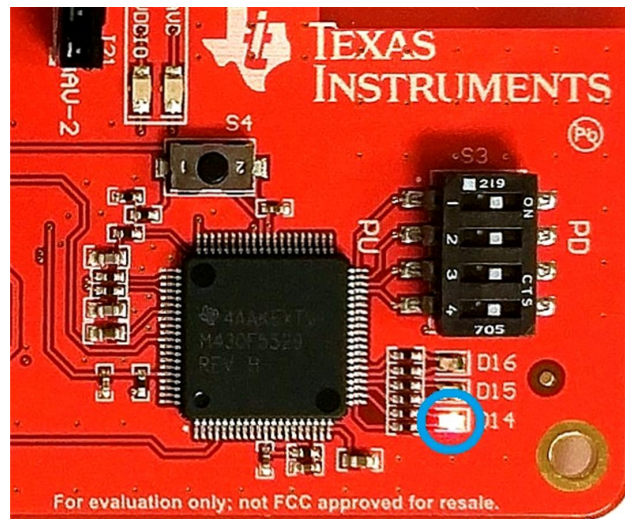
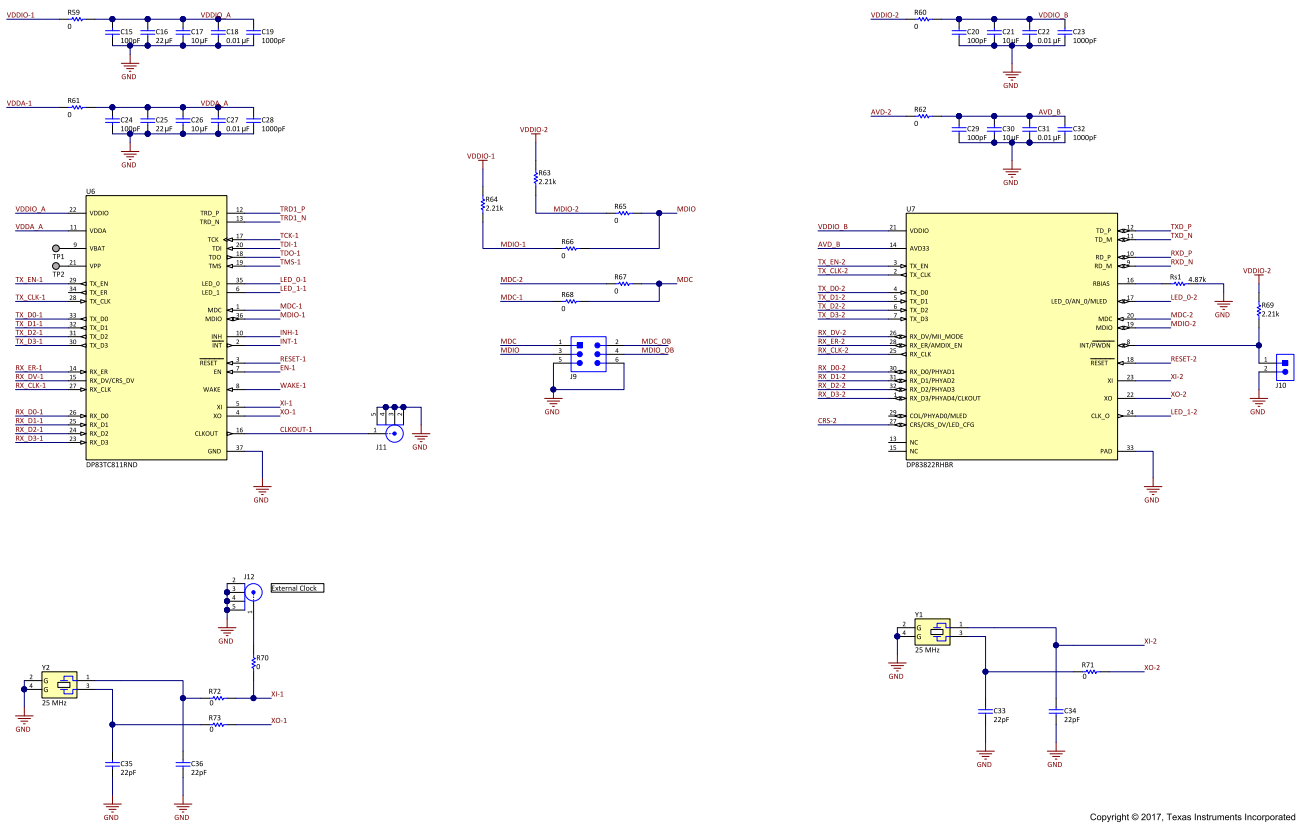


Figure 10. LED D14 Both Green and Red

## 5 Schematics

### 5.1 Main Block Schematic



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Figure 11. DP83TC811 Main Block



## 5.2 Main Power Schematic

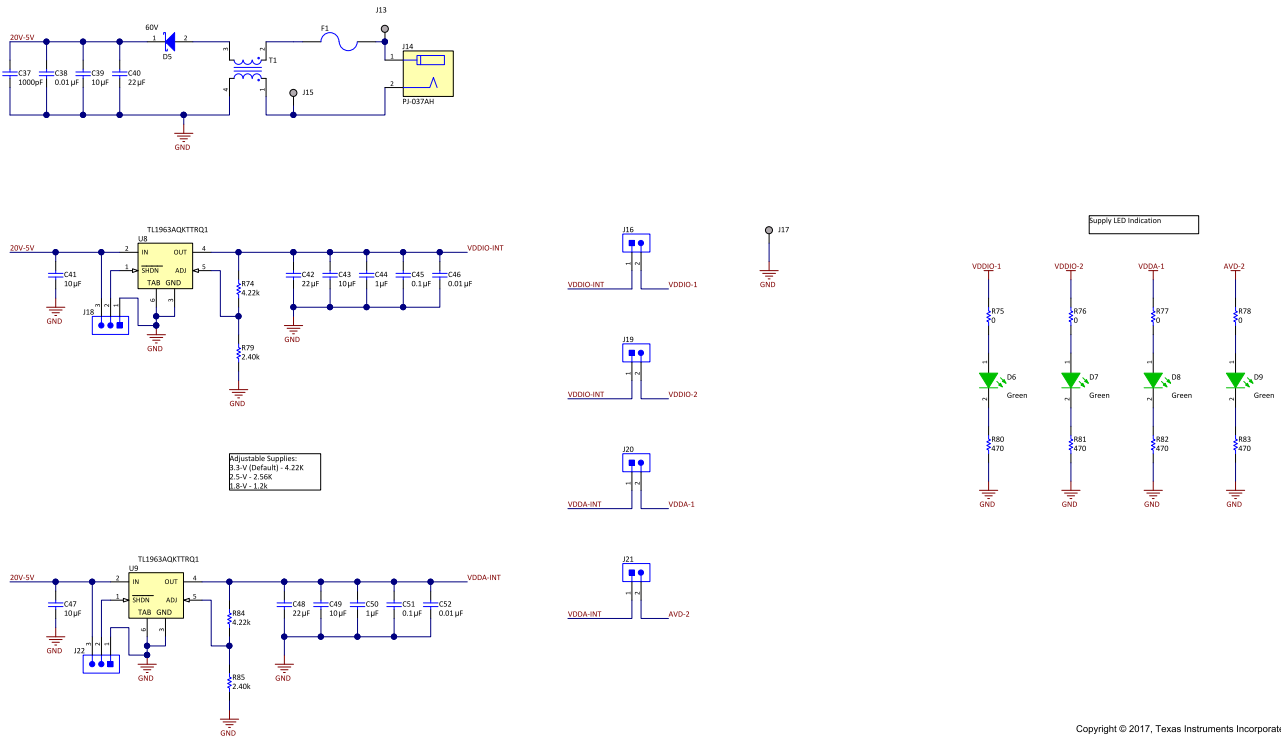
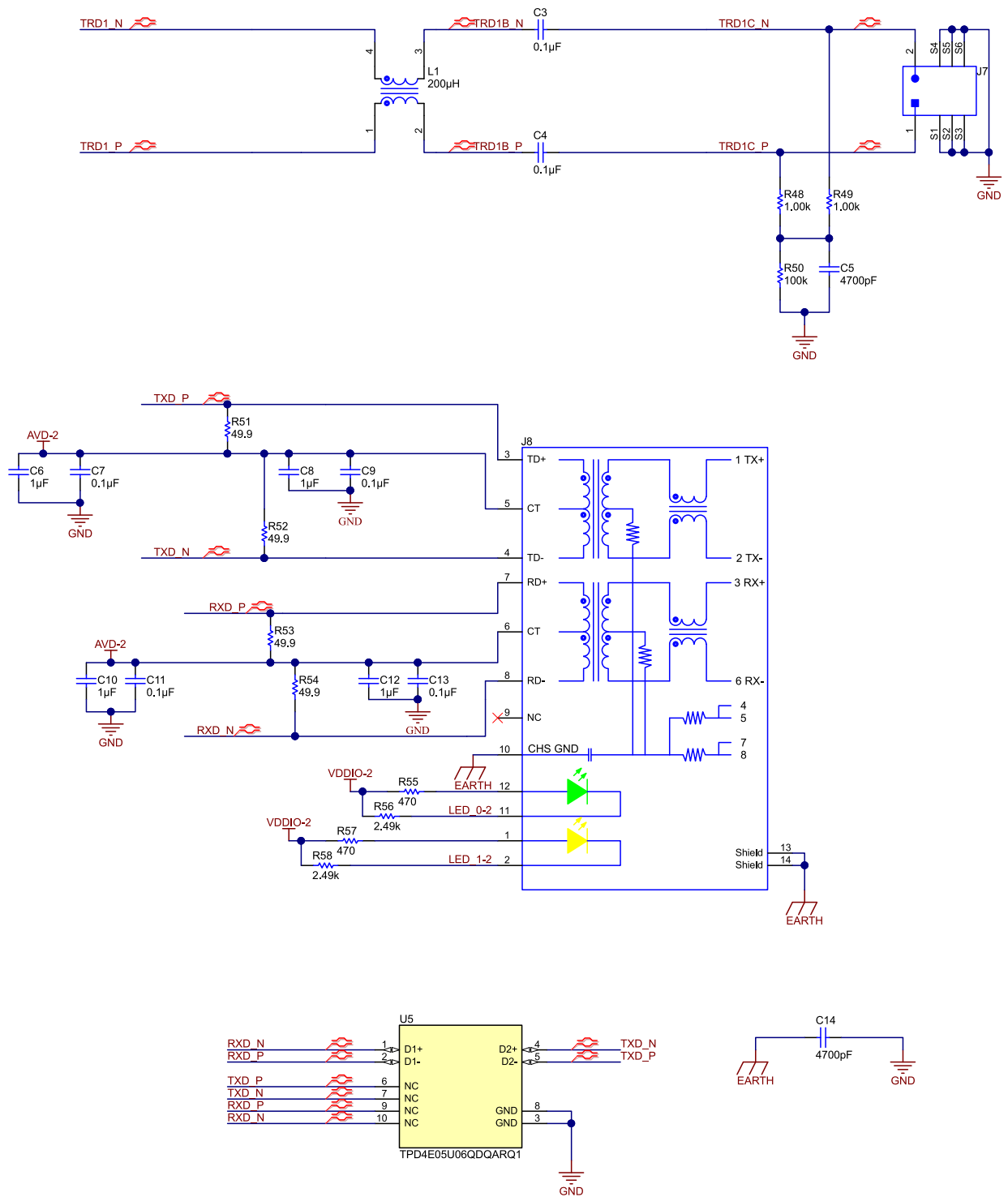


Figure 12. DP83TC811 Main Power

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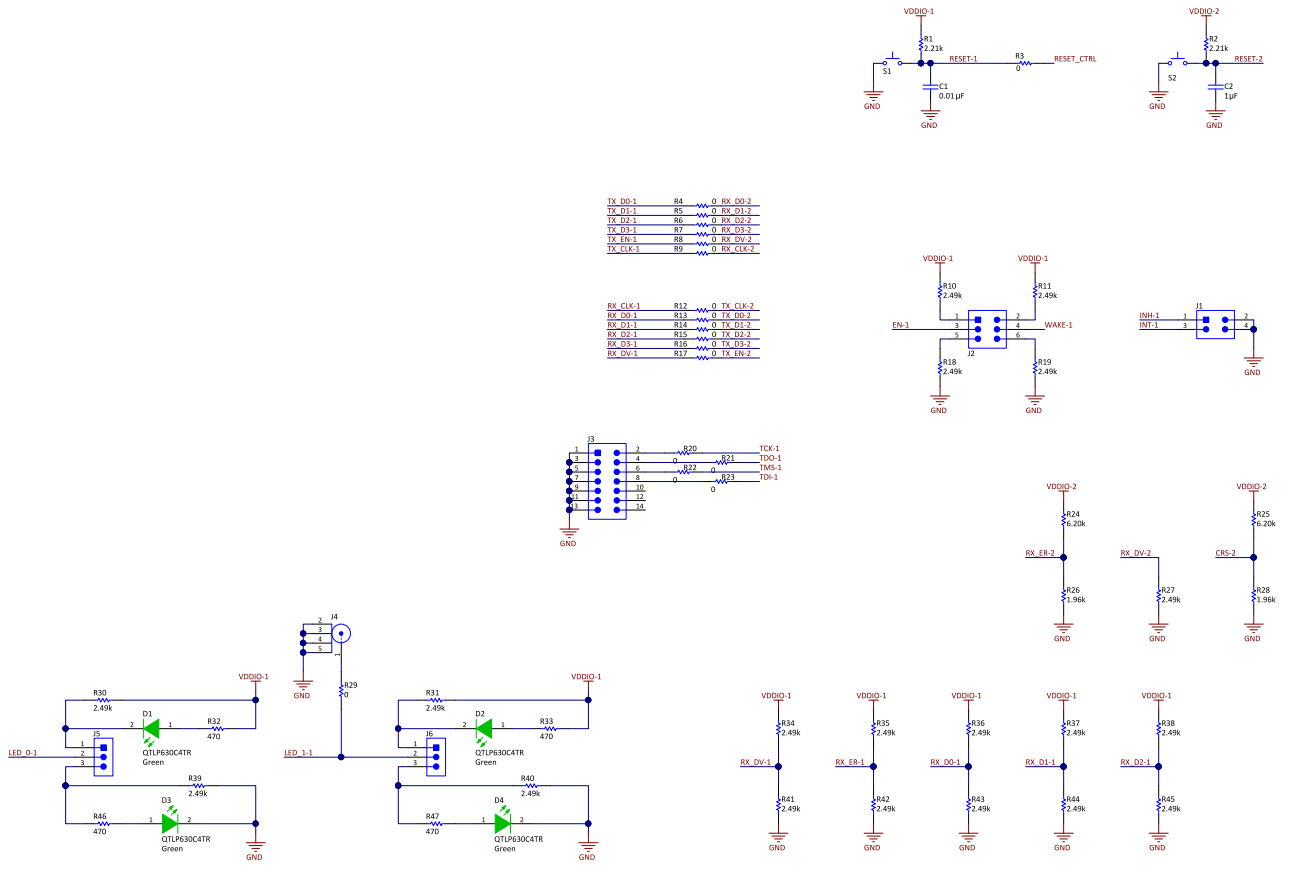
### 5.3 Analog Front-End Schematic



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Figure 13. DP83TC811 AFE

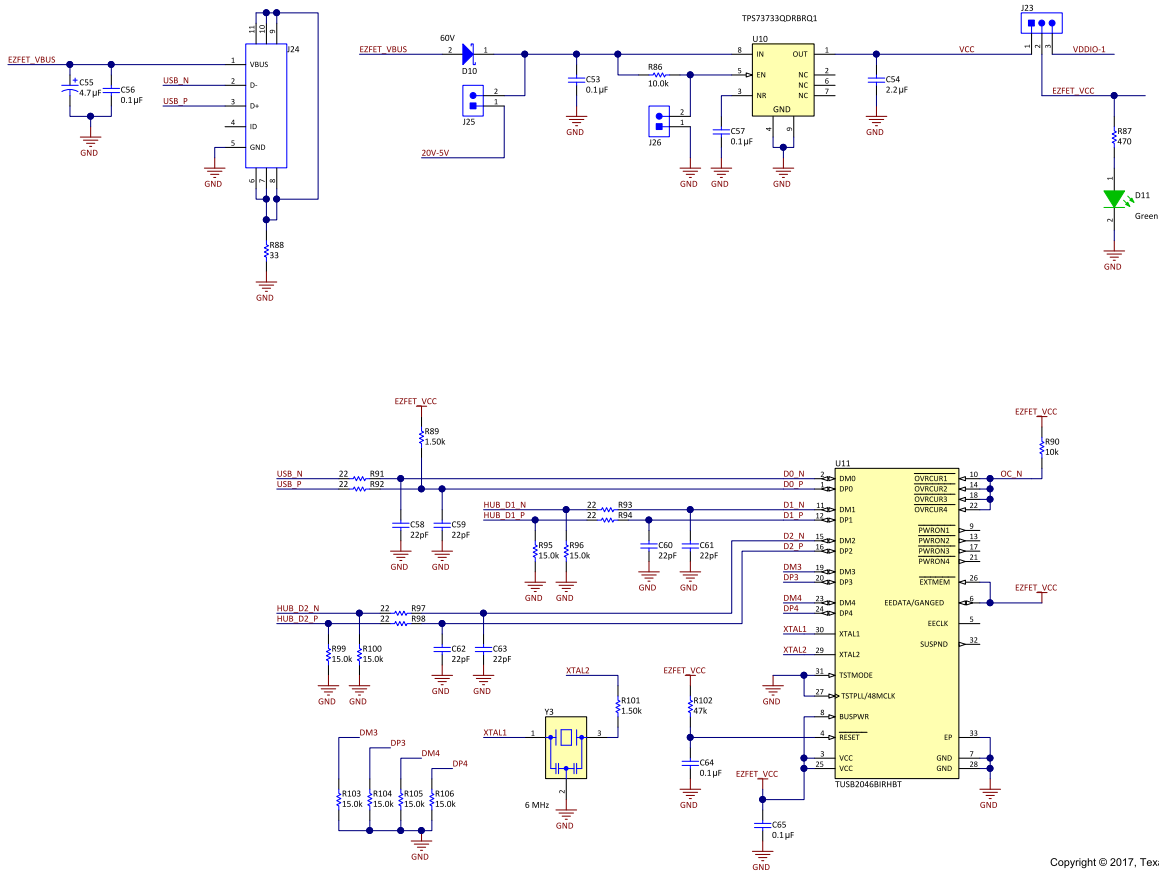
### 5.4 Interface Schematic



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Figure 14. DP83TC811 Interface

### 5.5 COMs Schematic



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Figure 15. DP83TC811 COMs



### 5.6 COMs #1 Schematic

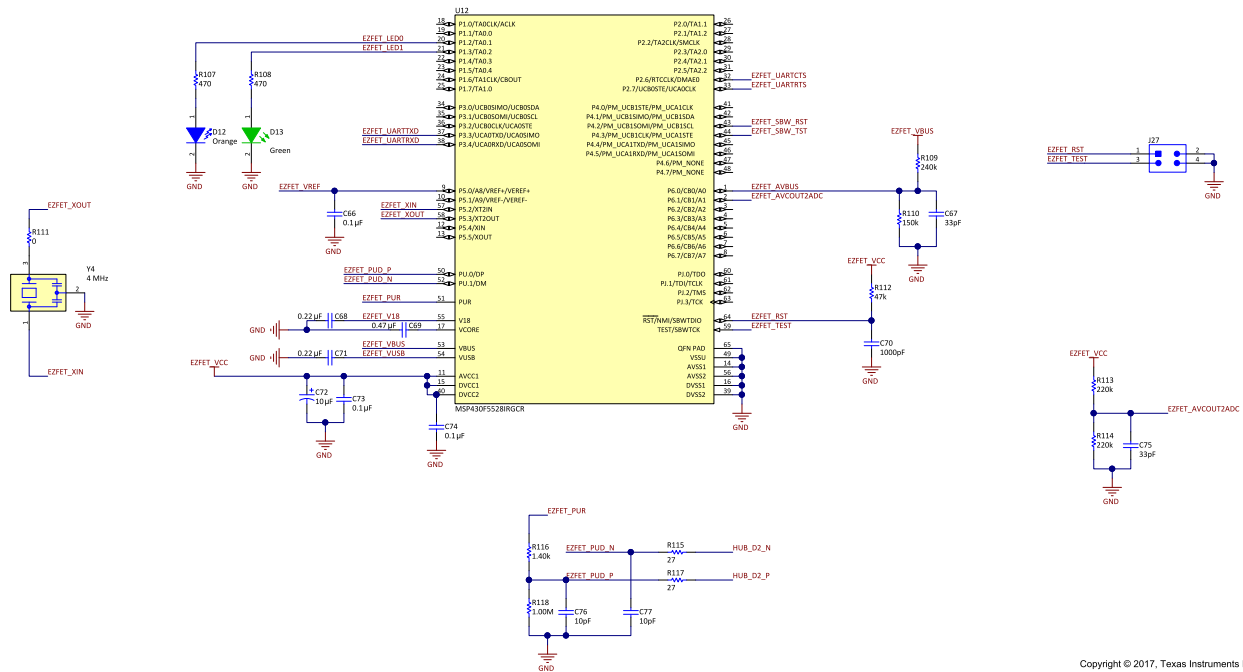


Figure 16. DP83TC811 COMs #1

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### 5.7 COMs #2 Schematic

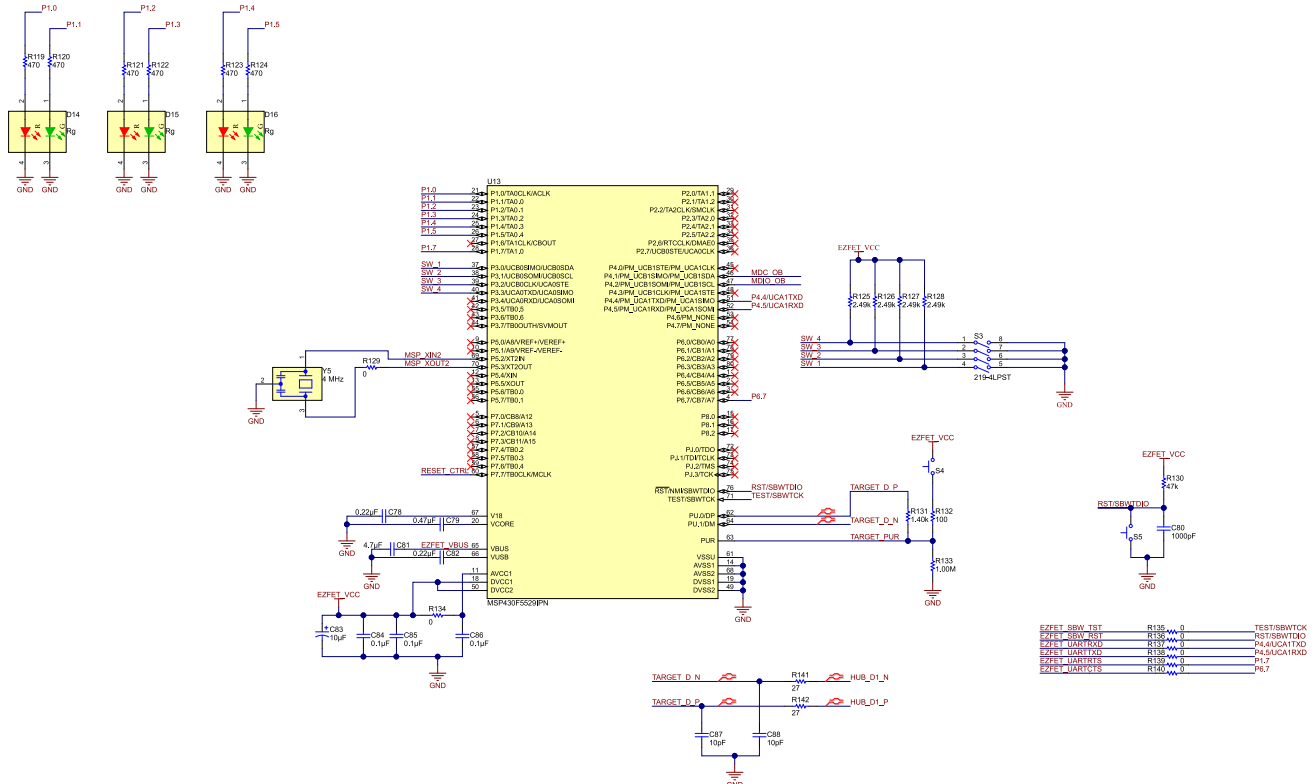
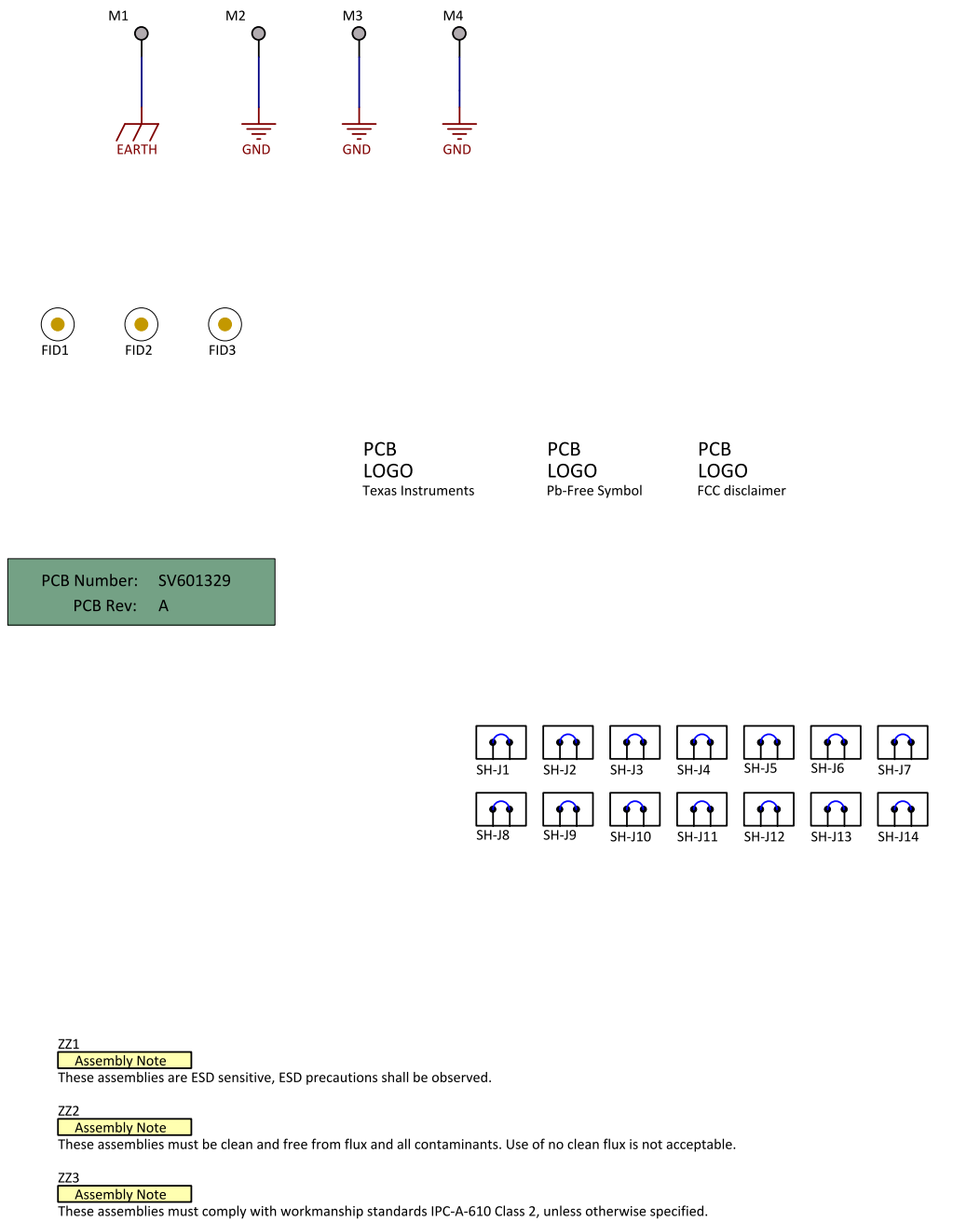


Figure 17. DP83TC811 COMs #2

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## 5.8 Hardware Schematic



ZZ1

**Assembly Note**

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ2

**Assembly Note**

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ3

**Assembly Note**

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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**Figure 18. DP83TC811 Hardware**

## 6 Layout

### 6.1 Top Overlay

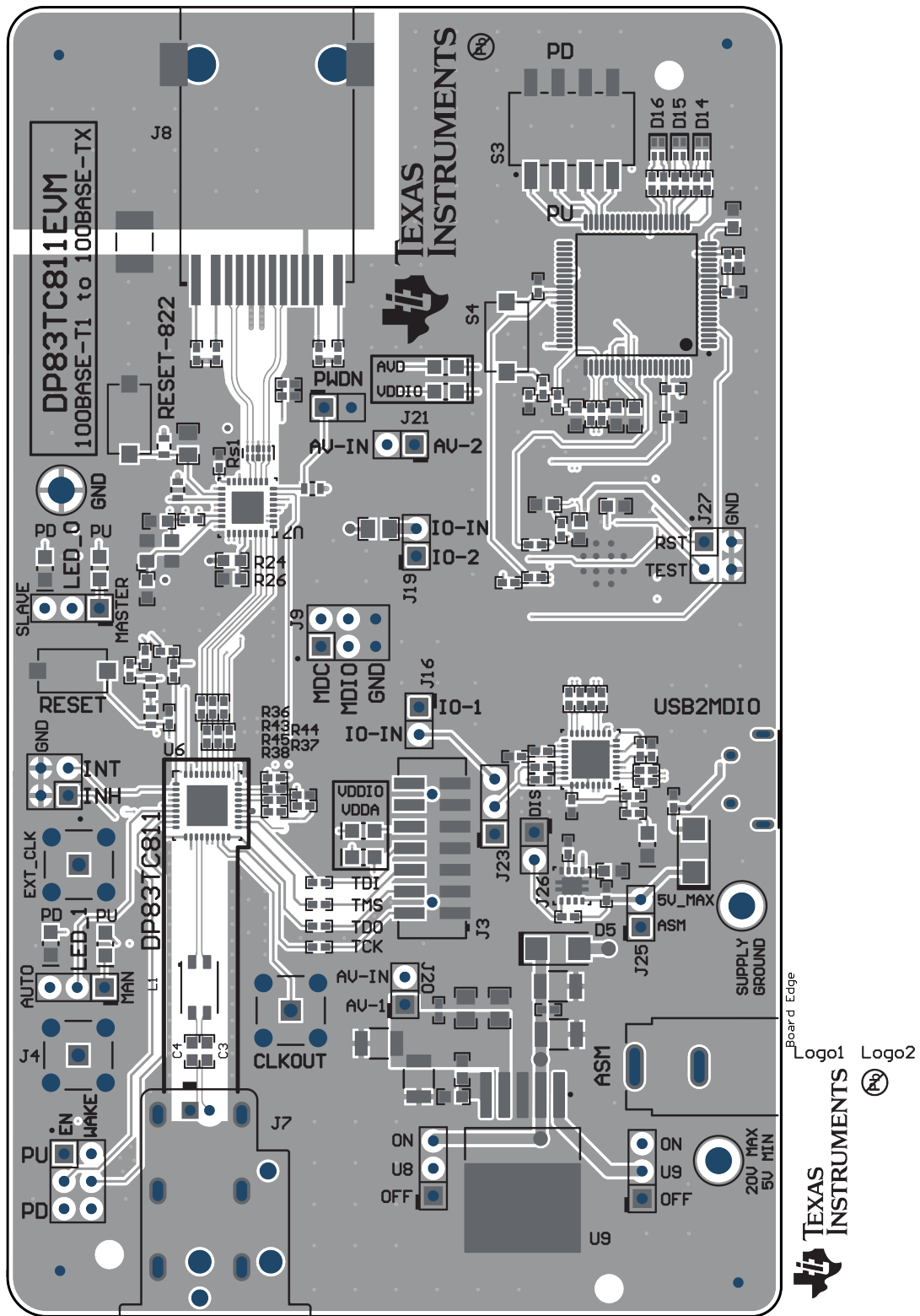


Figure 19. Top Overlay

## 6.2 Top Layer Mask

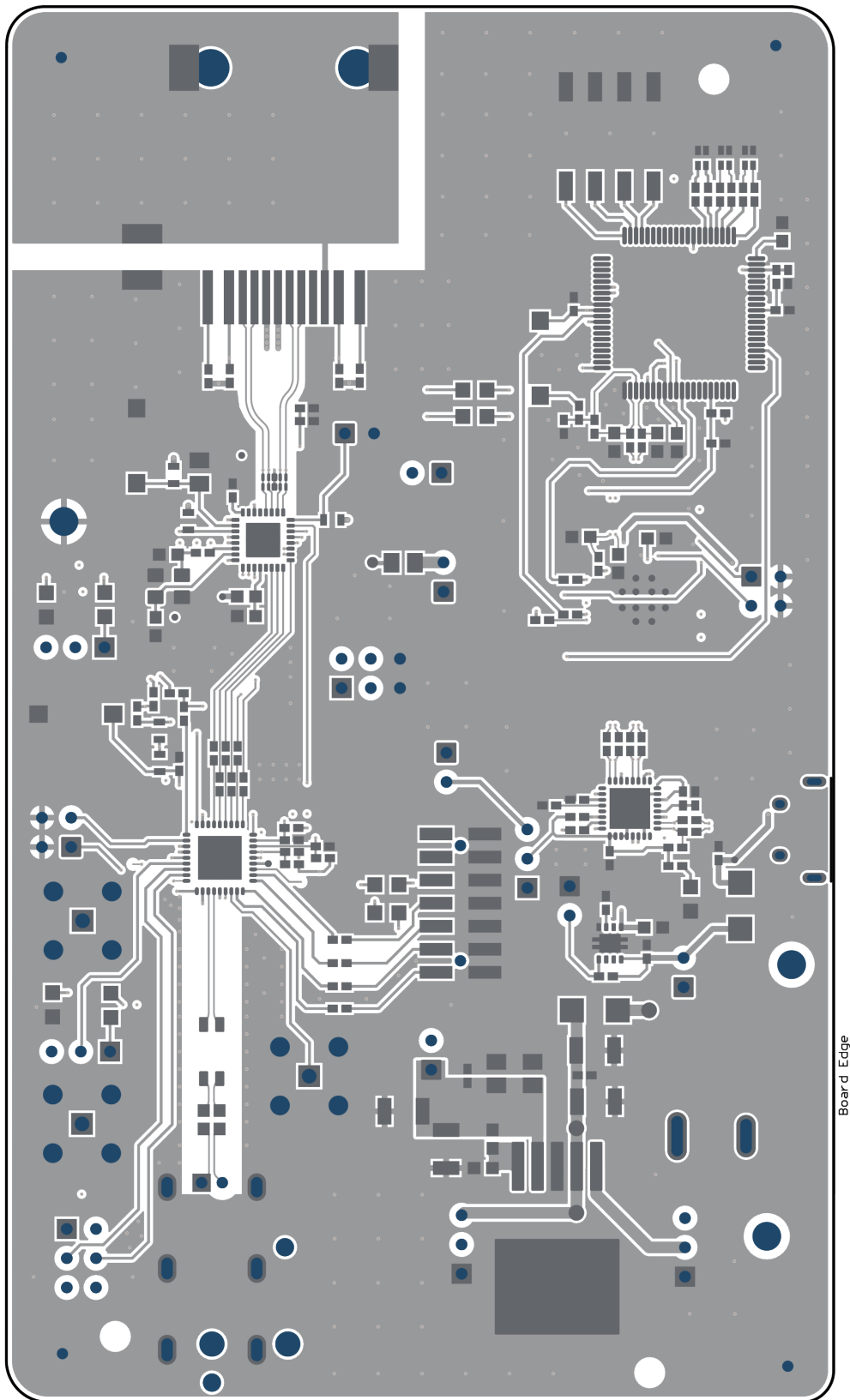
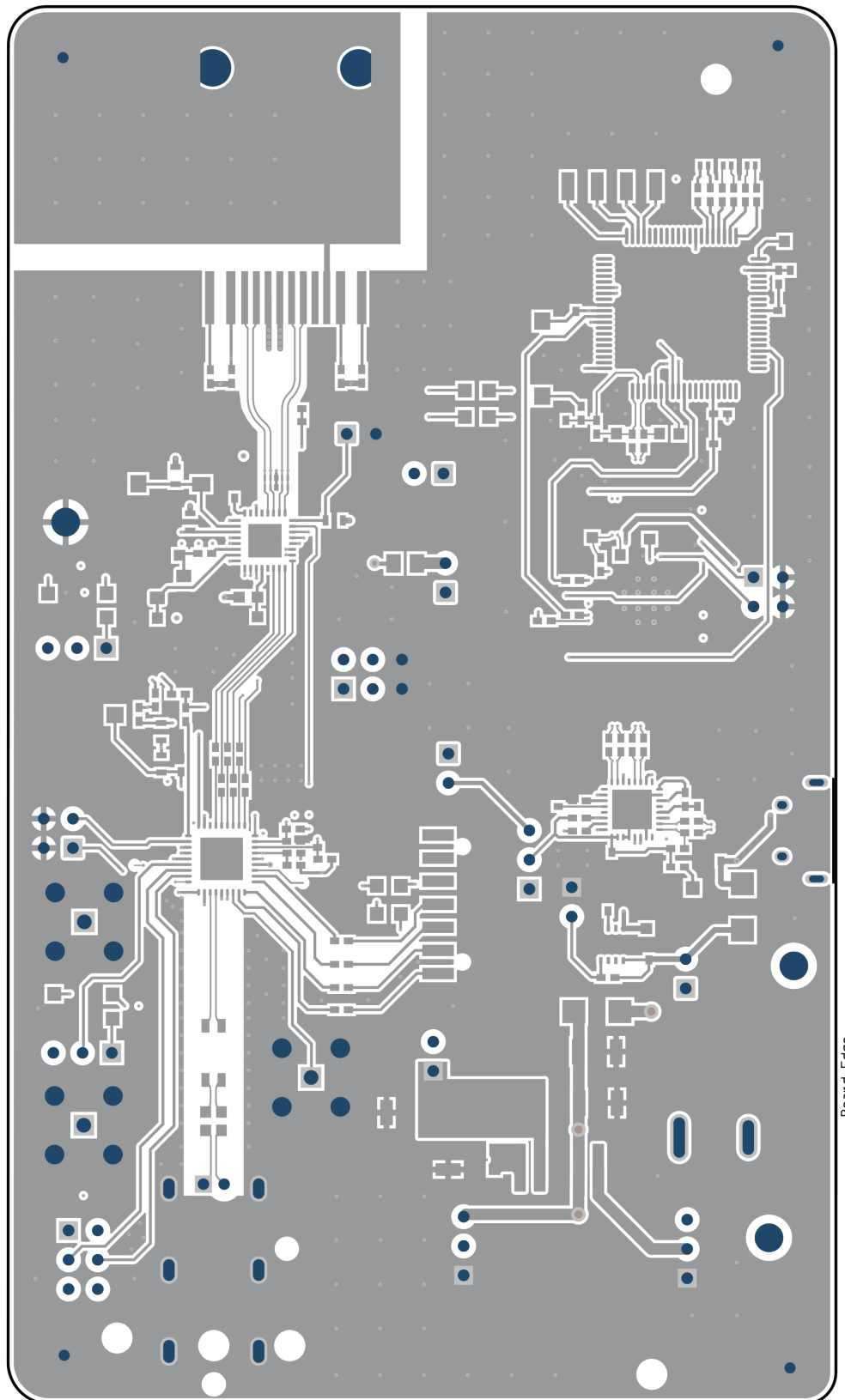


Figure 20. Top Layer Mask

### 6.3 Top Layer



**Figure 21. Top Layer**

## 6.4 Signal Layer 2

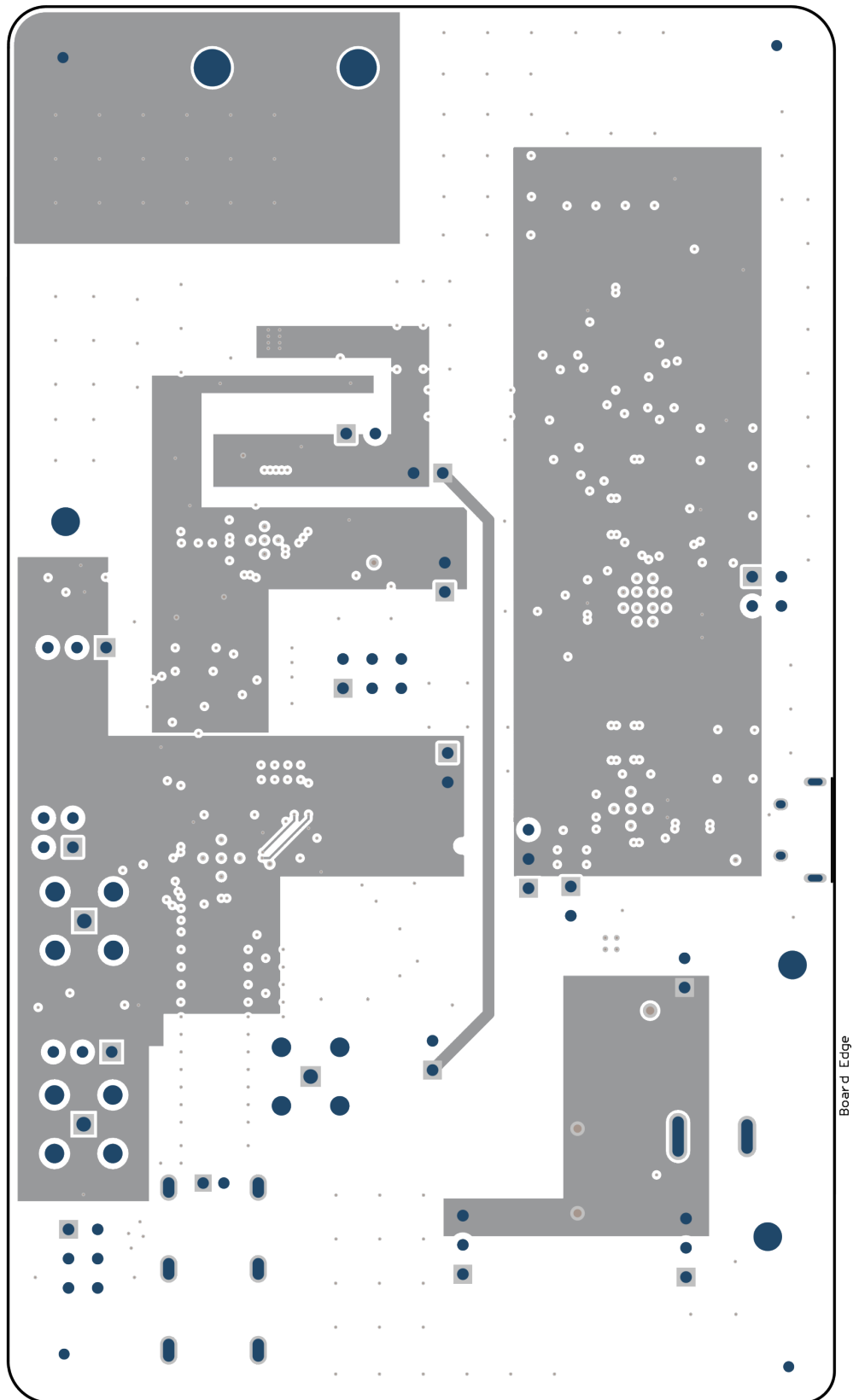


Figure 22. Signal Layer 2

### 6.5 Signal Layer 3

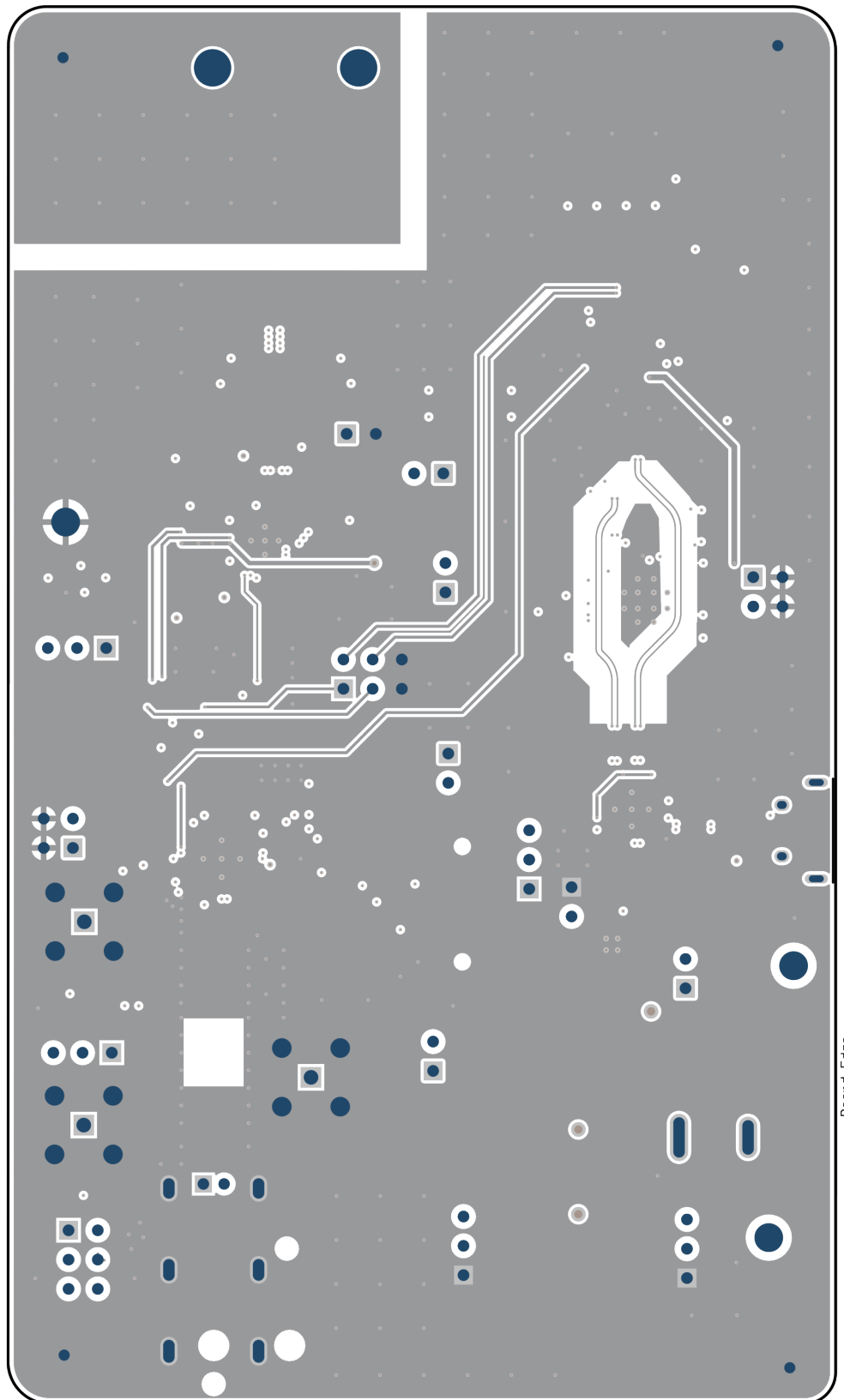


Figure 23. Signal Layer 3



## 6.6 Signal Layer 4

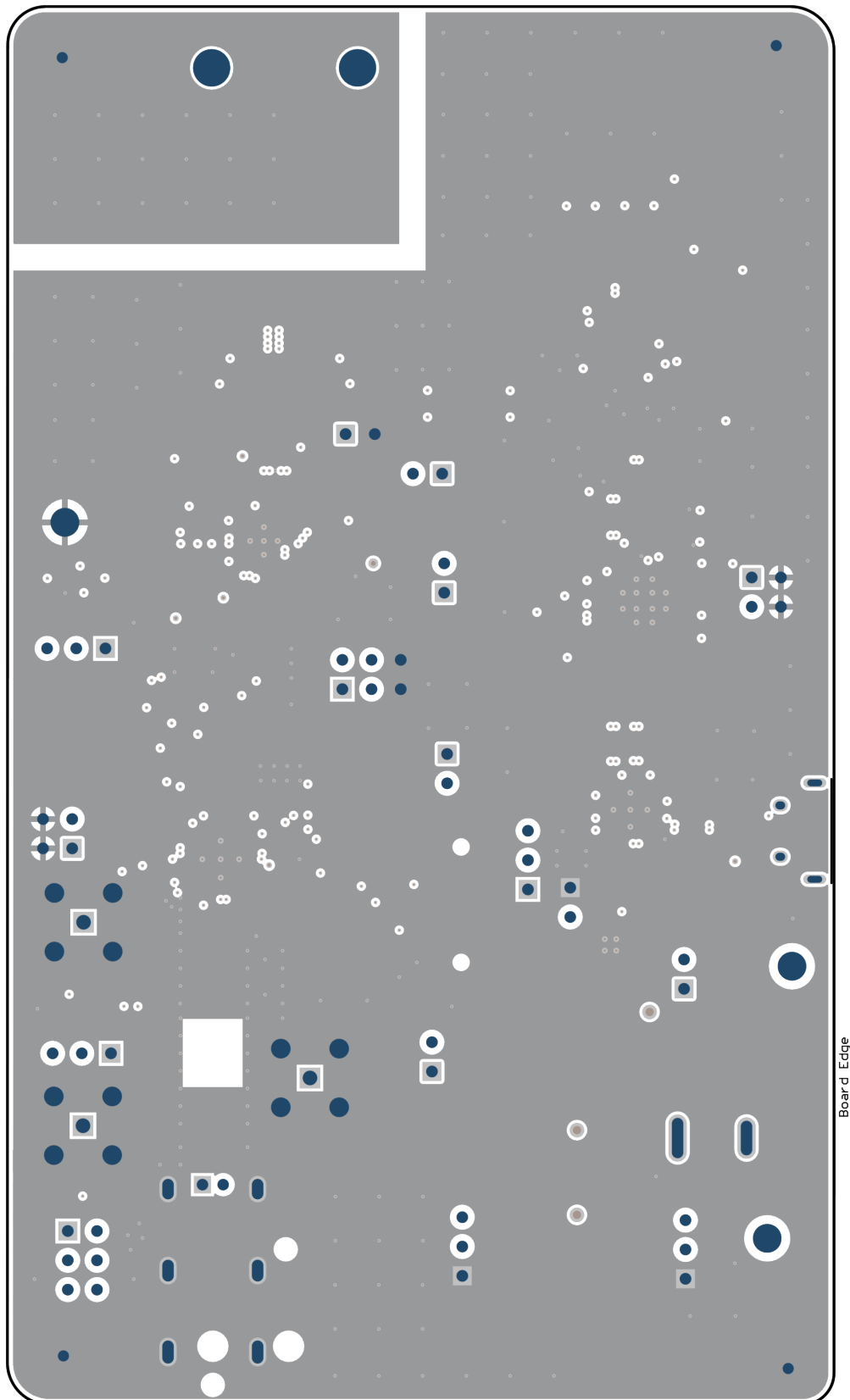


Figure 24. Signal Layer 4

## 6.7 Bottom Layer

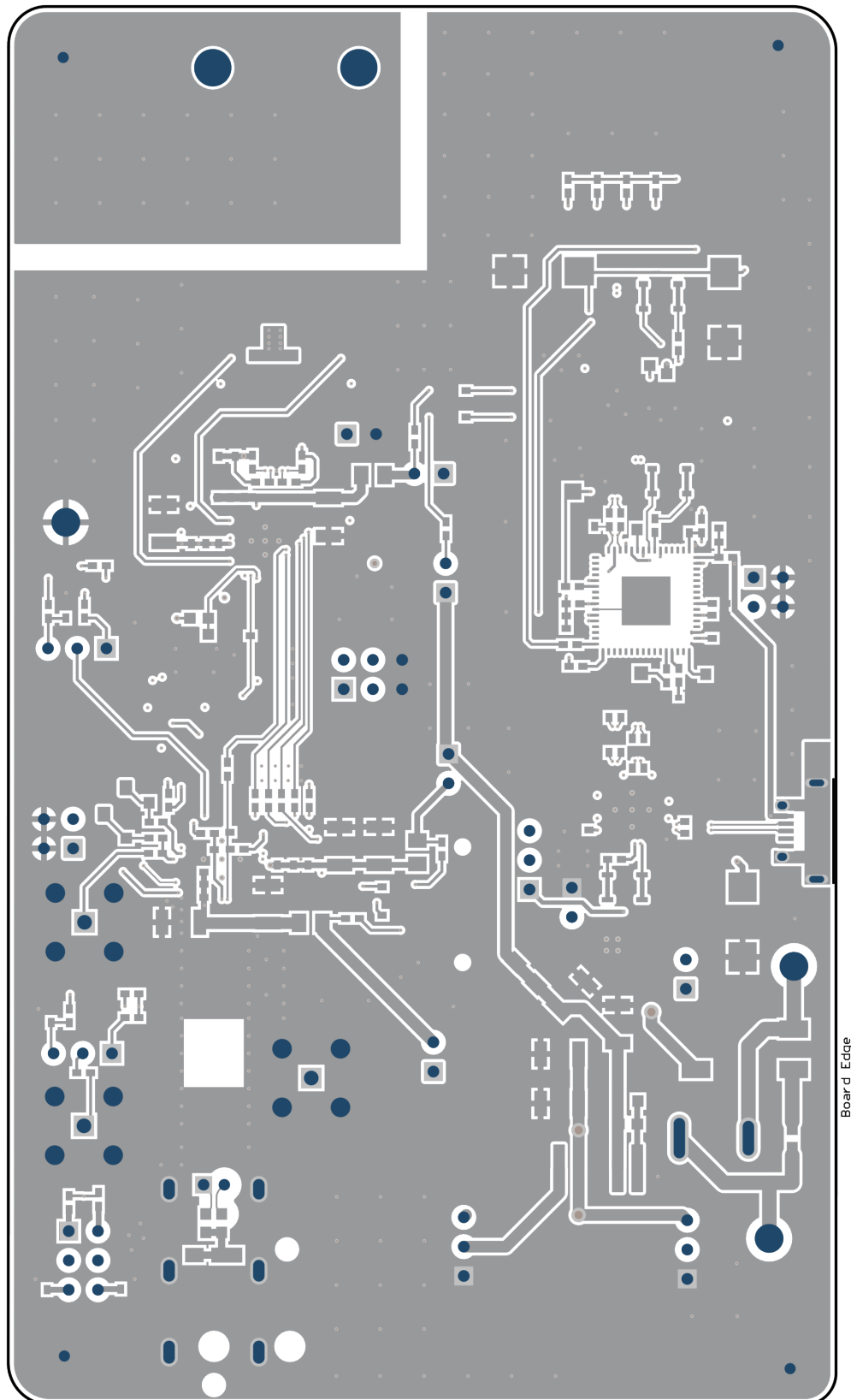


Figure 25. Bottom Layer

## 6.8 Bottom Layer Mask

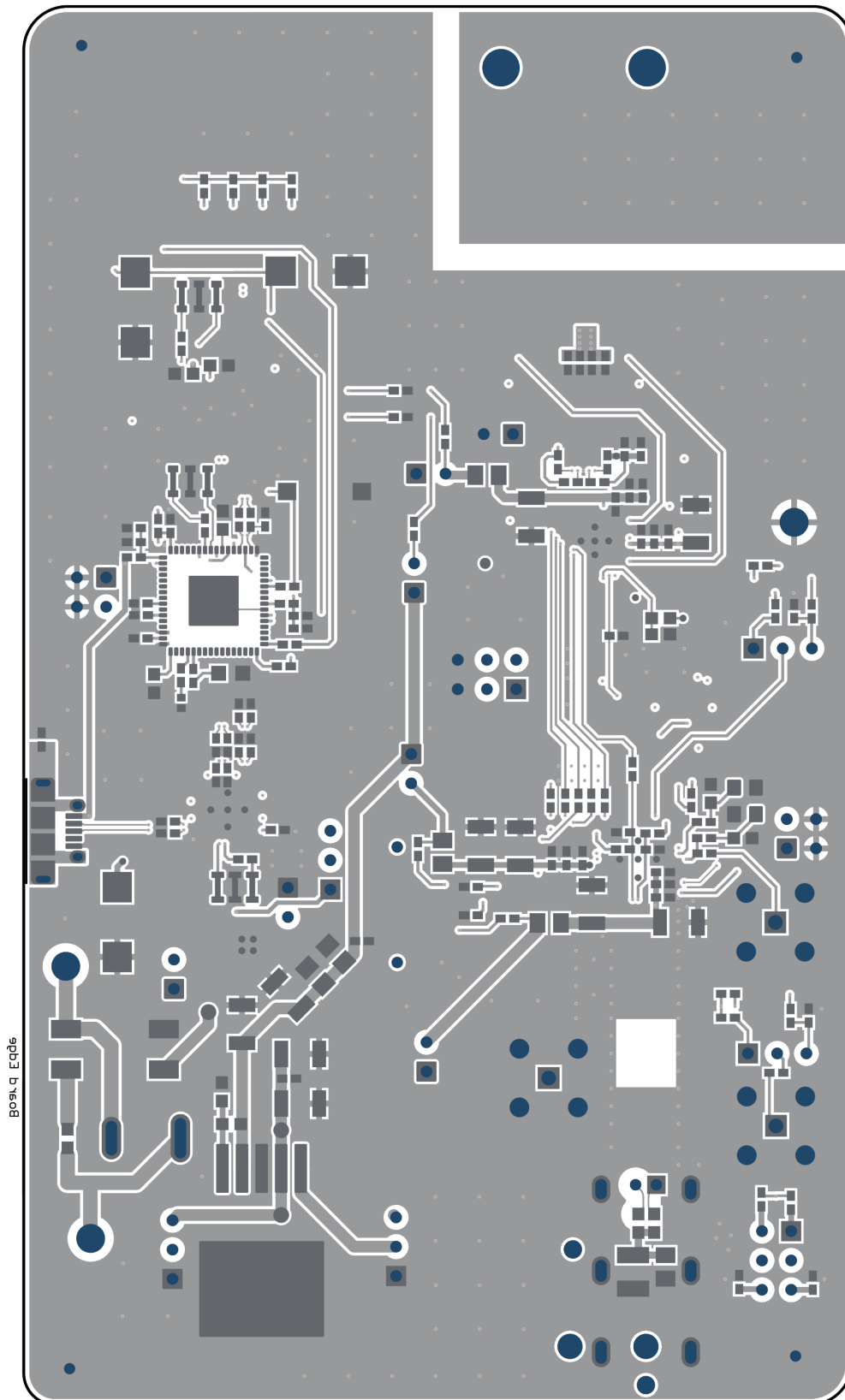


Figure 26. Bottom Layer Mask

6.9 Bottom Overlay

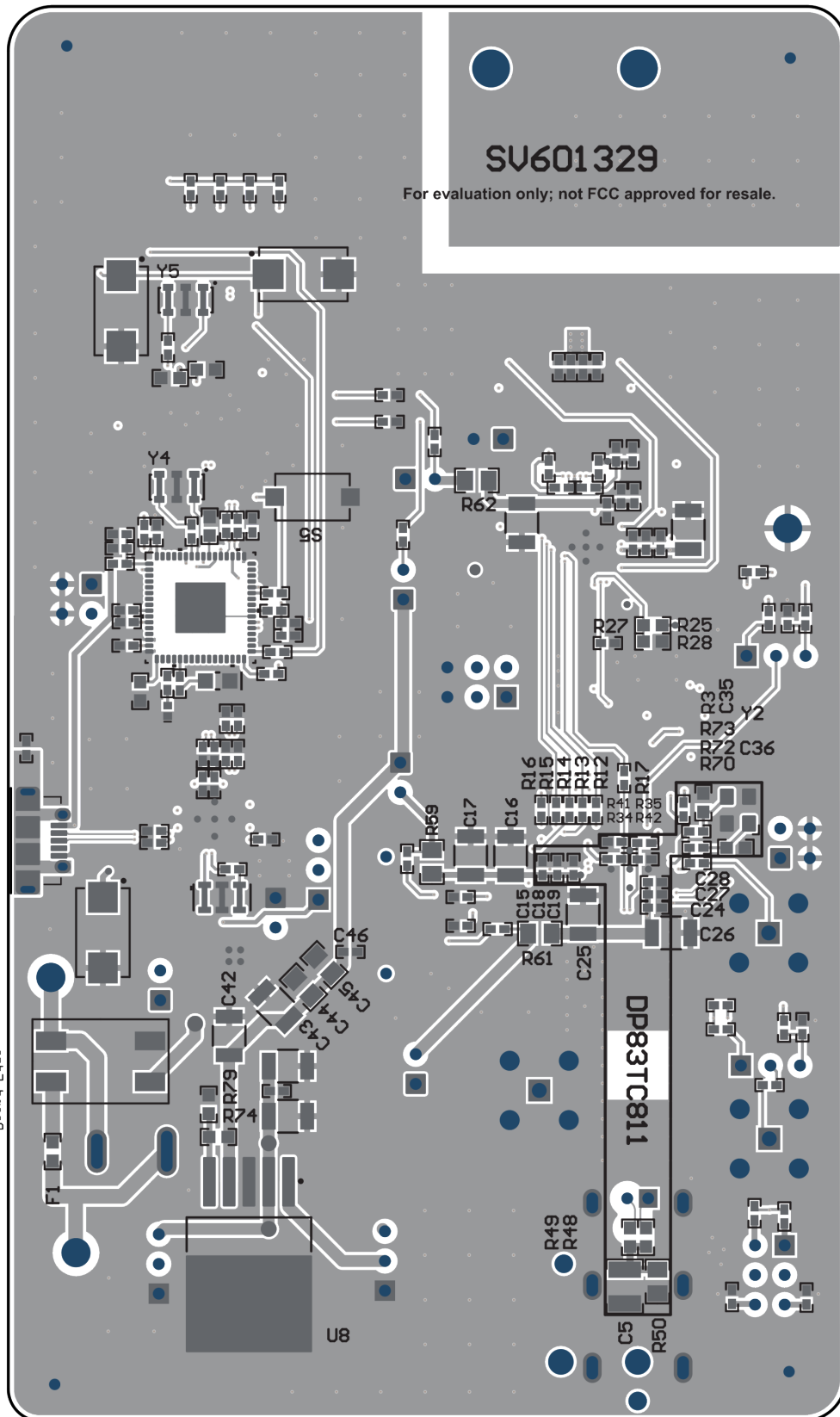
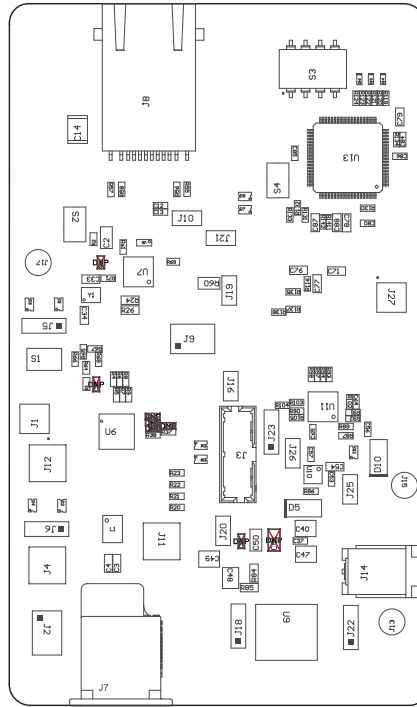
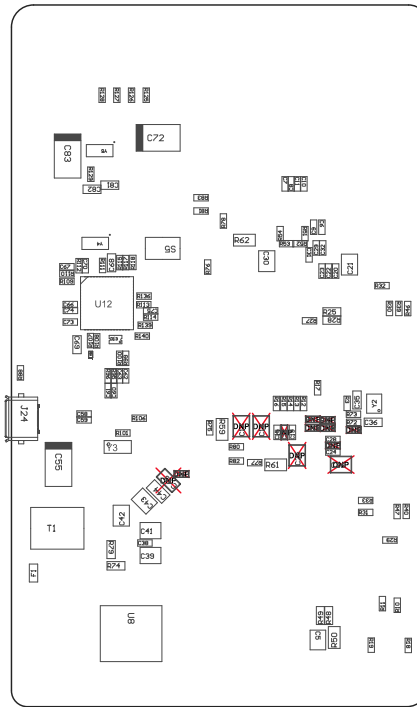


Figure 27. Bottom Overlay

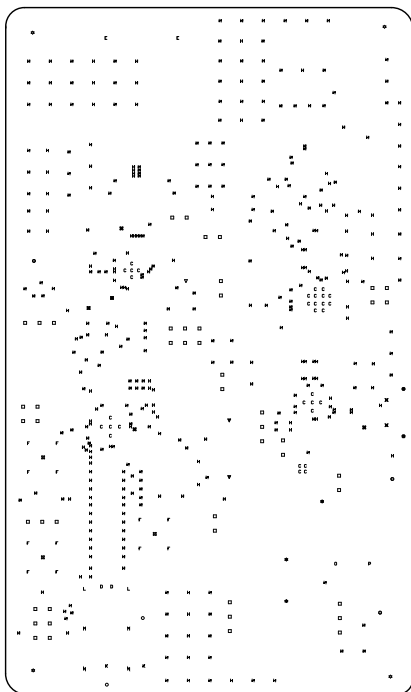
## 6.10 Board Assembly



**Figure 28. Top Assembly**



**Figure 29. Bottom Assembly**



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
▽	2	38,37mil (1,000mm)		NPTH	Round	Top Layer - Bottom Layer
○	2	62,99mil (1,600mm)		NPTH	Round	Top Layer - Bottom Layer
K	2	96,61mil (2,200mm)		NPTH	Round	Top Layer - Bottom Layer
E	2	127,95mil (3,250mm)		NPTH	Round	Top Layer - Bottom Layer
H	374	6,20mil (0,152mm)		PTH	Round	Top Layer - Bottom Layer
C	31	7,87mil (0,200mm)		PTH	Round	Top Layer - Bottom Layer
⊗	5	10,00mil (0,254mm)		PTH	Round	Top Layer - Bottom Layer
▽	1	16,00mil (0,406mm)		PTH	Round	Top Layer - Bottom Layer
☆	3	26,00mil (0,711mm)		PTH	Round	Top Layer - Bottom Layer
⊗	4	37,99mil (0,965mm)		PTH	Round	Top Layer - Bottom Layer
D	2	38,37mil (1,000mm)		PTH	Round	Top Layer - Bottom Layer
□	49	40,00mil (1,016mm)		PTH	Round	Top Layer - Bottom Layer
⊗	3	50,00mil (1,270mm)		PTH	Round	Top Layer - Bottom Layer
F	12	66,93mil (1,700mm)		PTH	Round	Top Layer - Bottom Layer
⊗	3	96,43mil (2,500mm)		PTH	Round	Top Layer - Bottom Layer
⊗	2	23,62mil (0,600mm)		PTH	Slot	Top Layer - Bottom Layer
X	2	27,56mil (0,700mm)		PTH	Slot	Top Layer - Bottom Layer
L	2	38,37mil (1,000mm)		PTH	Slot	Top Layer - Bottom Layer
M	2	38,37mil (1,000mm)		PTH	Slot	Top Layer - Bottom Layer
N	2	38,37mil (1,000mm)		PTH	Slot	Top Layer - Bottom Layer
P	1	38,37mil (1,000mm)		PTH	Slot	Top Layer - Bottom Layer
O	1	38,37mil (1,000mm)		PTH	Slot	Top Layer - Bottom Layer
507 Total						

Slot definitions: Routed Path Length = Calculated from tool start centre position to tool end centre position.  
 Hole Length = Routed Path Length + Tool Size + Slot Length as defined in the PCB layout

Figure 30. Drill Drawing

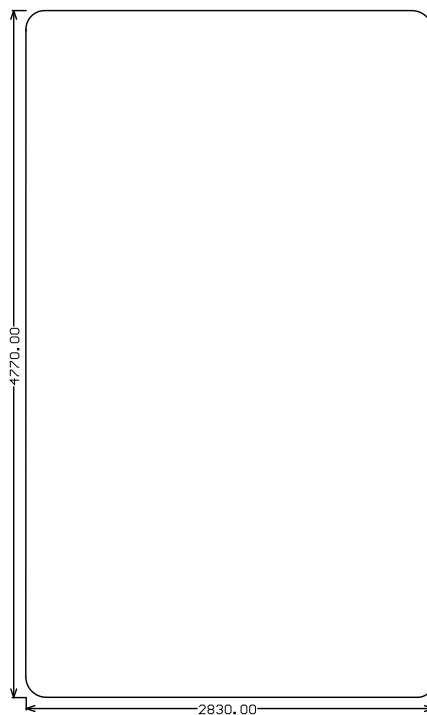


Figure 31. Board Dimensions

7 Bill of Materials

Table 4. Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C2, C44, C50	3	1 $\mu$ F	CAP, CERM, 1 $\mu$ F, 16 V, +/- 10%, X5R, 0805	GRM216R61C105KA88D	MuRata
C3, C4	2	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 50 V, +/- 10%, X7R, 0603	GCM188R71H104KA57D	MuRata
C5	1	4700 pF	CAP, CERM, 4700 pF, 2000 V, +/- 10%, X7R, 1210	C1210C472KGRACTU	Kemet
C6, C8, C10, C12	4	1 $\mu$ F	CAP, CERM, 1 $\mu$ F, 10 V, +/- 10%, X7S, 0402	C1005X7S1A105K050BC	TDK
C7, C9, C11, C13, C53, C56, C57, C64, C65, C66, C73, C74, C84, C85, C86	15	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 16 V, +/- 10%, X7R, 0402	GRM155R71C104KA88D	MuRata
C14	1	4700 pF	CAP, CERM, 4700 pF, 2000 V, +/- 10%, X7R, 1812	1812GC472KAT1A	AVX
C15, C20, C24, C29	4	100 pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H101J050BA	TDK
C19, C23, C28, C32, C37	5	1000 pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0402	CGA2B2C0G1H102J050BA	TDK
C21, C30, C39, C41, C43, C47, C49	7	10 $\mu$ F	CAP, CERM, 10 $\mu$ F, 25 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	CGA6P1X7R1E106M250AC	TDK
C22, C31, C38	3	0.01 $\mu$ F	CAP, CERM, 0.01 $\mu$ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
C33, C34, C35, C36	4	22 pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, AEC-Q200 Grade 1, 0603	CGA3E2C0G1H220J080AA	TDK
C40, C42, C48	3	22 $\mu$ F	CAP, CERM, 22 $\mu$ F, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	CGA6P1X7R1C226M250AC	TDK
C54	1	2.2 $\mu$ F	CAP, CERM, 2.2 $\mu$ F, 16 V, +/- 20%, X7S, AEC-Q200 Grade 1, 0603	CGA3E1X7S1C225M080AC	TDK
C55	1	4.7 $\mu$ F	CAP, TA, 4.7 $\mu$ F, 35 V, +/- 10%, 1.3 ohm, SMD	293D475X9035D2TE3	Vishay-Sprague
C58, C59, C60, C61, C62, C63	6	22 pF	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0402	C1005C0G1H220J050BA	TDK
C67, C75	2	33 pF	CAP, CERM, 33 pF, 50 V, +/- 5%, C0G/NP0, 0402	C1005C0G1H330J050BA	TDK
C68, C71, C78, C82	4	0.22 $\mu$ F	CAP, CERM, 0.22 $\mu$ F, 50 V, +/- 10%, X5R, 0603	C1608X5R1H224K080AB	TDK
C69	1	0.47 $\mu$ F	CAP, CERM, 0.47 $\mu$ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	CGA3E3X7R1H474K080AB	TDK
C70, C80	2	1000 pF	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0402	C1005NP01H102J050BA	TDK
C72, C83	2	10 $\mu$ F	CAP, TA, 10 $\mu$ F, 35 V, +/- 10%, 0.125 ohm, SMD	TPSD106K035R0125	AVX
C76, C77, C87, C88	4	10 pF	CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0603	CGA3E2NP01H100D080AA	TDK

**Table 4. Bill of Materials (continued)**

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
C79	1	0.47 $\mu$ F	CAP, CERM, 0.47 $\mu$ F, 50 V, +/- 10%, X6S, 0603	C1608X6S1H474K080AB	TDK
C81	1	4.7 $\mu$ F	CAP, CERM, 4.7 $\mu$ F, 35 V, +/- 10%, X5R, 0603	C1608X5R1V475K080AC	TDK
D1, D2, D3, D4, D6, D7, D8, D9, D11, D13	10	Green	LED, Green, SMD	QTLP630C4TR	Everlight
D5, D10	2	60 V	Diode, Schottky, 60 V, 1 A, AEC-Q101, SMA	NRVBA160T3G	ON Semiconductor
D12	1	Orange	LED, Orange, SMD	SML-P12DTT86	Rohm
D14, D15, D16	3	Rg	LED, Rg, SMD	HSMF-C165	Avago
F1	1		Fuse, 3 A, 32 VDC, SMD	F0603E3R00FSTR	AVX
J1, J27	2		Header, 100 mil, 2x2, Gold, TH	TSW-102-07-G-D	Samtec
J2, J9	2		Header, 100 mil, 3x2, Gold, TH	TSW-103-07-G-D	Samtec
J3	1		Header(shrouded), 2mm, 7x2, Tin, SMT	87832-1420	Molex
J4, J11, J12	3		JACK, SMB 50 Ohm, TH	903-499J-51P2	Amphenol RF
J5, J6, J18, J22, J23	5		Header, 100 mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
J7	1		Header(shrouded), 6 Power, 2 Signal, TH	0-2290024-1	TE Connectivity
J8	1		Connector, RJ-45 with integrated magnetics, 1x1, Gold, R/A, SMT	J3011G21DNL	Pulse Engineering
J10, J16, J19, J20, J21, J25, J26	7		Header, 100 mil, 2x1, Gold, TH	TSW-102-07-G-S	Samtec
J13, J15, J17	3	Double	Terminal, Turret, TH, Double	1502-2	Keystone
J14	1		Power Jack, 2 mm, R/A, TH	TH PJ-037AH	CUI Inc.
J24	1		Connector, Receptacle, Micro-USB Type AB, R/A, Bottom Mount SMT	0475890001	Molex
L1	1	200 $\mu$ H	Coupled inductor, 200 $\mu$ H, 4.5 ohm, AEC-Q200 Grade 2, SMD	DLW43MH201XK2L	MuRata
R1, R2, R64, R69	4	2.21k	RES, 2.21k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	TNPW06032K21BEEA	Vishay-Dale
R3, R4, R5, R6, R7, R8, R9, R12, R13, R14, R15, R16, R17, R20, R21, R22, R23, R29, R65, R66, R67, R68, R71, R72, R73, R75, R76, R77, R78, R135, R136, R137, R138, R139, R140	35	0	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	Yageo America
R10, R11, R18, R19, R27, R30, R31, R37, R38, R39, R40, R56, R58, R125, R126, R127, R128	17	2.49k	RES, 2.49k, 1%, 0.063 W, 0402	CRCW04022K49FKED	Vishay-Dale
R24, R25	2	6.20k	RES, 6.20k, 1%, 0.1 W, 0603	RC0603FR-076K2L	Yageo America
R26, R28	2	1.96k	RES, 1.96k, 1%, 0.1 W, 0603	CRCW06031K96FKEA	Vishay-Dale



Table 4. Bill of Materials (continued)

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
R32, R33, R46, R47, R55, R57, R80, R81, R82, R83, R87, R107, R108, R119, R120, R121, R122, R123, R124	19	470	RES, 470, 5%, 0.063 W, 0402	CRCW0402470RJNED	Vishay-Dale
R48, R49	2	1.00k	RES, 1.00k, 1%, 0.1 W, 0603	CRCW06031K00FKEA	Vishay-Dale
R50	1	100k	RES, 100k, 5%, 0.125 W, 0805	CRCW0805100KJNEA	Vishay-Dale
R51, R52, R53, R54	4	49.9	RES, 49.9, 1%, 0.063 W, 0402	CRCW040249R9FKED	Vishay-Dale
R59, R60, R61, R62	4	0	RES, 0, 5%, 0.125 W, 0805	ERJ-6GEY0R00V	Panasonic
R74, R84	2	4.22k	RES, 4.22k, 1%, 0.1 W, 0603	CRCW06034K22FKEA	Vishay-Dale
R79, R85	2	2.40k	RES, 2.40k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	ERA-3AEB242V	Panasonic
R86	1	10.0k	RES, 10.0k, 1%, 0.063 W, 0402	CRCW040210K0FKED	Vishay-Dale
R88	1	33	RES, 33, 5%, 0.063 W, 0402	CRCW040233R0JNED	Vishay-Dale
R89, R101	2	1.50k	RES, 1.50k, 1%, 0.063 W, 0402	CRCW04021K50FKED	Vishay-Dale
R90	1	10k	RES, 10k, 5%, 0.063 W, 0402	CRCW040210K0JNED	Vishay-Dale
R91, R92, R93, R94, R97, R98	6	22	RES, 22, 5%, 0.063 W, 0402	CRCW040222R0JNED	Vishay-Dale
R95, R96, R99, R100, R103, R104, R105, R106	8	15.0k	RES, 15.0k, 1%, 0.063 W, 0402	CRCW040215K0FKED	Vishay-Dale
R102, R112, R130	3	47k	RES, 47k, 5%, 0.063 W, 0402	CRCW040247K0JNED	Vishay-Dale
R109	1	240k	RES, 240k, 5%, 0.063 W, 0402	CRCW0402240KJNED	Vishay-Dale
R110	1	150k	RES, 150k, 5%, 0.063 W, 0402	CRCW0402150KJNED	Vishay-Dale
R111, R129, R134	3	0	RES, 0, 5%, 0.063 W, 0402	CRCW04020000Z0ED	Vishay-Dale
R113, R114	2	220k	RES, 220k, 5%, 0.063 W, 0402	CRCW0402220KJNED	Vishay-Dale
R115, R117, R141, R142	4	27	RES, 27, 5%, 0.063 W, 0402	CRCW040227R0JNED	Vishay-Dale
R116, R131	2	1.40k	RES, 1.40k, 1%, 0.063 W, 0402	CRCW04021K40FKED	Vishay-Dale
R118, R133	2	1.00Meg	RES, 1.00 M, 1%, 0.063 W, 0402	CRCW04021M00FKED	Vishay-Dale
R132	1	100	RES, 100, 1%, 0.063 W, 0402	CRCW0402100RFKED	Vishay-Dale
Rs1	1	4.87k	RES, 4.87k, 1%, 0.063 W, 0402	CRCW04024K87FKED	Vishay-Dale
S1, S2, S4, S5	4		Switch, Normally open, 2.3N force, 200k operations, SMD	KSR221GLFS	C&K Components
S3	1		Switch, SPST 4 Pos, Top Actuated, SMT	219-4LPST CTS	Electrocomponents
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14	14		Shunt, 100 mil, Gold plated, Black	881545-2	TE Connectivity
T1	1		Common Mode Filter for Power Line	ACM9070-701-2PL	TDK

**Table 4. Bill of Materials (continued)**

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PART NUMBER	MANUFACTURER
U5	1		1, 4, 6 CHANNEL PROTECTION SOLUTION FOR SUPER-SPEED (UP TO 6 GBPS) INTERFACE, DQA0010A	TPD4E05U06QDQARQ1	Texas Instruments
U6	1		DP83TC811, RND0036A	DP83TC811RWRNDRQ	Texas Instruments
U7	1		10/100 Ethernet PHY, RHB0032B	DP83822RHBR	Texas Instruments
U8, U9	2		Single Output Fast Transient Response LDO, 1.5 A, Adjustable 1.21-V to 20-V Output, 2.1-V to 20-V Input, 5-pin DDPK (KTT), -40 to 125°C, Green (RoHS & no Sb/Br)	TL1963AQKTTRQ1	Texas Instruments
U10	1		Single Output Automotive LDO, 1 A, Fixed 3.3-V Output, 2.2-V to 5.5-V Input, with Reverse Current Protection, 8-pin SON (DRB), -40 to 125°C, Green (RoHS & no Sb/Br)	TPS73733QDRBRQ1	Texas Instruments
U11	1		4-Port Full-Speed USB Hub, 3.3V, -40 to 85°C, 32-Pin QFN (RHB), Green (RoHS & no Sb/Br)	TUSB2046BIRHBT	Texas Instruments
U12	1		25-MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 47 GPIOs, -40 to 85°C, 64-pin QFN (RGC), Green (RoHS & no Sb/Br)	MSP430F5528IRGCR	Texas Instruments
U13	1		25-MHz Mixed Signal Microcontroller with 128 KB Flash, 8192 B SRAM and 63 GPIOs, -40 to 85°C, 80-pin QFP (PN), Green (RoHS & no Sb/Br)	MSP430F5529IPN	Texas Instruments
Y1, Y2	2		Crystal, 25 MHz, 12 pF, SMD	ABM8AIG-25.000MHZ-12-2Z-T3	Abracon Corporation
Y3	1		Ceramic Resonator, 6 MHz, 15 pF, SMD	PBRC6.00MR50X000	AVX
Y4, Y5	2		Resonator, 4 MHz, 39 pF SMD	CSTCR4M00G15L99-R0	MuRata
C1, C18, C27, C46, C52	0	0.01 $\mu$ F	CAP, CERM, 0.01 $\mu$ F, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	CGA2B3X7R1H103K050BB	TDK
C16, C25	0	22 $\mu$ F	CAP, CERM, 22 $\mu$ F, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	CGA6P1X7R1C226M250AC	TDK
C17, C26	0	10 $\mu$ F	CAP, CERM, 10 $\mu$ F, 25 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	CGA6P1X7R1E106M250AC	TDK
C45, C51	0	0.1 $\mu$ F	CAP, CERM, 0.1 $\mu$ F, 16 V, +/- 10%, X7R, 0805	GRM219R71C104KA01D	MuRata
R34, R35, R36, R41, R42, R43, R44, R45	0	2.49k	RES, 2.49k, 1%, 0.063 W, 0402	CRCW04022K49FKED	Vishay-Dale
R63	0	2.21k	RES, 2.21k, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0603	TNPW06032K21BEEA	Vishay-Dale
R70	0	0	RES, 0, 5%, 0.063 W, 0402	RC0402JR-070RL	Yageo America



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