LMG3410R150-031 EVM User Guide

The LMG3410EVM-031 features two LMG3410R150 600V GaN power transistors with integrated drivers that are configured in a half bridge with all the required bias circuit and logic/power level shifting. Essential power stage and gate driving high frequency current loops are fully enclosed on the board to minimize parasitic inductances, reducing voltage overshoots and improving performance. The LMG3410EVM-031 is configured to have a socket style external connection for easy interface with external power stages to run the LMG3410R150 in various applications.

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Trademarks

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1 LMG3410EVM-031 User's Guide General TI High Voltage Evaluation User Safety Guidelines

Always follow TI's set-up and application instructions, including use of all interface components within their recommended electrical rated voltage and power limits. Always use electrical safety precautions to help ensure your personal safety and the safety of those working around you. Contact TI's Product Information Center http://support/ti./com for further information.

Save all warnings and instructions for future reference.

Failure to follow warnings and instructions may result in personal injury, property damage, or death due to electrical shock and/or burn hazards.

The term TI HV EVM refers to an electronic device typically provided as an open framed, unenclosed printed circuit board assembly. It is intended strictly for use in development laboratory environments, solely for qualified professional users having training, expertise, and knowledge of electrical safety risks in development and application of high-voltage electrical circuits. Any other use and/or application are strictly prohibited by Texas Instruments. If you are not suitably qualified, you must immediately stop from further use of the HV EVM.

- **Work Area Safety:**
  - Maintain a clean and orderly work area .
  - Qualified observer(s) must be present anytime circuits are energized.
  - Effective barriers and signage must be present in the area where the TI HV EVM and its interface electronics are energized, indicating operation of accessible high voltages may be present, for the purpose of protecting inadvertent access.
  - All interface circuits, power supplies, evaluation modules, instruments, meters, scopes and other related apparatus used in a development environment exceeding 50 V_{RMS}/75 VDC must be electrically located within a protected Emergency Power Off (EPO) protected power strip.
  - Use a stable and non-conductive work surface.
  - Use adequately insulated clamps and wires to attach measurement probes and instruments. No freehand testing whenever possible.
- **Electrical Safety:**

  As a precautionary measure, it is always a good engineering practice to assume that the entire EVM may have fully accessible and active high voltages.
  - De-energize the TI HV EVM and all its inputs, outputs, and electrical loads before performing any electrical or other diagnostic measurements. Confirm that TI HV EVM power has been safely de-energized.
  - With the EVM confirmed de-energized, proceed with required electrical circuit configurations, wiring, measurement equipment hook-ups and other application needs, while still assuming the EVM circuit and measuring instruments are electrically live.
  - When EVM readiness is complete, energize the EVM as intended.

  WARNING: While the EVM is energized, never touch the EVM or its electrical circuits as they could be at high voltages capable of causing electrical shock hazard.
- **Personal Safety:**
  - Wear personal protective equipment, for example, latex gloves and/or safety glasses with side shields or protect EVM in an adequate lucent plastic box with interlocks from accidental touch.
- **Limitation for Safe Use:**
  - EVMs are not to be used as all or part of a production unit.

Safety and Precautions

The EVM is designed for professionals who have received the appropriate technical training, and is designed to operate from an AC power supply or a high-voltage DC supply. Please read this user guide and the safety-related documents that come with the EVM package before operating this EVM.

CAUTION

Do not leave the EVM powered when unattended.

WARNING

Hot surface! Contact may cause burns. Do not touch!

WARNING

High Voltage! Electric shock is possible when connecting board to live wire. Board must be handled with care by a professional.

For safety, use of isolated test equipment with overvoltage and overcurrent protection is highly recommended.

2 Description

The LMG3410EVM-031 operates as a daughter card as part of a larger custom designed system or with the LMG34XX-BB-EVM breakout motherboard.

2.1 LMG3410EVM-031

The LMG3410EVM-031 configures two LMG3410R150 GaN FETs in a half bridge. All the bias and level shifting components are included, allowing low side referenced signals to control both FETs. High frequency bypass capacitors are included on the power stage in an optimized layout to minimize parasitic inductance and reduce voltage overshoot.

There are 7 logic pins on the FET card.

Table 1. Logic Pin Function Description

PIN	DESCRIPTION
AGND	Logic and bias power ground return pin. Functionally isolated from PGND.
12V	Auxiliary power input for Q2. Used as auxiliary power input for Q1 when the LMG3410EVM-031 is configured in bootstrap mode.
5V	Auxiliary power input for the LMG3410EVM-031. Used to power logic isolators. Used as input bias power of LMG3410R050 devices when configured in isolated power mode.
FA_2	FAULT signal from bottom LMG3410R150 Q2. Pin is either pulled to AGND or 5V.
FA_1	FAULT signal from top LMG3410R150 Q1 Pin is either pulled to AGND or 5V.
Q2	AGND referenced logic gate signal input for bottom LMG3410R150 Q2. Compatible with both 3.3V and 5V logic.
Q1	AGND referenced logic gate signal input for top LMG3410R150 Q1. Compatible with both 3.3V and 5V logic.

There are 3 power pins on the FET card.

Table 2. Power Pin Function Description

PIN	DESCRIPTION
VSW	Switch node of the half bridge
VDC	Input DC voltage of the half bridge
PGND	Power ground of the half bridge. Connected to AGND.

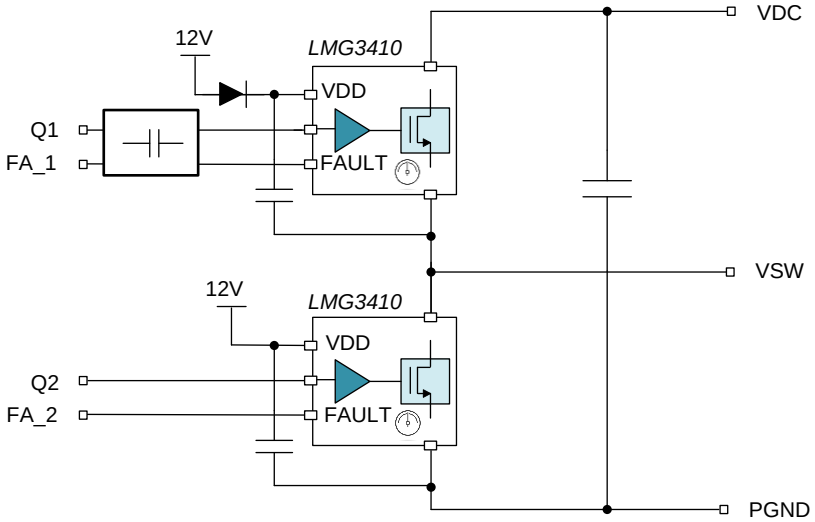

Figure 1. Simplified LMG3410EVM-031 Schematic

WARNING

To minimize the risk of electrical shock hazard caused by high-voltage levels on the evaluation module whenever it is energized, proper precautions must be taken when working with the EVM. Refer Section 1 for high voltage evaluation user safety guidelines.

2.1.1 FAULT

The FA_1 and FA_2 are the fault signal for top and bottom LMG3410EVM-031 respectively. They are active low when an under voltage lockout on an auxiliary voltage rail, over temperature or overcurrent even occurs on the LMG3410R150. The fault signal FA_1 for the top LMG3410R150 device is level shifted to AGND and the fault signal FA_2 for the bottom LMG3410R150 device is referenced to AGND.

CAUTION

Please do NOT ignore fault signal when using LMG3410EVM-031. Turn off both top and bottom devices, if any device is generating fault signal. The device under fault condition may operate in undesired 3rd-quadrant mode and may be over heated and damaged due to the high source-drain voltage drop if the other device is still switching.

2.1.2 Power Pins

While there are some power stage bypass capacitors on the LMG3410EVM-031 from VDC to PGND to minimize voltage overshoot during switching, more bulk capacitance is required to hold up the DC voltage during operation. It is highly recommended to minimize, and ideally prevent, any overlap and parasitic capacitance from VSW to VDC, PGND and any logic pins. The two grounds PGND and AGND are connected to each other on the LMG3410EVM-031.

2.1.3 Bootstrap Mode

The LMG3410EVM-031 operates in bootstrap mode, where the 12V bias voltage is used to power both LMG3410R150 devices. The isolated power supply board can be separated from the main board along the score line to save the space. The isolated power supply board must not be connected to the main board under the bootstrap mode.

2.1.4 Isolated Power Supply Mode

The LMG3410EVM-031 card can be modified to enable the top LMG3410R150 Q1 to operate in the isolated power supply mode. This can be achieved by populating a 0 Ω resistor on R1 and two 2-position sockets with 1.27 mm pitch mating such as M50-3140245 on J4 and J5. The isolated power supply board needs to be separated from the main board along the score line and placed on the main board though J4 and J5, shown in Figure 4 and Figure 5. Make sure the direction of the isolated power supply following the illustration in Figure 5. To disconnect from the boostrap mode, D1 and R2 needs to be removed. Do NOT power up the LMG3410EVM-031 when R1, R2 and D1 are all populated with the isolated power supply board connected.

2.1.5 Heatsink

The heatsink is installed to help with heat dissipation of the LMG3410R150. Exposed copper pads that are attached to the die attach pad (DAP) of both the high and low side devices are provided for a low thermal impedance point to a heatsink. The two copper pads have high voltage potential difference between them so an electrically isolative thermal interface material (TIM) is required. Please refer to Section 8 for the recommended TIM and mechanical fixture.

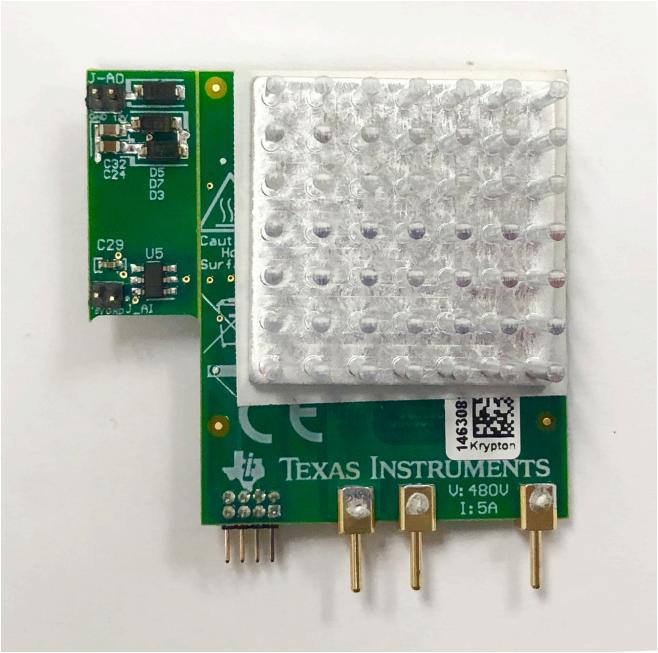

Figure 2. Top Side View of LMG3410EVM-031

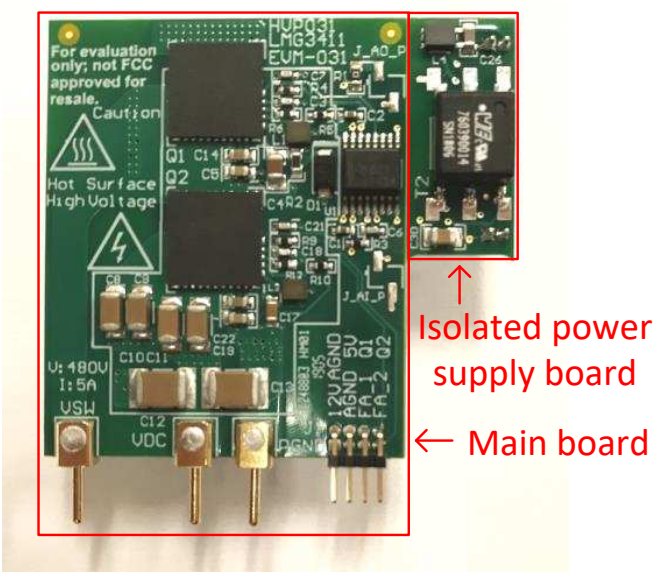

Figure 3. Back Side View of LMG3410EVM-031

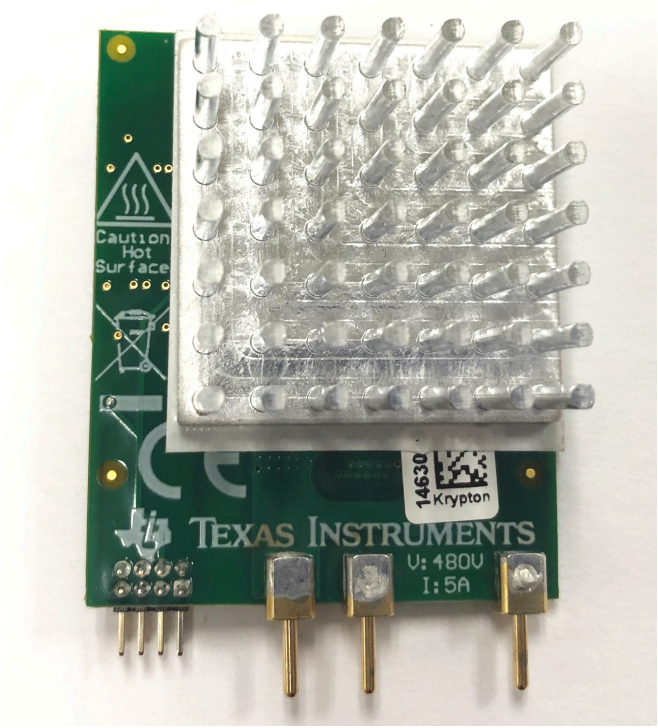

Figure 4. Top Side View of LMG3410EVM-031 in Isolated Power Supply Configuration

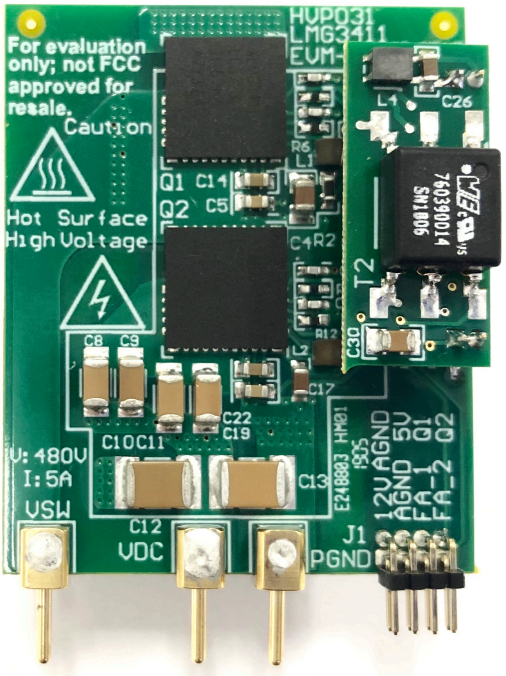

Figure 5. Back Side View of LMG3410EVM-031 in Isolated Power Supply Configuration

2.2 LMG34XX-BB-EVM

To allow for quick operation the LMG34XX-BB-EVM is available to interface with the LMG3410EVM-031. This mother board is designed to operate the LMG3410R150 as a synchronous open loop buck converter. Easy probe locations are provided for measurement of logic and power stage voltages.

2.2.1 Bias Supply

The motherboard requires one 12V bias supply. When the LMG3410EVM-031 is configured in bootstrap mode the 12V input is used to power the two LMG3410R150 devices. A linear drop off regulator steps the voltage down to a tightly regulated 5V for logic power of the LMG3410R150. When the LMG3410EVM-031 is configured in isolated power supply mode the 5V is also used for auxiliary power for the top LMG3410R150 Q1.

2.2.2 Logic PWM Input

The LMG34XX-BB-EVM supports a single PWM, with complimentary signal and corresponding dead time generated on board. A 0 V to 5 V magnitude input square wave is required. The complementary PWM generation circuit creates 50 ns of dead time between both transitions of the PWM signals.

2.2.3 Fault Protection

There is an option to disable PWM input to the FET card in the event of a fault signal from the LMG3410EVM-031. When the FAULT Protect jumper is placed in the EN mode PWM is disabled when either LMG3410R050 has an active fault. This disable is not latching, so when the fault clears PWM immediately resumes. If FAULT Protect mode is not desired it can be disabled by placing the jumper in the DIS position. The FAULT LED will still illuminate when either LMG3410R150 has an active fault, regardless of the position of FAULT Protect jumper.

2.3 Typical Applications

The LMG3410EVM-031 is designed for use in AC/DC, DC/DC and DC/AC applications.

- Totem-Pole PFC converters
- Phase-Shifted Full Bridge or LLC Converter
- Buck converter such as the LMG34XX-BB-EVM

2.4 Features

The LMG3410EVM-031 has the following features and specifications:

- Two options to bias the LMG3410, from bootstrap diode or using isolated power
- Over temperature, overcurrent, and under voltage lockout protection with FAULT indication that is level shifted to an AGND referenced signal
- Gate logic input support of either 3.3V or 5V logic
- Maximum recommended operating voltage of 480V and absolute maximum voltage of 600V

The LMG34XX-BB-EVM has the following features and specifications:

- Requires only a single 12V bias supply
- Requires only a single 0V to 5V PWM input to generate gate drive signal
- PWM disable in the event of a fault from the LMG3410EVM-031
- Maximum recommended operating voltage of 480V and absolute maximum voltage of 600V
- Maximum recommended operating inductor current of 5A

3 Schematic

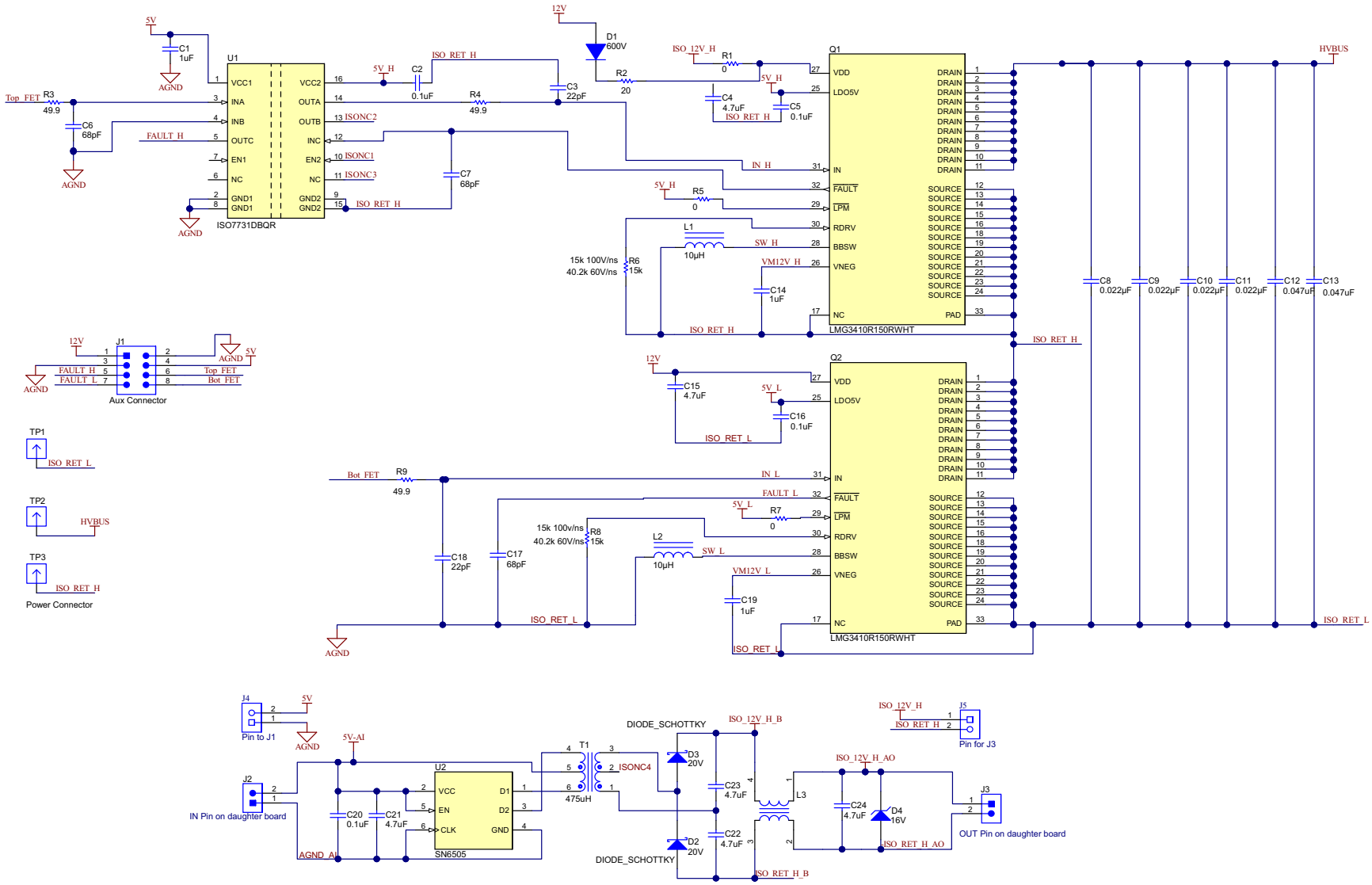

Figure 6. LMG3410EVM-031 Schematic

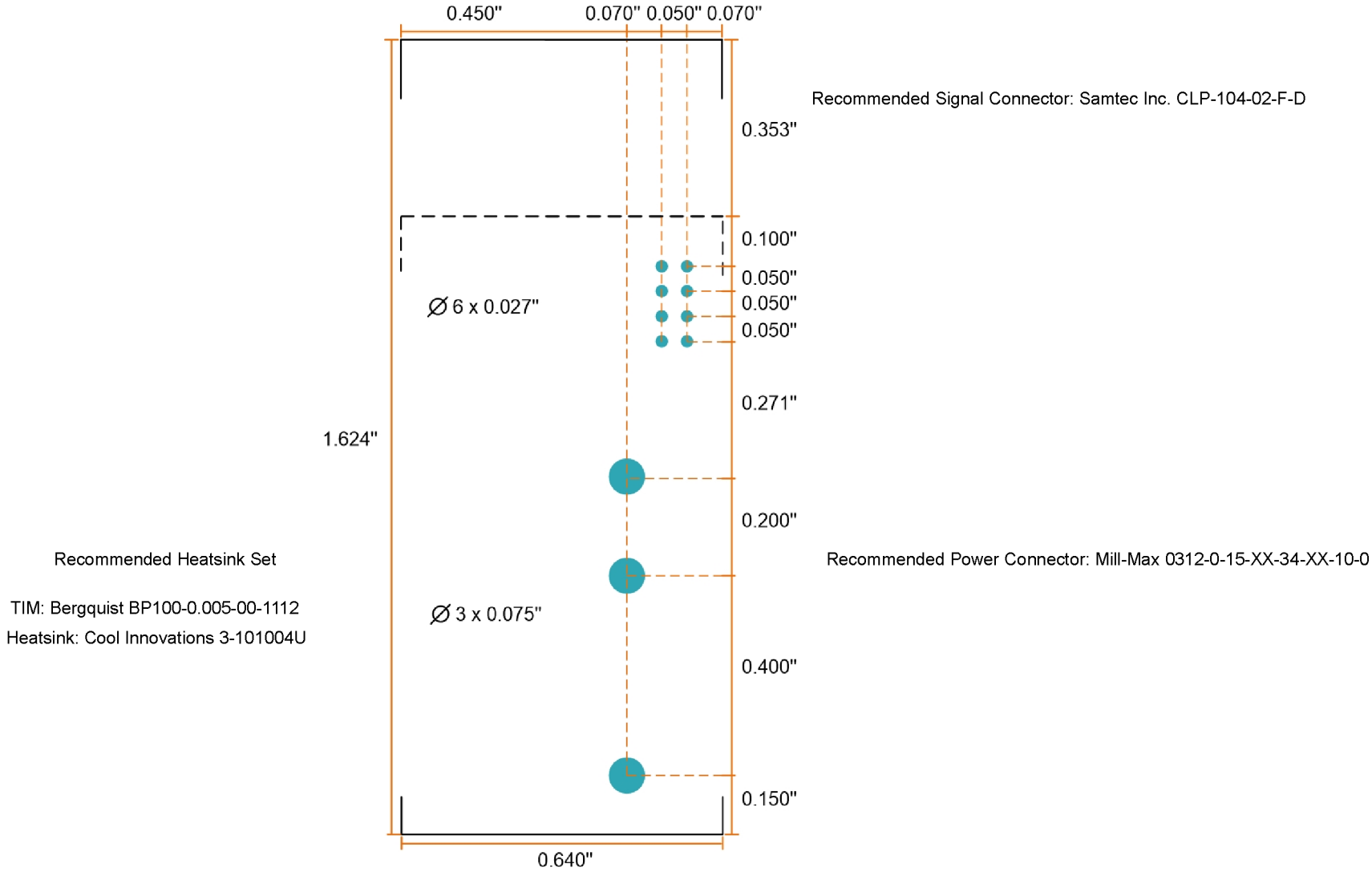

Figure 7. Recommended Footprint for LMG3410EVM-031

TI HV Synchronous Buck Motherboard

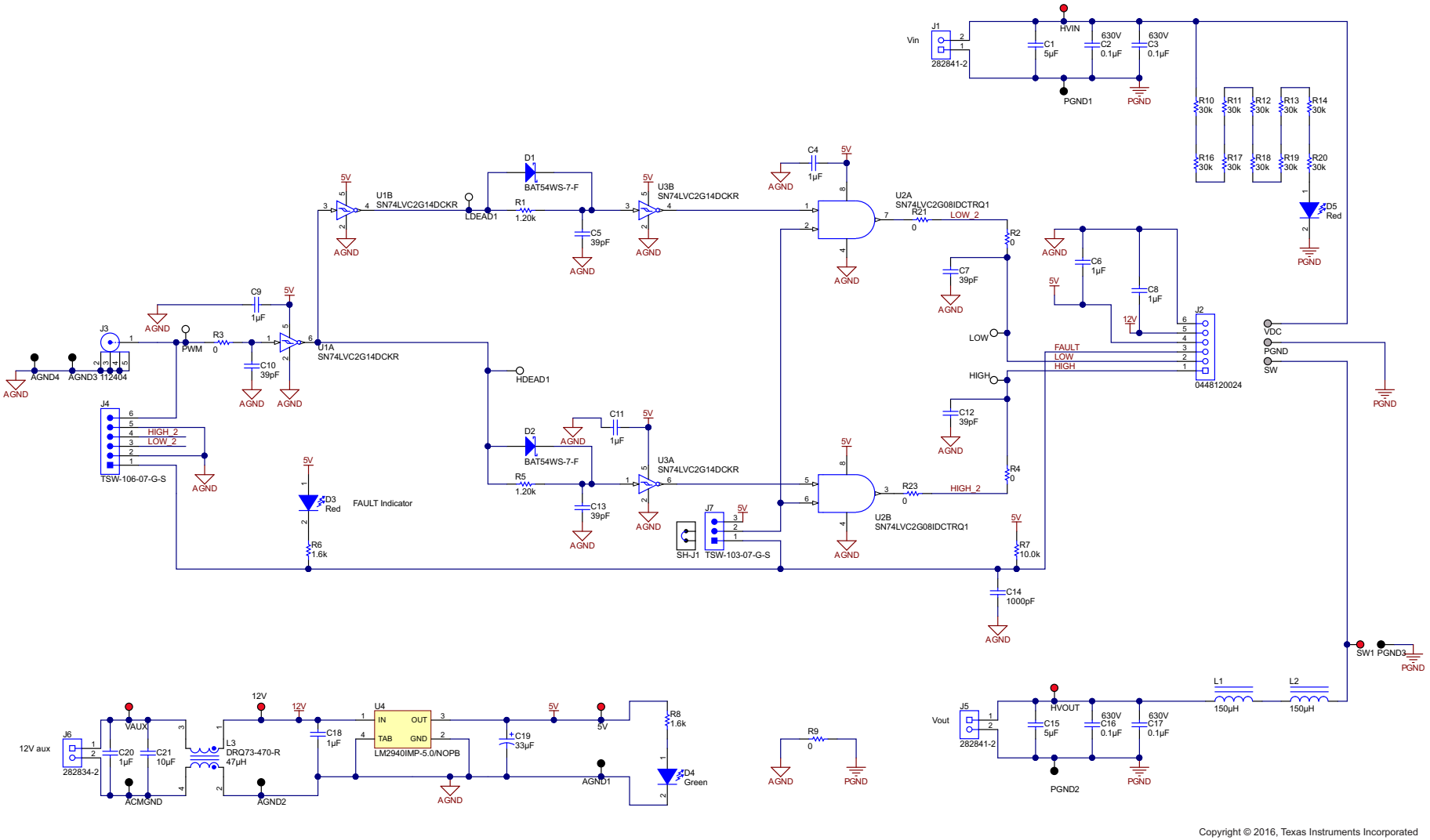

Figure 8. LMG34XX-BB-EVM Schematic

4 Test Setup

4.1 Test Equipment

DC Voltage Source: Capable of supplying the input of the EVM up to 480 V.

DC Bias Source: Capable of 12 V output at up to 0.7 A.

Function Generator: Capable of 0 V to 5 V square wave output with adjustable duty cycle and frequency in desired operating range. It is recommended to operate the LMG3410EVM-018 and LMG34XX-BB-EVM with a switching frequency between 50 kHz to 200 kHz.

Oscilloscope: Capable of at least 200 MHz operation. A 1 GHz or greater oscilloscope and probes with short ground springs are recommended for accurate measurements.

DC Multimeter(s): Capable of 600 V measurement, suitable for determining operation and efficiency (if desired).

DC Load: Capable of 600 V operation at up to 5 A in current-mode operation.

Fan: 200 LFM minimum airflow is recommended.

4.2 Recommended Test Setup

The LMG3410EVM-031 connects to the LMG34XX-BB-EVM as Figure 9 shows.

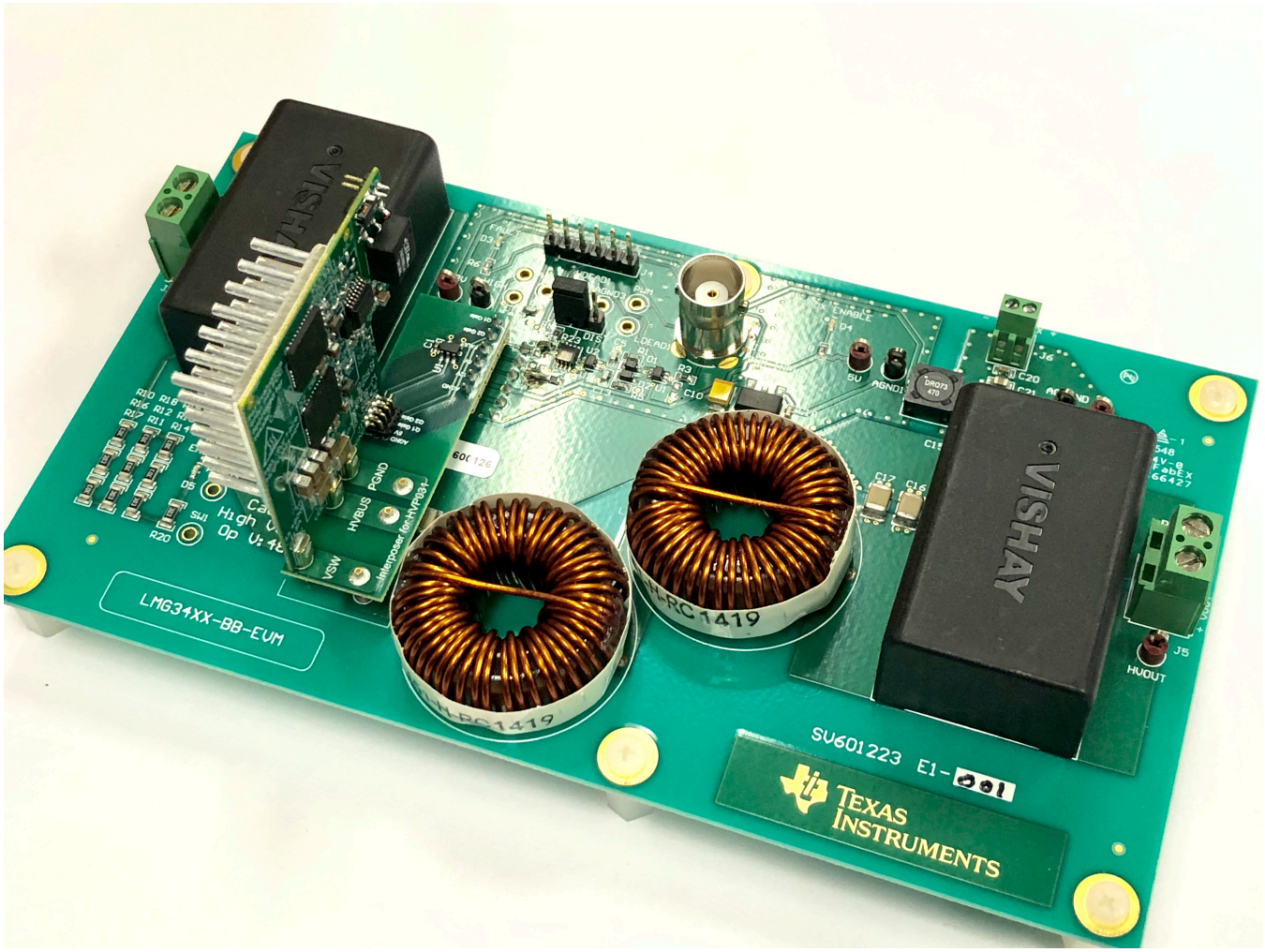

Figure 9. LMG3410EVM-031 Connected with LMG34XX-BB-EVM

The LMG34XX-BB-EVM power and probe connection points are shown in Figure 10.

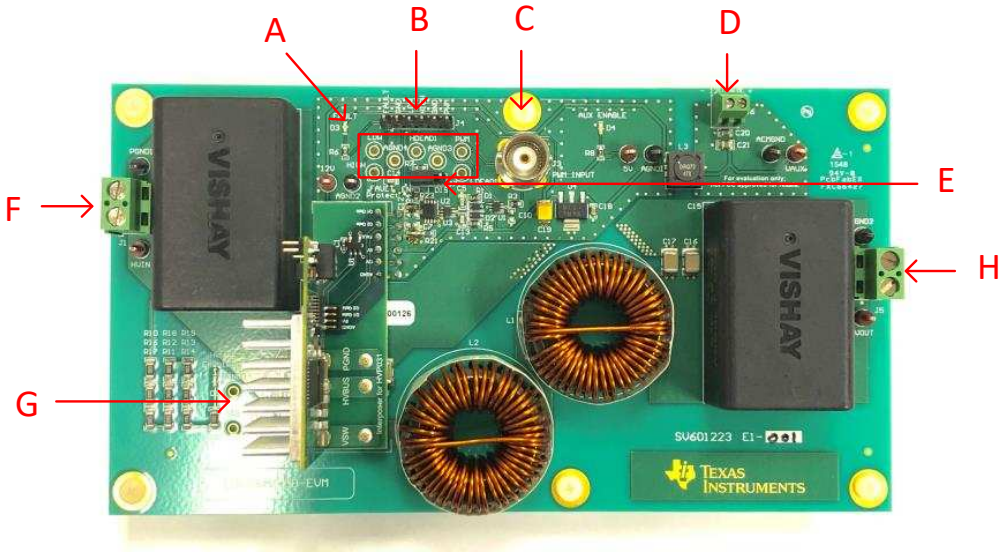

Figure 10. Recommended Connection Points

PCB Notes:

- A: Probe points for gate drive logic
- B:100 mil header for PWM input, PWM signals to LMG3410EVM-018 and FAULT output
- C: BNC connector for PWM input
- D: 12V bias supply input
- E: FAULT Protection option header
- F: Power stage high voltage input
- G: Probe point for power stage switch node
- H: Power stage high voltage output

WARNING

To minimize the risk of the electrical shock and burn hazard, precautions must be taken when handling the board due to the high voltages and elevated temperatures on the EVM.

4.3 List of Test Points

Key test points on this EVM have been designed for use with oscilloscope probes with short ground springs. Using the short ground spring instead of the alligator ground lead will minimize measurement error and produce a cleaner signal with the fast switching GaN devices used on this EVM. The data shown in this user guide has been obtained using such a measurement method.

Table 3. Test Point Functional Description

NAME	DESCRIPTION
VAUX	12 V bias input connection before filter
ACMGND	Ground for 12 V bias input before filter
5V	5 V bias
AGND1	Analog ground for logic
PWM	Single input PWM signal
LDEAD1	Low side PWM signal before dead time generation
AGND3	Analog ground for logic
HDEAD1	High side PWM signal before dead time generation
AGND4	Analog ground for logic
LOW	Low side PWM signal with dead time
HIGH	High side PWM signal with dead time
AGND2	Analog ground for logic
12V	12 V bias after filter
PGND1	Power ground
HVIN	DC input voltage
PGND2	Power ground
HVOUT	DC output voltage
PGND3	Power ground
SW1	Switch node voltage

4.4 List of Terminals

Table 4. List of Terminals

TERMINAL	NAME	DESCRIPTION
J1	VIN	Input DC voltage input
J5	VOUT	Output DC voltage output
J6	12V AUX	12 V bias voltage input
J3	PWM INPUT	Single 0 V to 5 V PWM input for gate
J4	LOGIC	Header to connect PWM, FAULT logic
J2	HB Card PIN	Connector to interface LMG3410EVM-031 board

5 Test Procedure

5.1 Setup

The following procedure is recommended to set up the LMG34XX-BB-EVM with the LMG3410EVM-031:

- Connect LMG3431EVM-018 to LMG34XX-BB-EVM.
- Connect oscilloscope or multimeter probes to desired test points as shown in A or G.
- Connect the 12 V bias supply, load to the output, and input supply to the input.
- Connect the function generator to either the BNC connector PWM input at C or 100 mil header connector input at pin 6 (PWM) and pin 5 (GND) at B.
- Cooling with an external fan is recommended to control the temperature of LMG3410R150 and the heatsink attached to it. Place the fan next to the EVM as shown in Figure 13.

5.2 Startup and Operating Procedure

The following procedure is recommended to enable the LMG34XX-BB-EVM with the LMG3410EVM-031:

1. Power up the 12 V bias supply. Ensure the top right green “Aux Enable” LED is illuminated.
2. Enable PWM on the function generator.
3. Power up high voltage input supply. Ensure the red “HV Enable” LED is illuminated when the input supply is above 20 V.

WARNING

Do NOT turn on device at absolute maximum voltage. It is recommended to start at voltages at or below 480 V, and then increase the input voltage slowly while monitoring V_{SW} to insure the peak voltage does not exceed the absolute maximum rating of 600 V.

5.3 Shutdown Procedure

1. Turn off input supply then PWM. Wait until red “HV Enable” LED turns off.
2. Disable 12 V bias supply.

5.4 Additional Operation Notes

- Fault protection on the LMG34XX-BB-EVM is not latching, so if a fault clears and the LMG34XX-BB-EVM is still operational PWM will resume.

6 Typical Characteristics

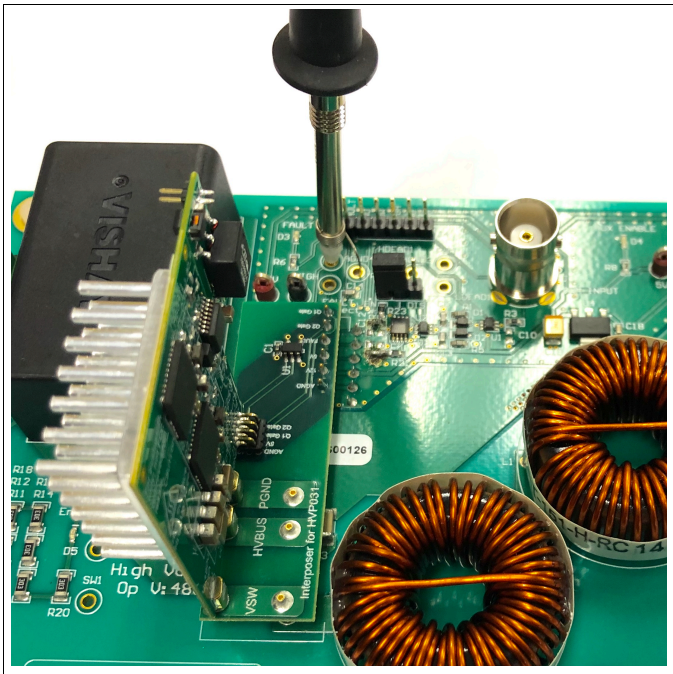

Figure 11. Recommended Probe Connection for Logic Signals

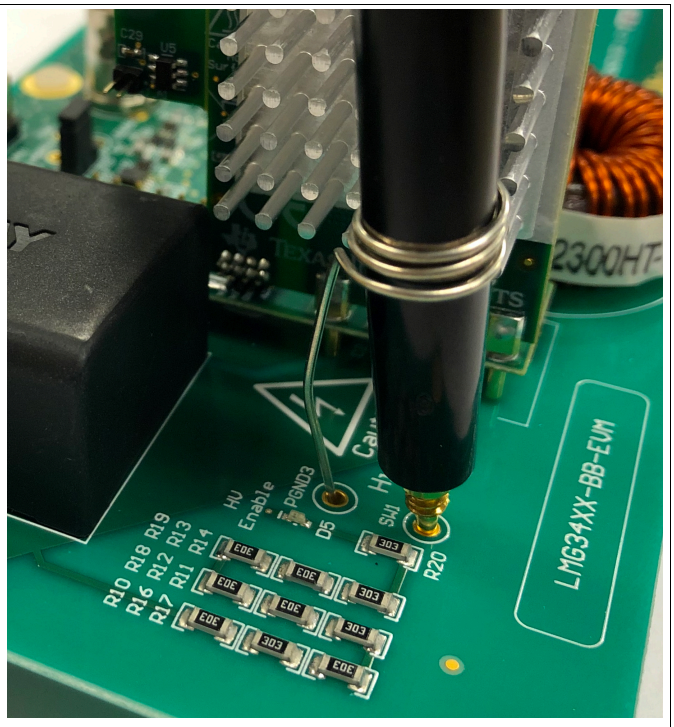

Figure 12. Recommended Probe Connection for High Voltage Switch Node

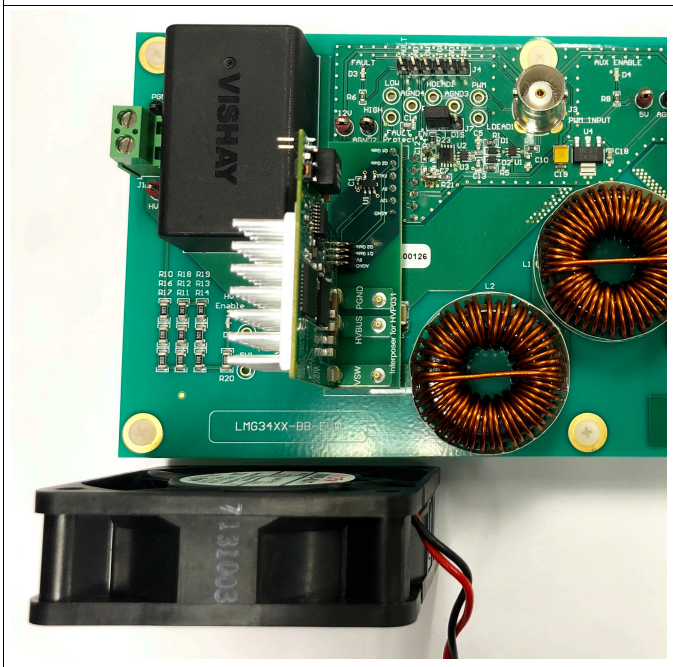

Figure 13. Recommended Configuration for Heatsink and Fan

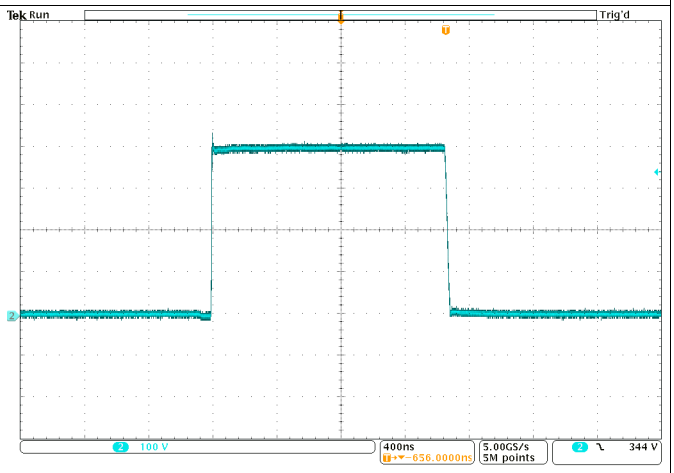

Figure 14. Switching Waveforms with 400V Input, 100kHz, 30% Duty Cycle, 4A Output

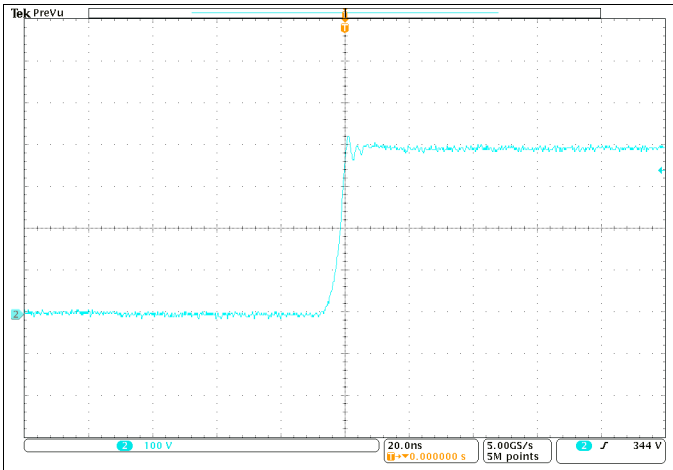

Figure 15. Low to High Transition Waveform with 400V Input, 100kHz, 30% Duty Cycle, 4A Output

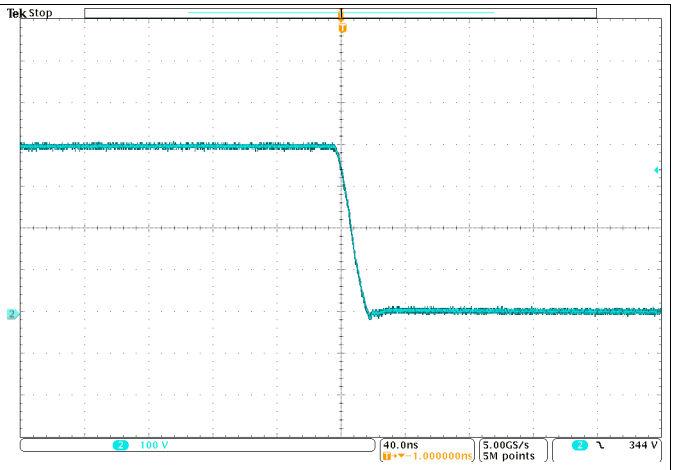

Figure 16. High to Low Transition Waveform with 400V Input, 100kHz, 30% Duty Cycle, 4A Output

7 EVM Assembly Drawing and PCB Layout

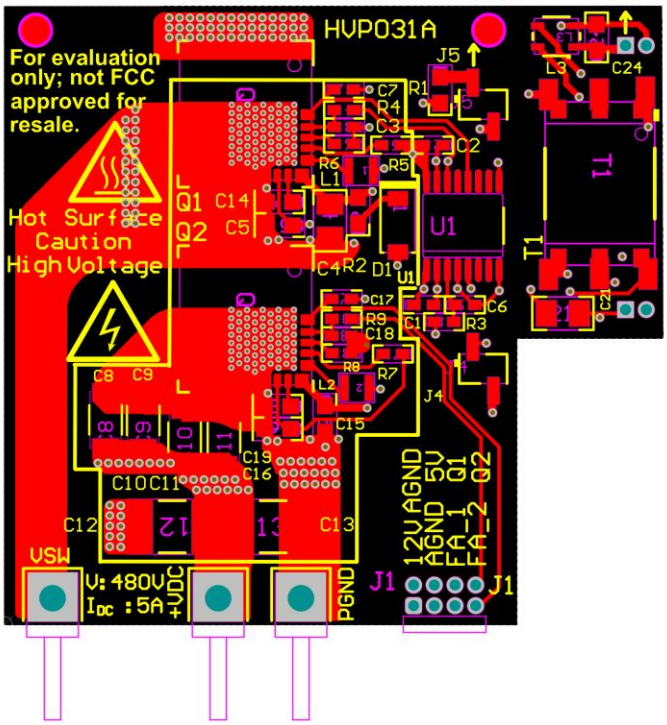

Figure 17. LMG3410EVM-031 Top Layer and Components

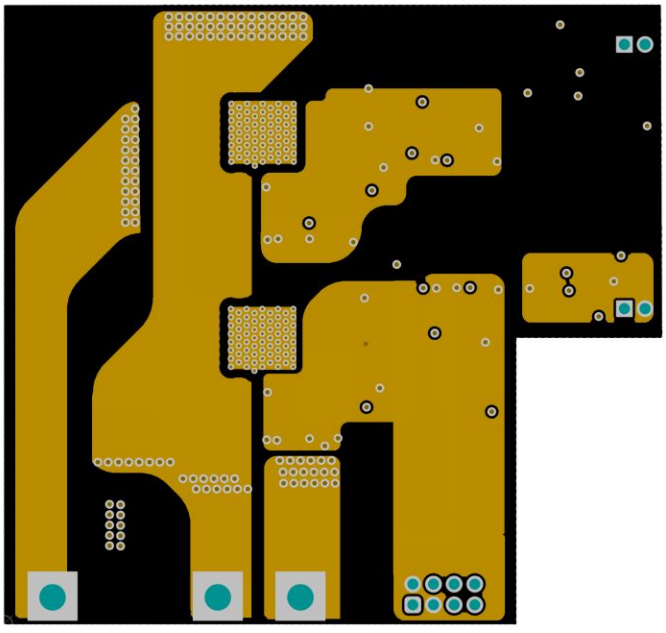

Figure 18. LMG3410EVM-031 Inner Copper Layer 1

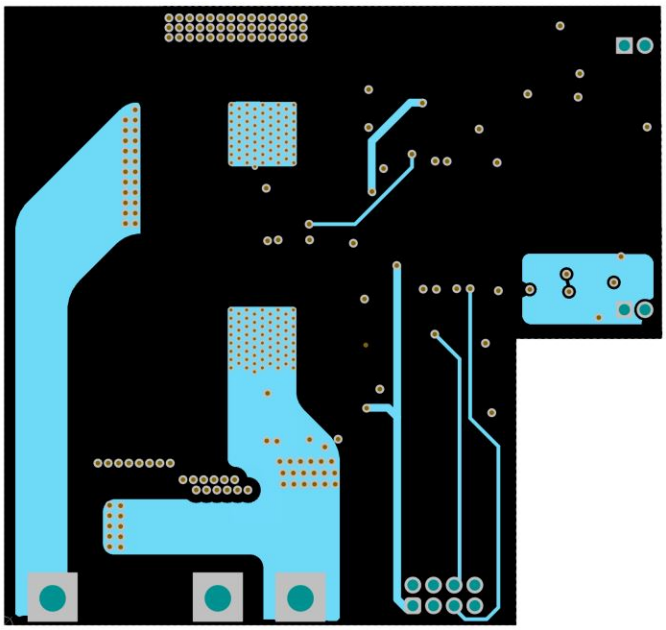

Figure 19. LMG3410EVM-031 Inner Copper Layer 2

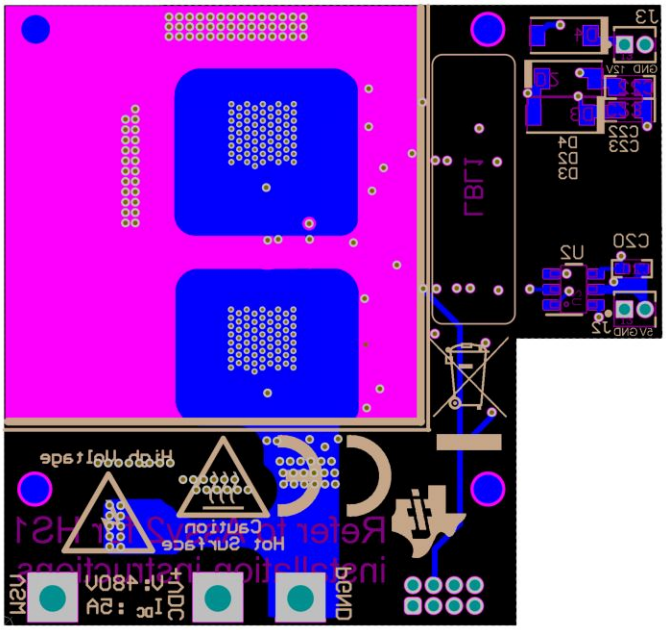

Figure 20. LMG3410EVM-031 Bottom Layer and Components

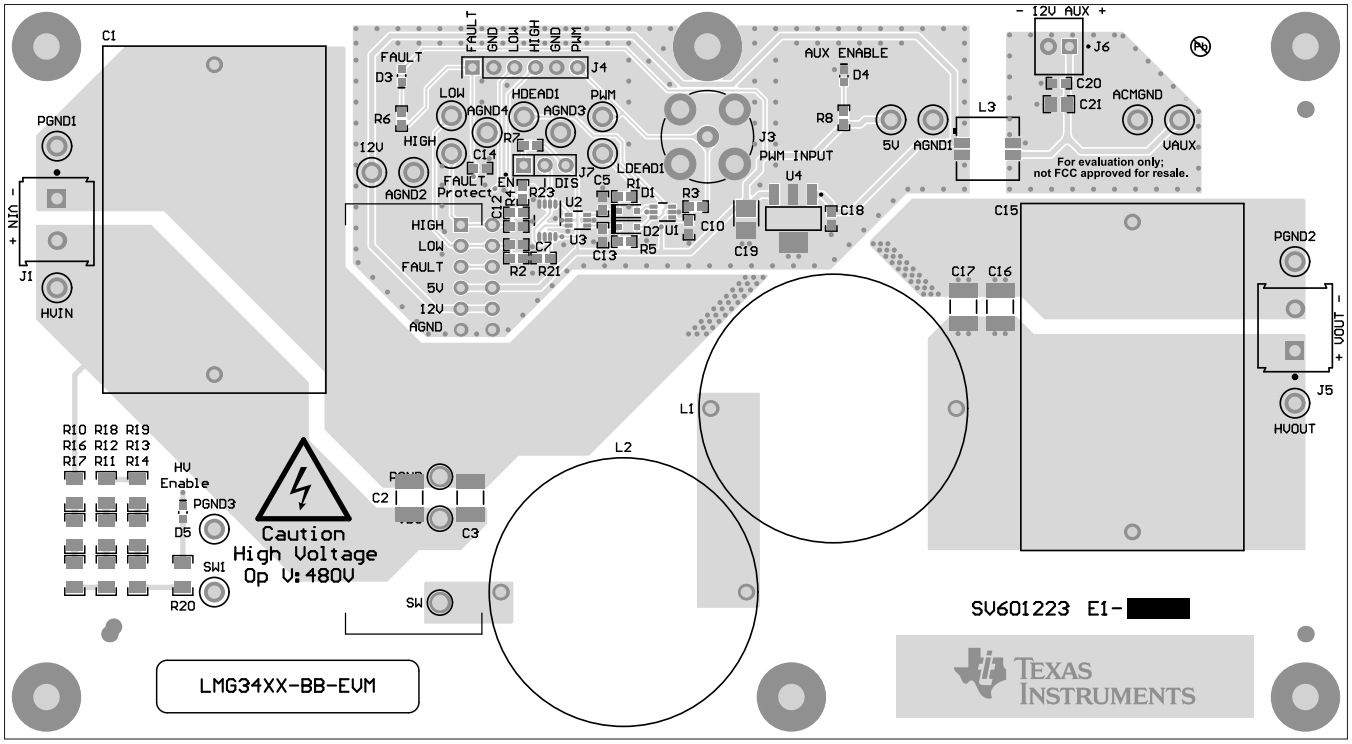

Figure 21. LMG34XX-BB-EVM Top Layer and Components

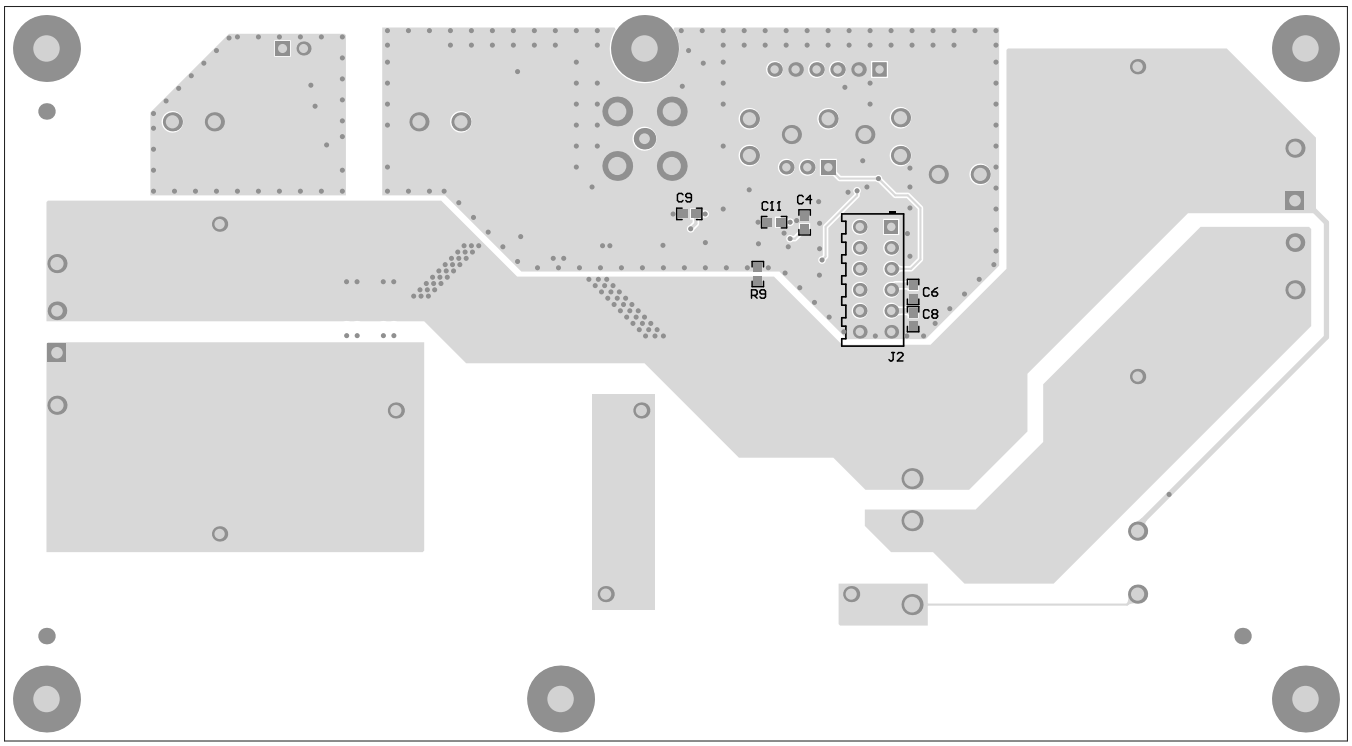

Figure 22. LMG34XX-BB-EVM Bottom Layer and Components

8 Bill of Materials

Table 5. LMG3410EVM-031 List of Materials

QTY	DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER
1	C1	CAP, CERM, 1 uF, 16 V, +/- 10%, X5R, 0402	EMK105BJ105KVHF	Taiyo Yuden
2	C2, C20	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0402	C1005X7R1H104K050BB	TDK
2	C3, C18	CAP, CERM, 22 pF, 50 V, +/- 5%, C0G/NP0, 0402	C1005C0G1H220J050BA	TDK
1	C4	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	GCM21BC71E475KE36L	MuRata
2	C5, C16	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, 0603	C1608X7R1H104K080AA	TDK
3	C6, C7, C17	CAP, CERM, 68 pF, 50 V, +/- 5%, C0G/NP0, 0402	GRM1555C1H680JA01D	MuRata
4	C8, C9, C10, C11	CAP, CERM, 0.022 µF, 1000 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206	C1206C223KDRACTU	Kemet
2	C12, C13	CAP, CERM, 0.047 uF, 1000 V, +/- 10%, X7R, 1812	C1812V473KDRACTU	Kemet
2	C14, C19	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	C0603C105K3RACTU	Kemet
1	C15	CAP, CERM, 4.7 uF, 25 V, +/- 10%, X6S, 0603	GRM188C81E475KE11D	MuRata
1	C21	CAP, CERM, 4.7 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	GCM21BR71C475KA73K	MuRata
3	C22, C23, C24	CAP, CERM, 4.7 uF, 35 V, +/- 10%, X5R, 0603	GRM188R6YA475KE15D	MuRata
1	D1	Diode, Ultrafast, 600 V, 1 A, SOD-123FL	UFM15PL-TP	Micro Commercial Components
2	D2, D3	Diode, Schottky, 20 V, 0.5 A, SOD-123	MBR0520LT1G	ON Semiconductor
1	D4	Diode, Zener, 16 V, 500 mW, SOD-123	MMSZ4703T1G	ON Semiconductor
1	H1	Bergquist double sided thermal tape, TI-Bond Ply100 0.005"/.127mm(1).cu-27.0mm by 27.0mm	BP100-0.005-00-1112	Burgquist
1	H2	Heat sink 1.00"x1.00"	3-101004U	Cool Innovations
1	J1	Header, 1.27mm, 4x2, Gold, R/A, TH	20021112-00008T4LF	Amphenol FCI
2	J2, J3	Header, 50mil, 2x1, Gold, TH	GRPB021VWVN-RC	Sullins Connector Solutions
2	L1, L2	Inductor, Shielded, Metal Composite, 10 µH, 0.65 A, 0.768 ohm, SMD	VLS201610HBX-100M-1	TDK
1	L3	Coupled inductor, 0.2 A, 0.45 ohm, SMD	ACM2520-601-2P-T002	TDK
1	LBL1	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	THT-14-423-10	Brady
2	Q1, Q2	600-V 150mohm GaN With Integrated Driver and Latched Overcurrent Protection, RWH0032A (VQFN-32), RWH0032A (VQFN-32)	LMG3410R150RWHT	Texas Instruments
1	R1	RES, 0, 5%, 0.1 W, 0603	MCR03EZPJ000	Rohm
1	R2	RES, 20, 5%, 0.1 W, AEC-Q200 Grade 0, 0603	CRCW060320R0JNEA	Vishay-Dale
3	R3, R4, R9	RES, 49.9, 1%, 0.063 W, 0402	RC0402FR-0749R9L	Yageo America
2	R5, R7	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	CRCW04020000Z0EDHP	Vishay-Dale
2	R6, R8	RES, 15 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	CRCW040215K0JNED	Vishay-Dale
1	T1	Transformer, 475uH, SMT	760390014	Wurth Elektronik
3	TP1, TP2, TP3	Edge-Mount Pin, Gold	3620-1-32-15-00-00-08-0	Mill-Max
1	U1	High Speed, Robust EMC Reinforced Triple-Channel Digital Isolator, DBQ0016A (SSOP-16)	ISO7731DBQR	Texas Instruments
1	U2	Low-Noise 1 A, 420 kHz Transformer Driver, DBV0006A (SOT-23-6)	SN6505BDBVR	Texas Instruments
0	FID1, FID2, FID3, FID4, FID5, FID6	Fiducial mark. There is nothing to buy or mount.	N/A	N/A
0	J4, J5	Receptacle, 1.27mm, 2x1, Gold with Tin tail, SMT	M50-3140245	Harwin

Table 6. LMG34XX-BB-EVM List of Materials

QTY	DESIGNATOR	DESCRIPTION	PART NUMBER	MANUFACTURER
5	5V, 12V, HVIN, HVOUT, VAUX	Test Point, Compact, Red, TH	5005	Keystone
5	ACMGND, AGND1, AGND2, PGND1, PGND2	Test Point, Compact, Black, TH	5006	Keystone
2	C1, C15	CAP, Film, 5 µF, 1000 V, +/- 5%, 0.016 ohm, TH	MKP1848S55010JP2C	Vishay-Components
4	C2, C3, C16, C17	CAP, CERM, 0.1uF, 630V, +/-10%, X7R, 1812	GRM43DR72J104KW01L	MuRata
5	C4, C6, C8, C9, C11	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	C1608X7R1E105K080AB	TDK
2	C5, C13	CAP, CERM, 39 pF, 50 V, +/- 5%, C0G/NP0, 0603	C1608C0G1H390J	TDK
1	C14	CAP, CERM, 1000 pF, 25 V, +/- 5%, C0G/NP0, 0603	GRM1885C1E102JA01D	MuRata
2	C18, C20	CAP, CERM, 1 µF, 25 V, +/- 10%, X7R, 0603	GRM188R71E105KA12D	MuRata
1	C19	CAP, TA, 33 µF, 16 V, +/- 10%, 0.35 ohm, SMD	TPSB336K016R0350	AVX
1	C21	CAP, CERM, 10 µF, 25 V, +/- 10%, X5R, 0805	GRM219R61E106KA12D	MuRata
2	D1, D2	Diode, Schottky, 30 V, 0.2 A, SOD-323	BAT54WS-7-F	Diodes Inc.
2	D3, D5	LED, Red, SMD	LS L29K-G1J2-1-Z	OSRAM
1	D4	LED, Green, SMD	LG L29K-G2J1-24-Z	OSRAM
6	H1, H2, H3, H4, H9, H10	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	NY PMS 440 0025 PH	B and F Fastener Supply
6	H5, H6, H7, H8, H11, H12	Standoff, Hex, 0.5"L #4-40 Nylon	1902C	Keystone
2	J1, J5	Terminal Block, 2x1, 5.08mm, TH	282841-2	TE Connectivity
1	J2	Receptacle, 2.54mm, 6x1, Gold, TH	448120024	Molex
1	J3	Connector, TH, BNC	112404	Amphenol Connex
1	J4	Header, 100mil, 6x1, Gold, TH	TSW-106-07-G-S	Samtec
1	J6	Terminal Block, 2x1, 2.54mm, TH	282834-2	TE Connectivity
1	J7	Header, 100mil, 3x1, Gold, TH	TSW-103-07-G-S	Samtec
2	L1, L2	Inductor, Toroid, 150 µH, 7.5 A, 0.05 ohm, TH	2300HT-151-H-RC	Bourns
1	L3	Coupled inductor, 47 µH, 1.14 A, 0.241 ohm, +/- 20%, SMD	DRQ73-470-R	Cooper Bussman
3	PGND, SW, VDC	Pin Receptacle, .032-.046" .075" Dia, Gold, TH	0312-0-15-15-34-27-10-0	Mill-Max
2	R1, R5	RES, 1.20 k, 1%, 0.1 W, 0603	RC0603FR-071K2L	Yageo America
6	R2, R3, R4, R9, R21, R23	RES, 0, 5%, 0.1 W, 0603	CRCW06030000Z0EA	Vishay-Dale
2	R6, R8	RES, 1.6 k, 5%, 0.1 W, 0603	CRCW06031K60JNEA	Vishay-Dale
1	R7	RES, 10.0 k, 1%, 0.1 W, 0603	ERJ-3EKF1002V	Panasonic
10	R10, R11, R12, R13, R14, R16, R17, R18, R19, R20	RES, 30 k, 5%, 0.25 W, 1206	CRCW120630K0JNEA	Vishay-Dale
1	SH-J1	Shunt, 100mil, Gold plated, Black	969102-0000-DA	3M
2	U1, U3	Dual Schmitt-Trigger Inverter, DCK0006A	SN74LVC2G14DCKR	Texas Instruments
1	U2	Dual 2-input Positive-and Gate, DCT0008A	SN74LVC2G08IDCTRQ1	Texas Instruments
1	U4	1A Low Dropout Regulator, 4-pin SOT-223, Pb-Free	LM2940IMP-5.0/NOPB	Texas Instruments

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