Application Report
SNVA190B–December 2006–Revised May 2013

AN-1533 Over Voltage Protection Circuit for Automotive Load Dump

ABSTRACT

This application report discusses an over voltage protection circuit for automotive load dump.

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1 Introduction

Transient bus voltages are a serious danger to integrated circuits. The maximum voltage that an integrated circuit can handle depends upon its design process and can be particularly low for small geometry CMOS devices. Transient or persistent over voltage conditions that exceed an IC's absolute maximum voltage rating will permanently damage a device. The need for over voltage protection is particularly common in automotive 12V and 24V systems where peak "load dump" transients can be as high as 60V. Some load protection approaches shunt input transient to ground using devices like avalanche diodes and MOVs. The difficulty with the shunt approach is that large amounts of energy may have to be absorbed. Shunt approaches can also be unattractive if there is a requirement to provide continuous protection while in an over voltage condition (as occurs with double battery).

2 The Circuit

The circuit shown in Figure 1 is a precision series disconnect that was designed to protect a switching regulator load that had an absolute maximum input voltage of 24V. The circuit is designed from low cost discrete devices and uses a single Texas Instruments LMV431AIMF. Since this circuit uses a PFET pass device (Q_1), there is little forward voltage drop or associated power loss.

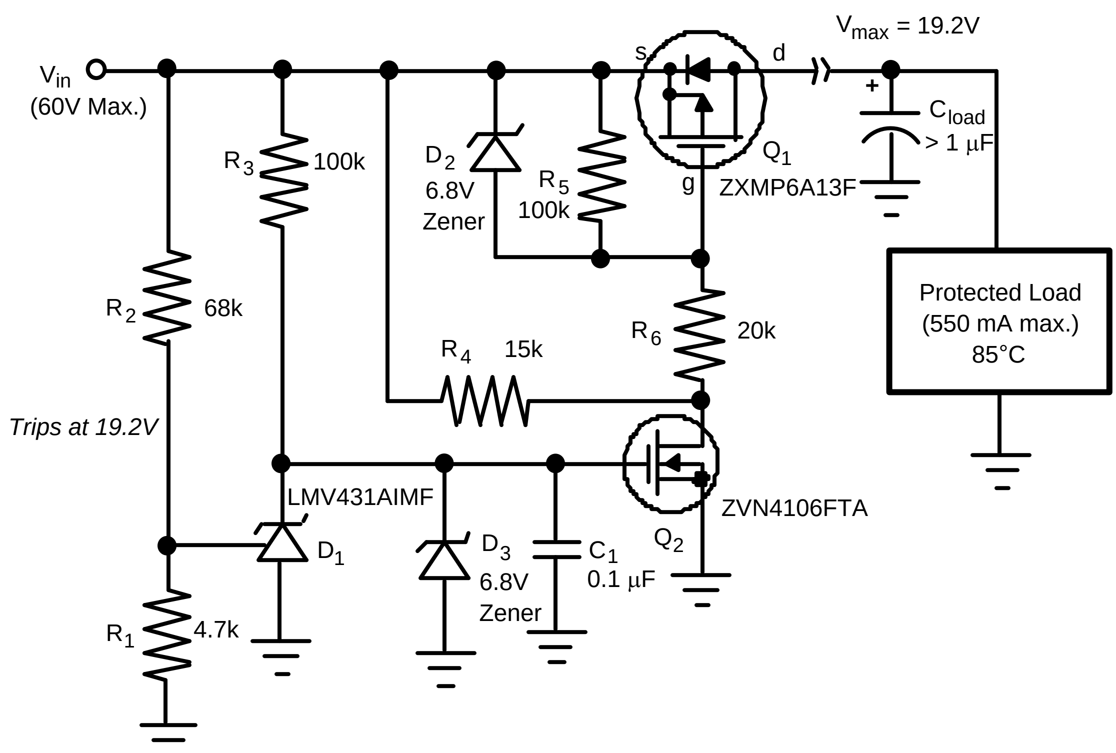

Figure 1. Over Voltage Protection

The LMV431AIMF (D_1) adjustable reference is ideal for this problem because it provides a low cost means to determine a precision trip point and maintain temperature stability that is not possible with a zener diode or with other approaches (1% for the A version, 0.5% for the B version). In order to preserve this precision, resistors R_1 and R_2 should be 1% tolerance or better.

Adjustable references are often misunderstood. As in: "What's that third wire coming out of that diode?" There are many flavors of adjustable reference. Some have different internal reference voltage and some have different gain polarity. They all have two basic (and very useful) components: A temperature stable, precision band gap reference, and a high gain error amplifier (used as a comparator in this circuit). Most devices have uni-polar output in the form of an open collector or emitter. Figure 2 shows conceptually what is inside Texas Instruments LMV431AIMF.

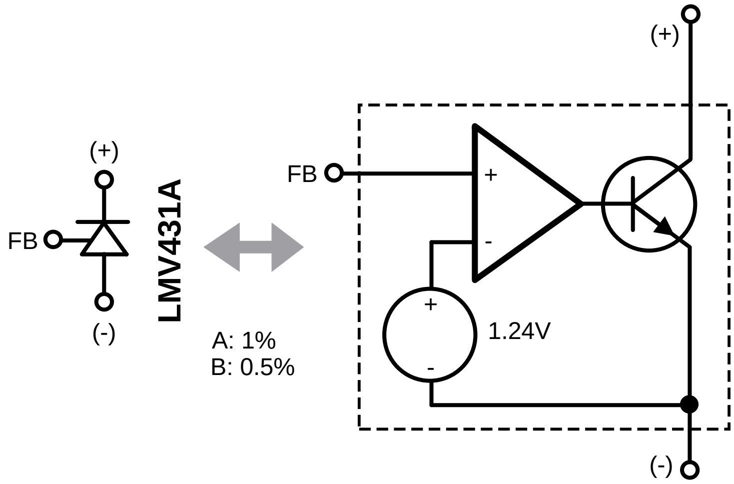

Figure 2. Adjustable Reference Concept

The input voltage is monitored by the LMV431 through voltage divider R_1 and R_2. The circuit shown in Figure 1 is set to trip at 19.2V but an arbitrary trip point can be selected and is determined with these equations:

$$V_{trip} = 1.24 \times \frac{R_1 + R_2}{R_1}$$

$$R_2 = R_1 \times \left(\frac{V_{trip}}{1.24} - 1\right) \tag{1}$$

The output of the LMV431 pulls down when the reference pin exceeds 1.24V. The cathode of an LMV431 can pull down to a saturation point of about 1.2V. This is sufficient to turn Q_2 off. Q_2 was specifically selected to have a high gate threshold (>1.3V). Do not make substitution for Q2 without taking this into account.

The device states for D_1, Q_2, and Q_1 are shown in Table 1 for the case of a 19.2V trip point.

Table 1. Truth Table

	LM431 Q1	NFET Q2	PFET Q1
<2.7 V	OFF	?	OFF
2.7V to 19.2	OFF	ON	ON
>19.2 V	ON	OFF	OFF

The circuit's function is shown in Figure 3. The trip point can be anywhere in the 2.7V to 60V range. Below about 2.7V the circuit will enter the off state. This is because there is no longer sufficient input voltage to satisfy the gate to source thresholds of Q_1 and Q_2.

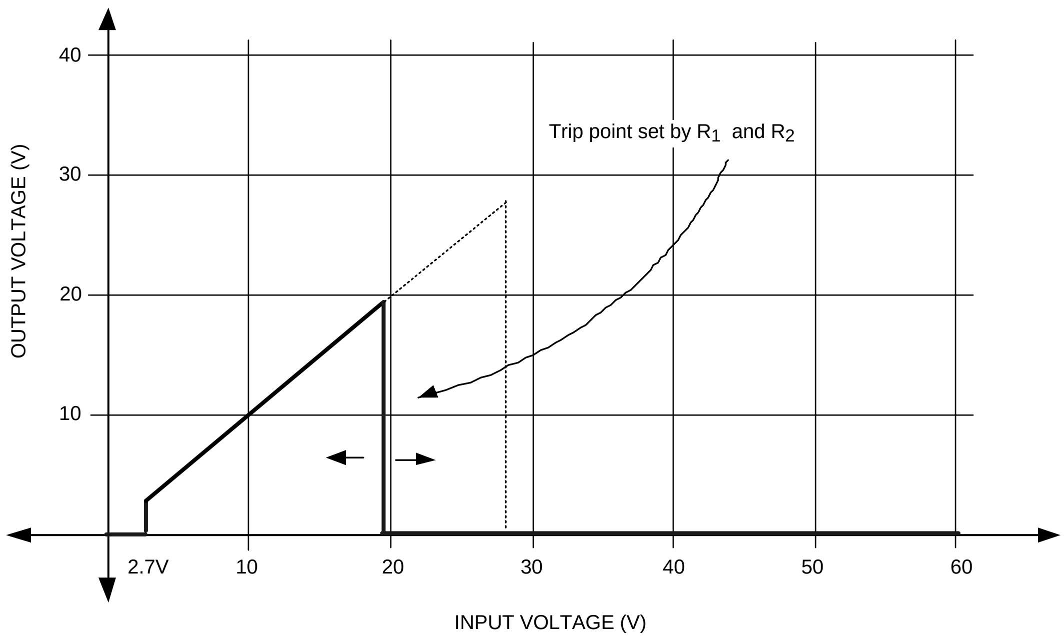

Figure 3. Circuit Function

When in the off state, the circuit presents about 42 kΩ to the input (off state quiescent load). Zener diodes D_2 and D_3 are necessary to limit the maximum gate to source voltages seen by Q_1 and Q_2 (which cannot exceed 20V). D_3 also prevents the cathode of D_1 from exceeding its maximum of 35V. Resistor R_4 provides a small amount of bias to Q2 in order to satisfy Q_2's drain leakage in the off state. Note that the body diode in Q_1 means that there is no protection to the load for reverse battery (negative input voltages). In order to protect against reverse battery, either a blocking diode or a second (back to back) PFET is required.

The circuit is designed to actuate quickly but reconnect more slowly. Capacitor C_1 rapidly discharges to ground through the LMV431 when over voltage is detected. When conditions return to normal, reconnect is delayed by the R3•C1 time constant. Most loads (usually regulators) contain large input capacitors which provide time for the disconnect circuit to engage by limiting the transient slew rate. The nature of the expected transient along with the available capacitance will determine the required response time. The shut off action of this circuit occurs in about 12 µsec. Maximum transient rise times are limited in proportion to this time interval by C_{load}. This circuit was tested with a C_{load} of 1 µF. Larger Cload is allowed and recommended if fast rising, low source impedance transients are expected.

3 Response Time Measurement

The response to a normal 12V ON and OFF cycle is shown in Figure 4. The off portion decays slowly because of the 1 µF Cload dissipating into the 1 kΩ test load. The driving waveform also shows this decay because the test source used could not sink current.

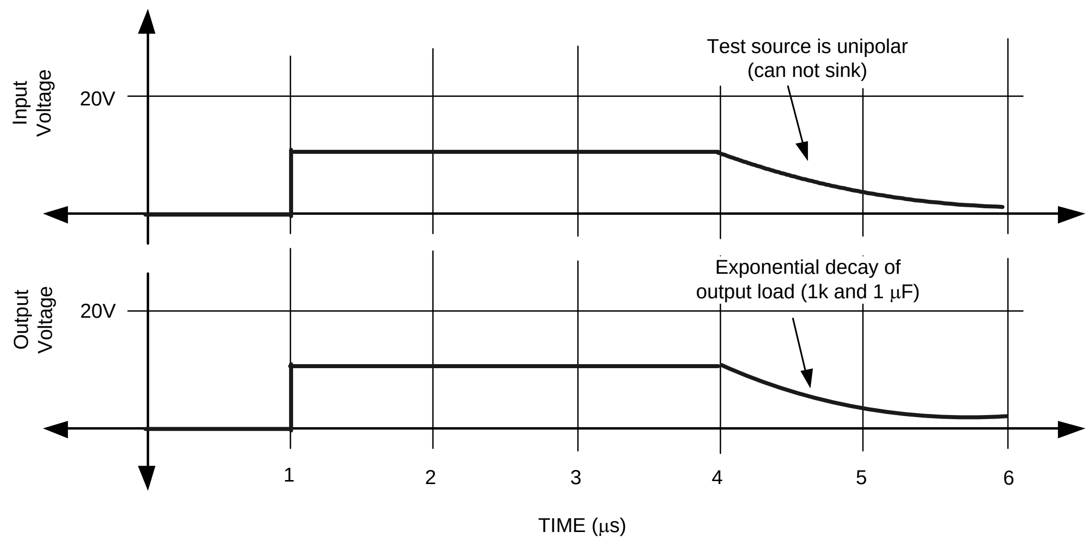

Figure 4. Normal 12V Operation

The response to an over voltage is shown in Figure 5. Note that the fast rising over voltage event has time to charge the output to 19.2V where the circuit disconnects. After this, the disconnected output voltage decays into the 1 kΩ load.

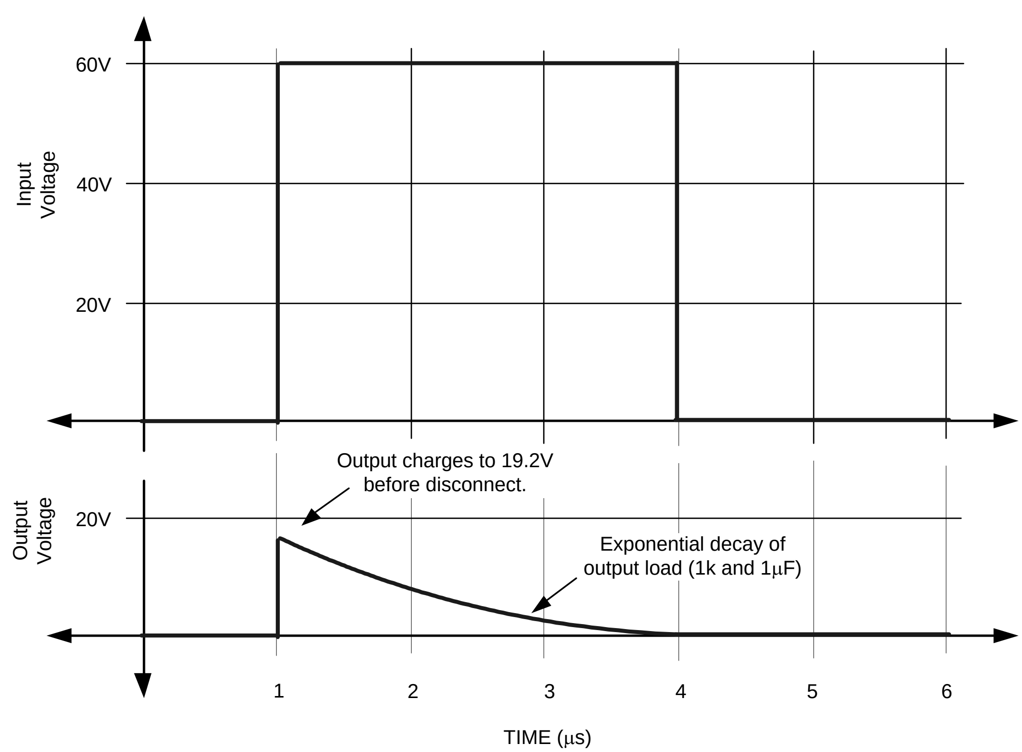

Figure 5. Response to 60V Step Input, C_{load} = 1 µF

If the 1µF C_{load} capacitor is removed the actuation speed of the disconnect can be observed. This is shown in Figure 6. Since the rise time of the input transient isn't limited by any capacitance the output voltage is charged to the full 60V before action is taken. For this reason, C_{load} should be sized appropriately for the expected transient rise time and expected transient source impedance.

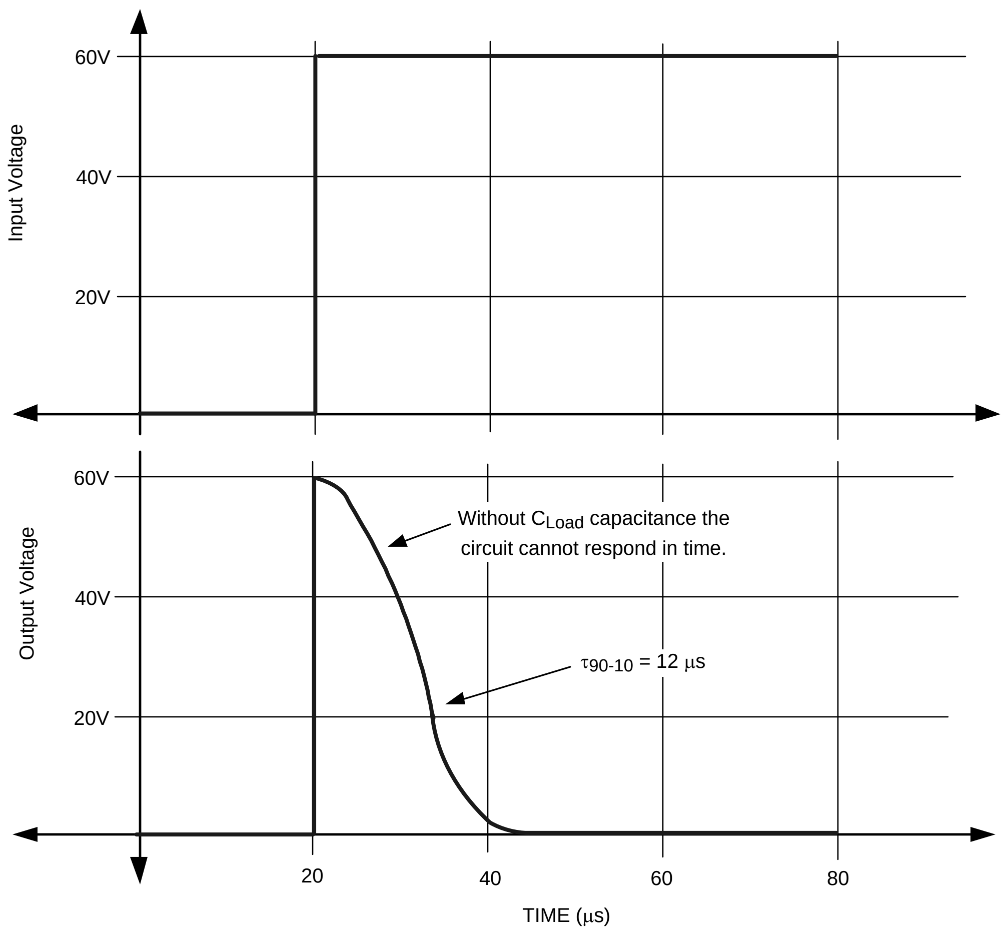

Figure 6. Raw Response to 60V Input, Cload = 0 µF

4 Load Limits

The 550 mA maximum allowed load is set by the thermal limits of Q1 at 85°C. When making this calculation, remember that $R_{DS(ON)}$,on is highest when the gate to source voltage is low. For larger loads replace Q1 with a 60V PFET with more thermal capacity (smaller θ_{JA}) or lower $R_{DS(ON)}$.

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