Understanding and Applying Current-Mode Control Theory

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UNDERSTANDING AND APPLYING CURRENT-MODE CONTROL THEORY

Practical Design Guide for Fixed-Frequency, Continuous Conduction-Mode Operation

by

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Notes:

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Abstract

The basic operation of current mode control is covered, including DC and AC characteristics of the modulator gain. Feed-forward methods show how the slope compensation requirement for any operating mode is easily met. Sampling-gain terms are explained and incorporated into the design approach. Switching models for the buck, boost and buck-boost are related to the equivalent linear model. This facilitates the practical design using simplified, factored expressions. Design examples show how the concepts and methods are applied to each of the three basic topologies.

Current-Mode Control

For current-mode control there are three things to consider:

1. Current-mode operation. An ideal current-mode converter is only dependent on the dc or average inductor current. The inner current loop turns the inductor into a voltage-controlled current source, effectively removing the inductor from the outer voltage control loop at dc and low frequency.

2. Modulator gain. The modulator gain is dependent on the effective slope of the ramp presented to the modulating comparator input. Each operating mode will have a unique characteristic equation for the modulator gain.

3. Slope compensation. The requirement for slope compensation is dependent on the relationship of the average current to the value of current at the time when the sample is taken. For fixed-frequency operation, if the sampled current were equal to the average current, there would be no requirement for slope compensation.

Current-Mode Operation

Whether the current-mode converter is peak, valley, average, or sample-and-hold is secondary to the operation of the current loop. As long as the dc current is sampled, current-mode operation is maintained. The current-loop gain splits the complex-conjugate pole of the output filter into two real poles, so that the characteristic of the output filter is set by the capacitor and load resistor. Only when the impedance of the output inductor equals the current-loop gain does the inductor pole reappear at higher frequencies.

To understand how this works, the basic concept of pulse-width modulation is used to establish the criteria for the modulator gain. This allows a linear model to be developed, illustrating the dc- and ac-gain characteristics. For simplicity, the buck regulator is used to illustrate the operation.

Modulator Gain

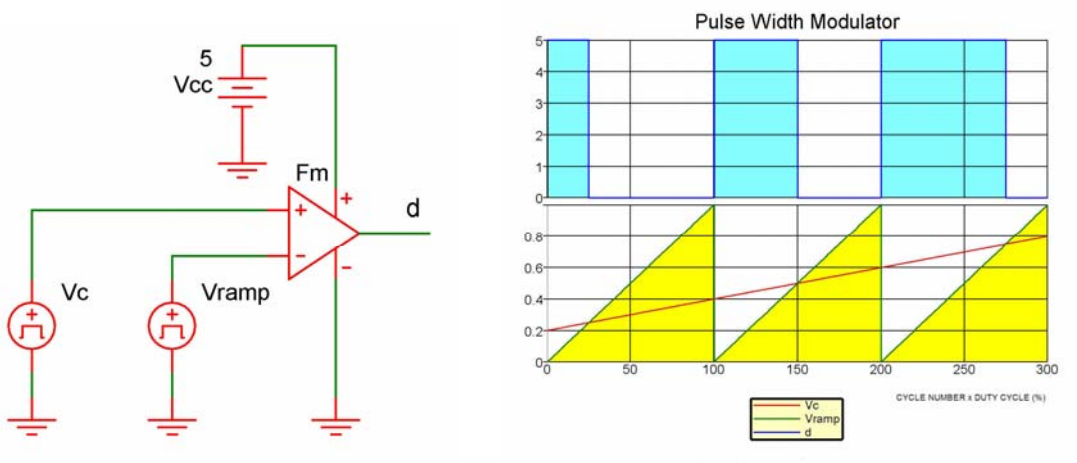

Figure 1. Pulse-width modulator.

Pulse-Width Modulator

A comparator is used to modulate the duty cycle. Fixed-frequency operation is shown in Figure 1, where a sawtooth voltage ramp is presented to the inverting input. The control or error voltage is applied to the non-inverting input. The modulator gain F_m is defined as the change in control voltage which causes the duty cycle to go from 0% to 100%:

$$F_m = \frac{d}{v_C} = \frac{1}{V_{RAMP}}$$

The modulator voltage gain K_m, which is the gain from the control voltage to the switch voltage is defined as:

$$K_m = V_{IN} \cdot F_m = \frac{V_{IN}}{V_{RAMP}}$$

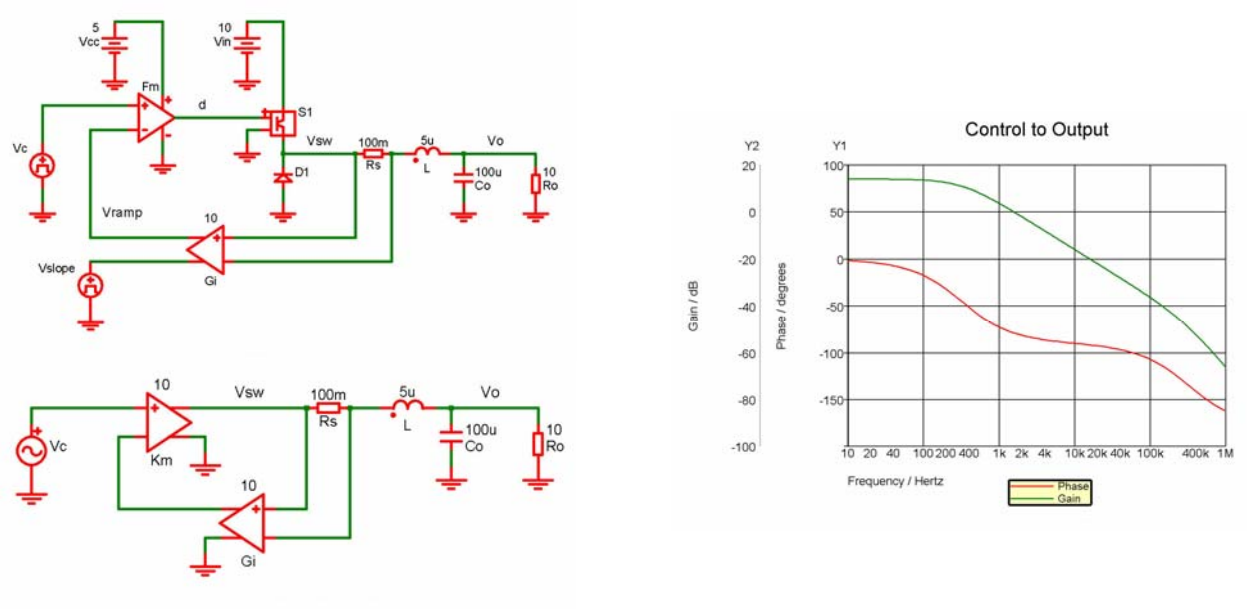

Figure 2. Current-mode buck, linear model and frequency response.

Current-Mode Linear Model

For current-mode control, the ramp is created by monitoring the inductor current. This signal is comprised of two parts: the ac ripple current, and the dc or average value of the inductor current. The output of the current-sense amplifier G_i is summed with an external ramp V_{SLOPE}, to produce V_{RAMP} at the inverting input of the comparator.

In Figure 2 the effective V_{RAMP} = 1 V. With V_{IN} = 10 V, the modulator voltage gain K_m = 10.

The linear model for the current loop is an amplifier which feeds back the dc value of the inductor current, creating a voltage-controlled current source. This is what makes the inductor disappear at dc and low frequency. The ac ripple current sets the modulator gain.

The current-sense gain is usually expressed as the product of the current-sense amplifier gain and the sense resistor:

$$R_i = G_i \cdot R_S$$

The current-sense gain is an equivalent resistance, the units of which are volts/amp. The current-loop gain is the product of the modulator voltage gain and the current-sense gain, which is also in volts/amp.

The modulator voltage gain is reduced by the equivalent divider ratio of the load resistor R_O and the current-loop gain $K_m \cdot R_i$. This sets the dc value of the control-to-output gain. Neglecting the dc loss of the sense resistor:

$$\frac{V_O}{V_C} = K_m \cdot \frac{R_O}{R_O + K_m \cdot R_i}$$

This is usually written in factored form:

$$\frac{V_O}{V_C} = \frac{R_O}{R_i} \cdot \frac{1}{1 + \frac{R_O}{K_m \cdot R_i}}$$

The dominant pole in the transfer function appears when the impedance of the output capacitor equals the parallel impedance of the load resistor and the current-loop gain:

$$\omega_P = \frac{1}{C_O} \cdot \left(\frac{1}{R_O} + \frac{1}{K_m \cdot R_i} \right)$$

The inductor pole appears when the impedance of the inductor equals the current-loop gain:

$$\omega_L = \frac{K_m \cdot R_i}{L}$$

The current loop creates the effect of a lossless damping resistor, splitting the complex-conjugate pole of the output filter into two real poles.

For current-mode control, the ideal steady-state modulator gain may be modified depending upon whether the external ramp is fixed, or proportional to some combination of input and output voltage. Further modification of the gain is realized when the input and output voltages are perturbed to derive the effective small-signal terms. However, the concepts remain valid, despite small-signal modification of the ideal steady-state value.

Slope Compensation

The difference between the average inductor current and the dc value of the sampled inductor current can cause instability for certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of next switching cycle. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node.

For peak current mode control, sub-harmonic oscillation occurs with a duty cycle greater than 50%.

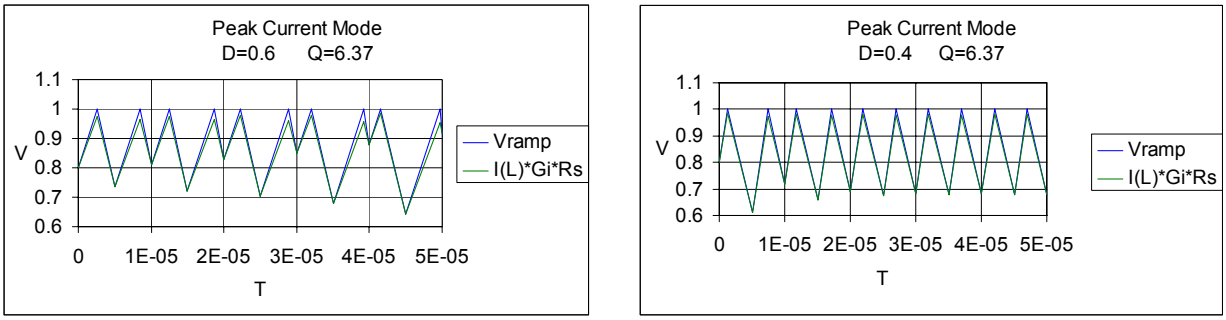

Figure 3. Peak current-mode sub-harmonic oscillation. For D<0.5, sub-harmonic oscillation is damped. For D>0.5, sub-harmonic oscillation builds with insufficient slope compensation.

By adding a compensating ramp equal to the down-slope of the inductor current, any tendency toward sub-harmonic oscillation is damped within one switching cycle. This is demonstrated graphically in Figure 4.

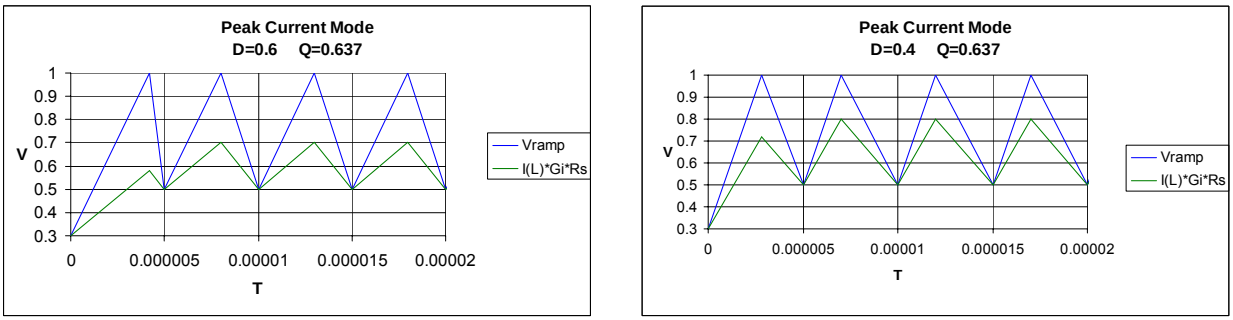

Figure 4. Optimally compensated peak current-mode converter.

For valley current-mode, sub-harmonic oscillation occurs with a duty cycle less than 50%. It is now necessary to use slope compensation equal to the up-slope of the inductor current.

For emulated peak current-mode, the valley current is sampled on the down-slope of the inductor current. This is used as the dc value of current to start the next cycle. In this case, a ramp equal to the sum of both the up-slope and down-slope is required.

General Slope Compensation Criteria

For any mode of operation (peak, valley or emulated), the optimal slope of the ramp presented to the modulating comparator input is equal to the sum of the absolute values of the inductor up-slope and down-slope scaled by the current-sense gain. This will cause any tendency toward sub-harmonic oscillation to damp in one switching cycle.

For the buck regulator, this is equivalent to a ramp whose slope is $V_{IN} \cdot R_i / L$.
Up-slope = $(V_{IN} - V_O) \cdot R_i / L$
Down-slope = $V_O \cdot R_i / L$

For the boost regulator, this is equivalent to a ramp whose slope is $V_O \cdot R_i / L$.
Up-slope = $V_{IN} \cdot R_i / L$
Down-slope = $(V_O - V_{IN}) \cdot R_i / L$

For the buck-boost regulator, this is equivalent to a ramp whose slope is $(V_{IN} + V_O) \cdot R_i / L$.
Up-slope = $V_{IN} \cdot R_i / L$
Down-slope = $V_O \cdot R_i / L$

To avoid confusion, V_{IN} and V_O represent the magnitude of the input and output voltages as a positive quantity. By identifying the appropriate sensed inductor slope, it is easy to find the correct slope-compensating ramp.

Sampling Gain

A current-mode switching regulator is a sampled-data system, the bandwidth of which is limited by the switching frequency. Beyond half the switching frequency, the response of the inductor current to a change in control voltage is not accurately reproduced.

For the control-to-output transfer function, the sampling gain is modeled in series with the closed-current feedback loop. The linear model sampling-gain term H(s) is defined as:

$$H(s) = 1 + s \cdot K_e + \frac{s^2}{\omega_n{}^2} \qquad \text{where} \quad \omega_n = \frac{\pi}{T}$$

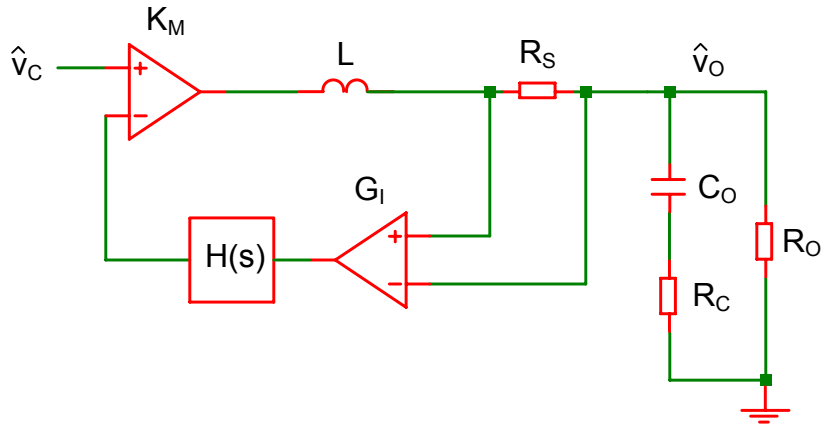

Figure 5. Buck regulator with sampling gain H(s) in the closed current-loop feedback path.

In general, K_e represents the time delay (or phase shift) for the sample-and-hold function of the emulated architecture. For the simplified model, the proportional slope compensation is incorporated into K_e as well as K_m. In the appendix of reference [1], a more general model shows how the proportional slope compensation may be modeled as a feed-forward term. The term $\frac{s^2}{\omega_n{}^2}$ shows that a 180° phase shift occurs at half the switching frequency. No useful signal from the control voltage will be accurately reproduced above this frequency.

Sampling Gain Q

For the closed current-loop control-to-output transfer function, the factored form shows a complex-conjugate pole at half the switching frequency. The sampling gain works in conjunction with the inductor pole, setting the Q of the circuit. Using a value of $Q = 2 / \pi = 0.637$ will cause any tendency toward sub-harmonic oscillation to damp in one switching cycle.

With respect to the closed current-loop control-to-output function, the effective sampled-gain inductor pole is given by:

$$f_L(Q) = \frac{1}{4 \cdot T \cdot Q} \cdot \left(\sqrt{1 + 4 \cdot Q^2} - 1 \right)$$

This is the frequency at which a 45° phase shift occurs due to the sampling gain. For Q = 0.637, $f_L(Q)$ occurs at 24% of the switching frequency, which sets an upper limit for the crossover frequency of the voltage loop. For the peak current-mode buck with a fixed slope-compensating ramp, the effective sampled-gain inductor pole is only fixed in frequency with respect to changes in line voltage when Q = 0.637. Proportional slope-compensation methods will achieve this for other operating modes.

Transfer Functions

For all transfer functions:

$$Z_O = \left(\frac{1}{s \cdot C_O} + R_C \right) \| R_O = \frac{R_O \cdot (1 + s \cdot C_O \cdot R_C)}{1 + s \cdot C_O \cdot (R_O + R_C)} \qquad Z_L = s \cdot L + R_L + R_S$$

R_O represents the load resistance, while R represents the dc operating point V_O / I_O.

For a resistive load $R_O = R$.

For a non-linear load such as an LED, $R_O = R_D$, where R_D represents the dynamic resistance of the load at the operating point, plus any series resistance.

For a constant-current load, $R_O = \infty$.

In order to show the factored form, the simplified transfer functions assume poles which are well separated by the current-loop gain. The control-to-output transfer function with sampling-gain term accurately represents the circuit's behavior to half the switching frequency.

The current-sense gain $R_i = G_i \cdot R_S$, where G_i is the current-sense amplifier and R_S is the sense resistor.

For peak or valley current-mode with a fixed slope-compensating ramp, $\omega_n \cdot Q = \omega_L$, where $\omega_L = \frac{K_m \cdot R_i}{L}$.

G_V represents the error amplifier gain as a positive quantity.

Buck Regulator Example

Figure 6 shows a typical synchronous buck regulator. The slope-compensating ramp could be either fixed, or proportional to V_O. For this example, a fixed ramp is used for V_{SLOPE} which is set for $Q = 2 / \pi = 0.637$. The error amplifier G_V has an open loop gain of 3300 (70 dB) and is modeled with a single-pole gain-bandwidth of 10 MHz.

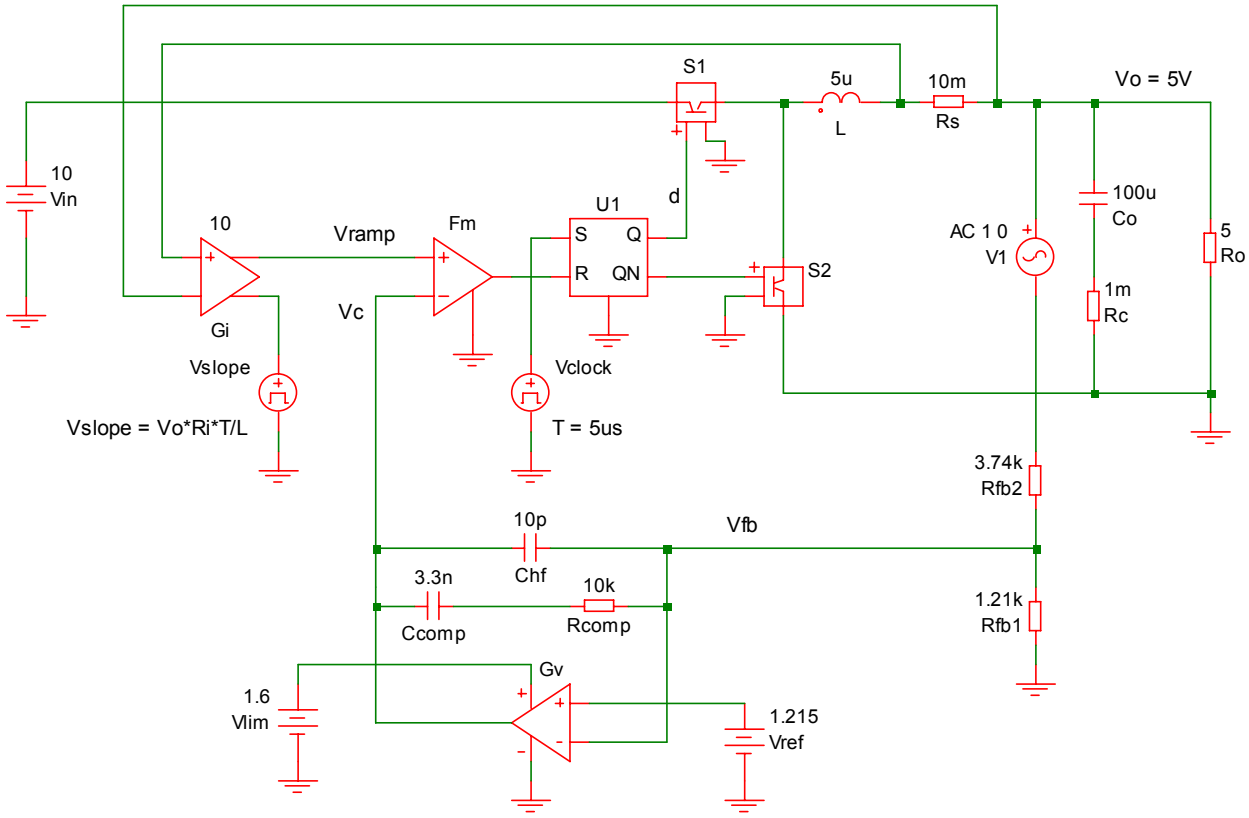

Figure 6. Peak current-mode buck switching model.

The control-to-output gain is first characterized, and the error amplifier compensation tailored to produce the highest crossover frequency with a phase margin of 45°. The simplified factored control-to-output equation is used for the design analysis.

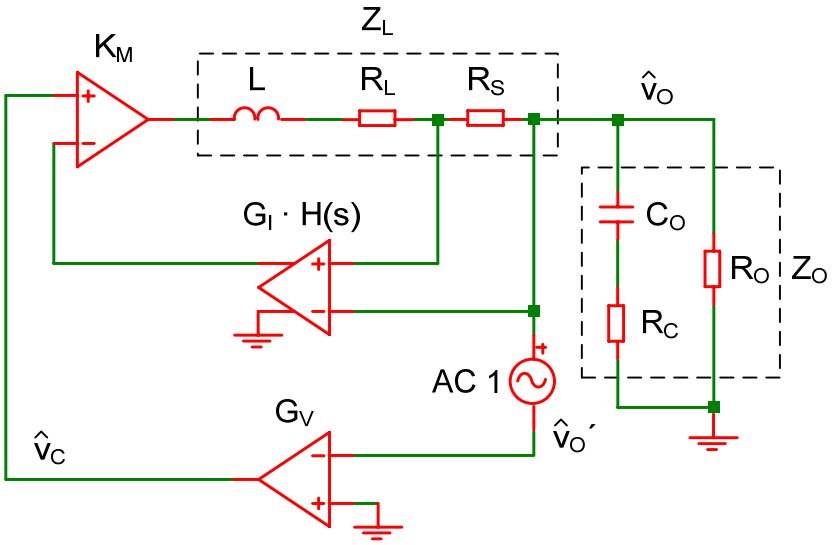

Figure 7. Buck simplified linear voltage loop model.

Linear Model Coefficients

$$V_{ap} = V_{IN} \qquad D = \frac{V_O}{V_{IN}} \qquad D' = 1 - D = \frac{V_{IN} - V_O}{V_{IN}} \qquad R = \frac{V_O}{I_O}$$

Transfer Functions

Control-to-Output (Impedance Form):

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{K_m \cdot Z_O}{Z_O + Z_L + K_m \cdot R_i \cdot H(s)}$$

Current-Mode Buck – Transfer Functions

Simplified Control-to-Output:

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{R_O}{R_i \cdot K_D} \cdot \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{{\omega_n}^2}\right)}$$

Where:

$$K_D = 1 + \frac{R_O}{K_m \cdot R_i} \qquad \omega_Z = \frac{1}{C_O \cdot R_C} \qquad \omega_P = \frac{K_D}{C_O \cdot R_O}$$

For an ideal current-mode buck, $K_D \approx 1$. In this case, only the single-pole characteristic of ω_P is modeled. This may provide a good approximation at a lower crossover frequency ($< 0.1 \cdot f_{SW}$). For accurate results, the complete expressions should be used.

Voltage Loop:

$$\frac{\hat{v}_O}{\hat{v}'_O} = -G_V \cdot \frac{\hat{v}_O}{\hat{v}_C}$$

DC Input Impedance:

$$\frac{\hat{v}_{IN}}{\hat{i}_{IN}}(dc) = -\frac{R}{D^2}$$

Buck Design Example – Control-to-Output

DC gain terms:

$$D = D' = 0.5 \qquad R_i = G_i \cdot R_S = 0.1 \qquad V_{SL} = V_O \cdot R_i \cdot \frac{T}{L} = 0.5$$

$$K_m = \frac{1}{(0.5 - D) \cdot R_i \cdot \frac{T}{L} + \frac{V_{SL}}{V_{ap}}} = 20 \qquad K_D = 1 + \frac{R_O}{K_m \cdot R_i} = 3.5 \qquad \frac{\hat{v}_O}{\hat{v}_C}(dc) = \frac{R_O}{R_i \cdot K_D} = 14.3 = 23dB$$

Capacitor pole frequency:

$$f_P = \frac{\omega_P}{2 \cdot \pi} = 1.1\text{kHz}$$

Sampled-gain inductor pole:

$$f_L(Q) = \frac{1}{4 \cdot T \cdot Q} \cdot \left(\sqrt{1 + 4 \cdot Q^2} - 1 \right) = 49\text{kHz}$$

ESR zero frequency:

$$f_Z = \frac{\omega_Z}{2 \cdot \pi} = 1.6\text{MHz}$$

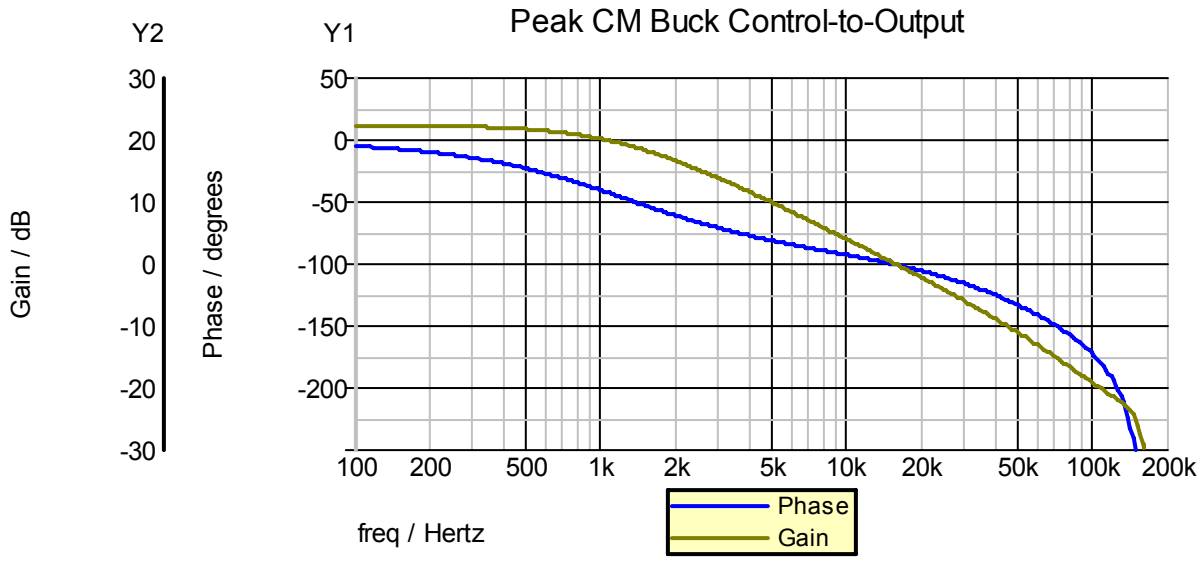

Figure 8. Buck control-to-output.

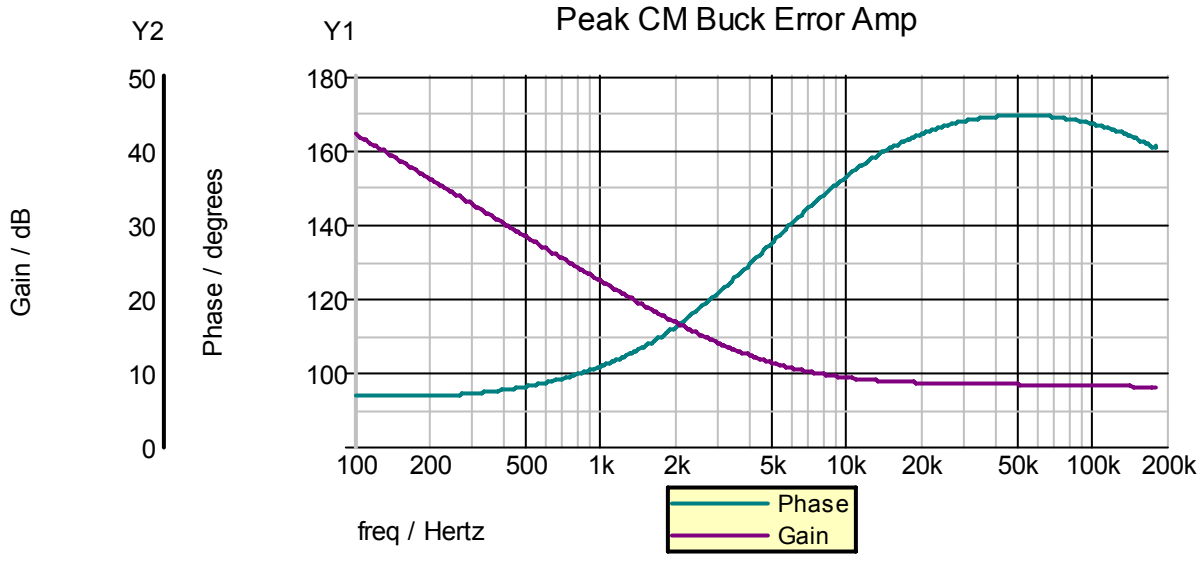

Figure 9. Buck error amplifier.

Buck Design Example – Error Amplifier

There is a pole at low frequency. The mid-band gain is set to produce the desired voltage loop crossover frequency. The error amp zero is generally set about a decade below this frequency. The high frequency pole attenuates switching noise at the error amp output and is not always required, depending on the bandwidth of the amplifier.

$$f_{ZEA} = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C_{COMP}} = 4.8\text{kHz} \qquad G_{EA} = \frac{R_{COMP}}{R_{FB2}} = 2.7 = 8.5\text{dB} \qquad f_{HF} = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C_{HF}} = 1.6\text{MHz}$$

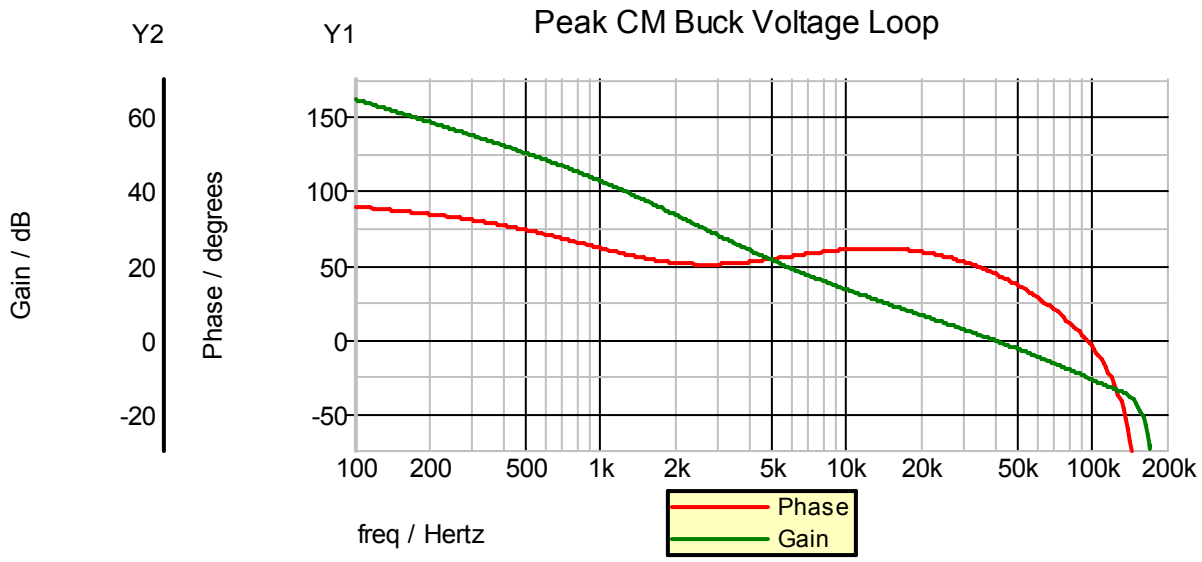

Figure 10. Buck voltage loop.

Buck Design Example – Voltage Loop

The voltage loop plot is simply the sum of the control-to-output and error amplifier plots. For this example, the crossover frequency is 40 kHz with 45° phase margin. The gain margin at 95 kHz is 10 dB.

Boost Regulator Example

Figure 11 shows a typical boost regulator. For many applications, the synchronous switch S2 is replaced by a diode rectifier. The slope-compensating ramp could be either fixed, or proportional to V_O - V_{IN}. For this example, a fixed ramp is used for V_{SLOPE} which is set for Q = 2 / π = 0.637. The error amplifier G_V has an open loop gain of 3300 (70 dB) and is modeled with a single-pole gain-bandwidth of 10 MHz.

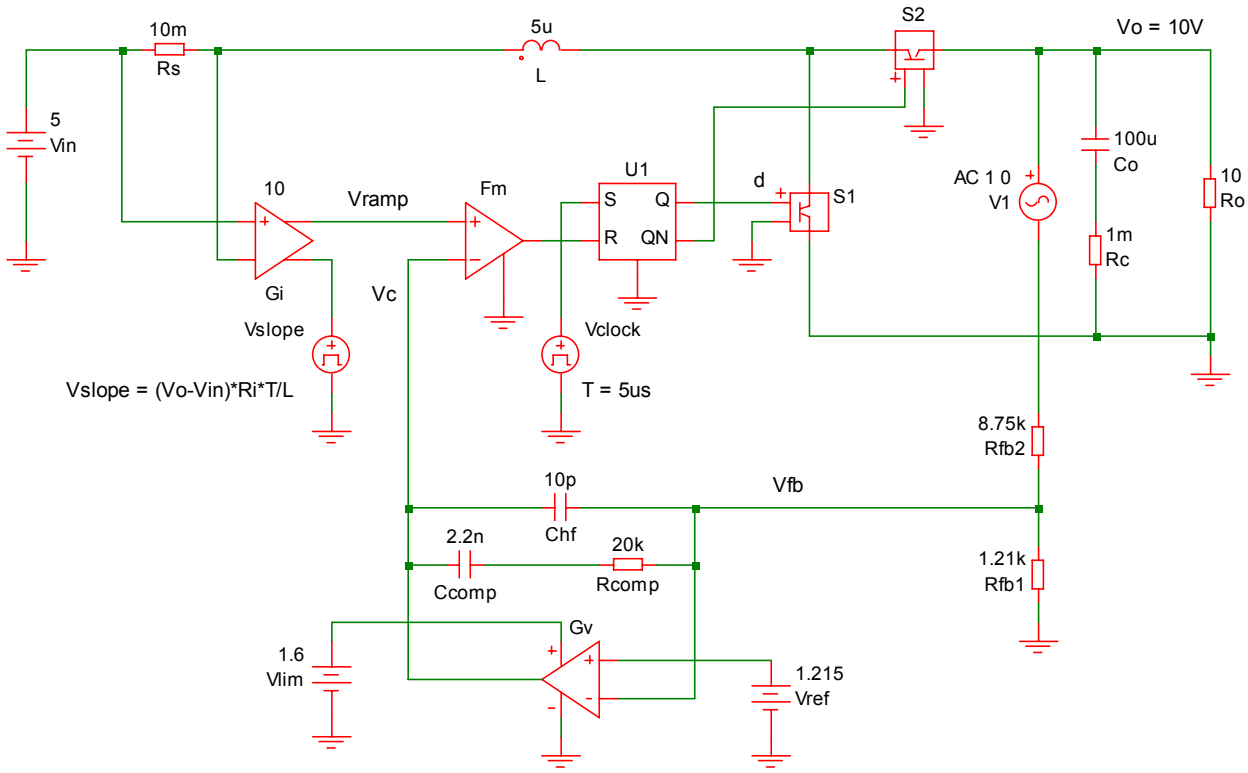

Figure 11. Peak current-mode boost switching model.

The control-to-output gain is first characterized, and the error amplifier compensation tailored to produce the highest crossover frequency with a phase margin of 45°. The simplified factored control-to-output equation is used for the design analysis.

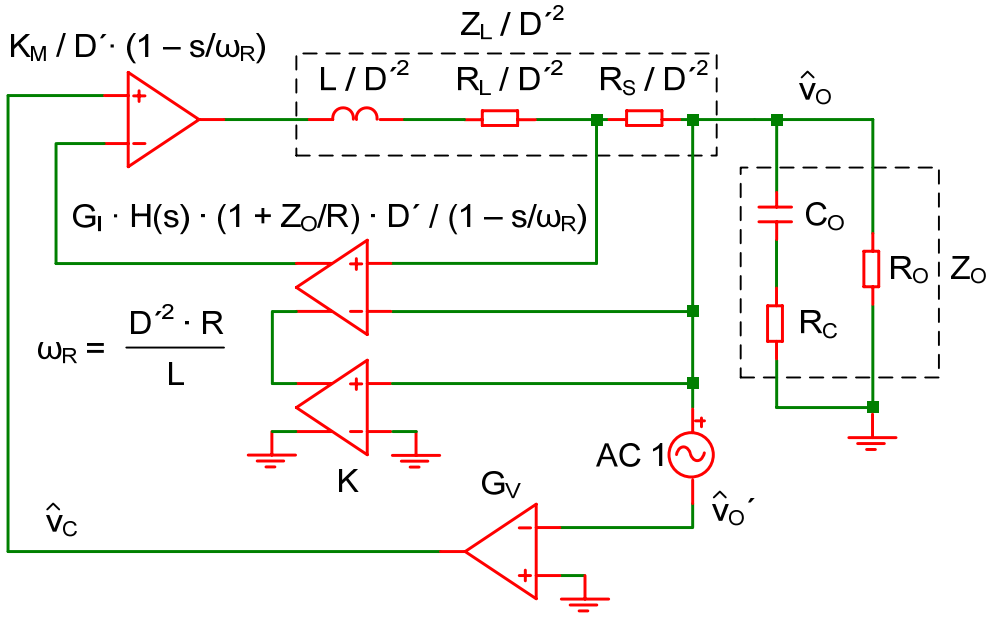

Figure 12. Boost simplified linear voltage loop model.

Linear Model Coefficients

$$V_{ap} = V_O \qquad D = \frac{V_O - V_{IN}}{V_O} \qquad D' = 1 - D = \frac{V_{IN}}{V_O} \qquad R = \frac{V_O}{I_O}$$

Transfer Functions

Control-to-Output (Impedance Form):

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{\frac{K_m}{D'} \cdot \left(1 - \frac{Z_L}{D'^2 \cdot R}\right) \cdot Z_O}{Z_O + \frac{Z_L}{D'^2} + \cdot \frac{K_m \cdot R_i \cdot H(s)}{D'^2} \cdot \left(1 + \frac{Z_O}{R}\right) + \frac{K_m \cdot K}{D'} \cdot \left(1 - \frac{Z_L}{D'^2 \cdot R}\right) \cdot Z_O}$$

Current-Mode Boost – Transfer Functions

Simplified Control-to-Output:

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{R_O \cdot D'}{R_i \cdot K_D} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{{\omega_n}^2}\right)}$$

Where:

$$K_D = 1 + \frac{R_O}{R} + \frac{R_O \cdot D'^2}{R_i} \cdot \left(\frac{1}{K_m} + \frac{K}{D'}\right) \qquad \omega_R = \frac{R \cdot D'^2}{L} \qquad \omega_Z = \frac{1}{C_O \cdot R_C} \qquad \omega_P = \frac{K_D}{C_O \cdot R_O}$$

For an ideal current-mode boost with resistive load, $K_D \approx 2$. In this case, only the single-pole characteristic of ω_P and right-half-plane zero of ω_R are modeled. This may provide a good approximation at a lower crossover frequency ($< 0.1 \cdot f_{SW}$). For accurate results, the complete expressions should be used.

Voltage Loop:

$$\frac{\hat{v}_O}{\hat{v}'_O} = -G_V \cdot \frac{\hat{v}_O}{\hat{v}_C}$$

DC Input Impedance:

$$\frac{\hat{v}_{IN}}{\hat{i}_{IN}}(dc) = -D'^2 \cdot R$$

Boost Design Example – Control-to-Output

DC gain terms:

$$D = D' = 0.5 \qquad R_i = G_i \cdot R_S = 0.1 \qquad V_{SL} = (V_O - V_{IN}) \cdot R_i \cdot \frac{T}{L} = 0.5$$

$$K_m = \frac{1}{(0.5 - D) \cdot R_i \cdot \frac{T}{L} + \frac{V_{SL}}{V_{ap}}} = 20 \qquad K = 0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D' = 0.0125$$

$$K_D = 1 + \frac{R_O}{R} + \frac{R_O \cdot D'^2}{R_i} \cdot \left(\frac{1}{K_m} + \frac{K}{D'}\right) = 3.88 \qquad \frac{\hat{v}_O}{\hat{v}_C}(dc) = \frac{R_O \cdot D'}{R_i \cdot K_D} = 12.9 = 22dB$$

Capacitor pole frequency:

$$f_P = \frac{\omega_P}{2 \cdot \pi} = 620\text{Hz}$$

Right-half-plane zero frequency:

$$f_R = \frac{\omega_R}{2 \cdot \pi} = 80\text{kHz}$$

Sampled-gain inductor pole:

$$f_L(Q) = \frac{1}{4 \cdot T \cdot Q} \cdot \left(\sqrt{1 + 4 \cdot Q^2} - 1 \right) = 49\text{kHz}$$

ESR zero frequency:

$$f_Z = \frac{\omega_Z}{2 \cdot \pi} = 1.6\text{MHz}$$

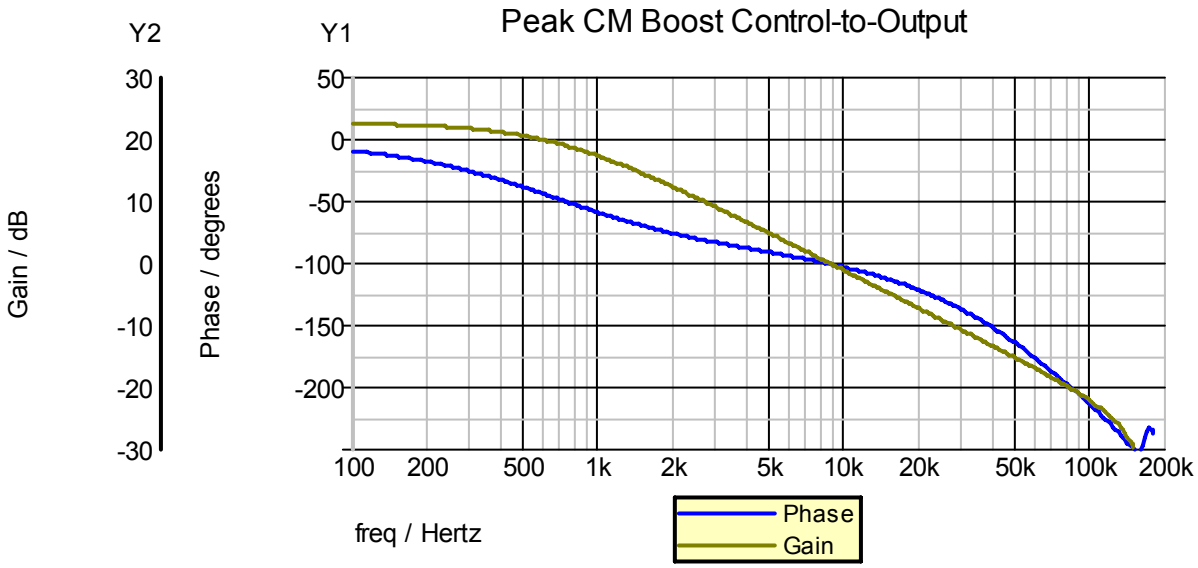

Figure 13. Boost control-to-output.

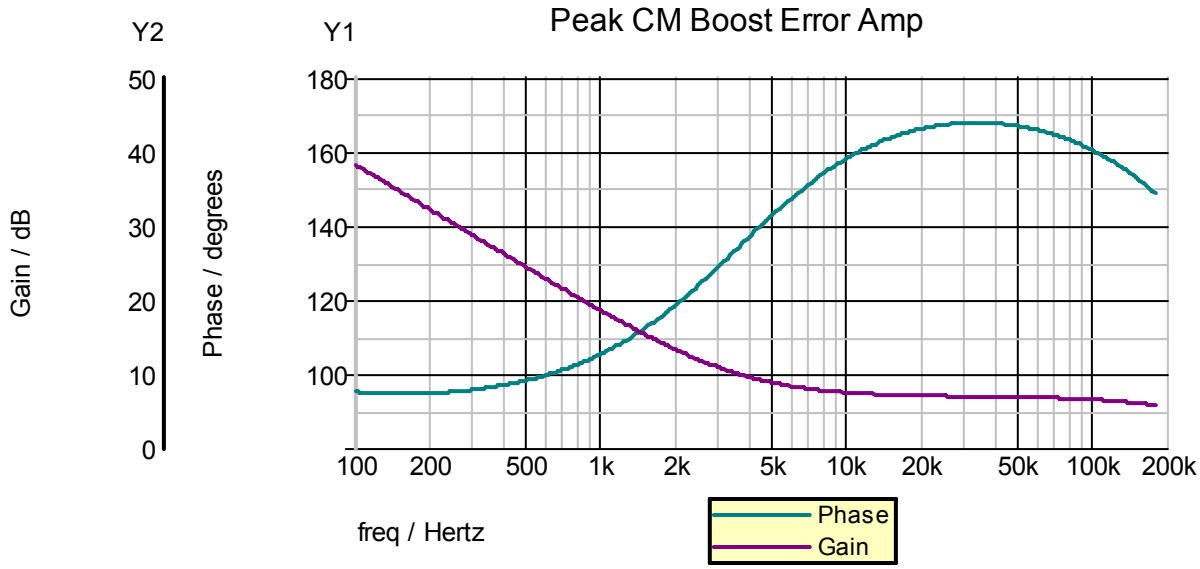

Figure 14. Boost error amplifier.

Boost Design Example – Error Amplifier

There is a pole at low frequency. The mid-band gain is set to produce the desired voltage loop crossover frequency. The error amp zero is generally set about a decade below this frequency. The high frequency pole attenuates switching noise at the error amp output and is not always required, depending on the bandwidth of the amplifier.

$$f_{ZEA} = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C_{COMP}} = 3.6\text{kHz} \qquad G_{EA} = \frac{R_{COMP}}{R_{FB2}} = 2.3 = 7.2\text{dB} \qquad f_{HF} = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C_{HF}} = 800\text{kHz}$$

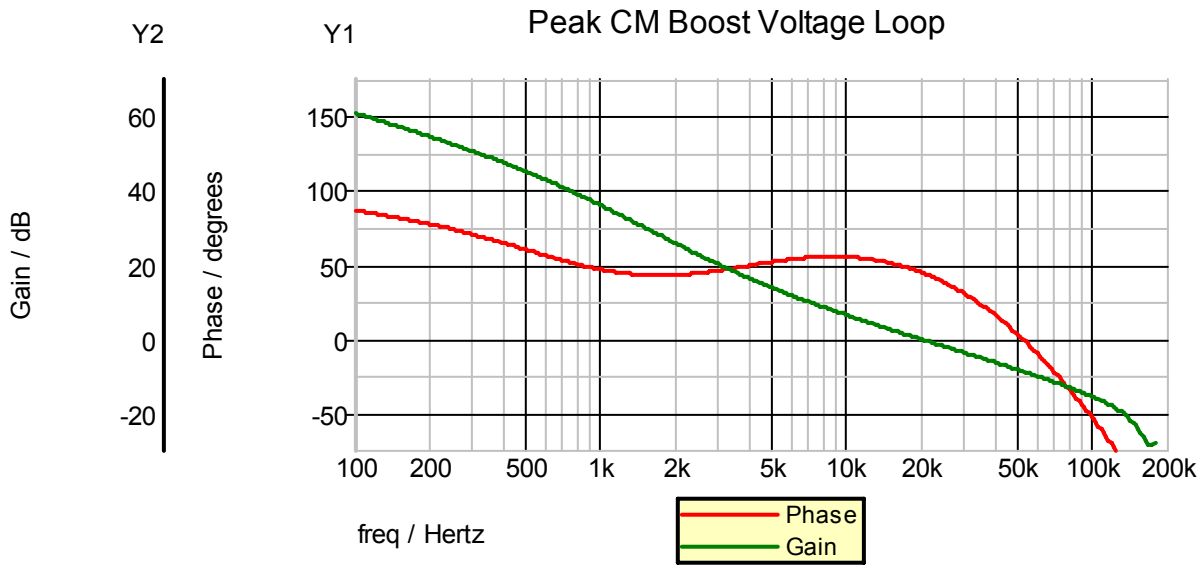

Figure 15. Boost voltage loop.

Boost Design Example – Voltage Loop

The voltage loop plot is simply the sum of the control-to-output and error amplifier plots. For this example, the crossover frequency is 20 kHz with 45° phase margin. The gain margin at 52 kHz is 9 dB.

Buck-Boost Regulator Example

Figure 16 shows a typical buck-boost regulator. For many applications, the synchronous switch S2 is replaced by a diode rectifier. The slope-compensating ramp could be either fixed, or proportional to V_O. For this example, a fixed ramp is used for V_{SLOPE} which is set for $Q = 2 / \pi = 0.637$. The error amplifier G_V has an open loop gain of 3300 (70 dB) and is modeled with a single-pole gain-bandwidth of 10 MHz.

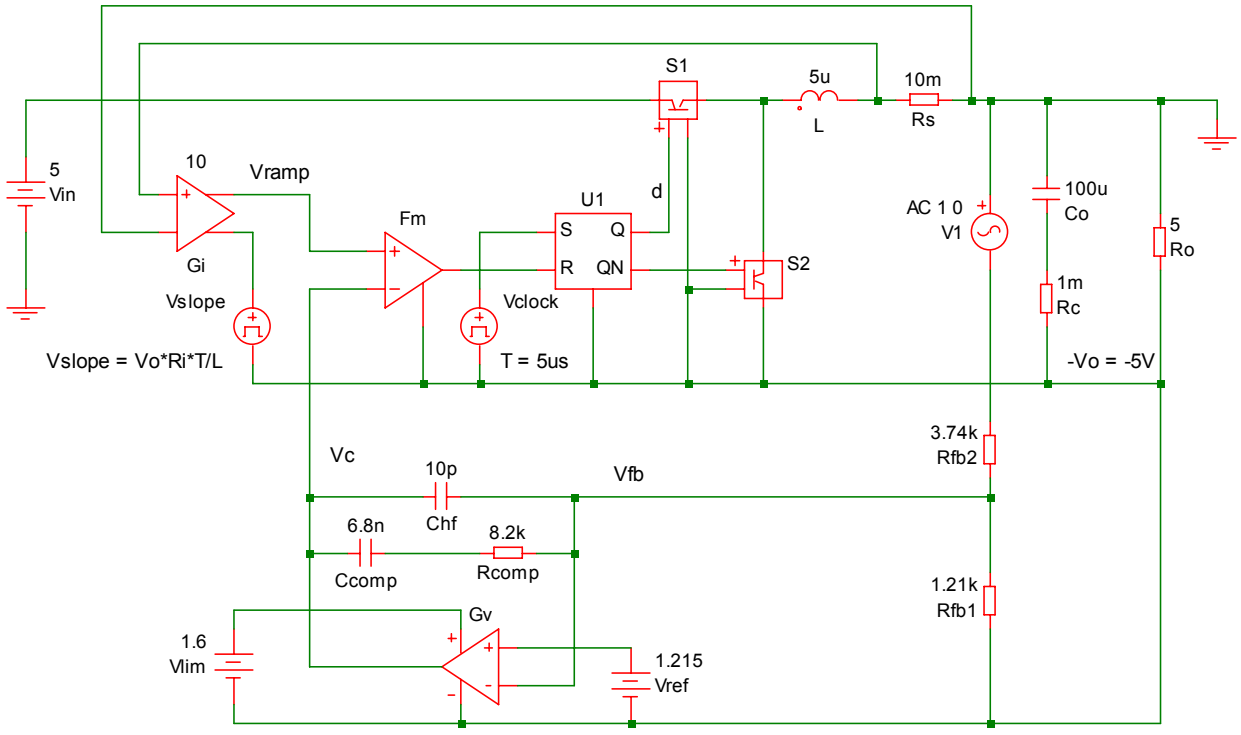

Figure 16. Peak current-mode buck-boost switching model. The control circuit for this example is referenced to the negative output. To measure the frequency response, signals must be differentially sensed with respect to -Vo.

The control-to-output gain is first characterized, and the error amplifier compensation tailored to produce the highest crossover frequency with a phase margin of 45°. The simplified factored control-to-output equation is used for the design analysis.

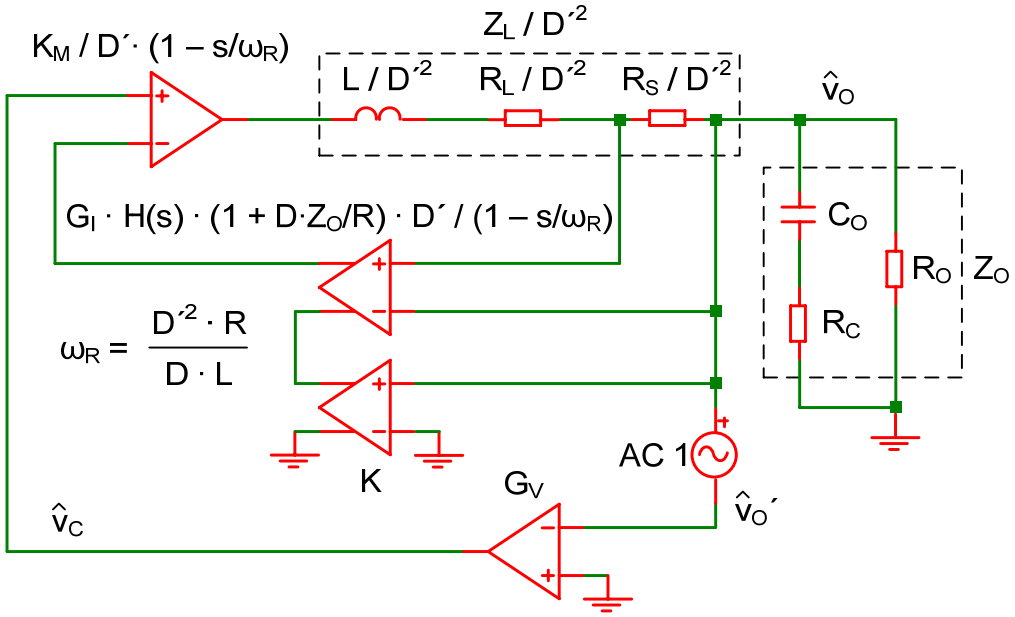

Figure 17. Buck-boost simplified linear voltage loop model.

Linear Model Coefficients

$$V_{ap} = V_{IN} + V_O \qquad D = \frac{V_O}{V_{IN} + V_O} \qquad D' = 1 - D = \frac{V_{IN}}{V_{IN} + V_O} \qquad R = \frac{V_O}{I_O}$$

Transfer Functions

Control-to-Output (Impedance Form):

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{\frac{K_m}{D'} \cdot \left(1 - \frac{D \cdot Z_L}{D'^2 \cdot R}\right) \cdot Z_O}{Z_O + \frac{Z_L}{D'^2} + \cdot \frac{K_m \cdot R_i \cdot H(s)}{D'^2} \cdot \left(1 + \frac{D \cdot Z_O}{R}\right) + \frac{K_m \cdot K}{D'} \cdot \left(1 - \frac{D \cdot Z_L}{D'^2 \cdot R}\right) \cdot Z_O}$$

Current-Mode Buck-Boost – Transfer Functions

Simplified Control-to-Output:

$$\frac{\hat{v}_O}{\hat{v}_C} = \frac{R_O \cdot D'}{R_i \cdot K_D} \cdot \frac{\left(1 - \frac{s}{\omega_R}\right) \cdot \left(1 + \frac{s}{\omega_Z}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{\omega_n \cdot Q} + \frac{s^2}{{\omega_n}^2}\right)}$$

Where:

$$K_D = 1 + \frac{R_O \cdot D}{R} + \frac{R_O \cdot D'^2}{R_i} \cdot \left(\frac{1}{K_m} + \frac{K}{D'}\right) \qquad \omega_R = \frac{R \cdot D'^2}{L \cdot D} \qquad \omega_Z = \frac{1}{C_O \cdot R_C} \qquad \omega_P = \frac{K_D}{C_O \cdot R_O}$$

For an ideal current-mode buck-boost with resistive load, $K_D \approx 1 + D$. In this case, only the single-pole characteristic of ω_P and right-half-plane zero of ω_R are modeled. This may provide a good approximation at a lower crossover frequency ($< 0.1 \cdot f_{SW}$). For accurate results, the complete expressions should be used.

Voltage Loop:

$$\frac{\hat{v}_O}{\hat{v}'_O} = -G_V \cdot \frac{\hat{v}_O}{\hat{v}_C}$$

DC Input Impedance:

$$\frac{\hat{v}_{IN}}{\hat{i}_{IN}}(dc) = -\frac{D'^2 \cdot R}{D^2}$$

Buck-Boost Design Example – Control-to-Output

DC gain terms:

$$D = D' = 0.5 \qquad R_i = G_i \cdot R_S = 0.1 \qquad V_{SL} = V_O \cdot R_i \cdot \frac{T}{L} = 0.5$$

$$K_m = \frac{1}{(0.5 - D) \cdot R_i \cdot \frac{T}{L} + \frac{V_{SL}}{V_{ap}}} = 20 \qquad K = 0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D' = 0.0125$$

$$K_D = 1 + \frac{R_O \cdot D}{R} + \frac{R_O \cdot D'^2}{R_i} \cdot \left(\frac{1}{K_m} + \frac{K}{D'}\right) = 2.44 \qquad \frac{\hat{v}_O}{\hat{v}_C}(dc) = \frac{R_O \cdot D'}{R_i \cdot K_D} = 10.2 = 20.2dB$$

Capacitor pole frequency:

$$f_P = \frac{\omega_P}{2 \cdot \pi} = 780\text{Hz}$$

Right-half-plane zero frequency:

$$f_R = \frac{\omega_R}{2 \cdot \pi} = 80\text{kHz}$$

Sampled-gain inductor pole:

$$f_L(Q) = \frac{1}{4 \cdot T \cdot Q} \cdot \left(\sqrt{1 + 4 \cdot Q^2} - 1 \right) = 49\text{kHz}$$

ESR zero frequency:

$$f_Z = \frac{\omega_Z}{2 \cdot \pi} = 1.6\text{MHz}$$

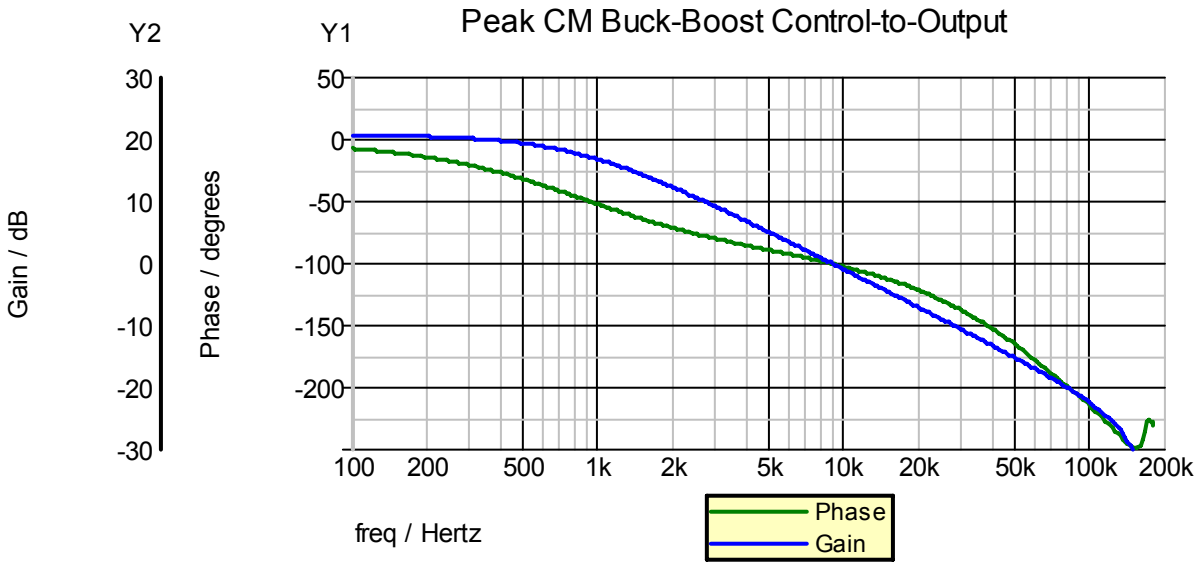

Figure 18. Buck-boost control-to-output.

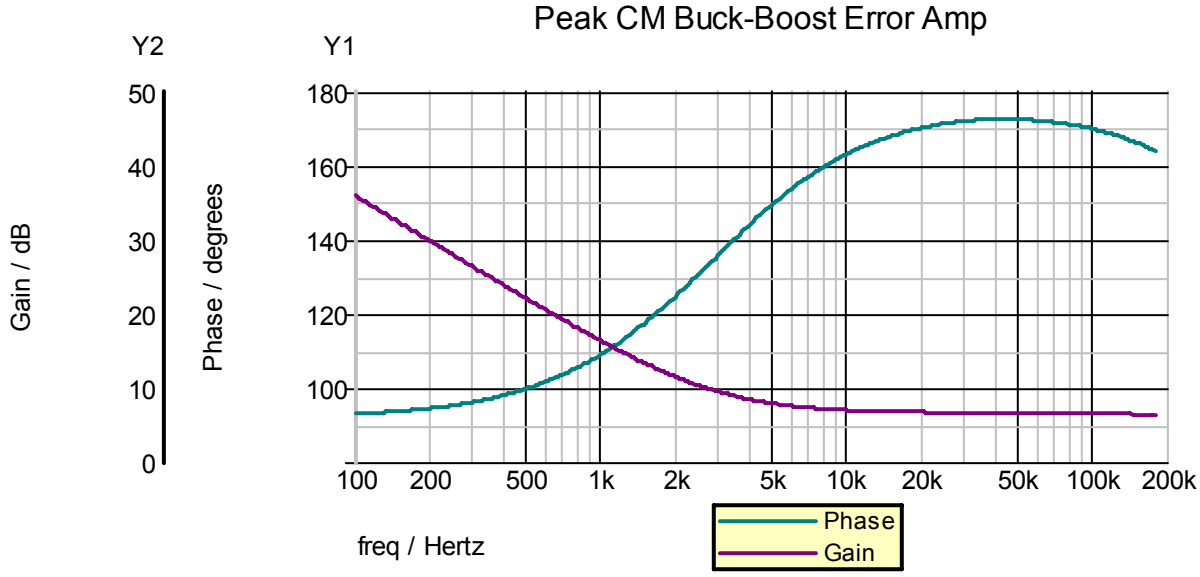

Figure 19. Buck-boost error amplifier.

Buck-Boost Design Example – Error Amplifier

There is a pole at low frequency. The mid-band gain is set to produce the desired voltage loop crossover frequency. The error amp zero is generally set about a decade below this frequency. The high frequency pole attenuates switching noise at the error amp output and is not always required, depending on the bandwidth of the amplifier.

$$f_{ZEA} = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C_{COMP}} = 2.9\text{kHz} \quad G_{EA} = \frac{R_{COMP}}{R_{FB2}} = 2.2 = 6.8\text{dB} \quad f_{HF} = \frac{1}{2 \cdot \pi \cdot R_{COMP} \cdot C_{HF}} = 1.9\text{MHz}$$

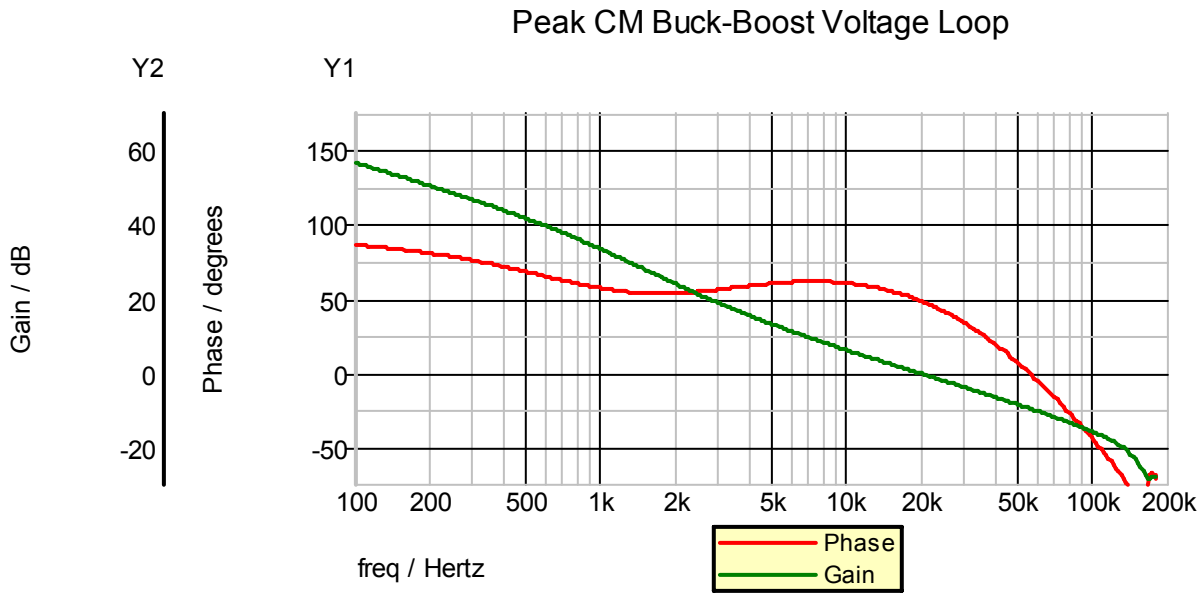

Figure 20. Buck-boost voltage loop.

Buck-Boost Design Example – Voltage Loop

The voltage loop plot is simply the sum of the control-to-output and error amplifier plots. For this example, the crossover frequency is 20 kHz with 48° phase margin. The gain margin at 55 kHz is 10 dB.

General Gain Parameters

General gain parameters are listed in Table 1. These parameters are independent of topology, being written in terms of the terminal voltage V_{ap} and duty cycle D. This table has been updated to show that S_n always refers to the inductor current up-slope and S_f always refers to the inductor current down-slope. See reference [1] for additional operating modes and models.

TABLE 1
SUMMARY OF GENERAL GAIN PARAMETERS $V_{SLOPE} = S_e \cdot T$ $S_{ap} = S_n + S_f$

Mode	S_e, S_n, S_f, S_{ap}	m_c, Q	K_m, K	K_e
PCM1	$S_e = \frac{V_{SL}}{T}$ $S_n = \frac{V_{ap} \cdot D' \cdot R_i}{L}$	$m_C = 1 + \frac{S_e}{S_n}$ $Q = \frac{1}{\pi \cdot (m_C \cdot D' - 0.5)}$	$K_m = \frac{1}{(0.5 - D) \cdot R_i \cdot \frac{T}{L} + \frac{V_{SL}}{V_{ap}}}$ $K = 0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D'$	$K_e = 0$
PCM2	$S_e = \frac{V_{ap} \cdot D \cdot K_{SL}}{T}$ $S_n = \frac{V_{ap} \cdot D' \cdot R_i}{L}$	$m_C = 1 + \frac{S_e}{S_n}$ $Q = \frac{1}{\pi \cdot (m_C \cdot D' - 0.5)}$	$K_m = \frac{1}{(0.5 - D) \cdot R_i \cdot \frac{T}{L} + 2 \cdot K_{SL} \cdot D}$ $K = 0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D' + K_{SL} \cdot D^2$	$K_e = -K_{SL} \cdot D \cdot \frac{L}{R_i}$
VCM1	$S_e = \frac{V_{SL}}{T}$ $S_f = \frac{V_{ap} \cdot D \cdot R_i}{L}$	$m_C = 1 + \frac{S_e}{S_f}$ $Q = \frac{1}{\pi \cdot (m_C \cdot D - 0.5)}$	$K_m = \frac{1}{(D - 0.5) \cdot R_i \cdot \frac{T}{L} + \frac{V_{SL}}{V_{ap}}}$ $K = -0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D'$	$K_e = 0$
VCM2	$S_e = \frac{V_{ap} \cdot D' \cdot K_{SL}}{T}$ $S_f = \frac{V_{ap} \cdot D \cdot R_i}{L}$	$m_C = 1 + \frac{S_e}{S_f}$ $Q = \frac{1}{\pi \cdot (m_C \cdot D - 0.5)}$	$K_m = \frac{1}{(D - 0.5) \cdot R_i \cdot \frac{T}{L} + 2 \cdot K_{SL} \cdot D'}$ $K = -0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D' - K_{SL} \cdot D'^2$	$K_e = -K_{SL} \cdot D' \cdot \frac{L}{R_i}$
EPCM1	$S_e = \frac{V_{SL}}{T}$ $S_{ap} = \frac{V_{ap} \cdot R_i}{L}$	$m_C = \frac{S_e}{S_{ap}}$ $Q = \frac{1}{\pi \cdot (m_C - 0.5)}$	$K_m = \frac{1}{(D - 0.5) \cdot R_i \cdot \frac{T}{L} + \frac{V_{SL}}{V_{ap}}}$ $K = -0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D'$	$K_e = -D \cdot T$
EPCM2	$S_e = \frac{V_{ap} \cdot K_{SL}}{T}$ $S_{ap} = \frac{V_{ap} \cdot R_i}{L}$	$m_C = \frac{S_e}{S_{ap}}$ $Q = \frac{1}{\pi \cdot (m_C - 0.5)}$	$K_m = \frac{1}{(D - 0.5) \cdot R_i \cdot \frac{T}{L} + K_{SL}}$ $K = -0.5 \cdot R_i \cdot \frac{T}{L} \cdot D \cdot D' + K_{SL} \cdot D$	$K_e = -D \cdot T$

Table Notation:

PCM – Peak Current-Mode
VCM – Valley Current-Mode
EPCM – Emulated Peak Current-Mode

1 – Fixed slope compensation using V_{SL}
2 – Proportional slope compensation using K_{SL}

Using mode 2, for Q = 0.637 (single cycle damping), $K_{SL} = R_i \cdot \frac{T}{L}$

Additional Design Points

The examples used here represent results which are possible to achieve given the right selection of components. For many practical designs, a target phase margin of 60° is considered good design practice. Even a 3 MHz amplifier in a closed loop system may demonstrate a measurable phase shift at frequencies below 100 kHz. Combined with delays in the drive and control circuits, this additional phase shift may limit the available bandwidth. For the continuous conduction-mode boost and buck-boost, the right-half-plane zero is usually the limiting factor.

Many integrated circuits have internal slope-compensation, which is not available to the user. In these cases, a careful review of the data sheet parameters may provide enough information to correctly model V_{SLOPE}. The user may find too little or too much slope compensation under certain operating conditions, limiting the performance of the circuit. A moderate variation in the slope-compensating ramp is acceptable for the general application. It is better to have too much slope compensation when it is not needed, rather than too little when it is. The only performance drawback with too much slope compensation is a lower crossover frequency. For this case, it is possible to add a phase boost with a lead network around the top feedback divider resistor.

For closed voltage loop measurements, the output ripple voltage may be amplified by the mid-band gain of the error amplifier, causing an additional ramp component on the control voltage. This may cause a discrepancy between the calculated and measured modulator gain. When the error amplifier is properly modeled, SPICE simulations will generally agree with the measured data.

Switching regulators exhibit a negative input impedance. For current-mode control this negative input impedance remains flat up until the crossover frequency of the voltage loop. This is useful when designing an input filter, which can oscillate at resonance if not properly damped. The criterion for critical damping is:

$$\delta = \frac{1}{2} \cdot \left(\frac{R_{IN} + ESR}{Z_S} + \frac{Z_S}{Z_{IN}} \right) \qquad Z_S = \sqrt{\frac{L_{IN}}{C_{IN}}} \qquad f_S = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{IN} \cdot C_{IN}}}$$

Z_S is the characteristic source impedance and f_S is the resonant frequency. L_{IN} and C_{IN} represent the input filter values. R_{IN} is the input wiring and inductor resistance. ESR is the series resistance of the input capacitor. Z_{IN} is the negative input impedance of the converter, which is $-V_{IN} / I_{IN}$ at dc.

References

[1] Robert Sheehan, "*Current-Mode Modeling for Peak, Valley and Emulated Control Methods*," National Semiconductor white paper, July 31, 2007.

[2] Robert Sheehan, "*Emulated Current-Mode Control for Buck Regulators Using Sample-and-Hold Technique*," Power Electronics Technology Exhibition and Conference, PES02, October 2006.

An updated version of this paper is available from National Semiconductor Corporation which includes complete appendix material.

[3] R.B. Ridley, "*A New, Continuous-Time Model for Current-Mode Control*," IEEE Transactions on Power Electronics, Volume 6, Issue 2, pp. 271–280, 1991.

[4] F.D. Tan, R.D. Middlebrook, "*A Unified Model for Current-Programmed Converters*," IEEE Transactions on Power Electronics, Volume 10, Issue 4, pp. 397–408, 1995.

For reference [4] the following clarifications and corrections are made:

$$V_{off} = V_{ap} \qquad I_{on} = I_C$$

Buck	$\hat{i}_l = \hat{i}$	$L_e = L$	$E(s) = \frac{V_{off}}{D}$
Boost	$\hat{i}_l = \hat{i}_g$	$L_e = \frac{L}{D'^2}$	$E(s) = V_{off} \cdot \left(1 - \frac{s \cdot L}{D' \cdot V_{off} / I_{on}}\right)$
Buck-Boost	$\hat{i}_l = \hat{i} + \hat{i}_g$	$L_e = \frac{L}{D'^2}$	$E(s) = \frac{V_{off}}{D} \cdot \left(1 - \frac{s \cdot L}{D' \cdot V_{off} / I_{on}}\right)$

[5] Robert Sheehan, "*A New Way to Model Current-Mode Control, Part 1*," Power Electronics Technology Magazine, May 2007.

[6] Robert Sheehan, "*A New Way to Model Current-Mode Control, Part 2*," Power Electronics Technology Magazine, June 2007.

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