Application Report
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EMI and Thermal Design Tips and Tricks for 48-V IGBT/SiC/GaN Supply for Automotive Motor Drive Inverters

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ABSTRACT

This application note discusses the design and EMI/Thermal optimization of a 48-V IGBT gate drive supply for HEV/EV and mild-hybrid automotive applications. The design can be easily modified for SiC and GaN as well, and the tips and tricks will still apply. 48-V automotive applications present stringent requirements on EMI and reliability which requires optimized thermal performance. The content in this app note provides tips and tricks for optimizing EMI and thermal performance for this end equipment as well as any power design.

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1 Overview

The HEV/EV automobile market has surged in recent years with no sign of slowing down. The automotive customers are striving for more efficient, environmentally friendly modes of transportation and car companies are hearing the call. These automobiles have many complex systems which all need to work together, one of which we'll discuss in this app note. Every HEV/EV car will have an electric motor, and to drive the motor every HEV/EV car will have an inverter. In order to power this inverter the system needs an isolated, low-EMI, thermally optimized supply for the gate drivers. A previously released TI reference design, TIDA-00199, describes a 24-V fly-buck IGBT supply for traction inverters. The automotive market, however, is moving toward 48-V systems which, compared to 24 V, improves system-wide efficiency, weight and cost. But this comes with new challenges in EMI and thermal performance from the power supply. This app note explains how to convert TIDA-00199 to a 48-V design, how to optimize the layout for EMI and thermal performance, and how to modify the circuit to work with other high power switches including SiC and GaN.

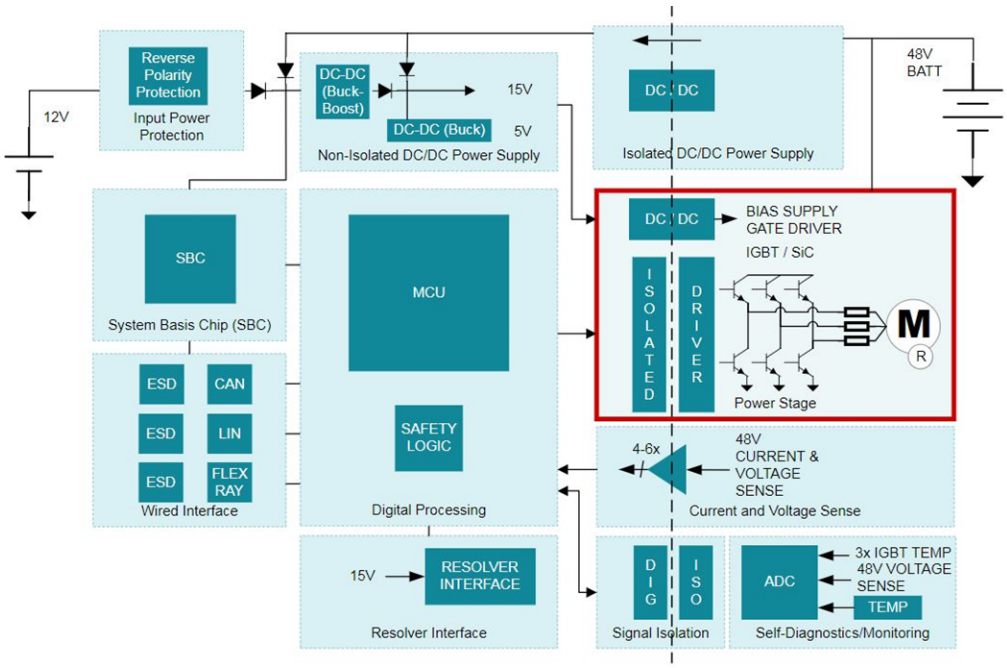

Figure 1. Typical Block Diagram for Full Traction Inverter End Equipment

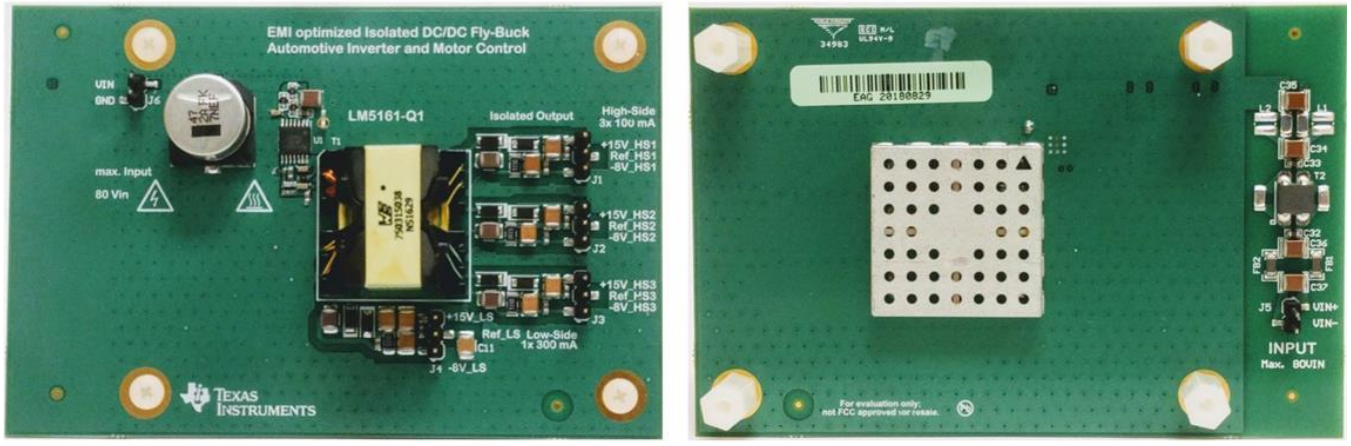

Figure 2. 48-V Flybuck IGBT Supply Design: Board Front (left) and Back (right)

2 Context from TIDA-00199

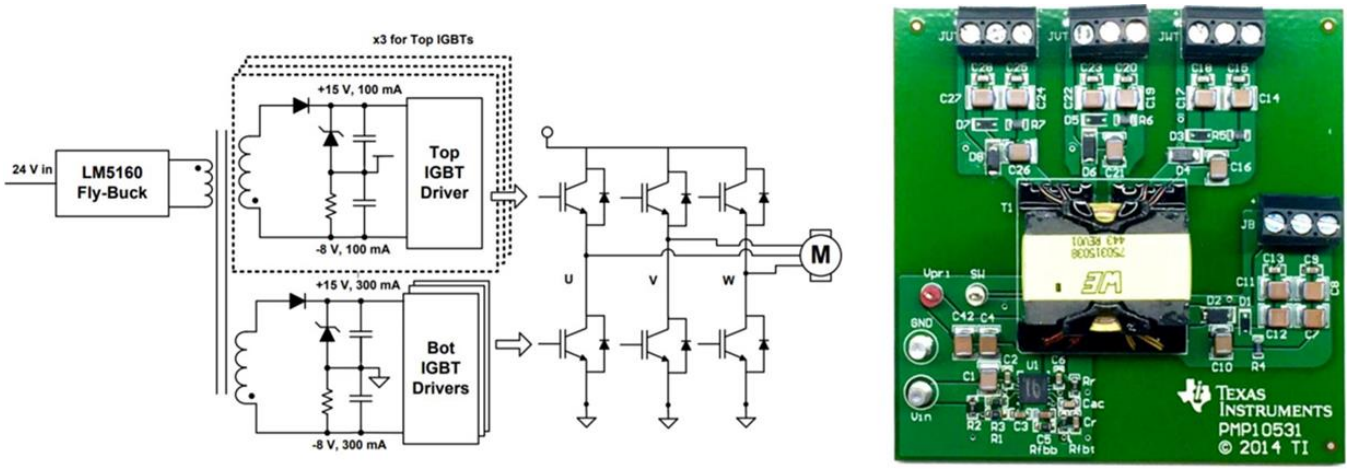

Figure 3. TIDA-00199 24-V Flybuck IGBT Supply Design: Simplified Schematic (left) and Board (right)

TIDA-00199 utilizes a 24-V input to create a fly-buck with 4 isolated outputs, 3 for the 3 top gate drives and 1 for the bottom gate drives. Each output is regulated to 23V which is split into +15 V/0 V/–8 V by a Zener voltage regulator. IGBT gate drivers require a supply of +15 V/0 V/–8 V. +15 V turns the IGBT ON whereas –8 V turns the IGBT off. IGBTs require –8 V to prevent the IGBT from unintentionally turning on due to voltage induced at the gate from the Miller effect.

The isolation protects all upstream circuitry from the high voltages used to drive the high-power motors through the IGBTs in the event of an IGBT failure. The design has one isolated supply for all three low-side gate drives because they are all referenced to high-power ground and any switching activity will not change the voltage (with respect to high-power ground) required to turn on and off these IGBTs. The high-side IGBTs on the other hand will turn on at a gate voltage referenced to their emitter. Since these IGBTs switch out of sync from one another the system needs three isolated supplies to turn each high-side IGBT on and off. The design allows the high-side gate drivers to supply 100 mA each where the single low-side drive is capable of delivering 300 mA (3 × 100 mA because it is supplying power to 3 gate drivers).

3 Modification for 48-V Input

TIDA-00199 utilizes a 24-V input. Many automobile manufacturers are starting to design with 48-V systems to improve energy density, increase power delivery capability, and improve efficiency in their HEV/EV and even mild-hybrid systems. Modifying this design to accept 48 V is straightforward.

First replace LM5160 with LM5161. LM5160 is a 65-V COT buck/fly-buck converter. The system requires margin for the 48-V HEV/mild hybrid systems in the event of load dump conditions so the design swaps the 65-V LM5160 converter with the 100-V LM5161.

Figure 4. Pinout Comparison: LM5160 (left) vs LM5161 (right)

Change the input capacitors to accommodate the higher voltage. Utilize 100-V rated capacitors to allow proper voltage margin and to account for capacitance derating.

Next, change the transformer. TIDA-00199 has V_{IN} = 24 V, $V_{OUT\_PRIMARY}$ = 10.5 V, and $V_{OUT\_SECONDARY}$ = 23 V so the transformer has a 1:2.3 turns ratio. V_{IN} is now 48 V and we'd like to maintain duty cycle of around 40-50% for the fly-buck. Design for $V_{OUT\_PRIMARY}$ = 24 V. $V_{OUT\_SECONDARY}$ cannot change so the design updates the transformer design to a 1:1 turns ratio. Lastly, adjust the feedback resistors as necessary to achieve the desired 24V primary voltage and subsequently 23 V (+15 V/–8 V) output on the secondary sides.

See Figure 5 through Figure 11 for the final schematic, layout, and board.

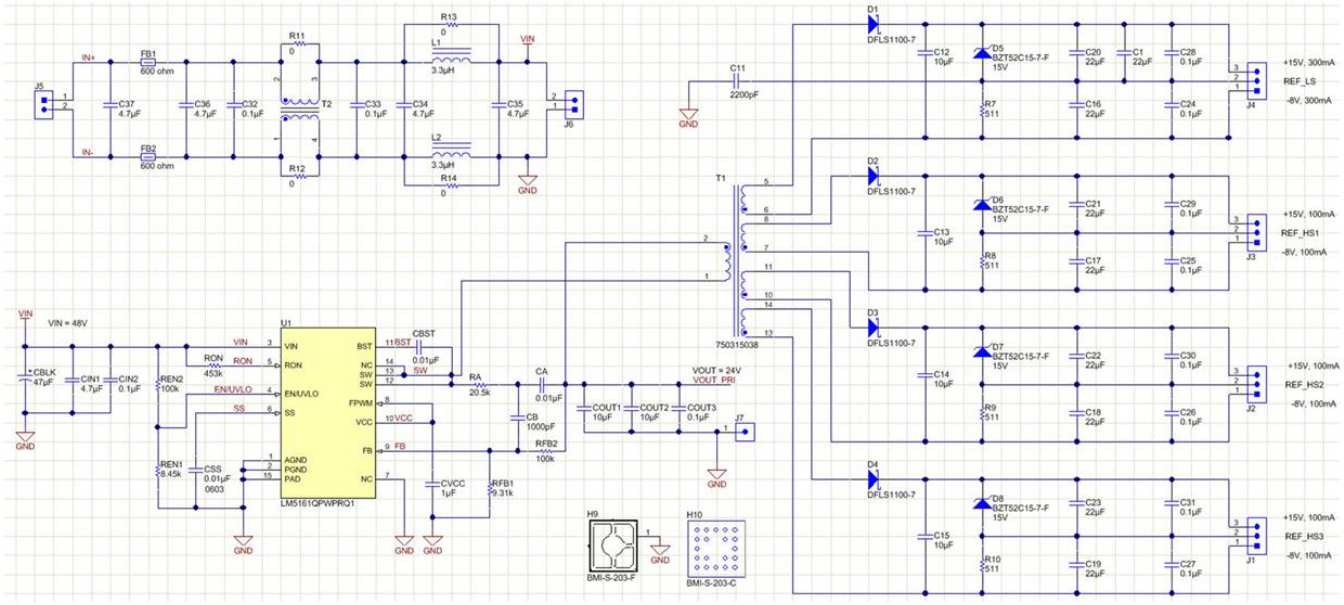

Figure 5. 48-V Flybuck IGBT Supply Design: Schematic

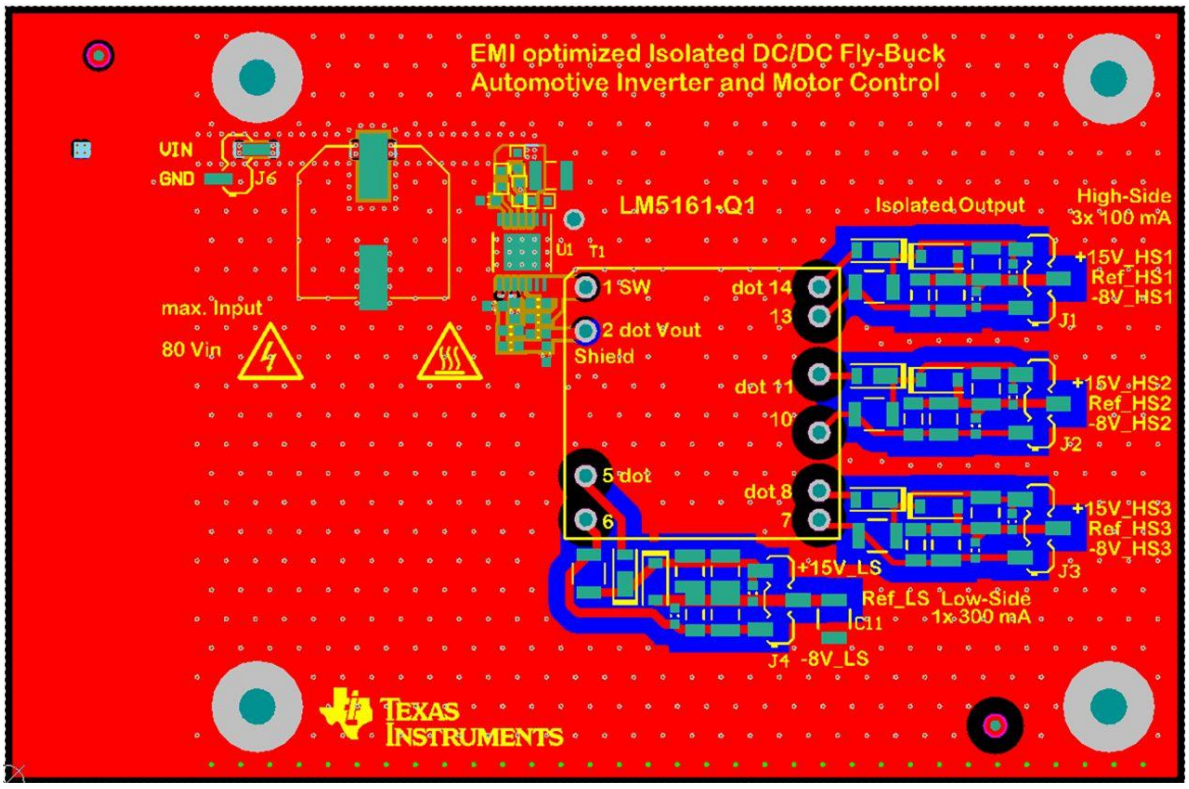

Figure 6. 48-V Flybuck IGBT Supply Design: Layout – Top Layer (red)

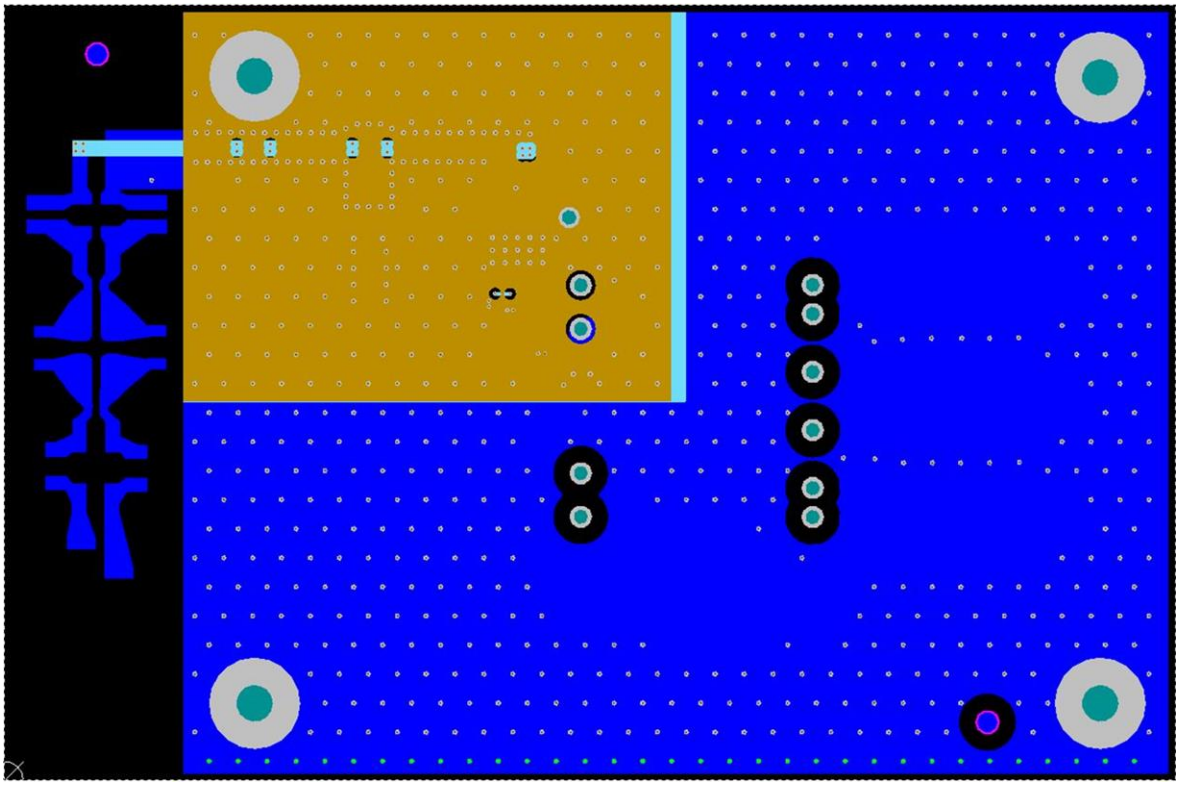

Figure 7. 48-V Flybuck IGBT Supply Design: Layout – Mid-Layer 1 (yellow)

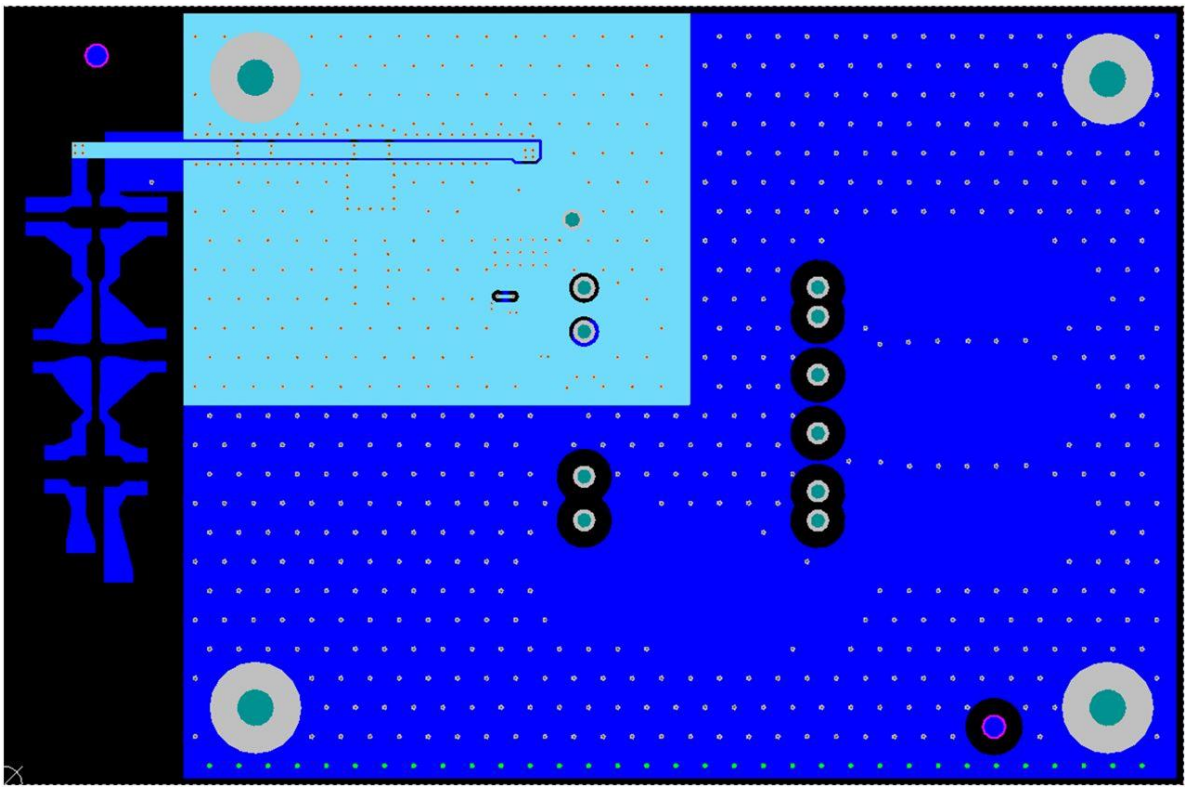

Figure 8. 48-V Flybuck IGBT Supply Design: Layout – Mid-Layer 2 (light blue)

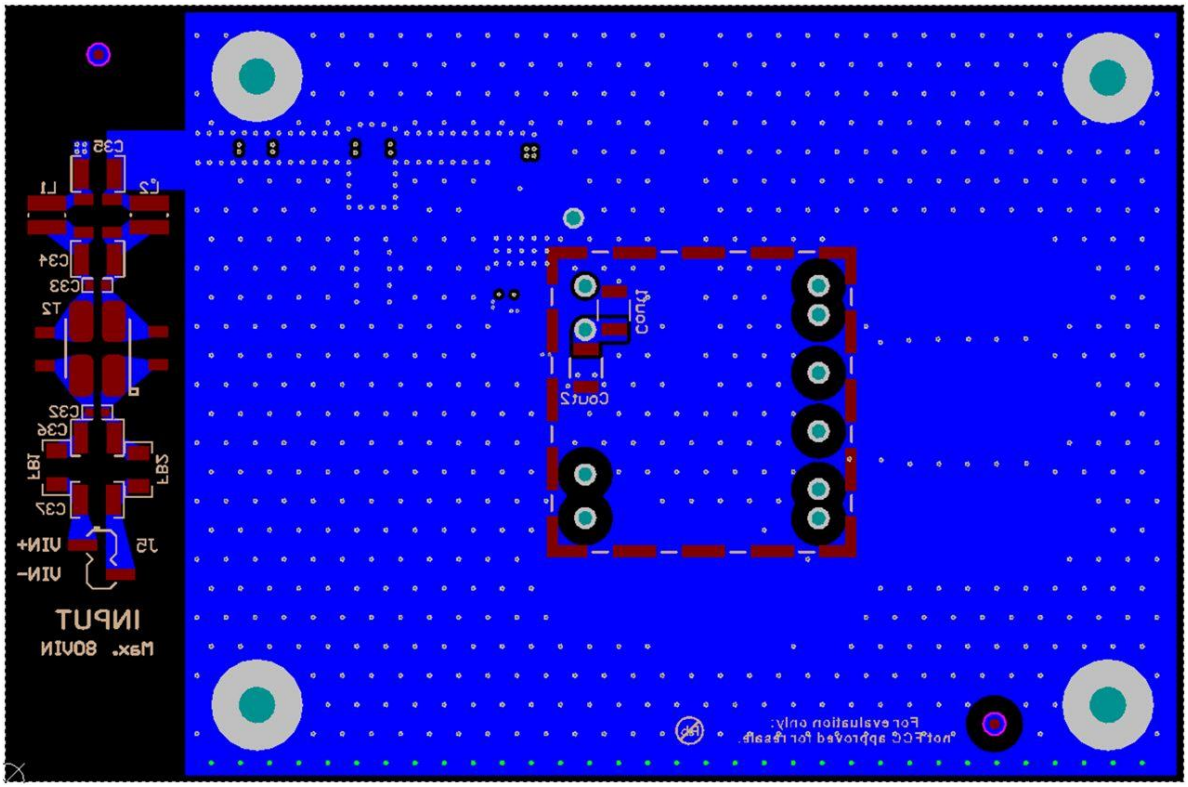

Figure 9. 48-V Flybuck IGBT Supply Design: Layout – Bottom Layer (dark blue)

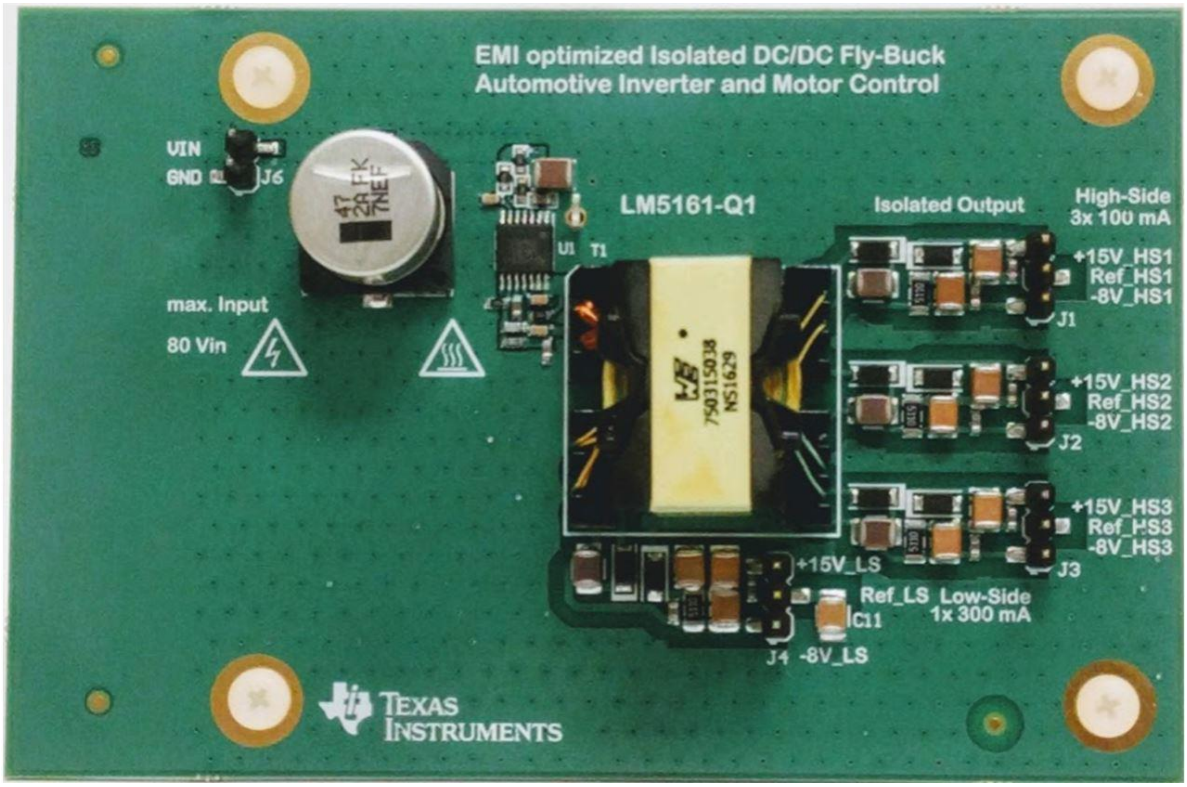

Figure 10. 48-V Flybuck IGBT Supply Design: Board - Top

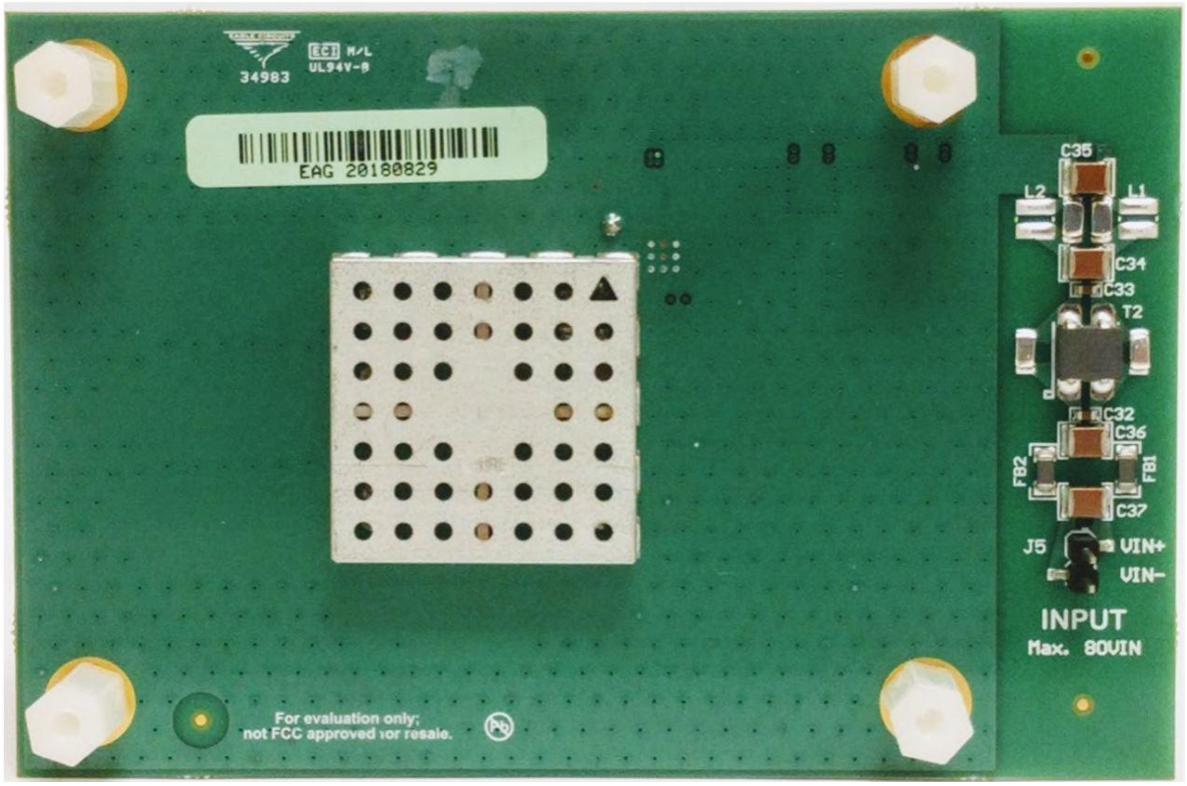

Figure 11. 48-V Flybuck IGBT Supply Design: Board - Bottom

4 EMI Layout Optimization

4.1 EMI Filter Component Selection

The EMI filter in this design utilizes the three most common elements in EMI filters - an LC filter, a common-mode choke, and a ferrite bead. The noise comes from the converter which is connected to V_{IN} (the right side of the circuit in Figure 12) so let's analyze from right to left and discuss each component in more detail.

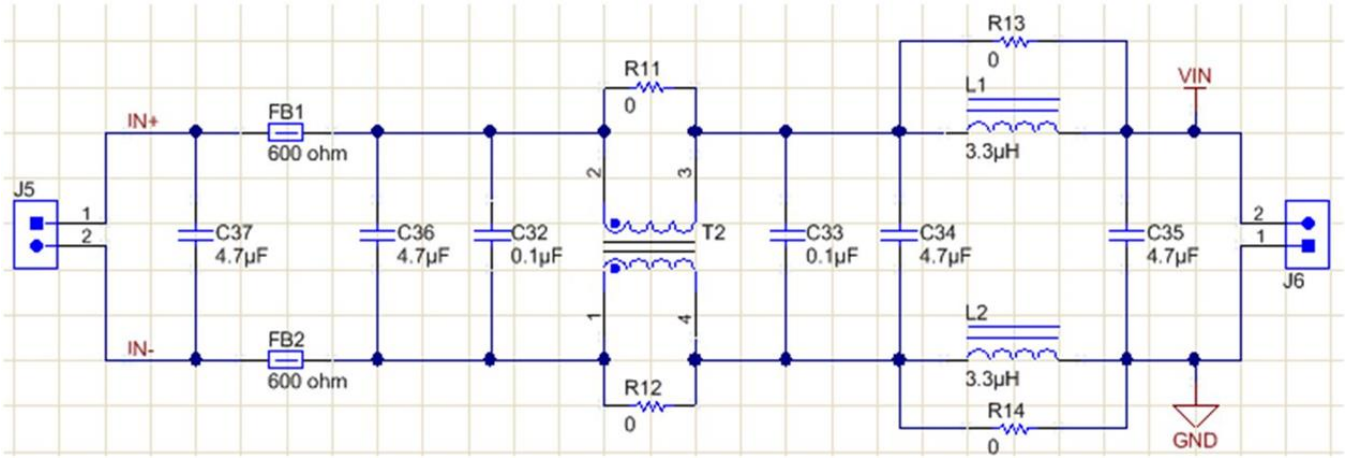

Figure 12. EMI Filter Schematic

First, the noise sees the LC pi filter. Note, R13 and R14 are there to bypass the inductors if that is desired during testing. These are "do not populate" for the board. The LC filter is the most common type of EMI filter. By selecting the values of inductance and capacitance one can filter certain frequencies. Typically LC filters are just one inductor and one capacitor (or two capacitors to make a pi filter) but this design utilizes two inductors (L1 and L2) with two capacitors (C34 and C35). The two 3.3-µH inductors with the two 4.7-µF capacitors have a corner frequency of ~ 40 kHz so ideally anything over 40 kHz would be attenuated as frequency increases. Real components, however, are not ideal. The capacitors will have parasitic inductance due to the package/size/placement/layout and the inductor will have parasitic capacitance due to the design/build/type of the inductor so the design needs further filtering.

The next filter element seen by the noise is the common-mode choke. R11 and R12 short out the choke so for this discussion assume the design depopulates these resistors. The common-mode choke will reject common-mode current. Any current flowing from pin 2 to 3 will induce a current in the opposite direction in the other pins (current flowing from pin 4 to 1). This means any current flowing from 2 to 3 rejects any current flowing from 1 to 4. This is a useful component in rejecting common-mode noise which can be a big issue, especially in an isolated design like this. We'll discuss more of this later.

The last filter element seen by the noise is the ferrite bead/capacitor pi filter. The ferrite bead is rated at 600 Ω at 100 MHz. This works to reject any extra high-frequency noise that seeps through the parasitic capacitance in L1 and T2.

Choose all surface-mount components, including J5 and J6. This keeps everything on the bottom layer to allow the top-layer GND pour to act as a shield. This is explained more in Section 4.2.

4.2 EMI Filter Layout

Layout can be one of the largest causes of EMI if done poorly which means good layout of the EMI filter is imperative. The design has to consider component selection, placement, and layout, among other things.

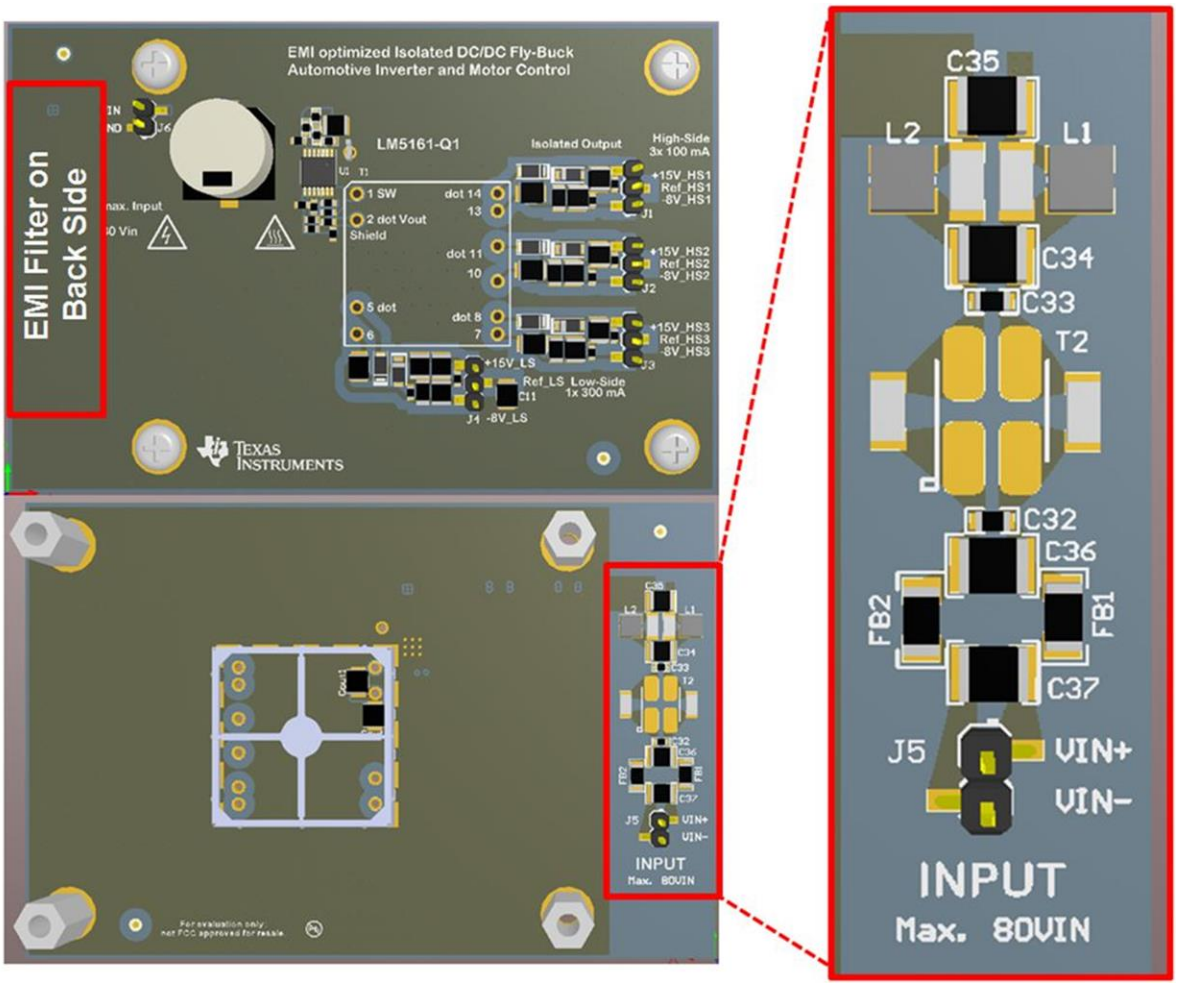

Figure 13. EMI Filter Layout

First, note that the entire filter is on the bottom side of the board. The top side has lots of switch noise from the SW node, transformer, and secondary-side circuitry. The design provides a free shield from the top-side GND plane over the EMI filter. This blocks any noise that would inject into, and potentially bypass the EMI filter.

Next, note that the bottom-side GND pour has been cut away around the EMI filter. This is to ensure the paths of the return current. The EMI filter works best if all current going through the entire EMI filter returns back through the entire EMI filter. This is a bigger deal if the circuit does not have the low-side inductor L2 or the design has multiple capacitors at the end of the filter (parallel with C35) and the designer wants the return current to hit every one of them in order.

The filter is laid out in a straight line with attention to minimizing loop area. For example, C32 and C36 are very close to one another. Any distance will just elongate the loop and increase loop area. Any loop introduces an opportunity for inductive coupling.

Note that the distance between L1 and L2 is not as small as it could be and this goes against the recommendations of the previous paragraph. This does increase the loop area but this is to prevent coupling from L1 to L2. Typically one would use an LC filter with a single L instead of an L on the positive and negative current paths, so this is not typically a consideration in board design. In this case, for optimized EMI, the design adds a second inductor and spaces it to reduce coupling.

4.3 Layout from EMI filter to V_{IN}

The circuit starts by taking V_{IN} at the start of the EMI filter and routing directly to mid-layer 2. This allows us to route V_{IN} across the board with a ground shield above and below (top layer and bottom layer, respectively). The layout also utilizes via stitching around the trace on mid-layer 2. See the “C.1” markings on Figure 14, especially on the light-blue mid-layer 2.

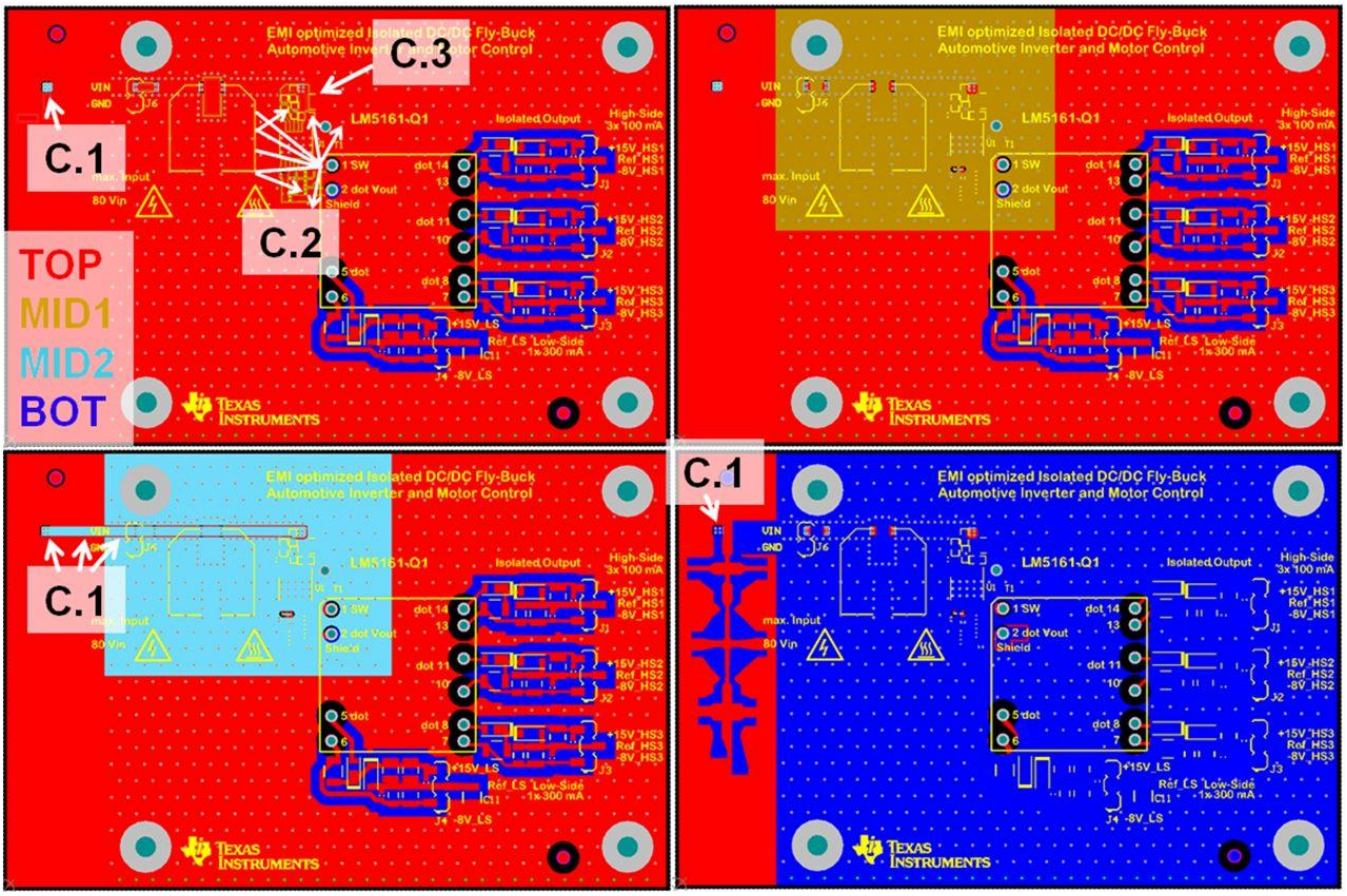

Figure 14. EMI to V_{IN} Layout Optimization

The layout ensures that there is a solid GND path under/above the V_{IN} trace. This allows for the V_{IN} return path to flow directly under/above V_{IN}. This reduces the loop width to as small as the thickness of the board which will minimize loop area and reduce any inductive coupling. This will also reduce the emitted magnetic flux from the time-changing currents on V_{IN}.

The electrolytic bulk capacitor is placed in direct line of sight between the V_{IN} pins (J6, also labeled V_{IN} and GND on the layout) and the switch node. See marking “C.2”. The SW node (as well as the transformer in general) will radiate EMI as portrayed by the white arrows. The electrolytic capacitor’s metal outside canister is connected to the GND pin of the capacitor which is connected to the GND plane. EMI will either be absorbed and redirected to GND or reflected.

Last consider the V_{IN} capacitors. See marker “C.3”. The layout places the smallest value closest to the IC because it can handle the highest frequencies (lower inductance due to smaller package/loop area can be placed closer to the IC). The layout then places the larger capacitor. The positive terminal is as close as possible to the V_{IN} pin of the IC, and the negative terminal has clear low-impedance return path that can flow directly beside or below the incoming current when possible.

4.4 Switch Node

The switch node is often the main source of EMI in power converters. This node will be swinging from 0 V to 48 V and back to 0 V at 400 kHz. This high dv/dt means this node can easily capacitively couple to nearby circuitry. For this reason the layout tries to reduce the area of this node, shield it as much as it can, and keep it a safe distance from susceptible circuitry such as the EMI filter.

This layout utilizes the “no connection” pin 14 of the LM5161 and routes straight through to the transformer as shown on Figure 15 marked “D.1”. If the IC had been rotated 90 degrees counter-clockwise to avoid this pin, the layout would need to leave more space between the IC and the transformer to fit the passives connected to the FB, FPWM, BST, and VCC pins (marking “D.2”). In the current configuration the layout has space for these components which keeps the SW trace length short. The layout also places the bootstrap capacitor close to the IC pins and uses short traces (marking “D.3”). One can also add stitching around the SW node to redirect any inter-layer noise back to GND.

Make sure to check the data sheet before connecting NC pins to other nodes. Sometimes it is not recommended but other times it can be utilized like it is here.

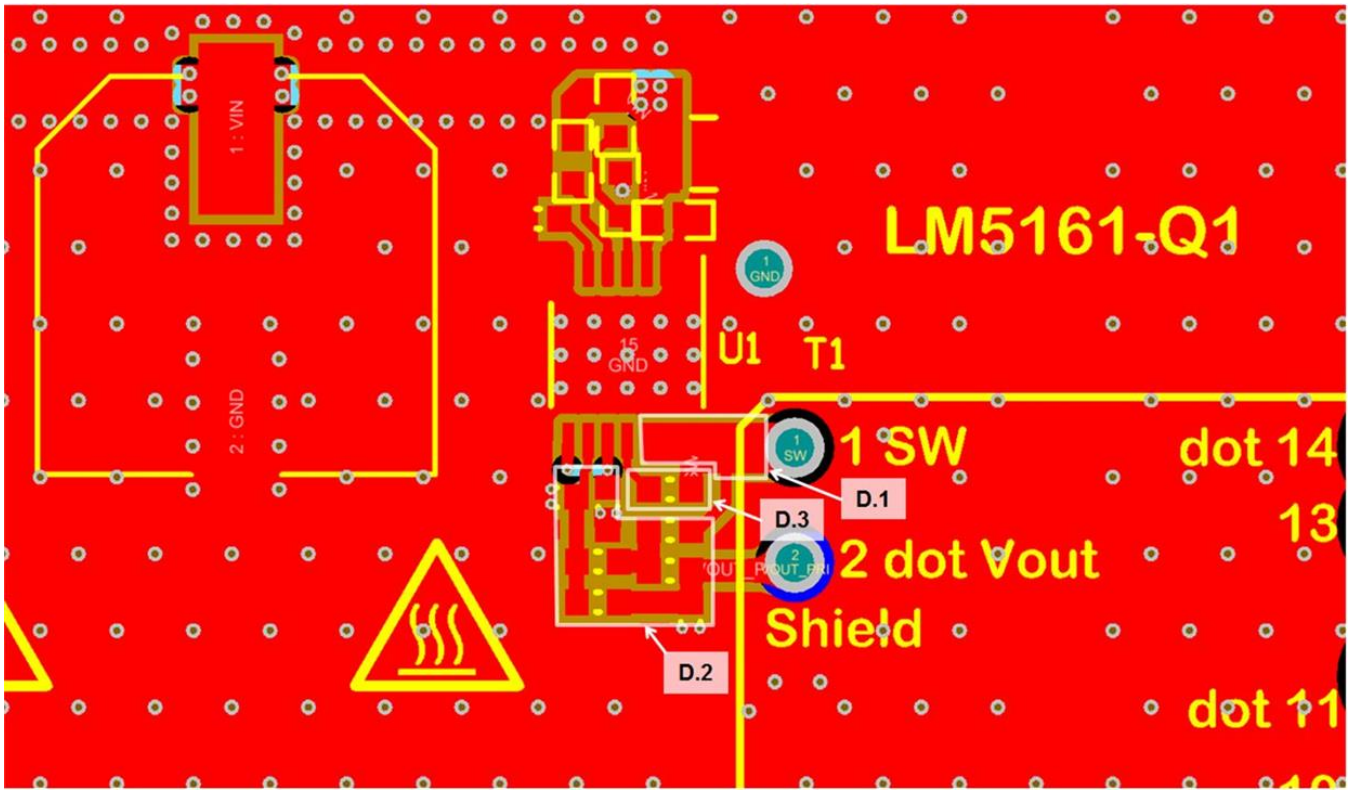

Figure 15. Switch Node Layout Optimization

4.5 Small Loops in COUT Return Path

The schematic in Figure 16 shows the primary-side V_{OUT} capacitors (COUT1/2/3) connected to GND but it is up to the layout to create an optimized path to make this connection.

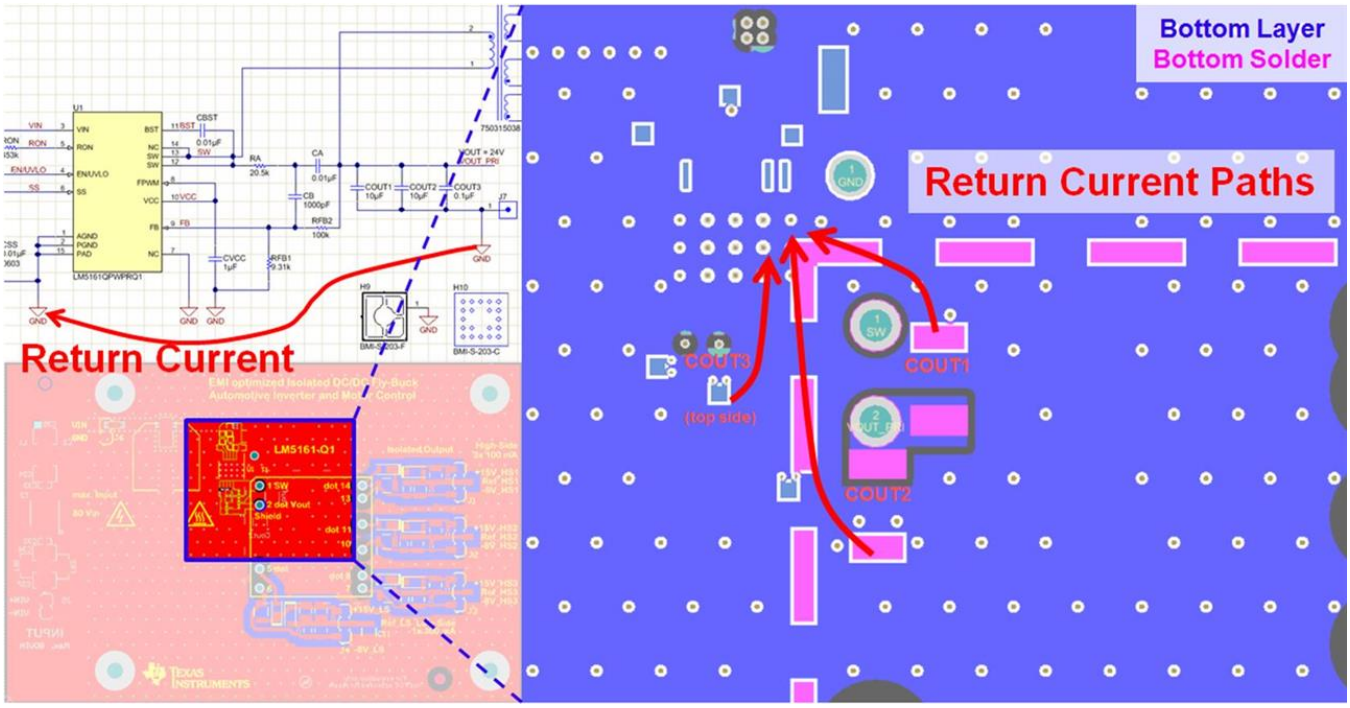

Figure 16. Output Capacitors Layout Optimization

COUT1 and COUT2 are on the bottom side. See the clear return path from the capacitor's negative terminals back to the GND pin of the LM5161 (through the vias to get back to the top layer).

COUT3 is on the top layer. The negative terminal has two vias touching the pad to allow the return current to go to the bottom layer (and mid layers), then travel to the GND pin on the LM5161 (through the DAP vias).

These return paths can travel very close, if not directly under the incoming current path. That means the loop area is effectively as small as the thickness of the board (top to bottom layer). This will reduce inductive coupling from this loop thus improving EMI performance. This strategy is implemented throughout the board layout and is a good idea to utilize whenever possible.

4.6 Transformer

The transformer plays a significant role in the EMI performance of a fly-buck, or any power design for that matter. There are many considerations when selecting or designing a transformer with EMI in mind.

Shielding secondary from primary: Shielding secondary from primary inside the transformer will yield better EMI performance. This reduces the capacitance between primary and secondary. The high dv/dt on the switch node can capacitively couple to the secondary through this capacitance if not shielded. The coupling pushes current into the secondary, which causes the entire secondary circuit voltage to swing up and down (with respect to primary GND). This will capacitively couple with the parasitic capacitor from the secondary copper traces to the copper GND plane under the board in the EMI tests, or the chassis in real-life applications (see Figure 17). This is common-mode current which, if large enough, causes the board to fail EMI tests. See Figure 18 for the equivalent schematic.

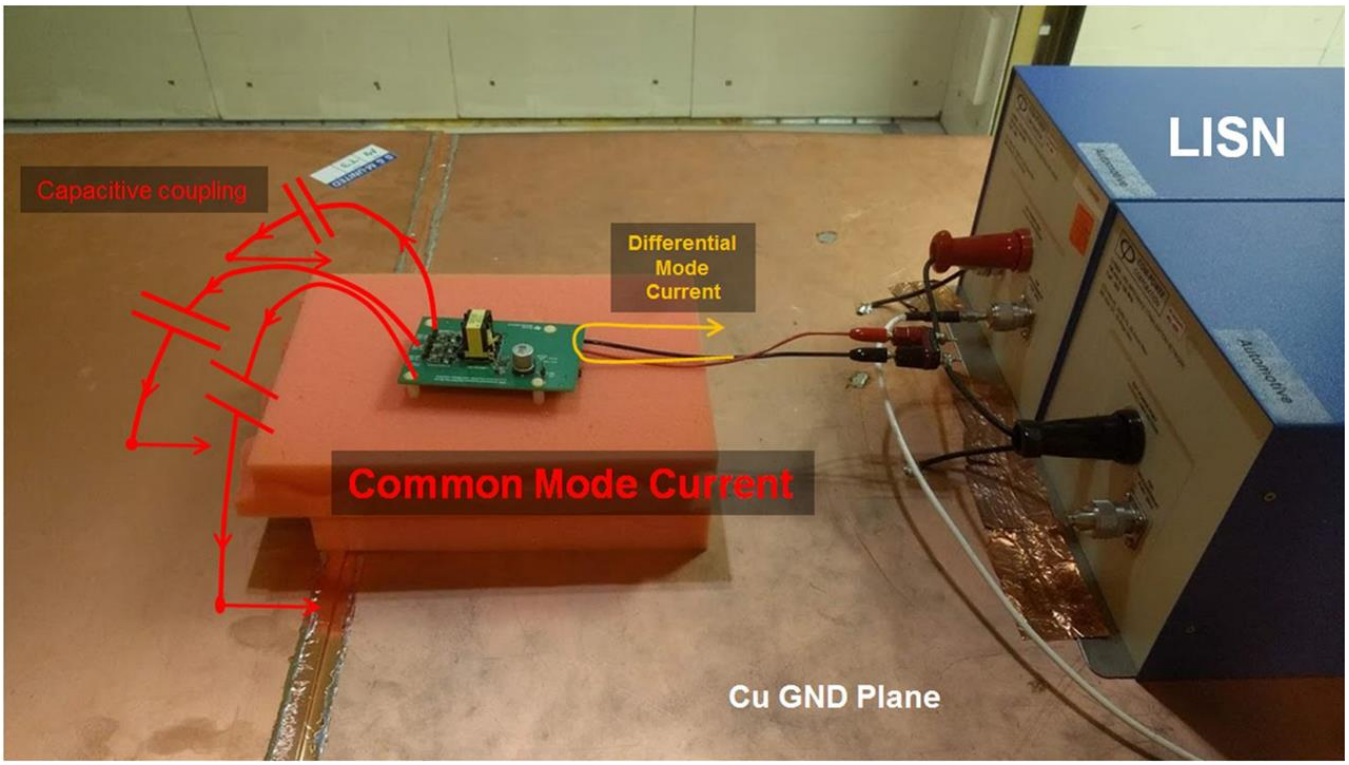

Figure 17. Common-Mode Current in EMI Test

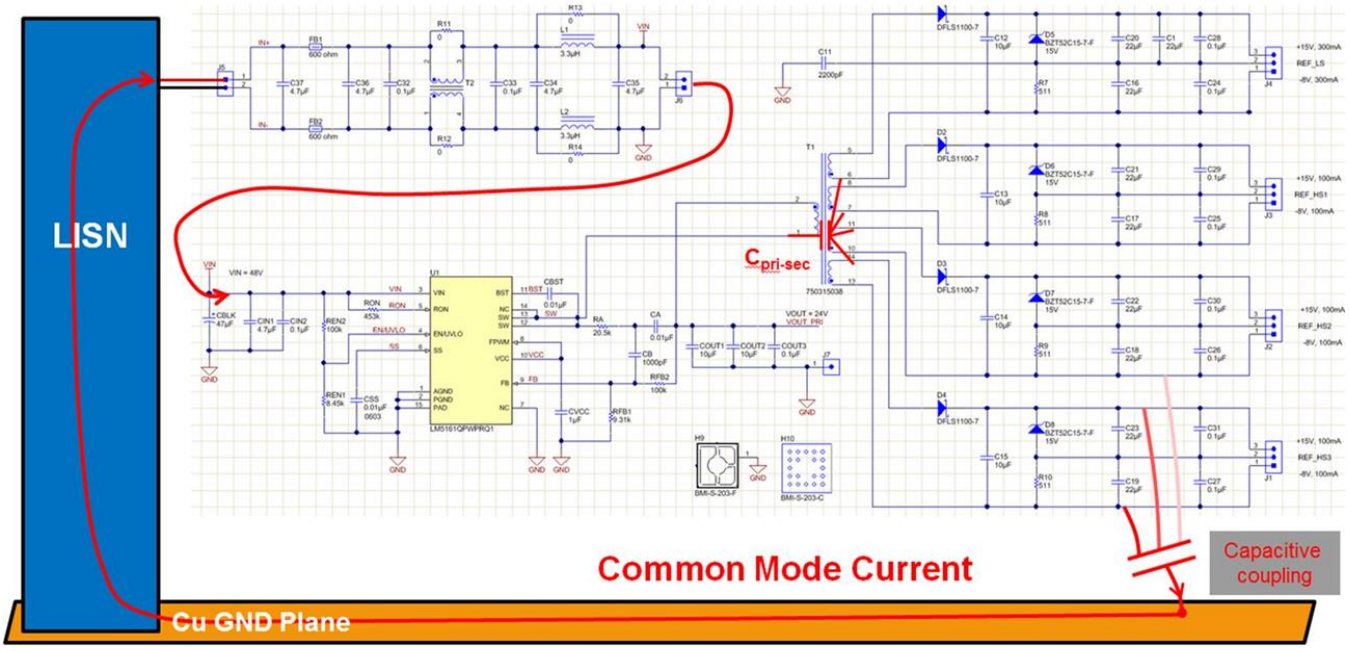

Figure 18. Common-Mode Current in EMI Test – Equivalent Schematic

However, adding a shield to a transformer design adds space between primary and secondary. This increases leakage inductance which can be harmful to the normal operation of the converter, especially for Fly-Bucks. Do some calculations and/or consult a transformer vendor to calculate the benefits and drawbacks of an internal shield. This design opts to construct the transformer without the shield and the EMI performance suffers in the test results.

External shielding: The transformer utilizes magnetic fields to transfer power from winding to winding. Those magnetic fields, if not contained, may couple into loops in the circuit at surprisingly far distances. See Figure 17 for example. The red and black wires going between the LISN and the board have space between them (this picture shows a bad case but even in better tests there's space). More space means more loop area which will pick up any stray magnetic fields, and since this jumps past the EMI filter, this will result in much worse EMI performance. If space and cost permits, one can use an externally shielded transformer for the best magnetic field containment. This may also be implemented with a flux band wrapped around the transformer core. This design did not go so far as to utilize an entirely externally shielded transformer, but more shielding is certainly an option to improve EMI.

Surface-mount: This layout places the EMI filter on the back-side. It would be best practice to select a surface-mount transformer as opposed to through-hole transformer to ensure the separation of the noisy transformer pins from the back-side of the board. Again, this design did not utilize a surface-mount transformer but the design has added an external metal shield on the back side to contain any EMI from the noisy pins.

Transformer placement: The transformer is placed in the center of the board. Inductive coupling decays by the distance squared and/or distance cubed between the source and the victim. By centering the transformer we're causing any inductive coupling to travel around the board to couple to the GND plane. A centered transformer minimizes the total amount of coupling.

Pin selection: Transformers and inductors are typically wound from inside-out. There is one pin which connects to the inside of the winding while the other connects to the outside. In a buck/Fly-Buck, one side of this winding is SW which is noisy, while the other side is V_{OUT} which is not noisy. If the circuit connects SW to the pin connected to the inside of the winding, the outside of the winding will effectively shield the inside windings. This transformer denotes which pin is connected to the inside of the winding. The design connects this pin to the SW node.

4.7 Y-cap on Low-Side Gate Drive Output:

Ideally the secondary voltage is steady with respect to the primary but the capacitive coupling through the transformer will cause the entire secondary side to swing up and down with SW (with respect to primary GND). See Figure 19 for an equivalent circuit showing the placement of each of these capacitors. Figure 20 shows a more intuitive schematic-like capacitor placement.

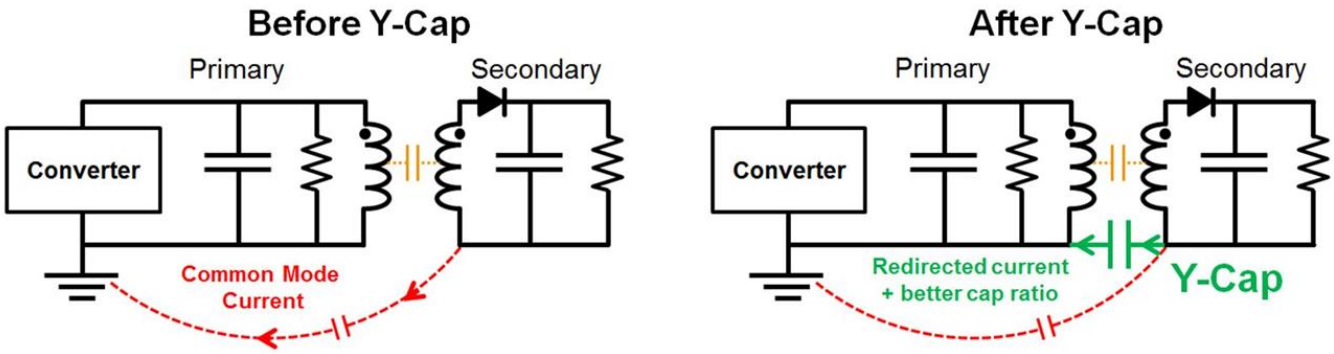

Figure 19. Y-Cap Effect on Circuit Performance Regarding Transformer Pri-Sec Capacitive Coupling

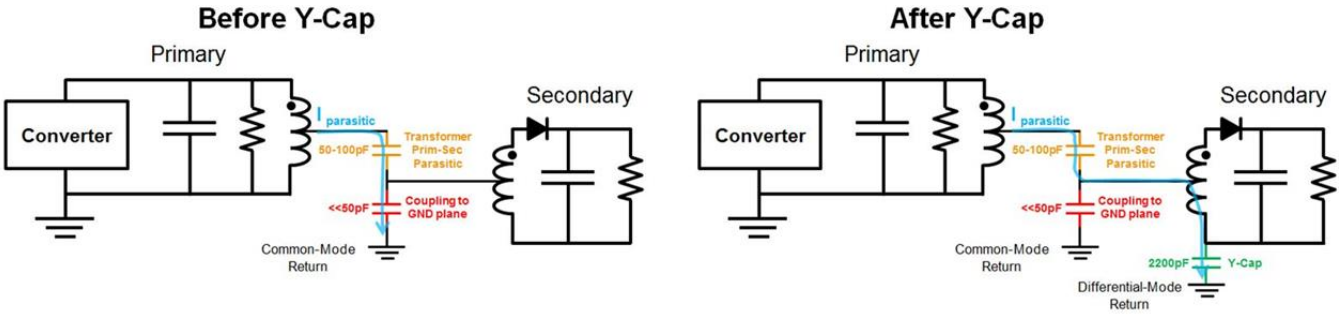

Figure 20. Y-Cap Effect on Circuit Performance Regarding Transformer Pri-Sec Capacitive Coupling With Rearranged Components

Before Y-Cap: Before placing the Y-Cap SW swings between 0 V and 48 V. This voltage is divided by the primary-secondary parasitic capacitor and the capacitance between the secondary and the GND plane (orange and red caps respectively). The prim-sec capacitor is much larger than the coupled cap to the GND plane so the 48-V swing is almost entirely seen on the secondary (due to the capacitor-divider principal). This large swing on the secondary, plus the large area of the secondary (components, traces) forces current through the coupled capacitor to GND. This current originally comes from the 48-V supply and returns through the GND plane/chassis of the 48-V supply. This is known as common-mode current and, if large enough, causes a failure in the EMI tests.

After Y-Cap: Now the circuit has added a “Y-Cap” from the secondary to the primary GND (see C11 on Figure 21). The Y-Cap is 20× to 40× larger than the primary-secondary capacitance. This means there will be a smaller voltage swing on the secondary (due to the capacitor-divider principal). This means less common-mode current and better EMI performance.

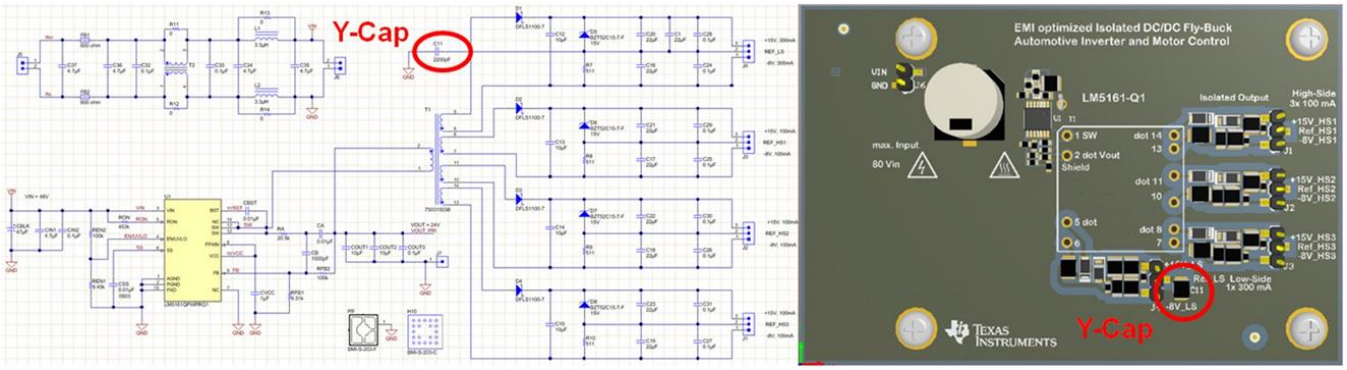

Figure 21. Y-Cap Placement on Schematic (left) and Layout (right)

A larger capacitor improves the EMI performance of this mitigation method, but there is an upper limit to the acceptable capacitance value. Isolation standards require no more than some tens of microamps to pass between primary and secondary. The exact value depends on the end-equipment and market. For this IGBT supply we’ve gone with a 2200-pF capacitor rated for 2 kV.

Unfortunately, the circuit can only add the Y-Cap to the secondary tied to the low-side gate drive. The low-side gate drive secondary GND is referenced to the emitter pin of the low-side IGBT which, in this case, is connected to high-power GND of the IGBT drive. The other three high-side gate drive secondaries are referenced to the emitters of the high-side IGBTs which are the switch nodes of the drive. Adding Y-caps to the other secondaries would create too much current in the capacitors and would not be acceptable for automotive standards.

4.8 Minimize Surface Area on Secondary

The secondary voltage capacitively couples to the chassis/GND plane and creates common-mode noise. This can be optimized through layout to minimize this effect.

First, the entire circuit is placed on the top-side of the board with a primary-GND plane on the bottom layer to absorb capacitive coupling straight through the board. There is also a primary-GND plane around the components with via stitching around the circuits. This picks up a bit more of the coupling.

Next the layout minimizes the surface area of the secondary side. The circuit selects small components and places them in order to reduce total trace length. It also reduces the trace width as much as possible without affecting proper regulation.

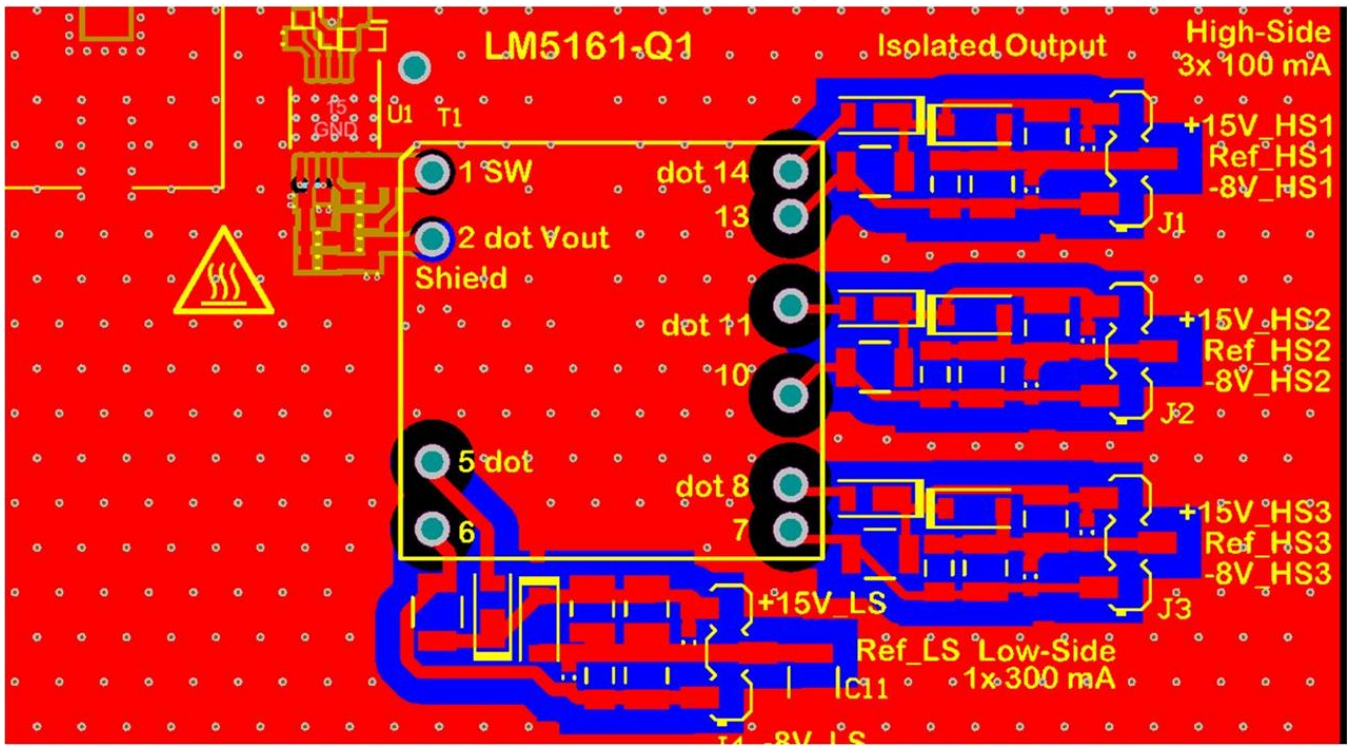

Figure 22. Layout of Secondary Circuitry With Minimized Trace Surface Area

4.9 Final Thoughts on EMI Optimization

The EMI tips and tricks mentioned in this section will help improve EMI performance of a Fly-Buck design, but these ideas can be extended to any circuit design. EMI typically takes thought, redesign, and optimization. Use these tips and tricks to help the design pass EMI.

5 Thermal Layout Optimization

Thermal design is another important consideration in board layout. A hotter IC is more susceptible to over-temperature shutdown and extended elevated temperature will negatively affect the lifetime of the IC. This converter is delivering up to around 600 mA at 24 V_{OUT}. This will generate heat which must be dissipated to the surrounding air. The layout can be optimized to increase the surface area of dissipation to spread the heat to reduce the temperature of the IC during operation.

The LM5160 and LM5161 each have a die attach pad (DAP), or thermal pad/exposed pad, on the bottom of the IC, which transfers the majority of the heat from the IC to the PCB (see Figure 23). Both designs have a copper GND pour over the board and under the IC which is soldered to the DAP. The heat flows from the DAP to the GND plane, but how does it spread from there?

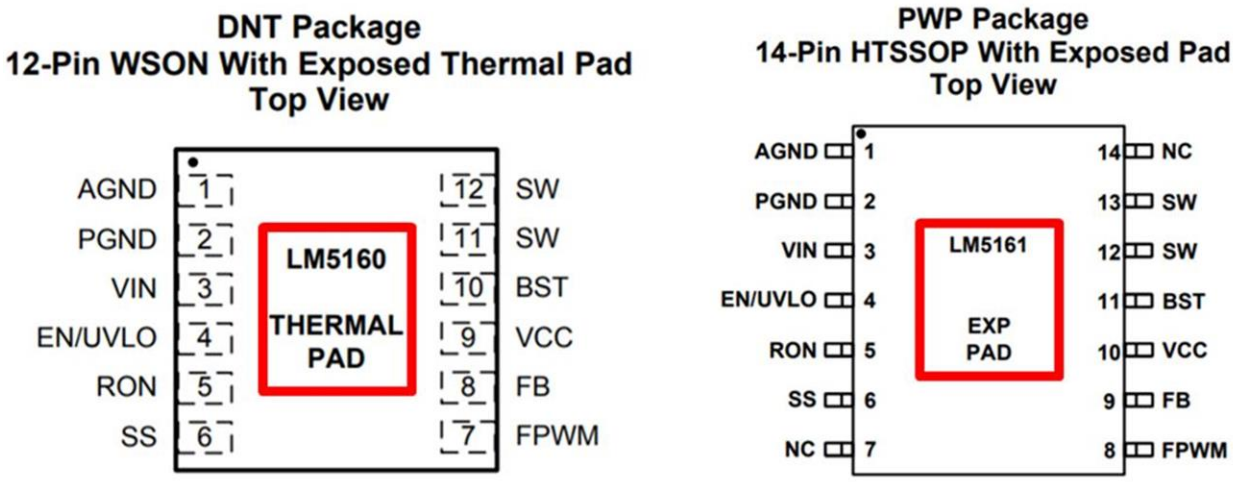

Figure 23. DAP/Thermal Pad: LM5160 (left) vs LM5161 (right)

See from TIDA-00199 on Figure 24 that the original board has a small GND plane around the circuitry on the primary. The majority of the heat is confined to this GND plane since FR4 (the green board material) has much poorer thermal conductivity than copper (GND plane). The reason for this small isolated plane on the original design is to ensure isolation between primary and secondaries. This design is not wrong, it is simply optimizing for overall performance. The new design, however, focuses on EMI and thermals. The new thermally optimized design, Figure 25, spreads this GND plane to the whole board with just enough clearance on the secondaries to ensure isolation.

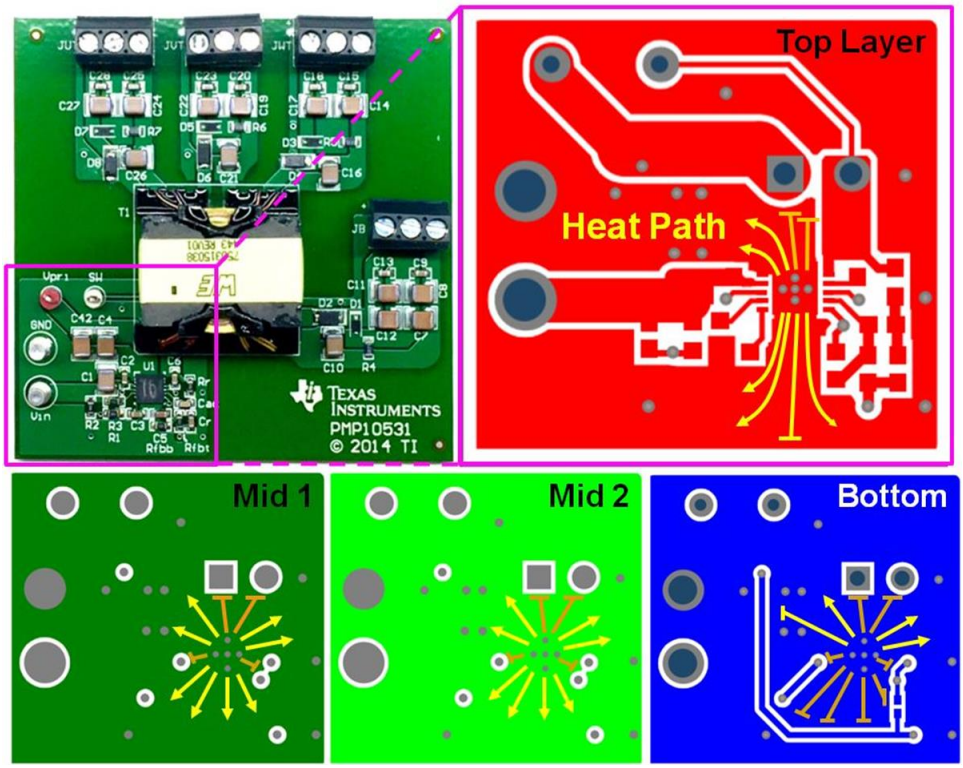

Figure 24. TIDA-00199 Layout Showing Heat Path

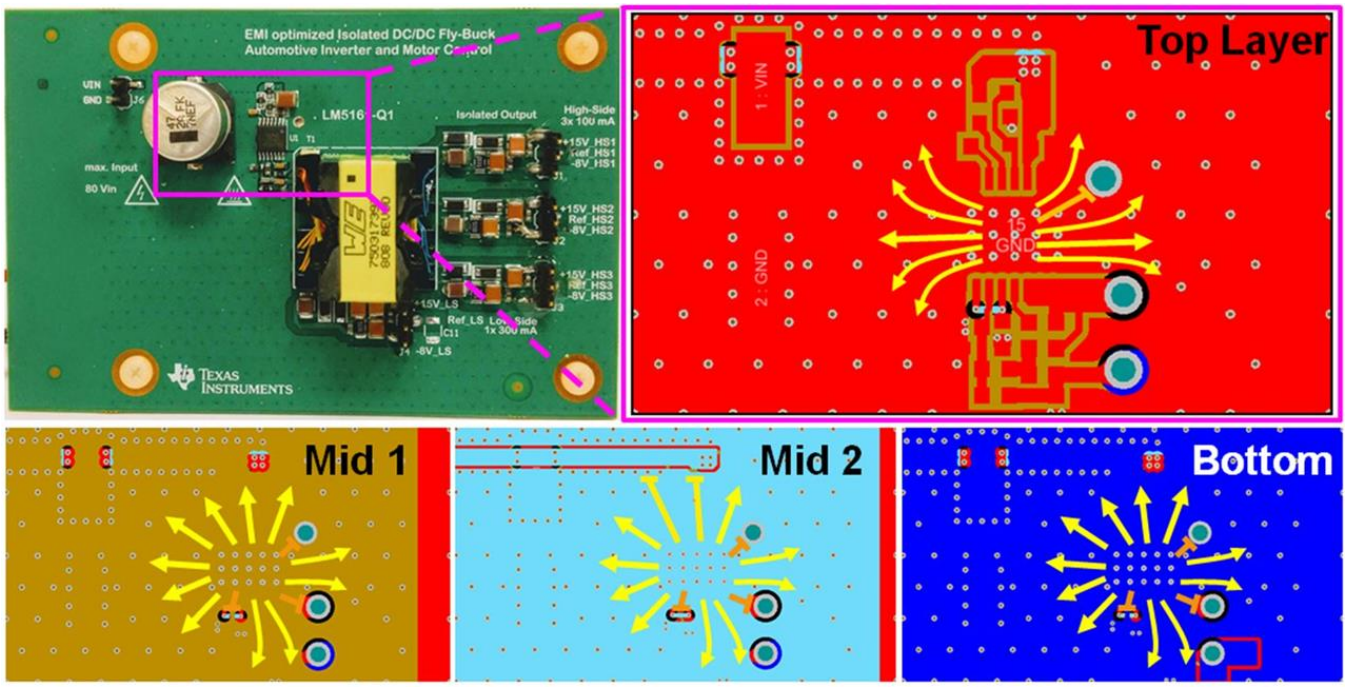

Figure 25. 48-V Optimized Board Layout Showing Heat Path

Next see that the heat path upward on Figure 24 is cut off by the V_{OUT} pin of the transformer (directly above the DAP of the LM5160). The new design switches these pins on the new transformer design to allow the IC and surrounding circuitry to move (to the left with respect to original layout, upward with respect to the optimized layout) so the transformer pin is not blocking any heat path.

The surrounding resistors and capacitor placement also has an effect on thermals. The original design places some components below and to the right/left of the IC, narrowing the path of the downward heat flow. The optimized design keeps these components beside the IC, not in the path of the heat. This allows maximal heat spread (to the left of the IC).

Thermal vias allow heat to move between layers more efficiently than through FR4 (the green board material). The new design has 15 vias under the thermal pad of the IC as well as via stitching across the entire board. These vias allow the heat to spread and utilize the other layers. In addition to this, midlayers 1 and 2 and the bottom layer all have clear unobstructed paths for the heat to flow away from the heat source.

The thermal tips and tricks mentioned above will help improve the thermal performance of the board. This reduces the likelihood of overtemperature reset, extending the useful lifetime of the IC.

6 Modification for SiC or GaN

Silicon Carbide (SiC) FETs are an alternative to IGBTs in the 48-V traction inverter space. IGBTs require +15 V/0 V/–8 V at around 100 mA per channel. SiC FETs require +20 V/0 V/-4 V at about 10 mA per channel. This design can be easily modified to drive SiC FETs.

First change the output voltage value. An IGBT supply has +15 V to –8 V which is a swing of 23 V. SiC supplies are +20 V to -4 V which is a swing of 24 V. Modify the lower feedback resistor RFB1 from 9.31 kΩ to 8.66 kΩ to increase the secondary output peak-to-peak value to 24 V.

Next change the secondary-side Zener regulator. Replace the 15-V Zener with a 20-V Zener to achieve +20 V and 0 V. Then adjust the bottom resistor from 511 Ω to 255 Ω to maintain the same current through the Zener as before.

Lastly pick a new transformer with the same specs but with a lower current rating. The transformer does not need to be designed for 100 mA per channel if it is only delivering 10 mA.

These changes modify the output from +15 V/0 V/–8 V to +20 V/0 V/–4 V. See Figure 26 for the new schematic with modified components boxed in red. See Table 1 for a list of modified components.

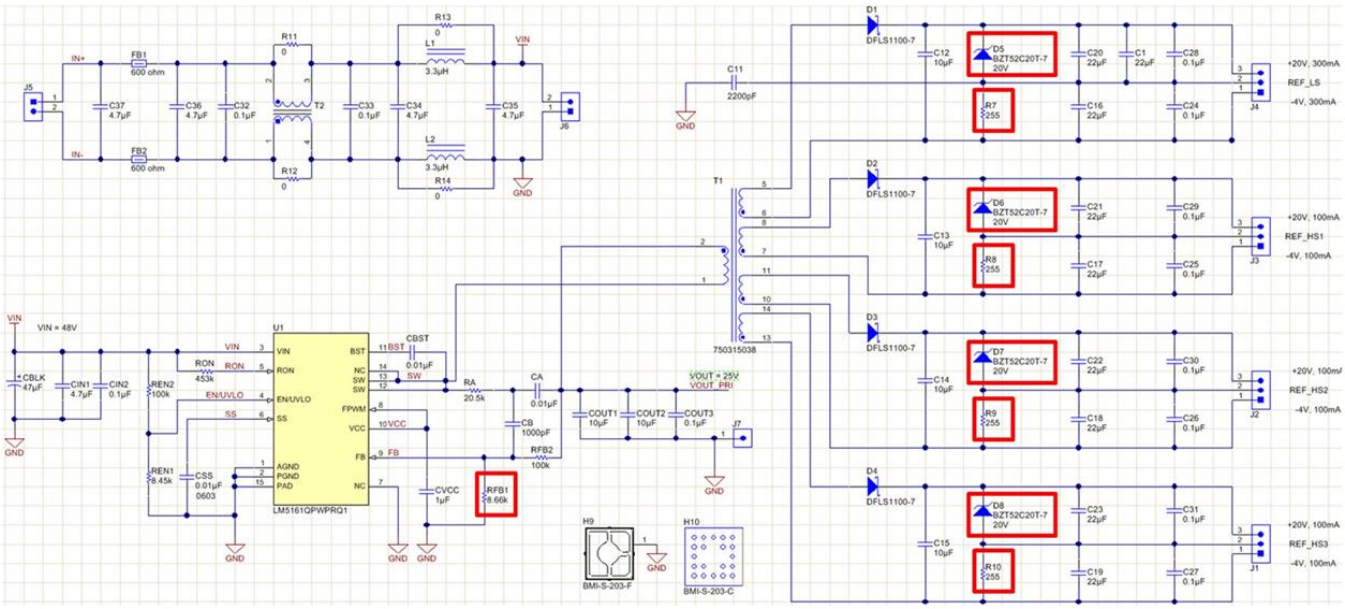

Figure 26. Updated Schematic for SiC Applications

Table 1. Components Changed When Converting IGBT Board for Use With SiC

COMPONENT	ORIGINAL IGBT VALUE	NEW SiC VALUE
RFB1	9.31 kΩ	8.66kΩ
D5, D6, D7, D8	15-V Zener	20-V Zener
R7, R8, R9, R10	511 Ω	255 Ω

This design can also be modified for GaN. GaN utilizes +6 V/0 V/–2 V. Follow the steps from Section 3 to modify the transformer turns ratio. Then follow the directions from this section to adjust the output voltage of the secondaries.

7 Test Results

The tests compare the new EMI/Thermally optimized layout against TIDA-00199 retrofitted for 48 V. This is to ensure a comparison between like-voltage and more closely related conditions. The retrofitted board replaces LM5160 with LM5161 like the new board but it maintains a nearly identical layout and component selection. This allows us to compare 48 V_{IN} with 48 V_{IN} between the two layouts.

7.1 Conducted EMI Results

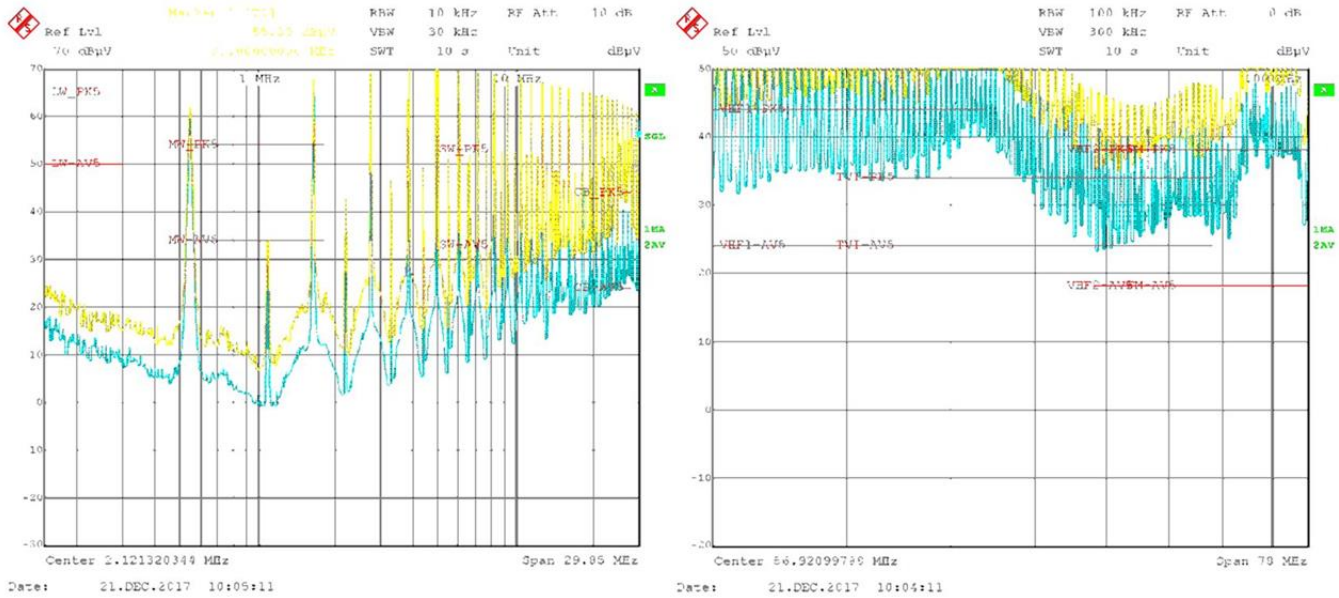

Figure 27. Conducted EMI Results for TIDA-00199 Modified for 48 VIN to CISPR 25 Class 5 – Low Frequency (left) and High Frequency (right)

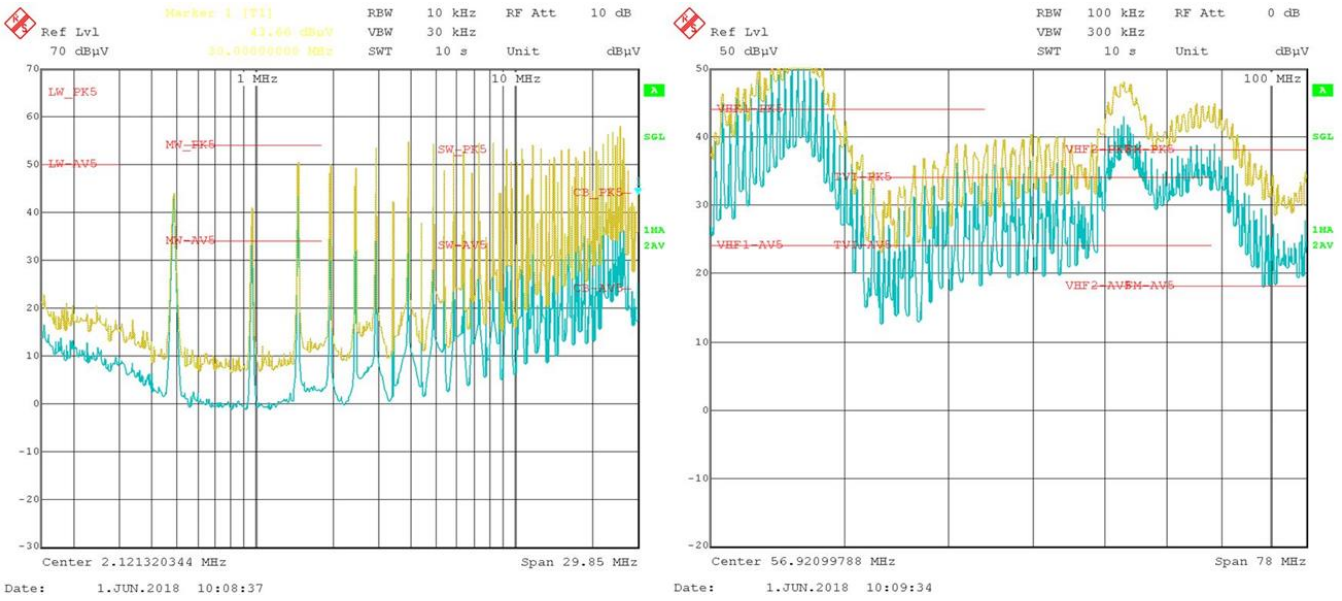

Figure 28. Conducted EMI Results for the Optimized Layout to CISPR 25 Class 5 – Low Frequency (left) and High Frequency (right)

The optimized layout is significantly better, around 20 dB for many regions of interest. Admittedly the optimized board is not passing either, but there are a few considerations to discuss before drawing conclusions.

1. This EMI test was taken from a board fresh from fabrication. This board has been optimized from the design but not from the applications-side lab-tested optimization. The design process takes a few passes and real-life optimization in the lab. This app note discusses the tips and tricks for EMI improvement and has demonstrated the kinds of improvement one can expect, even from a first pass design.
2. This design did not include an external shield for the transformer, SW-node via stitching, or most

importantly an internal shield between primary and secondary. The transformer spec shows a primary-secondary capacitance of 70 pF. If this transformer had a shield, this capacitance would drop drastically and the secondary sides would be much quieter resulting in less common-mode current and better EMI performance.

3. Figure 27 and Figure 28 show limit lines for CISPR 25 which is one of the toughest standards to pass. Other standards have more lenient tolerances so this board may pass for certain end equipments. These EMI suggestions lead to better EMI performance which can make the difference between passing and failing.

The tests show that EMI is markedly improved from the original board to the new EMI-optimized board.

As stated, this is a first pass test. Further debug will utilize some or all of the following optimization tests:

1. Place a flux band around the transformer and connect the band to Primary GND. Then try connecting it to VOUT. Compare with and without flux band, then compare connecting to GND vs V_{OUT}. Pick the one which yields the best results
2. Place a metal shield around the transformer. This can be copper tape (grounded around the transformer) or a custom shield. Compare results with and without shield.
3. Place a metal enclosure around the whole board. Connect the enclosure to primary GND on the board. This should block any capacitive or inductive coupling to the GND plane underneath the test setup which means the test results should only see differential-mode current. This means any bad EMI has to go through the EMI filter which means the EMI filter can be modified to see how much each component contributes to the overall EMI performance.
4. Place the Y-Cap and test, then remove the Y-Cap and test again. Try this with and without shielding.
5. Get the board up and running, then take a scope probe and remove the grabber to expose the tip. Without grounding the scope probe, hover the tip over different parts of the board. Zoom in to 10 mV/div at 1us/div (or another time scale to see a few switch cycles). This will allow the operator to see the areas with the largest dv/dt, and therefore the most likely to introduce capacitive coupling issues. One should see a square wave at the switch frequency when hovering over the switch node. If one see a similarly-sized square wave over the secondary sides, one may have significant capacitive coupling from primary to secondary and may consider internal shielding.

Use these tips and tricks to find the main EMI culprits from a power design.

7.2 Thermal Results

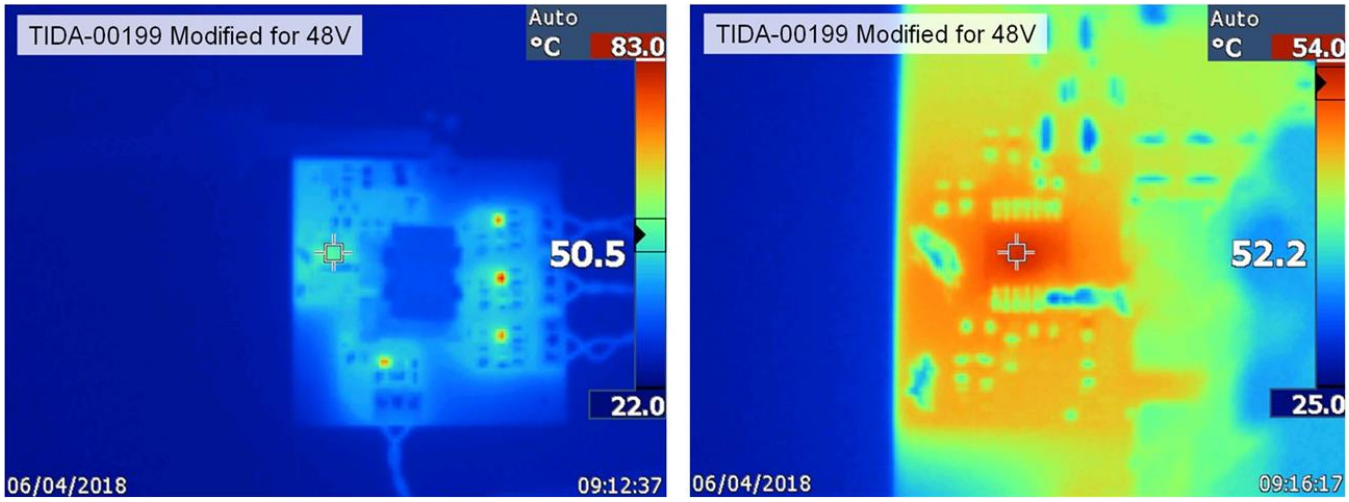

Figure 29. Thermal image for TIDA-00199, Modified for 48 VIN – Whole Board (left) and Close-up on IC (right)

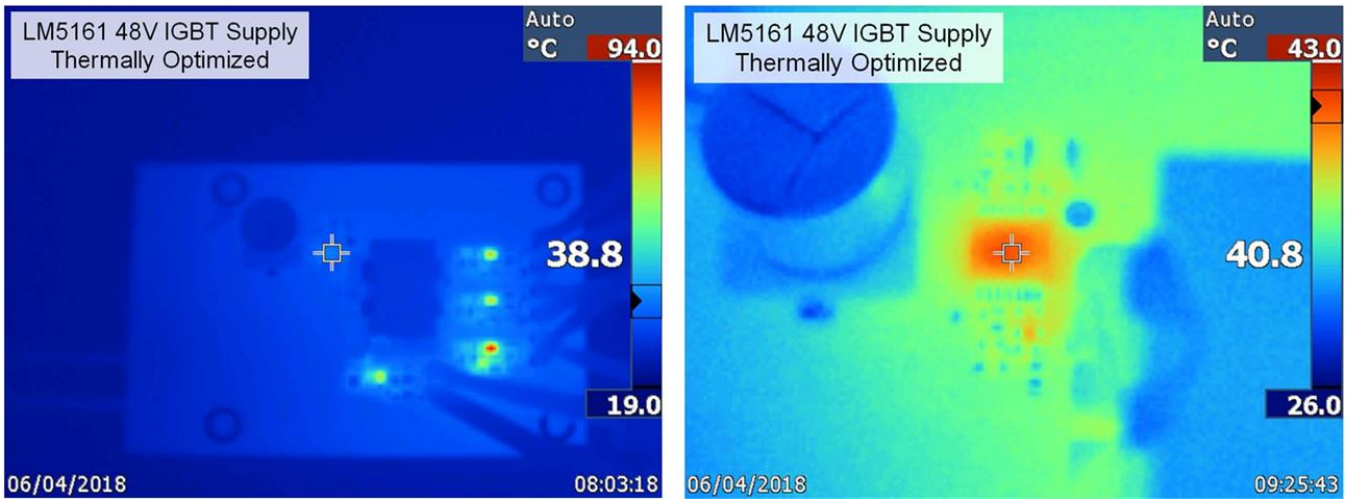

Figure 30. Thermal image for Optimized Layout – Whole Board (left) and Close-up on IC (right)

The IC temperature of the thermally optimized design is 12°C lower than the non-thermally optimized design. The larger, less obstructed copper GND pour layout allows the heat to spread with less thermal resistance. This reduces the temperature of the IC, thus reducing the chance of overtemperature reset as well as extending the lifetime of the IC.

You'll notice the bright red spots on the secondary. These are caused by the Zener regulator. The Zener regulator consists of a Zener diode and a resistor from +15 V to –8 V (creating 0 V at the midpoint). This constantly dissipates heat in order to properly regulate. Increasing the resistance reduces the power dissipated but it creates a less reliable regulator due to Zener tolerances and changing loads (current going into or out of the 0V node). Notice the color scale on the left-hand pictures. The Zeners on the thermally-optimized board are actually hotter. This is due to the reduced copper area from the EMI optimization. However, these temperatures are not dependent on intensity of load. Pulling 100 mA will yield the same Zener and resistor temperatures as no load. This is not ideal for light-load efficiency but this means that the Zener temp is already at worst-case and will not get hotter depending on load. This temperature can be reduced by utilizing more copper on the secondary (at the expense of EMI performance), using a physically larger package Zener and resistor to increase surface area to more easily dissipate heat (also at the expense of EMI), or increasing the resistance to a higher value (at the expense of regulation performance). The design can also use LDOs or other regulators as an alternative.

Note: The close-up thermal picture of the non-optimized board has strangely-shaped blue spots to the left of the IC and on the SW node. These are blobs of solder. These came about during the testing in attempts to further the EMI optimization of this board (which did not yield good enough results, hence the creation of this new board and app note). The solder (and other metals) has a very low emissivity that appears cold on the thermal images, but it is the same temperature as the surrounding board. One strategy being used by engineers is to spray the entire board with a matte black coating. This creates a uniform near-ideal emissivity which yields very accurate thermal images. Keep in mind, however, that further soldering/debugging/reworking of the board will be very difficult with the coating.

8 Summary

This application report explains the necessary steps to create an EMI and thermally optimized design for a 48-V IGBT supply for a traction inverter in HEV/EV automotive applications. The considerations conveyed in this report show significant improvement in EMI and thermal performance as compared to a board optimized for overall performance with no specific focus on EMI/Thermal performance. This design can be utilized as a reference for 48-V IGBT traction inverters in HEV/EV and mild-hybrid systems. These tips and tricks can be used to improve any EMI or thermal layout/design in Fly-Buck circuits but can be extended to nearly any power design. Utilize these tips and tricks to improve the EMI and thermal performance of your circuits.

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