

EMI Mitigation Techniques Using the LMZM23601

Jimmy Hua

ABSTRACT

Electromagnetic Interference (EMI) is an unwanted coupling of signals from one circuit or system to another. EMI is separated into two different categories: conducted and radiated. Conducted EMI is a form of conduction coupling caused by parasitic impedance, power and ground connections. Radiated EMI is the coupling of unwanted signals from radio transmission. This application note covers the EMI performance of several different techniques using both printed circuit board (PCB) layout changes and additional external circuitry using the LMZM23601 step-down power module. The PCB layouts in this experiment include the following: original LMZM23601 EVM, EVM with top layer shielding, perimeter fencing with vias, via stitching, and input/output via fencing. Two additional alternative techniques used to mitigate EMI noise are the high frequency(HF) bypass capacitor modification and an input filter design.

Contents

1	Introduction	2
2	EMI Mitigation Techniques	2
3	Conclusion	9
4	References	9

List of Figures

1	Board 1 PCB Layout	2
2	Default EVM vs. Default EVM With HF Bypass Capacitors	3
3	Board 2 PCB Layout	3
4	Default vs. Shielded	4
5	Board 3 PCB Layout	4
6	Shielded vs. Shielded + Via Stitching	5
7	Board 4 PCB Layout	5
8	Shielded vs. Shielded + I/O Fencing	6
9	Board 5 PCB Layout	6
10	Shielded vs. Shielded + Perimeter	7
11	Board 6 PCB Layout	7
12	Shielded vs. All Techniques	8
13	Input Filter Schematic Using the LMZM23601	8
14	Shielded vs. Default With Input Filter	9

List of Tables

1	PCB Layout Design Boards	2
---	--------------------------------	---

1 Introduction

Switch mode power supplies inherently generate noise emissions because of the high di/dt associated with their operation and parasitic inductance and capacitance in the circuit. EMI tests are often required at system level to ensure the complete system passes the relevant EMC standards. Some of the techniques available to help reduce EMI emissions in switch mode power supplies are input filtering, shielding, spread spectrum, and layout improvements.

This application note presents a study on the contribution of several different layout techniques to the overall radiated EMI performance of the LMZM23601 power module. The LMZM23601 is a 36-V, 1-A Step Down DC-DC integrated-inductor power module that has an output range of 2.5-V to 15-V. The tests in this report were done with 24-V input voltage 5-V output at 1-A load. Tests were performed on the default evaluation board, default evaluation board with an external input filter, default evaluation board with different high frequency(HF) bypass capacitors, and several other evaluation boards featuring different layer stack-up with ground shielding, perimeter via fencing, via stitching, and input/output via fencing. Below is a table for the different variations of EMI board techniques used for this experiment.

Table 1. PCB Layout Design Boards

Board Version	Shielding	Via Stitching (200mil)	Input/Output Fencing (50mil)	Perimeter Fencing (100mil)
1				
2	√			
3	√	√		
4	√		√	
5	√			√
6	√	√	√	√

NOTE: √ = layout technique implemented on the board

2 EMI Mitigation Techniques

The different EMI mitigation techniques explored in this experiment are: HF bypass capacitor modification, top layer ground shielding, via stitching, input/output fencing, perimeter fencing, all techniques, and input filter.

2.1 Default Layout With HF Bypass Capacitors Modification

This technique is a simple modification to the existing default LMZM23601 EVM and does not require any PCB layout stack-up change. By placing a low valued high frequency capacitor close to the input of the step-down converter, the EMI noise is significantly reduced at high frequency hence the HF bypass capacitor modification technique. With the simple addition of the HF bypass capacitors, the LMZM23601EVM was able to pass Class B limits.

Figure 1. Board 1 PCB Layout

LMZM23601 Original EVM PCB Layout

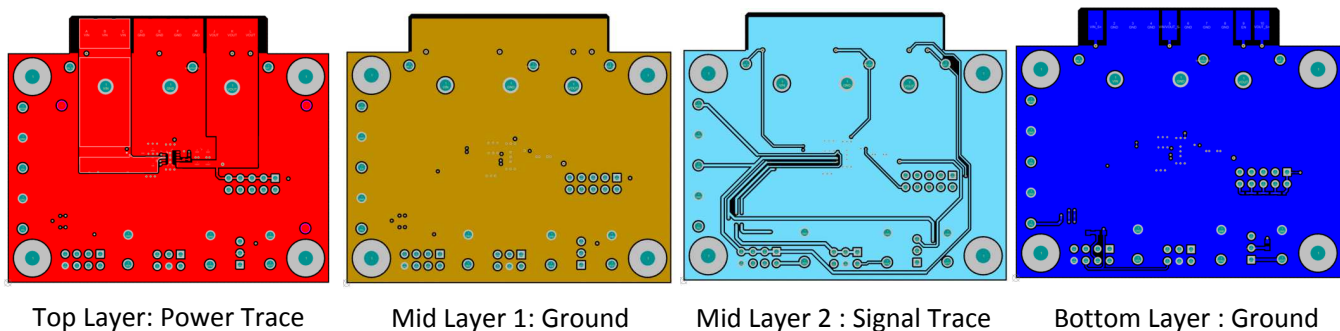
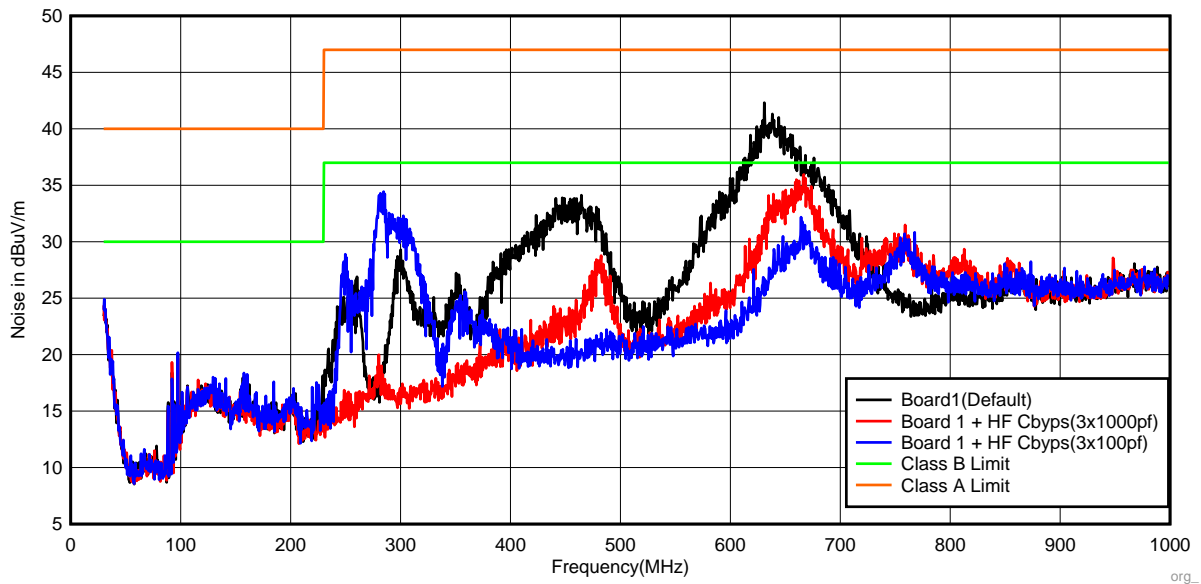


Figure 2. Default EVM vs. Default EVM With HF Bypass Capacitors



2.2 Shielding

The shielding technique implements dedicated ground planes above and below the signal traces to create a low impedance shield that protect against noise. This approach prevents unwanted interference from entering and exiting the sensitive areas of the circuit. Below is a comparison between a default EVM and an EVM with top layer ground plane shield.

Figure 3. Board 2 PCB Layout
LMZM23601EVM with Top Layer Shielding

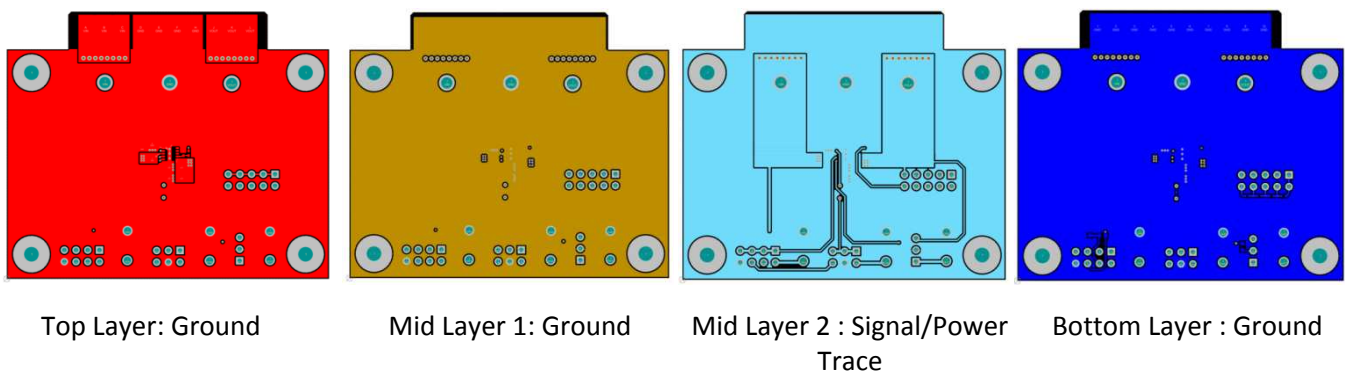
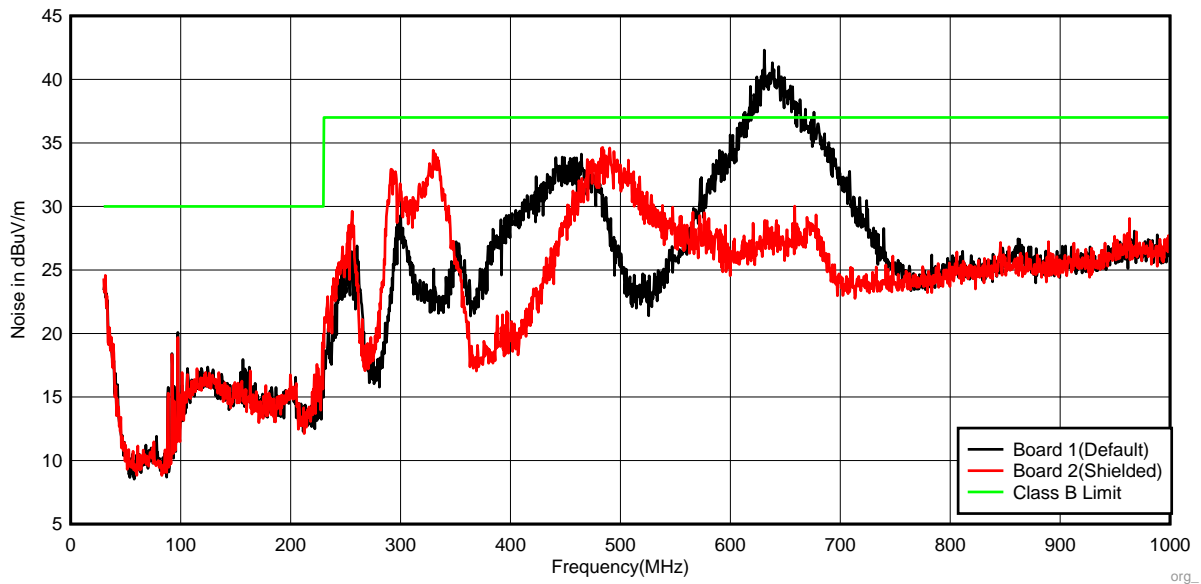


Figure 4. Default vs. Shielded



The radiated EMI test was performed in a 10-meter EMI chamber. The results show that the modified LMZM23601EVM with the top layer ground shielding complies with the CISPR22 Class B test while the original failed with the highest noise observed at around 650MHz. The remaining tests will use the shielded EVM as the controlled unit and Class B line as the limit for noise comparison.

2.2.1 Via Stitching

The stitching technique uses via connections between outer ground layers to mitigate EMI coupling. When using this technique, it is recommended to have the stitching vias evenly spaced around the entire PCB. The results below show that compared to the controlled unit, the addition of via stitching helped further reduce the high frequency noise.

Figure 5. Board 3 PCB Layout

LMZM23601EVM with Stitching

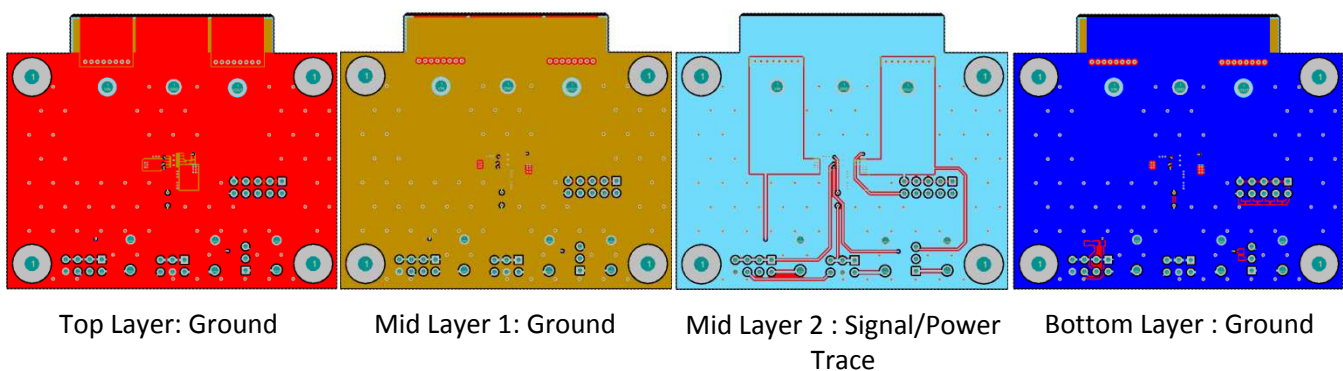
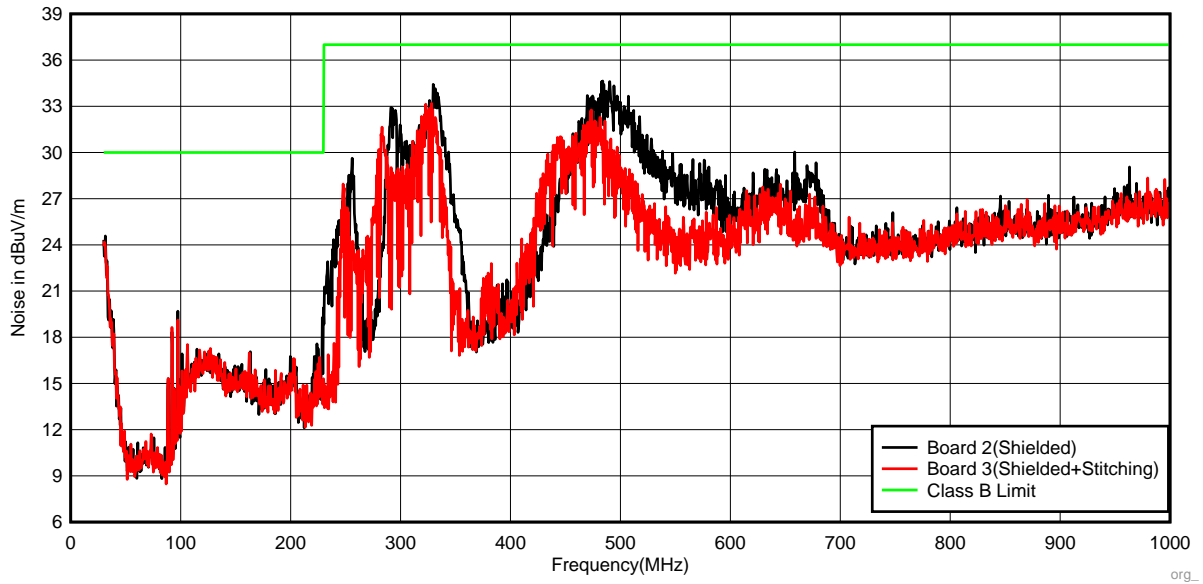


Figure 6. Shielded vs. Shielded + Via Stitching

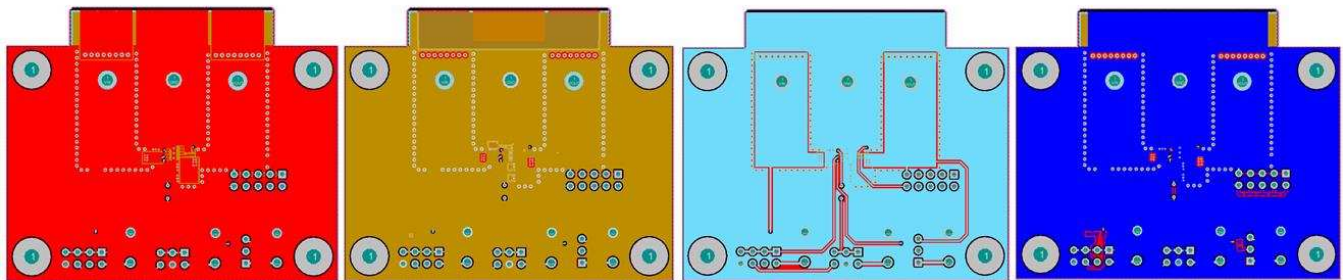


2.2.2 Input/Output Fencing

Input/Output fencing technique centralizes the stitching vias into a single array of vias around the input and output signal traces. Input/output fencing shows a slight reduction in noise around 200MHz to 350MHz.

Figure 7. Board 4 PCB Layout

LMZM23601EVM with Input/Output Fencing



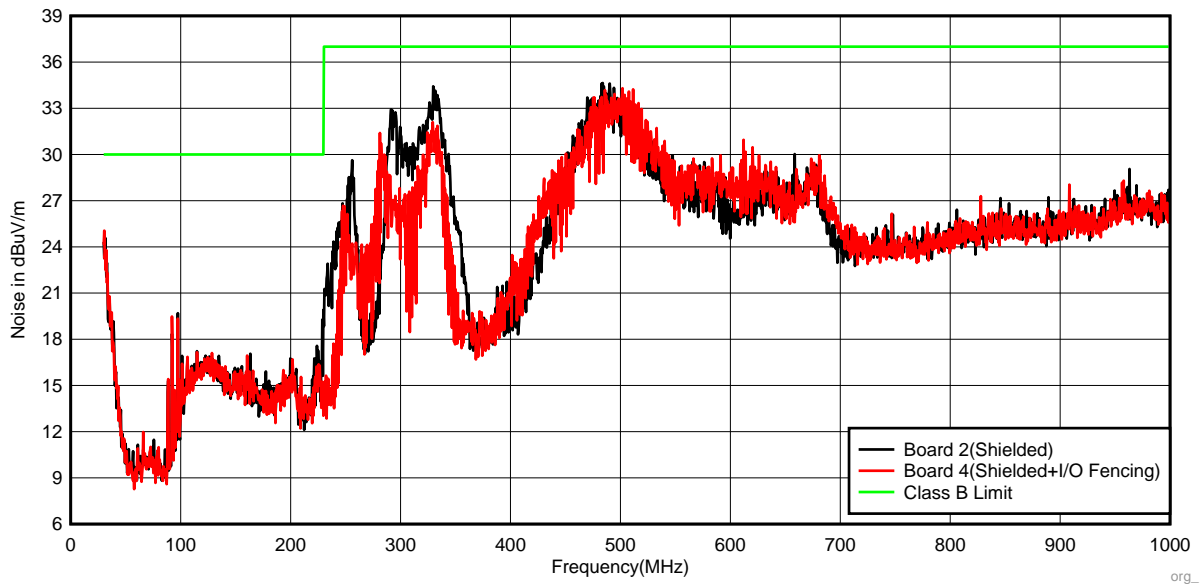
Top Layer: Ground

Mid Layer 1: Ground

Mid Layer 2 : Signal/Power Trace

Bottom Layer : Ground

Figure 8. Shielded vs. Shielded + I/O Fencing



2.2.3 Perimeter Fencing

Perimeter fencing uses the same idea as input/output fencing except placed around the perimeter of the PCB. Perimeter fencing result is similar to input/output fencing but has slightly better noise reduction at high frequency range of 600MHz to 750MHz.

Figure 9. Board 5 PCB Layout

LMZM23601EVM with Perimeter

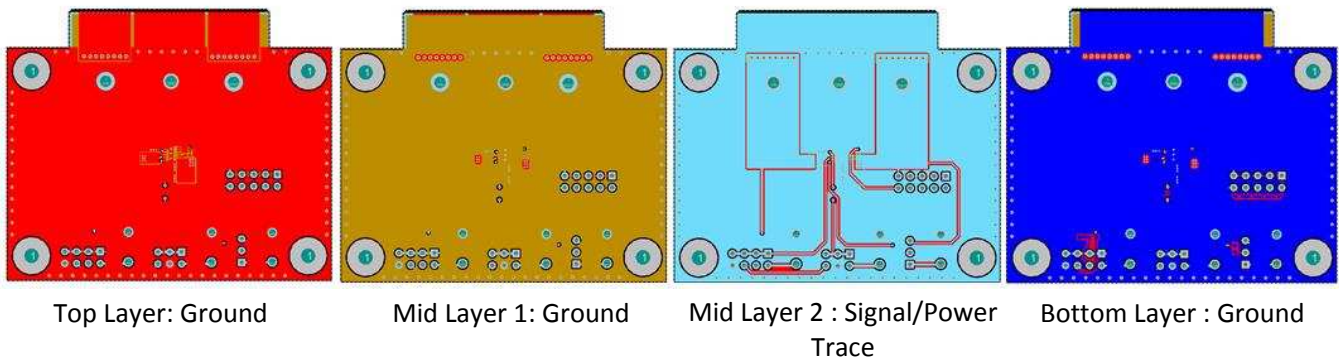
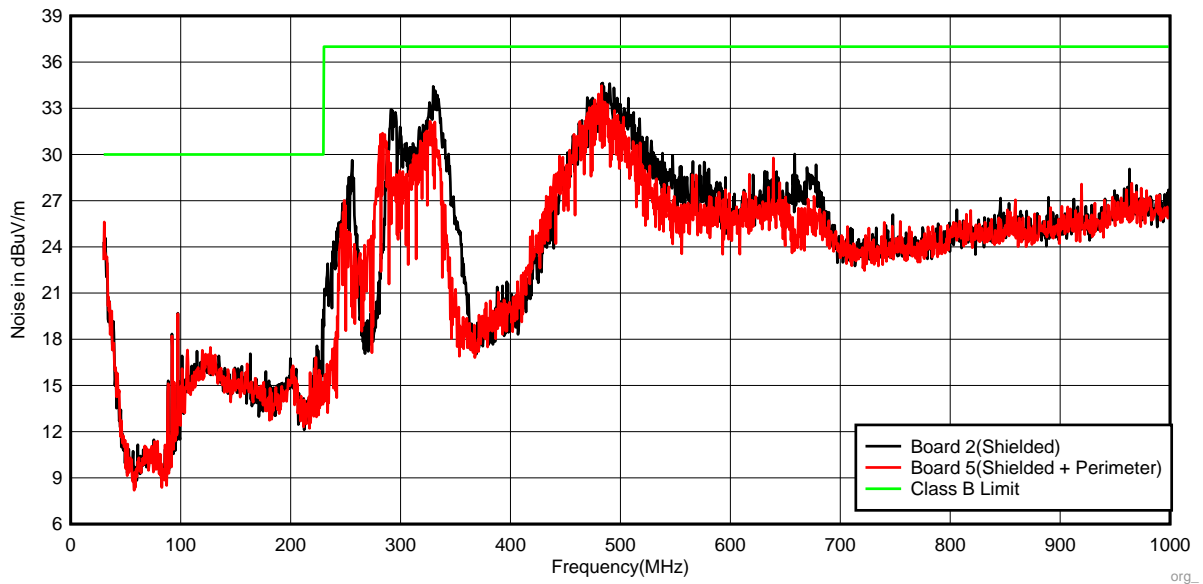


Figure 10. Shielded vs. Shielded + Perimeter



2.2.4 All PCB Layout Techniques

This PCB variation implements all of the PCB layout techniques previously discussed: perimeter, shielding, input/output fencing, and stitching. With the benefits at different frequency ranges using the "All Techniques" method, the result below agrees with the assumption that noise mitigation will improved compared to the controlled unit. Significant reduction in noise can be seen around the 270MHz to 320MHz range.

Figure 11. Board 6 PCB Layout
LMZM23601EVM with All Techniques

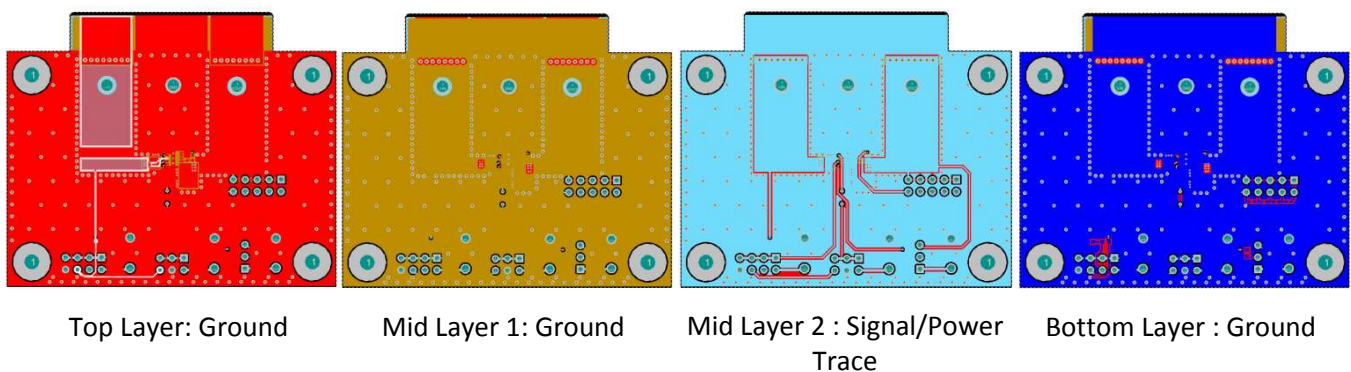
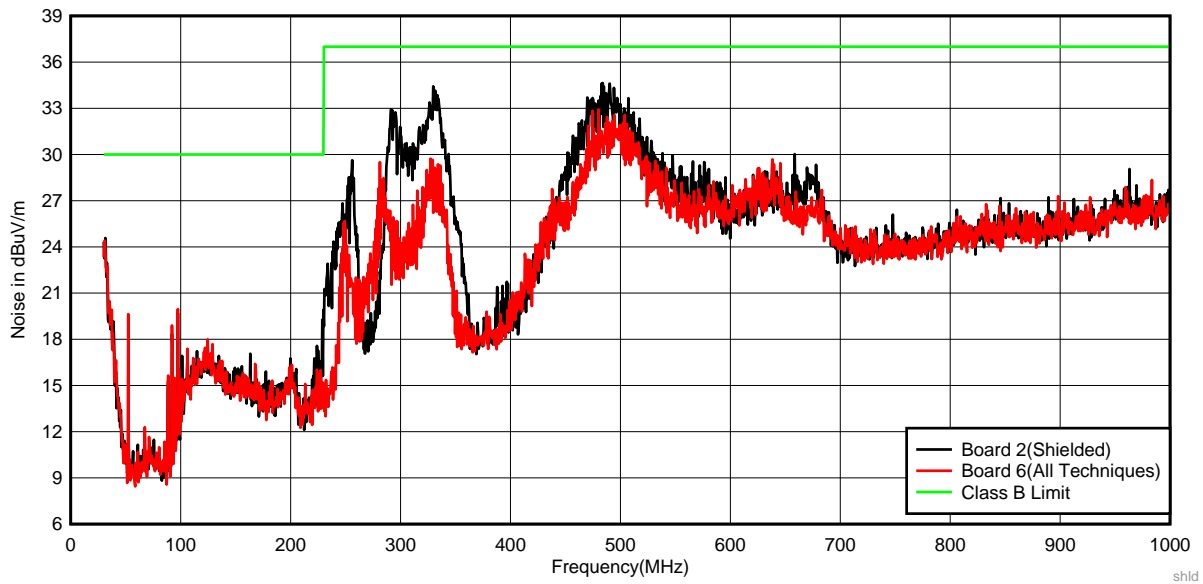


Figure 12. Shielded vs. All Techniques



2.2.5 Input Filter

The most effective way to reduce EMI noise for both conducted and radiated test is through an input filter. Refer to the [SNVA489C](#) application note for further information on designing an input filter.

Figure 13. Input Filter Schematic Using the LMZM23601

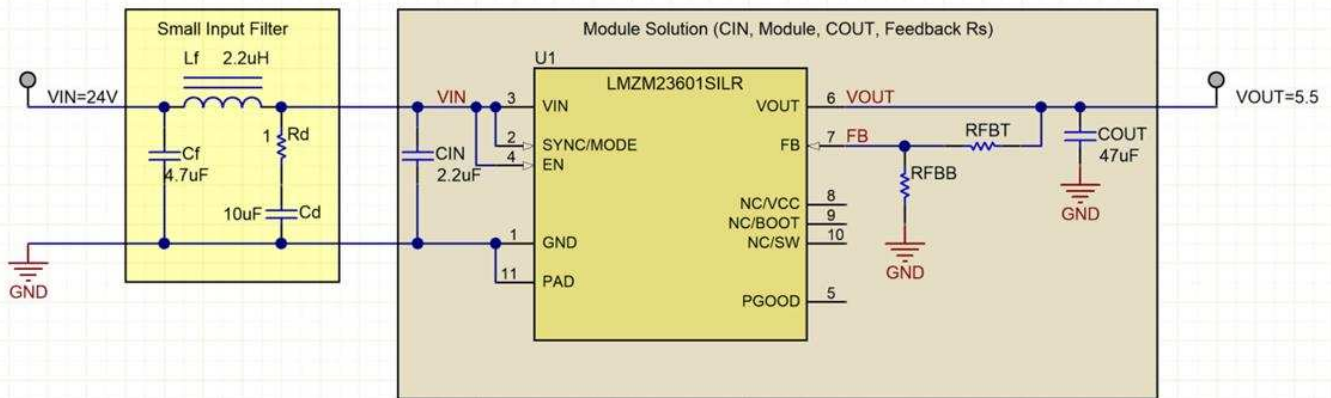
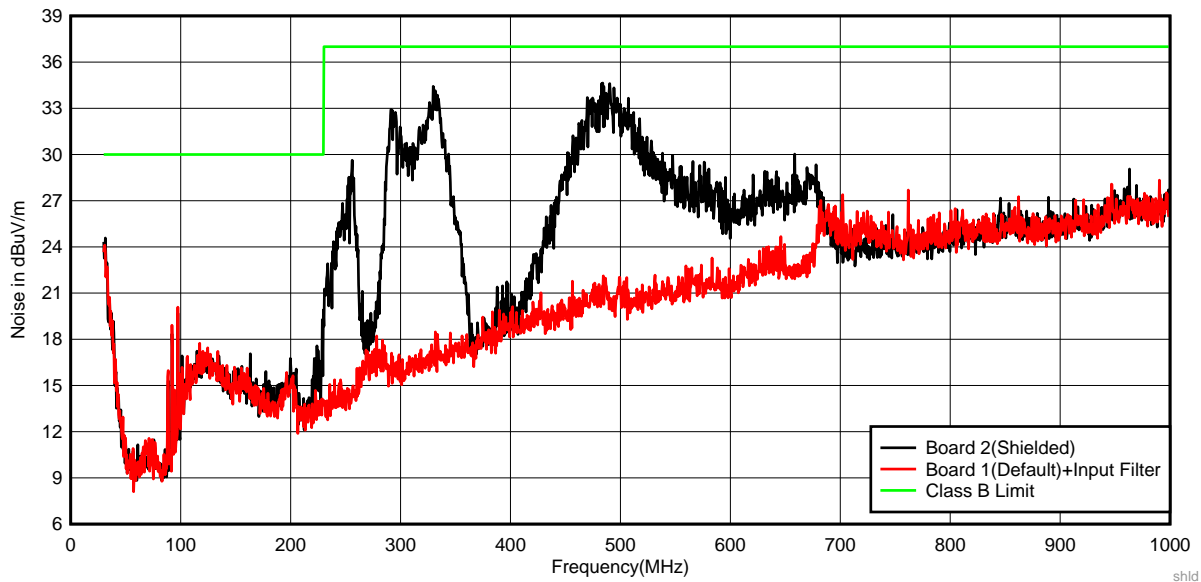


Figure 14. Shielded vs. Default With Input Filter


3 Conclusion

There are several EMI reduction techniques that can be implemented for DC-DC switching converters with each technique presenting different trade-offs. The experiments tested in this application show that adding a few high frequency bypass capacitors will allow the default LMZM23601EVM to pass Class B limits. The PCB layers can be utilized for effective shielding, via stitching, perimeter fencing and input/output fencing to further improve EMI performance of the system. Input EMI filter can be used to significantly improve radiated EMI for step-down converters at the cost of increased BOM.

4 References

1. A. Suntives, A. Khajooeizadeh, R. Abhari, "Using Via Fencing for Crosstalk Reduction in PCB Circuits"
2. Hartley, Richard, "Controlling Radiated EMI Through PCB Stack-Up"
3. X. Ye, D. M. Hockanson, M. Lin, W. Cui, S. Radu, J. L. Drewniak, T. P. VanDoren, T. H. Hubing, R. E. DuBroff, "The EMI benefits of ground plane stitching in multi-layer power bus stacks"
4. N. Moonen, F. Buesink, F. Leferink, "Optimizing Capacitor Placement in EMI-Filter using Back Annotation of 3D Field Coupling Parameters in Circuit Models"
5. F. Gisin, Z. P. Tanner, "Radiation From Printed Circuit Board Edge Structure"

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ("TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>), [evaluation modules](#), and [samples](http://www.ti.com/sc/docs/sampterm.htm) (<http://www.ti.com/sc/docs/sampterm.htm>).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2018, Texas Instruments Incorporated