Application Report
SNVA874–March 2019

Stability Analysis and Design of COT Type-3 Ripple Circuit

ABSTRACT

A constant on-time (COT) regulator offers an easy-to-use buck converter solution without the need for external compensation. However, maintaining stability with minimal output ripple voltage can be a challenge, especially in wide-V_{IN} applications like battery packs used in E-bikes and drones, as well as NOx sensor applications. Type-3 ripple injection is often employed when low output ripple voltage is required. An often overlooked subject is how type-3 ripple injection component selection is related to the frequency response of the control loop. This application report reviews type-3 ripple injection design and how the component selection relates to stability in the time and frequency domains.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Type-3 networks generate a ripple voltage that is in phase with and proportional to inductor ripple current. The ripple voltage is related to inductor current and is injected into the feedback loop. Type-3 ripple injection is often employed when using ceramic output capacitors with very low ESR, and in turn, provide very low output ripple voltage solutions. The output ripple voltage of low-ESR output capacitors is 90° out-of-phase with inductor current. Without type-3 ripple injection, the out-of-phase ripple voltage generated by low-ESR output capacitors causes instability.

Figure 1 shows a LM5164-Q1 converter with type-3 ripple injection. The type-3 ripple network uses R_A and C_A placed in parallel to the inductor and generates a triangular ripple voltage in phase with the inductor ripple current. The inductor ripple current amplitude and the chosen R_A and C_A determine the amplitude of generated ripple voltage. A second capacitor, designated C_B, AC couples the voltage generated across C_A into the feedback node.

Figure 1 also shows how type-3 networks introduce a capacitive path from V_{OUT} to FB, through a series configuration of C_A and C_B, which is in parallel to R_{FB1}. This path causes out-of-phase output ripple voltage to also AC couple into the feedback node. Previous literature recommends an amplitude of 25 mV in-phase ripple voltage to ensure stability [2]. However in some designs, the out-of-phase ripple voltage can corrupt the 25 mV of injected in-phase ripple, causing instability. Wide-V_{IN} applications, especially designs with lower input voltages, are susceptible to such instability.

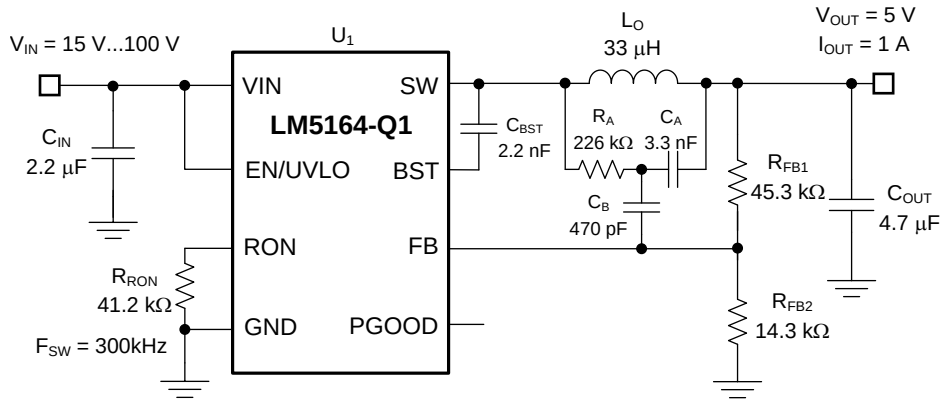


Figure 1. LM5164-Q1 Using Type-3 Ripple Injection

Figure 2 illustrates a timing diagram of in-phase and out-of-phase ripple voltages. If the out-of-phase ripple voltage is dominant, V_{FB} would be 90° out-of-phase with inductor current and after one on-time pulse, V_{FB} would not rise above the V_{REF}. For stable operation, there must be enough in-phase ripple voltage to increase the feedback node voltage above the reference during the on-time.

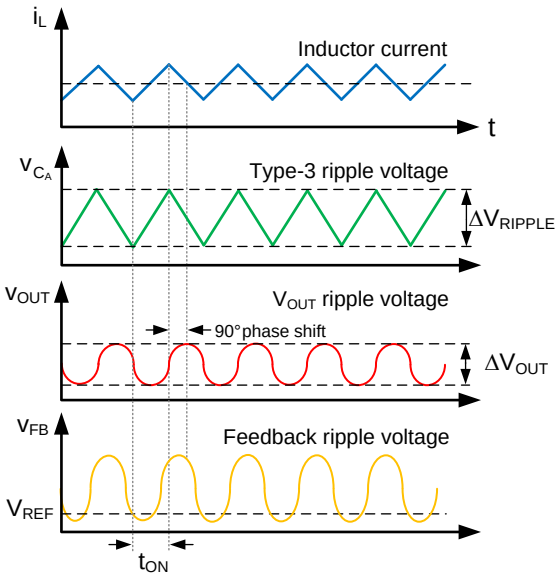


Figure 2. Timing Diagram of Type-3 Ripple Injection

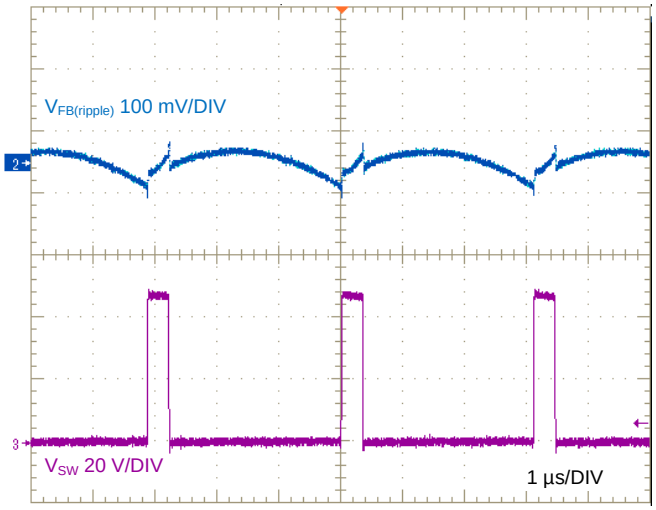


Figure 3. Stable Switching at V_{IN} = 48 V

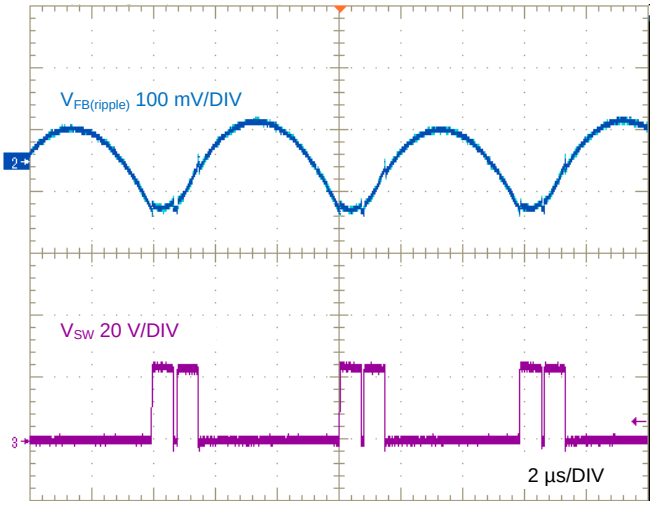
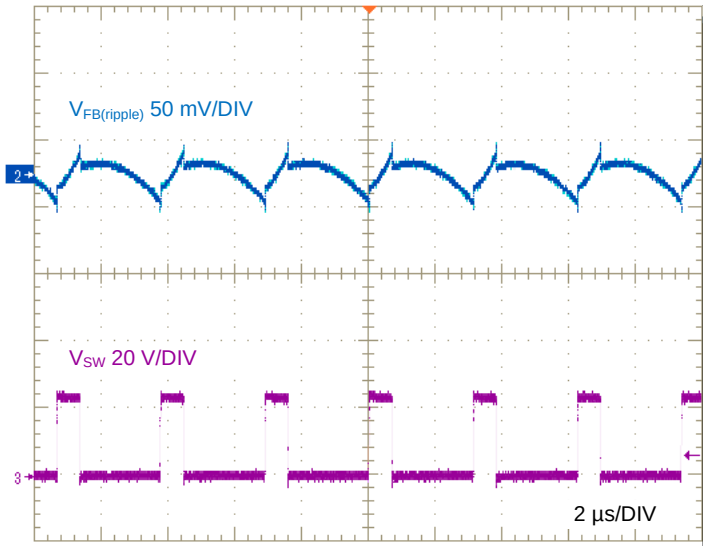


Figure 4. Unstable Switching at V_{IN} = 24 V

The circuit in Figure 1 generates 20 mV of in-phase ripple at V_{IN} = 48 V using the LM51640Q1 100-V, 1-A buck converter . [4] shows stable switching. The injected ripple voltage is greater than the out-of-phase ripple voltage at 48 V_{IN}, therefore the converter remains stable. However as V_{IN} decreases, the in-phase injected ripple voltage becomes smaller than the out-of-phase ripple voltage and leads to instability, as shown in Figure 4.

Large out-of-phase ripple voltage causes a voltage lag at the feedback node and a double pulse occurs as seen in Figure 4. As a result, the second on-time pulse overcharges output capacitor, which in turn causes an extended off-time. This cycle repeats, causing erratic switching and very large output ripple voltage. Instability can be fixed by either decreasing the out-of-phase ripple voltage or increasing the in-phase ripple voltage.



(1) Using the same design except C_{OUT} = 10 µF

Figure 5. Stable switching at V_{IN} = 24 V, C_{OUT} = 10 µF

Figure 5 shows stable switching. This is achieved by increasing the output capacitance, thereby reducing the out-of-phase ripple voltage at the feedback node. It is interesting to note that just by reducing the out-of-phase ripple voltage, stability can be achieved with much lower levels of injected in-phase ripple voltage. In designs with very low output ripple voltage of 1 mV or 2 mV, stability can be achieved with 7 mV of in-phase ripple voltage injected onto the feedback node.

2 Frequency Domain Analysis

The previous section showed power stage component selection and the type-3 ripple injection network affect stability. Bode plots and frequency analysis of a COT converter with various types of ripple injection schemes provide a useful perspective on how ripple network design affects stability. Constant on-time control is quasi-hysteretic using a feedback comparator; this control scheme is non-linear. Lin *et al* have derived a transfer function for this control model, which is used to analyze loop stability[1].

$$G(s) = \frac{V_{IN} \cdot \left(1 + \frac{s}{\omega_{ESR}}\right)}{1 + 2\delta\frac{s}{\omega_0} + \left(\frac{s}{\omega_0}\right)^2} \tag{1}$$

$$\omega_{ESR} = \frac{1}{C_O \cdot R_{ESR}}$$

$$\omega_o = \sqrt{\frac{1 + R_{DCR}/R_O}{L_O \cdot C_O}}$$

$$\delta = \frac{\sqrt{L/C_O} + R_O \cdot (R_{DCR} + R_{ESR}) \cdot \sqrt{C_O/L_O}}{2 \cdot R_O \cdot \sqrt{1 + R_{DCR}/R_O}}$$

Equation 1 describes the transfer function of the power stage. As in voltage-mode control schemes, there is a double-pole ω_0 determined by the output capacitance and inductor. As previously mentioned, type-3 ripple injection with ceramic output capacitors have low ESR, and the ESR zero ω_{ESR} is pushed out to a high frequency, higher than the bandwidth of the control loop. Having a second order system without compensation renders the loop unstable. Note how a large ESR of the output capacitor causes ω_{ESR} to move to a lower frequency. By increasing the ESR, ω_{ESR} decreases and eventually moves to a frequency below the crossover frequency, and provides phase boost to obtain adequate phase margin at the crossover frequency. COT type-1 and type-2 ripple voltage configurations achieve stability this way [2][3].

Equation 2 shows the transfer function of the controller with type-3 ripple injection.

$$\frac{\Delta D}{\Delta V_{OUT}} = -\frac{(R_A \cdot R_{FB1} \cdot C_A \cdot C_B) \cdot s^2 + R_A \cdot (C_A + C_B) \cdot s + 1}{(V_{IN} \cdot R_{FB1} \cdot C_B) \cdot s} \tag{2}$$

The zero locations of Equation 2 are approximately:

$$z_{type\text{-}3} \approx \frac{\omega_{coupling}\left(-1 \pm \sqrt{1 - 4\frac{\omega_{ripple}}{\omega_{coupling}}}\right)}{2} \tag{3}$$

$$\omega_{coupling} = \frac{1}{R_{FB1} \cdot C_B},\ \omega_{ripple} = \frac{1}{R_A \cdot C_A}$$

In the time domain, stability is achieved by increasing the in-phase ripple voltage at the feedback node, by either decreasing R_A or C_A. By observation of Equation 3, in the frequency domain this is equivalent to increasing the frequency of ω_{ripple}, increasing the frequency of where the type-3 zeros are located. Ideally, these zeros must be placed close to the power stage double pole to provide pole cancellation and phase boost at cross over frequency.

Due to the fixed on-time, the converter cannot respond to changes immediately. This delay is introduced to the transfer function and is modeled as Equation 4.

$$H_{delay}(s) = e^{-s \cdot D \cdot t_{ON}} \tag{4}$$

As shown in Equation 4, stability also depends on duty cycle (D). As input voltage is reduced, duty cycle increases, which can cause instability in certain conditions. Figure 6 uses SIMPLIS AC analysis of the circuit in Figure 1 to plot ripple ratio versus phase margin for different input voltages. A higher ripple ratio, or ratio of ΔV_{RIPPLE} to ΔV_{OUT}, is needed to achieve the same phase margin for lower input voltages.

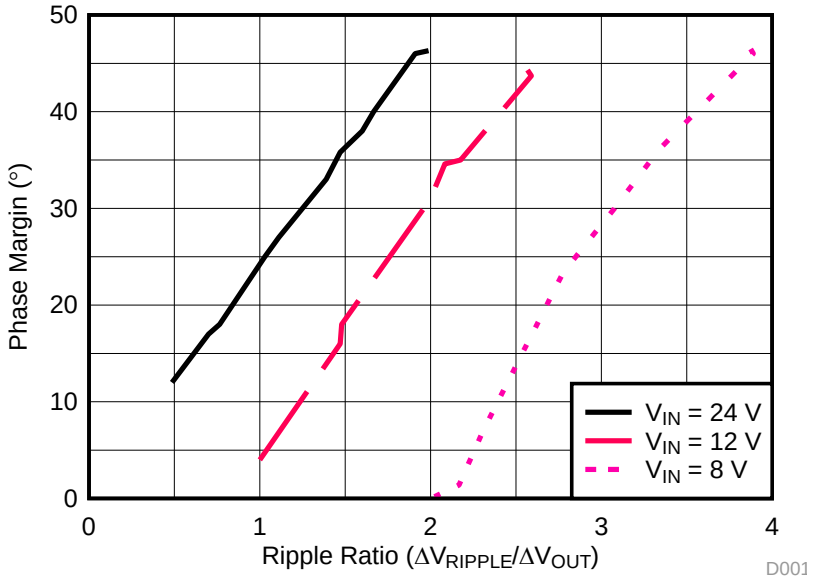
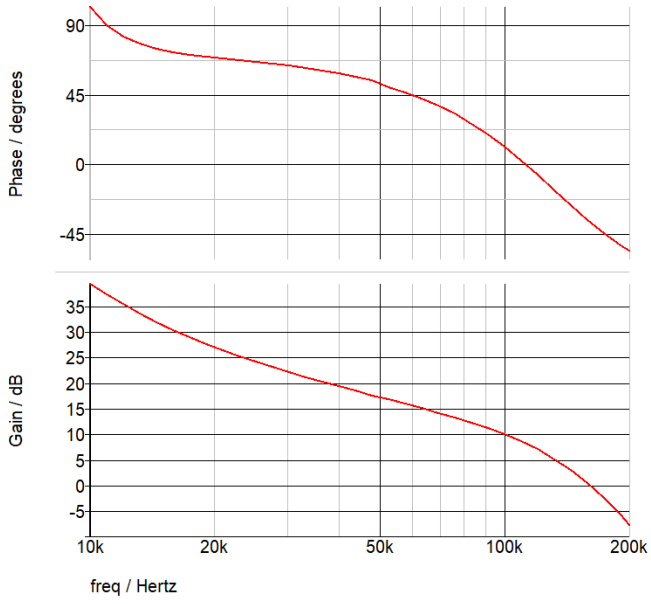


Figure 6. Ripple Ratio Versus Phase Margin at Various Input Voltages

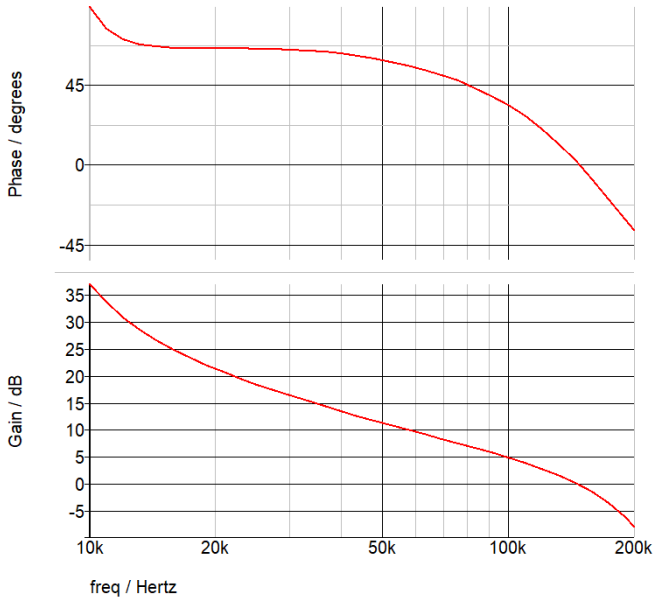
As shown in Figure 6, as the input voltage is reduced, the duty cycle increases, and a larger ripple ratio between ΔV_{RIPPLE} and ΔV_{OUT} is required to maintain stability. For example, at V_{IN} = 24 V, a ripple ratio of 2 is required to attain a phase margin of 45°, but with V_{IN} = 8 V, a ripple ratio of 4 is required to attain the same phase margin.

Figure 7 through Figure 10 show bode plots of different ripple ratios using the Figure 1 circuit at V_{IN} = 8 V. As shown in Figure 10, a phase margin of 47° is achieved when a ripple ratio of 4 is applied. As the ripple ratio is reduced, lower phase margin is achieved, as shown in Figure 7, Figure 8, and Figure 9.



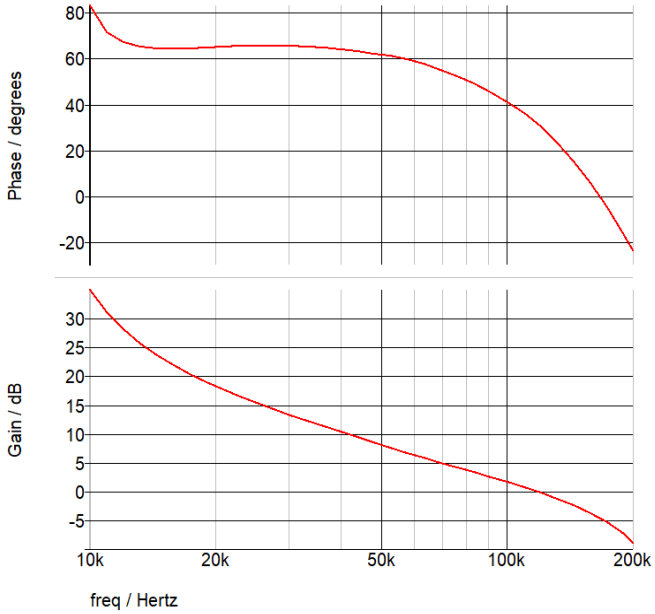
Unstable

Figure 7. Bode Plot V_{IN} = 8 V, Ripple Ratio = 1



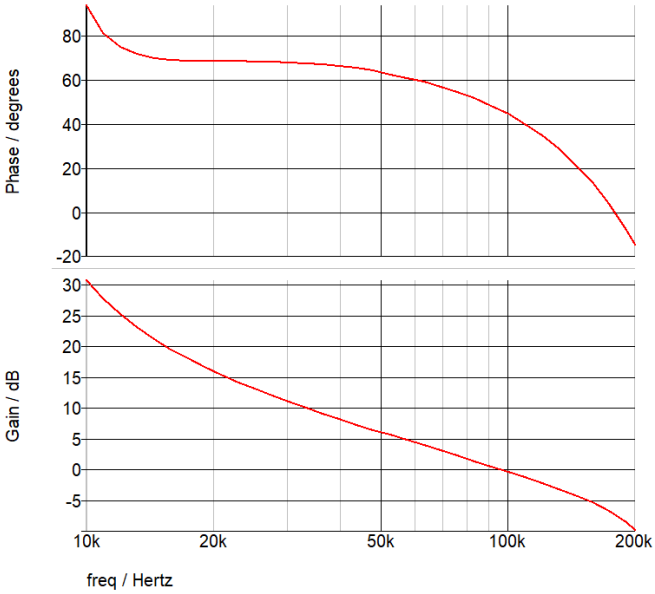
Phase margin of 1°, fc = 153 kHz

Figure 8. Bode Plot V_{IN} = 8 V, Ripple Ratio = 2



Phase margin of 31°, fc = 123 kHz

Figure 9. Bode Plot V_{IN} = 8 V, Ripple Ratio = 3



Phase margin of 47°, fc = 96 kHz

Figure 10. Bode Plot V_{IN} = 8 V, Ripple Ratio = 4

3 Understanding a Type-3 Ripple Network

Understanding what causes instability makes designing a type-3 ripple network straightforward. First, reduce the output ripple voltage, which is done by increasing the output capacitance. Calculate the output ripple voltage at $V_{IN(min)}$ using Equation 5. Limit the output ripple voltage to 0.1%–0.5% of V_{OUT}.

$$\Delta V_{OUT(min)} = \frac{\Delta I_{L(min)}}{8 \cdot F_{SW} \cdot C_{OUT}} \tag{5}$$

Choose C_A based on Equation 6.

$$C_A \geq \frac{10}{F_{SW} \cdot \left(R_{FB1} \| R_{FB2}\right)} \tag{6}$$

This ensures the time constant of C_A and the feedback network is 10x larger than the switching period. Choose R_A using Equation 7 to ensure that adequate in-phase ripple voltage is generated with respect to the output ripple voltage at the minimum input voltage.

$$R_A C_A \leq \frac{\left(V_{IN(min)} - V_{OUT}\right) \cdot t_{ON(min)}}{\left(4 \cdot \frac{V_{OUT}}{V_{IN(min)}} + 1\right) \cdot \Delta V_{OUT(min)}} \tag{7}$$

Choose a coupling capacitor C_B based on desired transient response settling time using Equation 8. A 75-µs settling time is recommended.

$$C_B \geq \frac{t_{TR\text{-}settling}}{3 \cdot R_{FB1}} \tag{8}$$

It is recommended to choose values for C_A and C_B close to the calculated results. Avoid choosing a large coupling capacitor C_B. A large capacitor on the feedback node slows down response time and overall converter loop response. Also avoid using a large ripple generation capacitance C_A. During startup and short circuit recovery the output voltage transient can AC-couple to the feedback node, which can cause poor performance during startup and short circuit recovery.

4 Conclusion

Constant on-time converters are considered for their simplicity, low cost, and fast transient response. Type-1 and type-2 ripple generation networks use a relatively high value ESR output capacitor to generate a feedback ripple voltage that is in-phase with the inductor current to achieve stability, type-3 ripple injection networks have no minimum output capacitor ESR requirement [2]. A designer is able to implement a low ripple voltage at the output by using ceramic capacitors and achieve stability by implementing type-3 ripple injection. Using type-3 ripple injection saves space and cost, and is more reliable than using electrolytic output capacitors. In order to attain stability over a wide input voltage range, a type-3 ripple injection network must be designed such that in-phase ripple voltage is at least 7 mV and greater than the out-of-phase ripple voltage.

5 References

1. M. Lin, T. Zaitsu, T. Sato, and T. Nabeshima, "Frequency Domain Analysis of Fixed On-Time With Bottom Detection Control for Buck Converter," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, pp. 481-485.
2. Texas Instruments,*Selecting an Ideal Ripple Generation Network for Your COT Buck Converter Application Report* (SNVA766)
3. Texas Instruments, *AN-1481: Controlling Output Ripple and Achieving ESR Independence in Constant On-Time (COT) Regulator Designs Application Note* (SNVA166)
4. Texas Instruments, *LM5164 6-V to 100-V input, 1-A synchronous DC-DC Buck Converter with Ultra-low I_Q Data Sheet* (SNVSB51)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265