Application Note

Design Consideration on Boot Resistor in Buck Converter

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ABSTRACT

As power supply efficiency becomes more important, faster switching speeds are necessary to reduce efficiency losses. However, as switching speeds are increased, there are trade-offs that must be considered, such as significant overshoot, ringing voltage on the switch node, and electromagnetic interference (EMI). The magnitude of the ringing is a function of the switching speed of the high-side NFET and the parasitic inductance in the layout and device package. There are several methods to reduce the ringing to keep the MOSFET switches within the safe operating region and the EMI noise so caused, such as a boot resistor, a high-side gate resistor, or an RC snubber.

This application note highlights design consideration when using a boot resistor to control switch-node ringing and optimize EMI.

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Trademarks

1 Introduction

The circuit in Figure 1-1 shows the power-stage components for a synchronous buck converter. The parasitic inductance and capacitance responsible for switch-node ringing is included in this model.

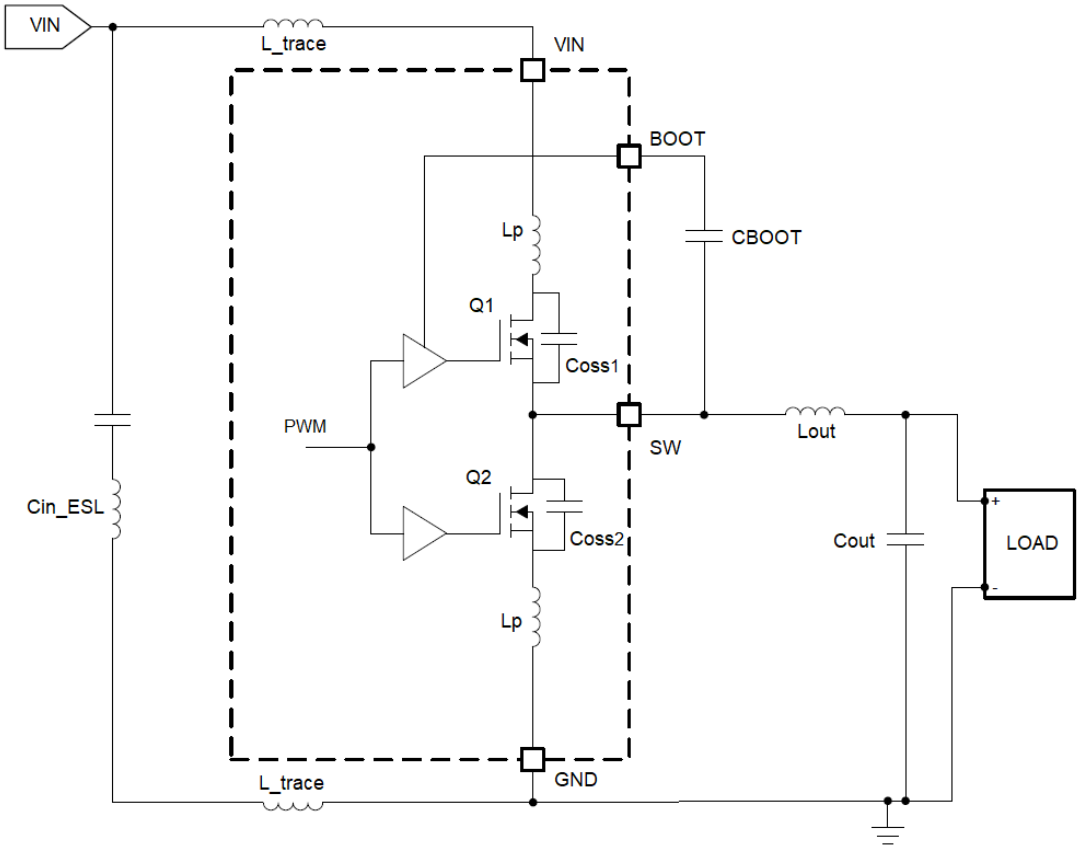


Figure 1-1. Power Stage Components

When the LS gate signal goes LOW, the low-side MOSFET turns off and the inductor current flows through the body diode of the low side MOSFET. After a short dead time, the high-side MOSFET is turned on and current flows to force the body diode of the low-side MOSFET off. As the body diode undergoes reverse recovery, the voltage on SW begins to rise and the ringing waveform results from the interaction of parasitic inductance and the switch-node capacitance. This interaction primarily consists of the $Coss_2$ of the low-side MOSFET, as shown in Figure 1-2.

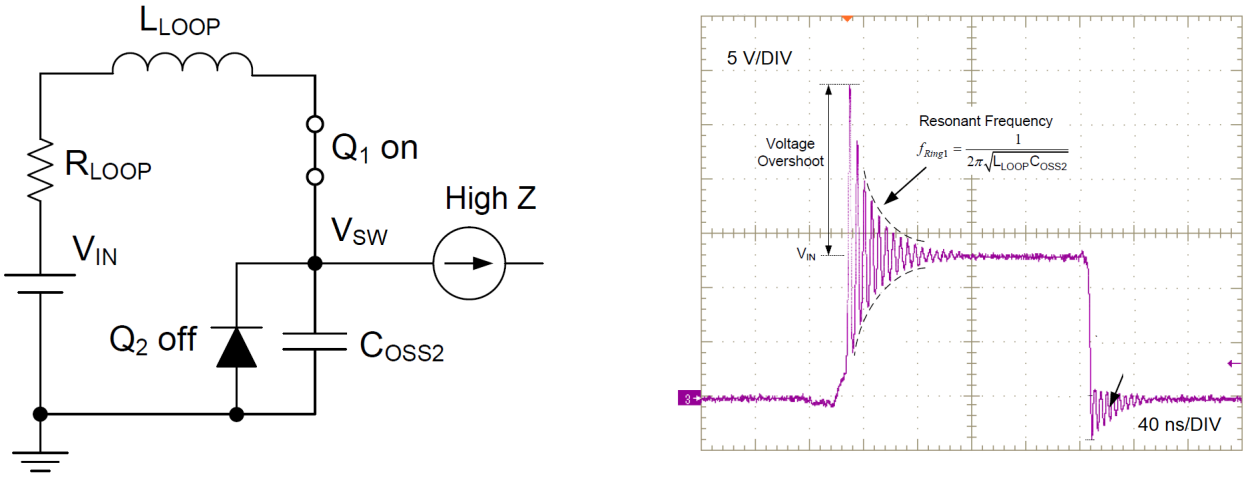
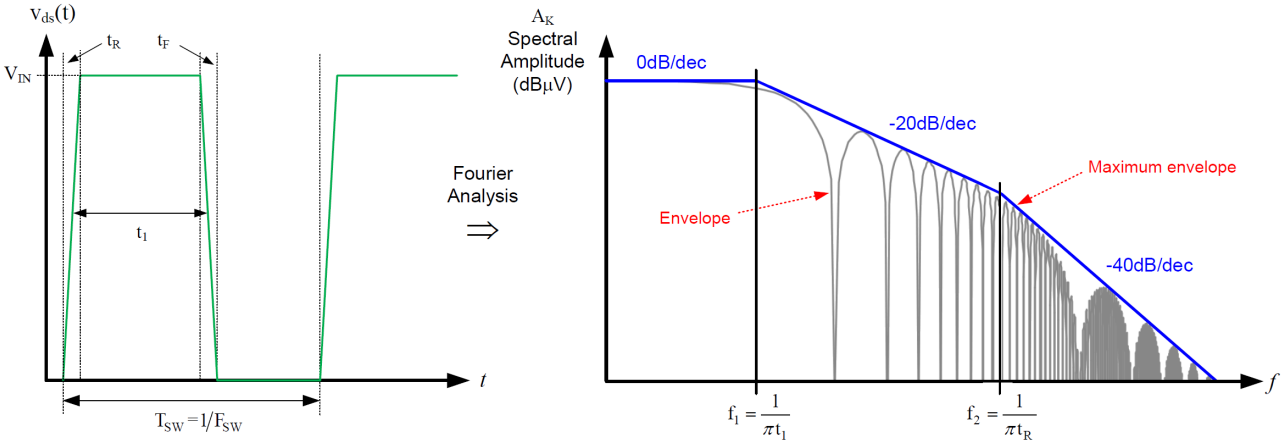


Figure 1-2. Switch-node Ringing

This ringing not only increases MOSFET switching loss and the peak drain-to-source voltage spike, the ringing also affects broadband EMI in the 50 MHz to 300 MHz range. The ringing must be monitored and controlled within the data sheet limits of the device voltage ratings to maintain reliable operation.

2 EMI Noise Caused by Instantaneous Switching

The left side of Figure 2-1 shows the simplified trapezoidal wave with period Tsw, pulse width t_1, rise time t_R, and fall times t_F. Using Fourier analysis, the frequency domain consists of the fundamental frequency and several upper harmonics. The harmonic amplitude envelope is a double-sinc function with corner frequencies of f_1 and f_2, depending on the pulse duration and rise and fall time of the time-domain waveform. Radiated EMI problems often occur in the 50 MHz to 300 MHz range, and increasing rise and fall times shift the f_2 point to lower frequencies, and the high frequencies roll-off more quickly with 40 dB/DEC. In the lower frequency range, the impact of slower rise and fall times is limited.



t_1 = pulse width (measured at half-maximum)
T_{SW} = switching period
D = duty cycle = t_1/T_{SW}
t_R = rise time; t_F = fall time of edge transition

Figure 2-1. Frequency Spectrum of SW Node Voltage

3 Optimize Circuit and Layout Design

There are several methods to reduce the ringing to keep the MOSFET switches and controller pins within the safe operating region and EMI noise so caused, such as a boot resistor, a high-side gate resistor, or a RC snubber. However, the first approach is to optimize the circuit design, component selection and PCB layout to minimize the parasitic inductor and loop area of critical path. TI provides many supporting documents for how to optimize the circuit and layout design for lower EMI.

If the EMI levels of the buck converter circuit exceed requirement levels and layout or filtering can not be improved, then reduction of the buck converter switching speed by boot resistor can help reduce the EMI levels.

4 Using a Boot Resistor

The charge-pump circuit in Figure 1-1 uses CBOOT to boost the high-side gate supply above the supply voltage of the power stage. One method to reduce ringing is to include a boot resistor in series with the boot capacitor, which slows down the turn on speed of the high side NFET as shown in Figure 5-2. This method allows more time for the parasitic network to discharge, ultimately limiting the ringing shown in Figure 4-1. The value of the boot resistor is determined by starting at 0 and increasing the resistance until the desired ringing or EMI level is achieved.

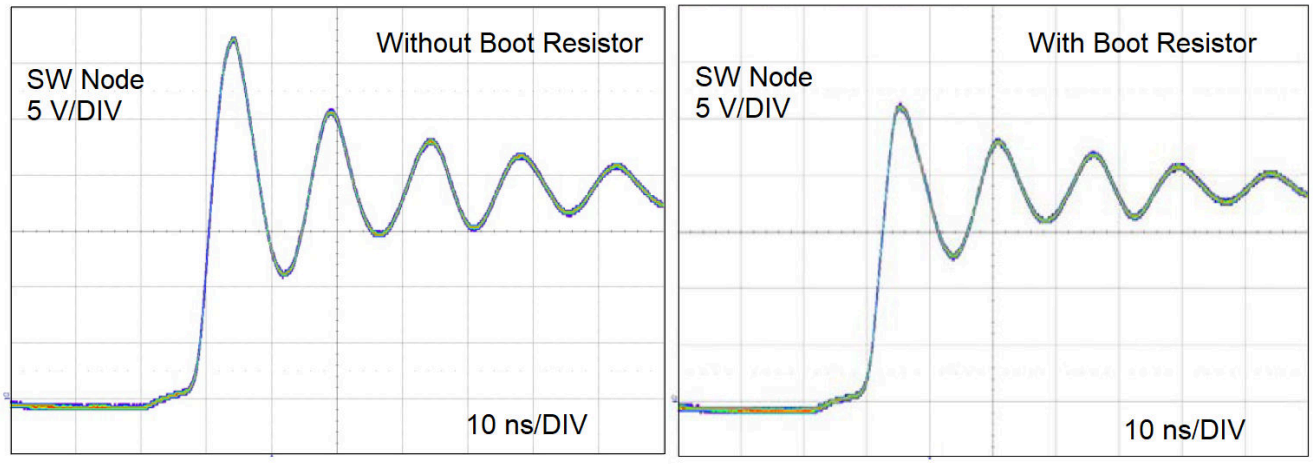


Figure 4-1. Reduce SW Ringing by RBOOT

5 Design Consideration on RBOOT

The RBOOT pin is in series with the CBOOT capacitor, which not only limits the HS driving current, but also impacts the voltage presented on BT-SW pin during the discharging and refresh period. The voltage between the BOOT to SW pins serves as the bias power supply for the HS driver, the level-shift circuitry that transmits control information between the controller and HS gate driver. It must be noted that adding a resistor in series with the bootstrap capacitor can introduce circuit effects beyond slowing the high-side MOSFET transition time.

5.1 BT-SW UVLO

When the HS MOSFET is turned on, the current that flows from the bootstrap capacitor through RBOOT causes a drop in the voltage from the BOOT to SW pins. If this voltage drop is large, the voltage on the HS MOSFET gate-source is reduced, leading to potential slow device turn-on and or triggering the BOOT UVLO circuit.

LM53602 is a 36-V, 2-A synchronous buck converter. The BT-SW voltage UVLO threshold is 2.5 V (typical) with 50 ns (typical) delay time. Figure 5-1 shows the BT-SW voltage measured on the LM53602 application circuit for 12 V to 3.3 V conversion at 2 MHz and FWPM mode. With an RBOOT value of 20 Ω, the BT-SW voltage drops below 2.5 V for 44 ns, which risks hitting the UVLO threshold.

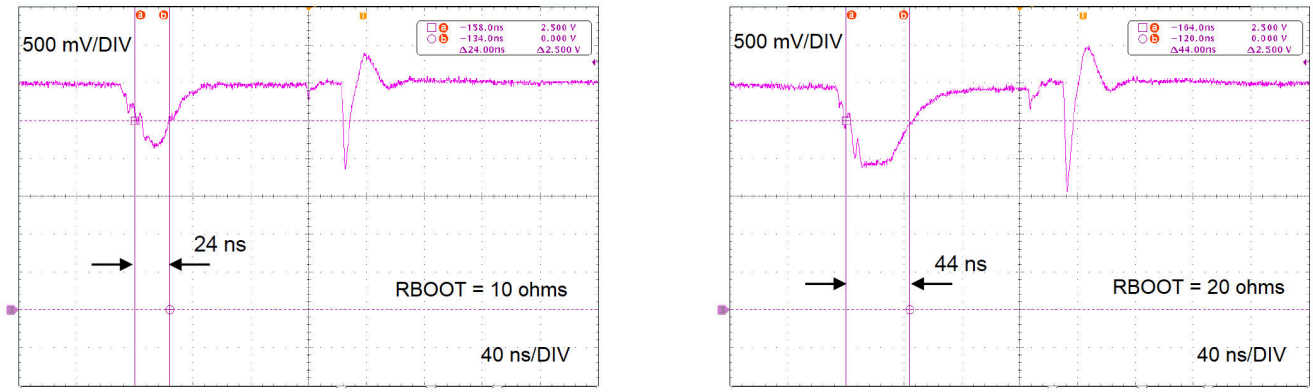


Figure 5-1. BT-SW Voltage Drop

Typically, the HS FET is turned-off immediately until the next cycle when BOOT UVLO is triggered, but there can be unexpected switching behavior if combined with other abnormal conditions, so the BT-SW voltage must be carefully checked in various operating condition to avoid hitting the UVLO threshold.

5.2 Refresh Boot Capacitor

In applications with short off times, resulting from high duty-cycle applications or high switching frequency, the boot capacitor can not be fully charged in each cycle if the boot resistor is too large. For these reasons, the value of the boot resistor must be kept small and must be tested and evaluated completely under all conditions of Vin, Vout, Iout, and operating temperature to achieve robust performance.

The charging current is not only limited by the RBOOT, but also limited by the parasitic inductors on the charging loop. Figure 5-2 shows the simplified block of the CBOOT charging loop of LM53602. Lparasitic is small proportion of the total parasitic inductance. Because of the 2-MHz switching frequency, the CBOOT never charges back to VCC. Simulations results show that with Lparasitic at only a few nHs and RBOOT at 10 Ω, V1 goes lower and lower over time and hits UVLO in the worst case. RBOOT at 6.8 Ω or lower is suggested for operating the LM53602 at 2 MHz frequency.

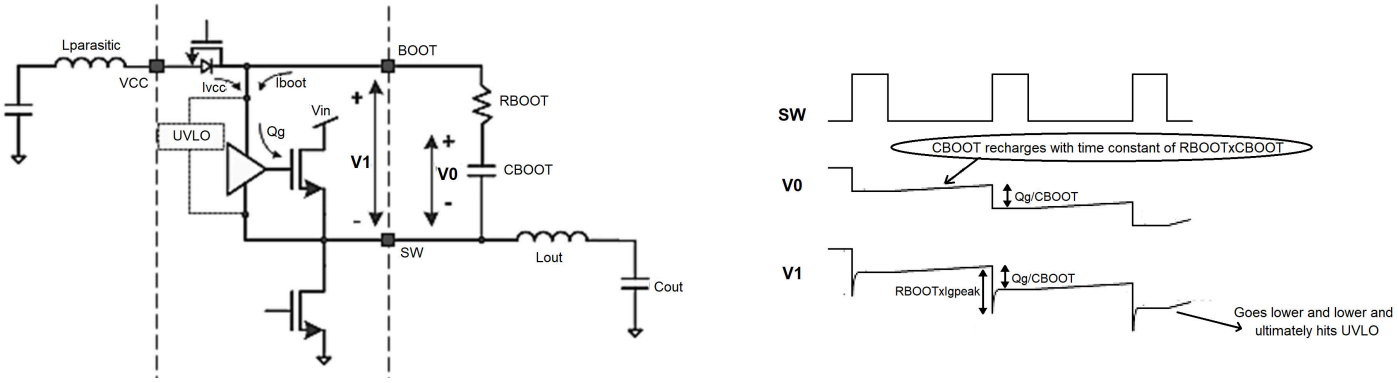


Figure 5-2. Refresh CBOOT

A larger RBOOT can be used if a small Schottky diode is paralleled with RBOOT which bypasses the RBOOT pin during the CBOOT charging period, as shown in Figure 5-3. The CBOOT capacitor can be charged up to 10 ns, which is shorter than the typical T-off_min of most buck converters of 100 ns to 200 ns.

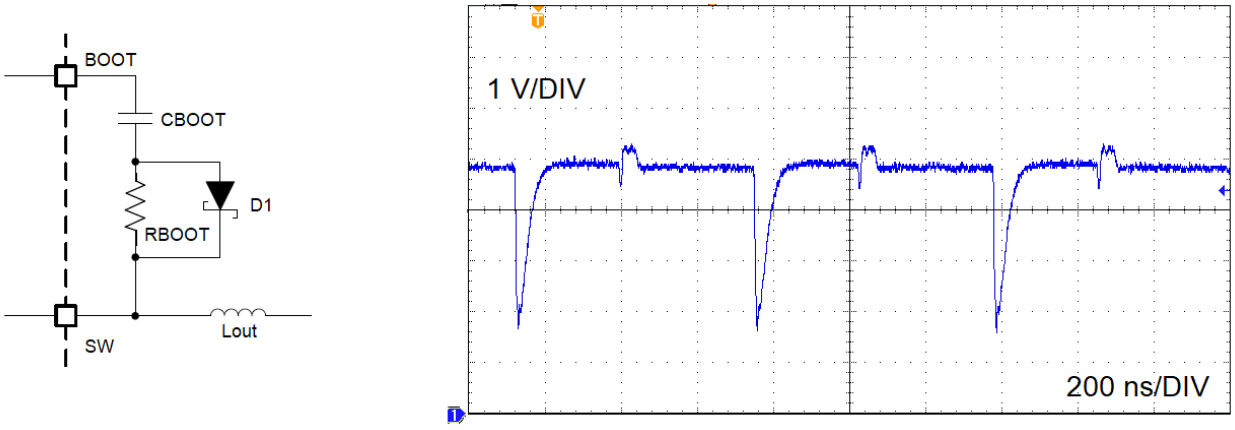


Figure 5-3. Parallel Diode With RBOOT

5.3 Thermal

Increasing the boot resistor can slow the MOSFET switch-on timing and increase switching power loss, resulting in diminishing efficiency. Take care to optimize the resistance to provide the best EMI while not generating too much heat, especially at high Vin, high Fsw, and maximum load current conditions.

6 Converter With Dedicated RBOOT Pin

The value of RBOOT depends on the size of the high side MOSFET. For most applications, approximately 5 Ω to 10 Ω is used. If the boot resistor value is too large, the boot capacitor can not fully charge in each cycle. When the value of the boot resistor is too large, the gate driver does not have sufficient voltage to keep the high-side FET on and can turn off in the middle of the cycle. This gate driver behavior limits the amount of ringing that can be reduced with the boot resistor method. To allow optimization of EMI with more flexibility, the LM61440/60 and LM61480/95 families are designed with a dedicated RBOOT pin to allow a resistor to select the strength of the high-side FET driver during turn on. Figure 6-1 shows the integrated RBOOT pin. The current drawn through the RBOOT pin, represented by the dotted loop in Figure 6-1, is magnified and drawn through from CBOOT (the dashed line in Figure 6-1). This feature allows a wide range of RBOOT values to optimize EMI.

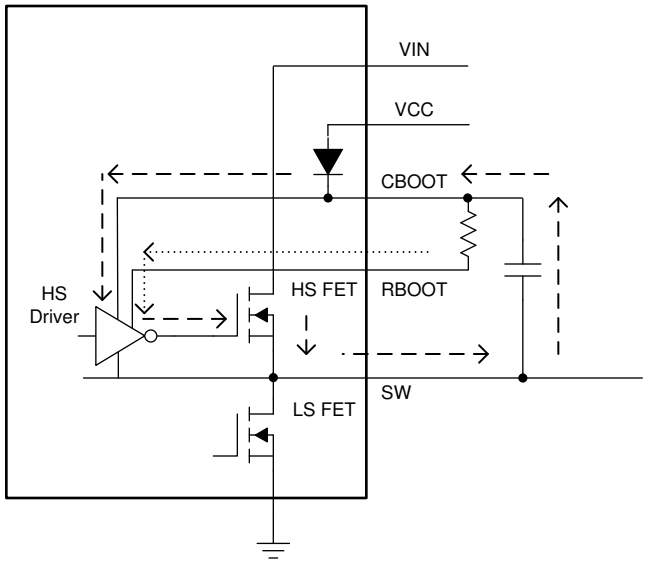


Figure 6-1. Simplified Circuit Showing How RBOOT Pin Functions

7 Summary

The need to control ringing produced by the switching of power semiconductors has existed in industry as long as semiconductor devices have been used in switching mode power supplies. It is interesting to note that the boot resistor affects only the turn-on speed of the high-side FET, making this method an efficient approach to reduce ringing with a small impact on the total solution efficiency. Using this boot resistor method significantly reduces the noise in the entire system, which can be a good trade-off.

RBOOT does not reduce the frequency of the switch node ringing which can be needed to address EMI issues. In situations where additional switch-node ring control is required, a snubber can be added to reduce both the amplitude and the ring frequency found on SW node.

8 References

1. Texas Instruments, *Minimizing Switching Ringing at TPS53355 and TPS53353 Family Devices*, application note.
2. Texas Instruments, *AN-2155 Layout Tips for EMI Reduction in DC / DC Converters*, application note.
3. Texas Instruments, *Controlling Switch-Node Ringing in Synchronous Buck Converters*, analog design journal.

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