

# LMZ30604EVM-001, LMZ30604EVM-002, and LMZ30606EVM-003

## User's Guide



Literature Number: SNVU296A  
July 2013–Revised March 2014

# **LMZ3060xEVM-00x 2- to 6-A Simple Switcher Power Module**

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The LMZ30604EVM-001, LMZ30602EVM-002, and LMZ30606 evaluation modules (LMZ3060xEVM-00x) are designed as an easy-to-use platform that facilitates an extensive evaluation of the features and performance of the Simple Switcher power module. The EVM PCB may be configured with one of three devices (see [Table 1](#)).

## **1 Introduction**

This user's guide provides information on the correct usage of the EVM and an explanation of the numerous test points on the board.

**Table 1. LMZ3060xEVM-00x Device Configuration**

DEVICE	TITLE
LMZ30602	2.95 to 6-V input, 2-A output sync, step-down converter with PWM
LMZ30604	2.95 to 6-V input, 4-A output sync, step-down converter with PWM
LMZ30604	2.95 to 6-V input, 6-A output sync, step-down converter with PWM

## **2 Description**

The EVM features a LMZ3060x synchronous buck power module configured for operation with typical 3.3- and 5-V input bus applications. The output voltage can be set to one of five popular values by using a simple configuration jumper. In similar fashion, the switching frequency can be set to one of four values by use of a jumper. The full rated output current can be supplied by the EVM. A minimal amount of input and output capacitance is used on the board. Component pads are provided for additional input and output capacitors if desired. Monitoring test points are provided to allow measurement of efficiency, power dissipation, input ripple, output ripple, line and load regulation, and transient response. Control test points are provided for use of the PWRGD, Inhibit/UVLO, synchronization, and slow-start/tracking features of the device. The EVM uses a recommended PCB layout that maximizes thermal performance and minimizes output ripple and noise.

### 3 Getting Started

Figure 1 highlights the user interface items associated with the EVM. The polarized  $V_{IN}$  Power terminal block is used for connection to the host input supply and the polarized  $V_{OUT}$  Power terminal block is used for connection to the load. The terminal blocks can accept up to 16 AWG wire.

The  $V_{IN}$  monitor and  $V_{OUT}$  monitor test points located near the power terminal blocks are intended to be used as voltage monitoring points where voltmeters can be connected to measure  $V_{IN}$  and  $V_{OUT}$ . The voltmeter references should be connected to any of the four  $V_{IN}/V_{OUT}$  monitor grounds test points located between the power terminal blocks. Do not use these  $V_{IN}$  and  $V_{OUT}$  monitoring test points as the input supply or output load connection points. The PCB traces connecting to these test points are not designed to support high currents.

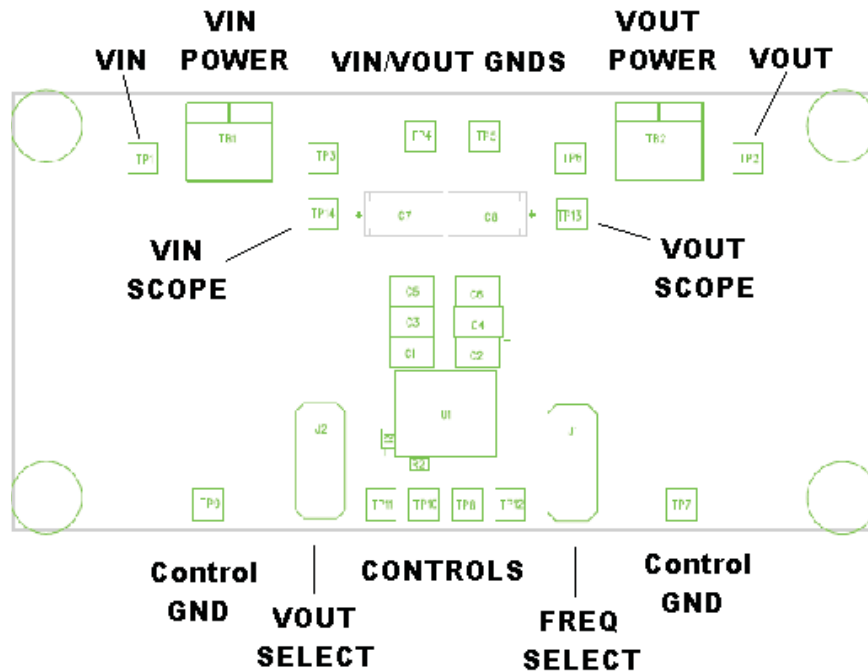


Figure 1. LMZ3060xEVM-00x User Interface

The  $V_{IN}$  scope and  $V_{OUT}$  scope test points can be used to monitor  $V_{IN}$  and  $V_{OUT}$  waveforms with an oscilloscope. These test points are intended for use with un-hooded scope probes. The scope probe tip should be connected to the socket labeled VIN or VOUT, and the scope ground barrel should lean against to the test point labeled GND. The GND TP may need to be cut or bent slightly to hold the probe barrel.

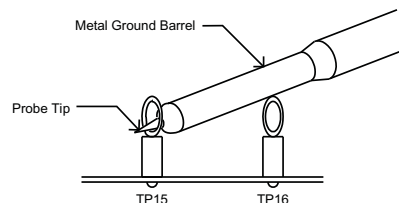


Figure 2. Tip and Barrel Measurement

The control test points located directly below the LMZ3060x device are made available to test the features of the device. Any external connections made to these test points should be referenced to either of the two control ground test points located along the bottom of the EVM. Refer to Section 4 of this user guide for more information on the individual control test points.

The  $V_{OUT}$ -select and  $F_{SW}$ -select configuration jumpers are provided for selecting the desired output voltage and appropriate switching frequency. Before applying power to the EVM, ensure that the jumpers are present and properly positioned for the intended output voltage. Refer to [Table 2](#) for the recommended jumper settings. Always remove input power before changing the jumper settings.

Once the jumper settings have been confirmed, configure the host input supply to apply the appropriate bus voltage listed in [Table 2](#) and confirm that the selected output voltage is obtained.

**Table 2. Output Voltage and Switching Frequency Jumper Settings**

$V_{OUT}$ SELECT	LMZ30602, $F_{SW}$ SELECT	LMZ30604, $F_{SW}$ SELECT	LMZ30606, $F_{SW}$ SELECT	$V_{IN}$ BUS VOLTAGE
3.3 V	1.5 MHz	1 MHz	1 MHz	5 V
2.5 V	1.5 MHz	1 MHz	1 MHz	5 V
1.8 V	1 MHz	1 MHz	1 MHz	5 V or 3.3 V
1.2 V	750 kHz	750 kHz	750 kHz	5 V or 3.3 V
0.8 V	650 kHz	650 kHz	650 kHz	5 V or 3.3 V

#### 4 Test Point Descriptions

Fourteen wire-loop test points have been provided as convenient connection points for digital voltmeters (DVM) or oscilloscope probes to aid in the evaluation of the device. A via labeled PH is available near U1 to scope on the switching frequency. A description of each test point is listed in [Table 3](#)

**Table 3. Test Point Descriptions**

TEST POINT	DESCRIPTION
VIN	Input voltage monitor. Connect DVM to this point for measuring efficiency.
VOUT	Output voltage monitor. Connect DVM to this point for measuring efficiency, line regulation, and load regulation.
GND	Input and output voltage monitor grounds (located between terminal blocks). Reference the above DVMs to any of these four ground points.
VIN (scope)	Input voltage scope monitor. Connect an oscilloscope to this set of points to measure input ripple voltage.
VOUT (scope)	Output voltage scope monitor. Connect an oscilloscope to this set of points to measure output ripple voltage and transient response.
PWRGD	Monitors the power good signal of the device. This is an open drain signal that requires an external pull-up resistor to $V_{IN}$ if monitoring is desired. A 10-k $\Omega$ to 100-k $\Omega$ pullup resistor is recommended. PWRGD is high if the output voltage is within 92% to 106% of its nominal value.
INH/UVLO	Connect this point to control ground to inhibit the device. Allow this point to float to enable the device. Do not use a pull-up resistor. An external resistor can be connected from this point to control ground to increase the under-voltage lockout (UVLO) of the device.
RT/CLK	Connects to the RT/CLK pin of the device. An external clock signal can be applied to this point to synchronize the device to an appropriate frequency.
SS/TR	Connects to the internal slow-start capacitor of the device. An external capacitor can be connected from this point to control ground to increase the slow-start time of the device. This point can also be used as an input for tracking applications.
GND	Control grounds (located along bottom of EVM). Reference any signals associated with the control test points to either of these two ground points.

## 5 Operation Notes

The UVLO threshold of the factory-stock EVM is approximately 3.05 V with 0.3 V of hysteresis. The input voltage must be above the UVLO threshold in order to startup the device. The UVLO threshold can be increased by adding a resistor to the INH/UVLO test point as described in [Table 3](#). After startup, the minimum input voltage to the device must be at least 2.95 V or ( $V_{OUT} + 1.1$  V), whichever is greater, in order to produce a regulated output. The maximum operating input voltage for the device is 6 V. For further information on the input voltage range and UVLO operation, refer to the device data sheet.

After application of the proper input voltage, the output voltage of the device will ramp to its final value in approximately 1 ms. If desired, this soft-start time can be increased by adding a capacitor to the SS/TR test point as described above. Refer to the device datasheet for further information on adjusting the soft-start time.

[Table 1](#) lists the recommended switching frequencies for each of the  $V_{OUT}$  selections. These recommendations cover operation over a wide range of input voltage and output load conditions. Several factors such as duty cycle, minimum on-time, minimum off-time, and current limit influence selection of the appropriate switching frequency. In some applications, other switching frequencies might be used for particular output voltages, depending on the above factors. For further information on switching frequency selection, including synchronization, refer to the device data sheet.

6 LMZ3060xEVM-00x Schematic

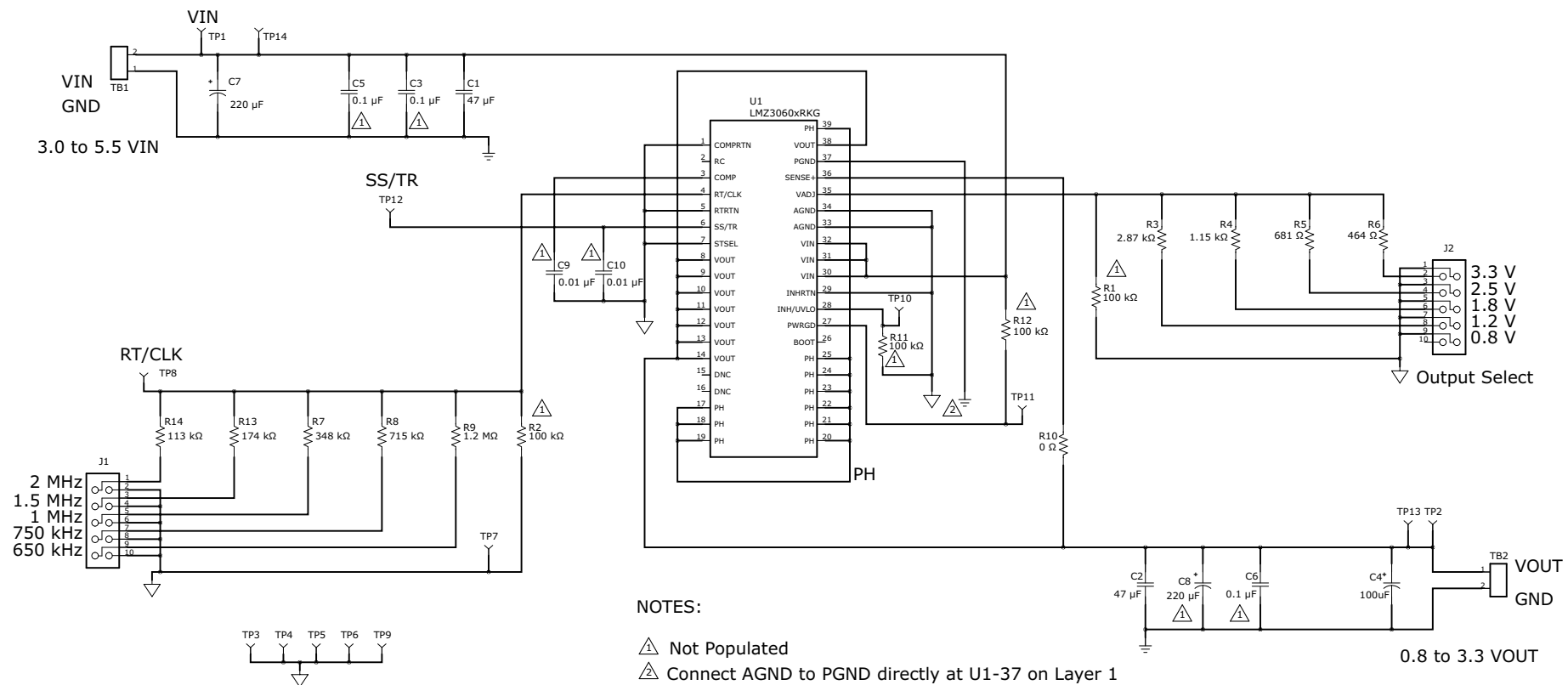


Figure 3. LMZ3060xEVM-00x Schematic

## 7 PCB Layouts

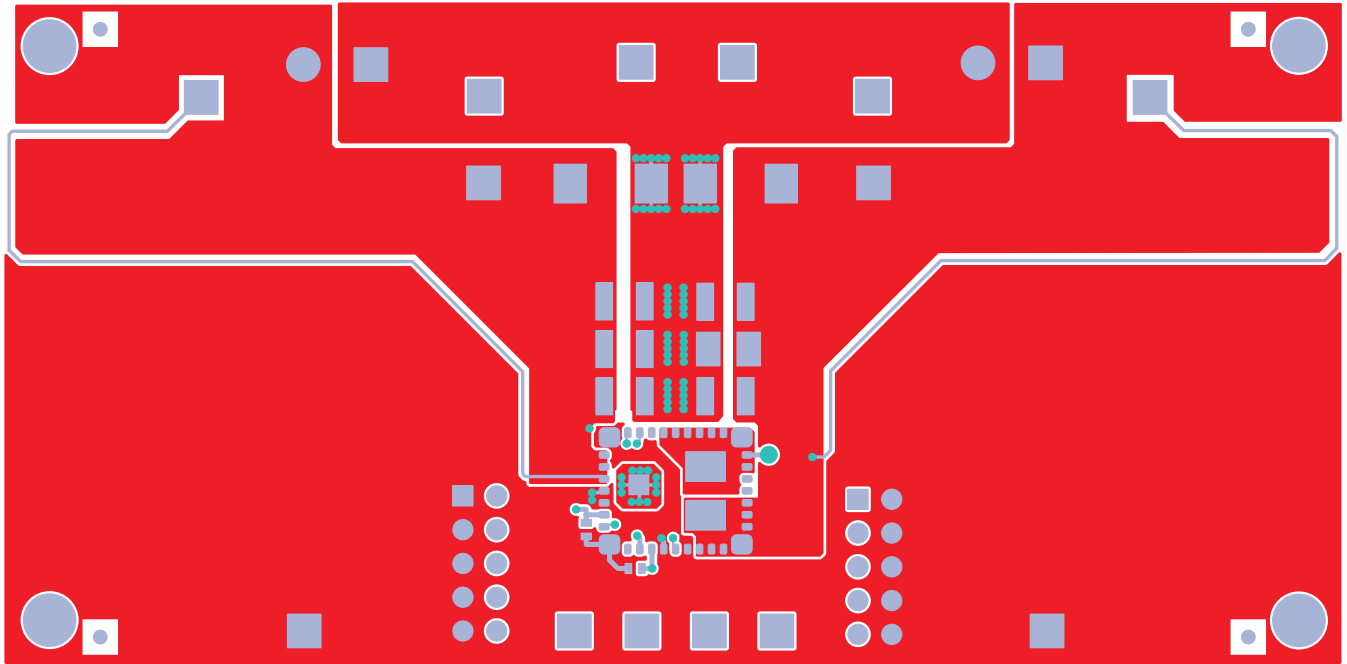


Figure 4. Top Layer

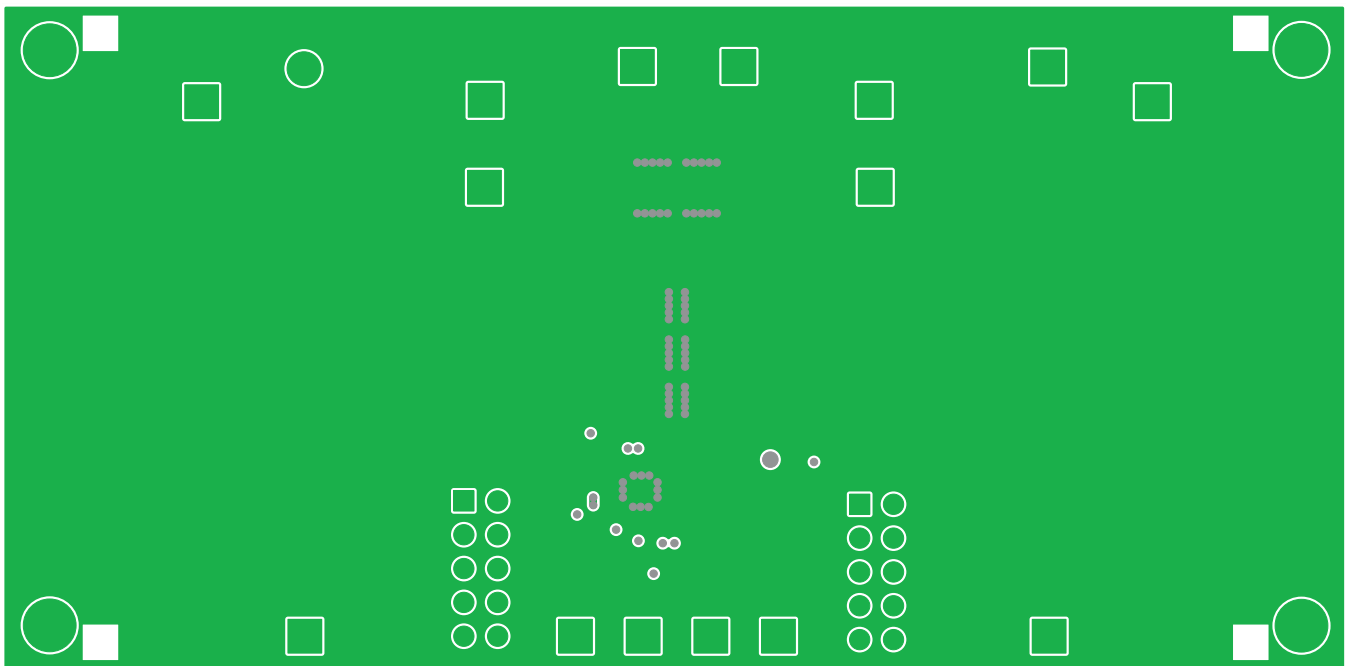
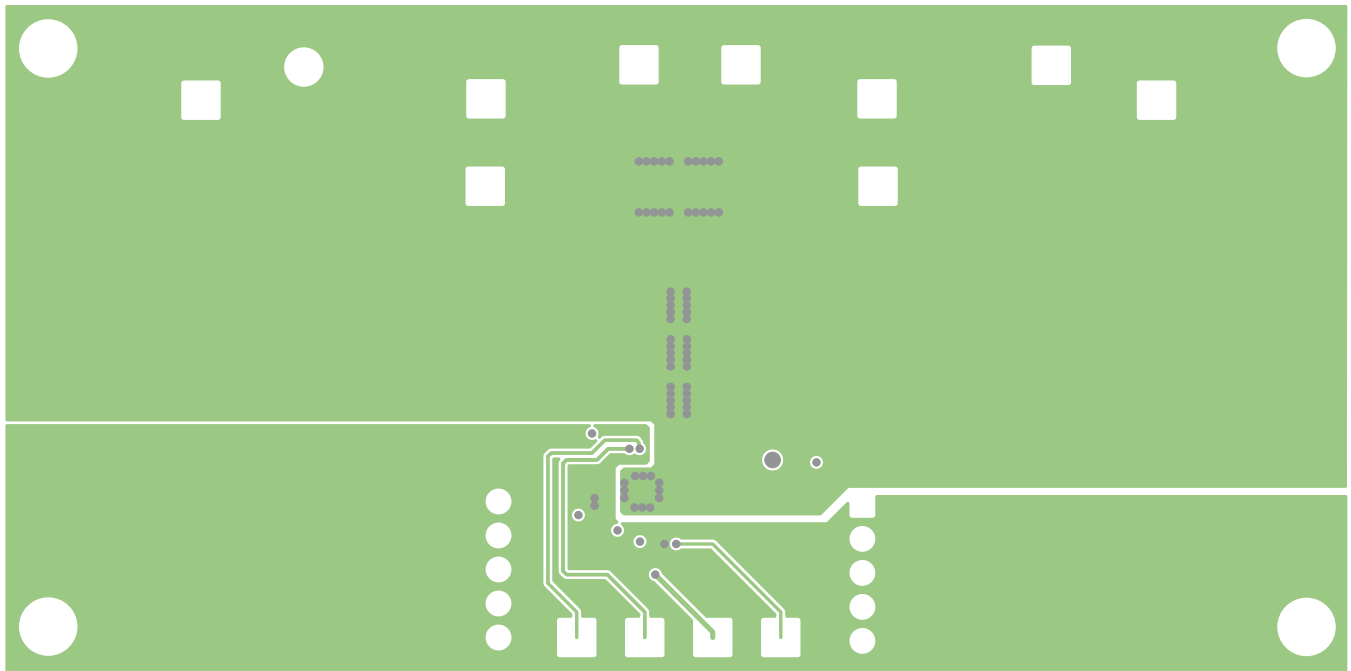
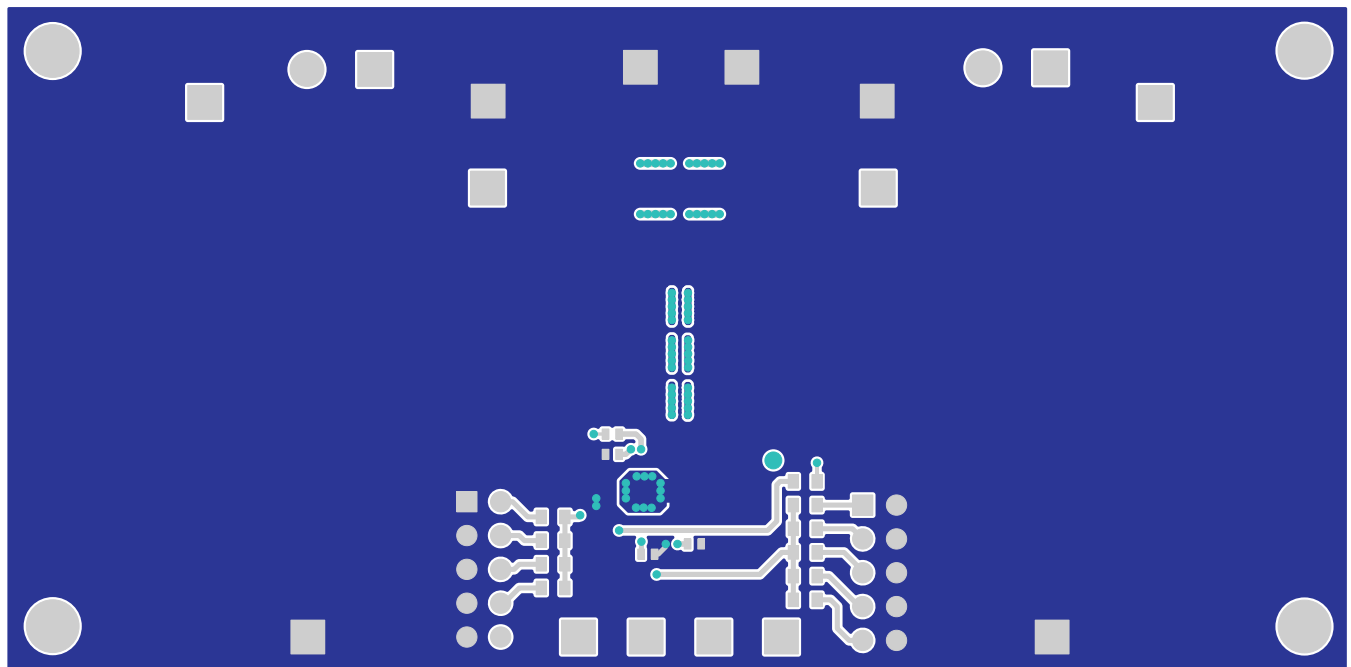


Figure 5. Internal Layer 1



**Figure 6. Internal Layer 2**

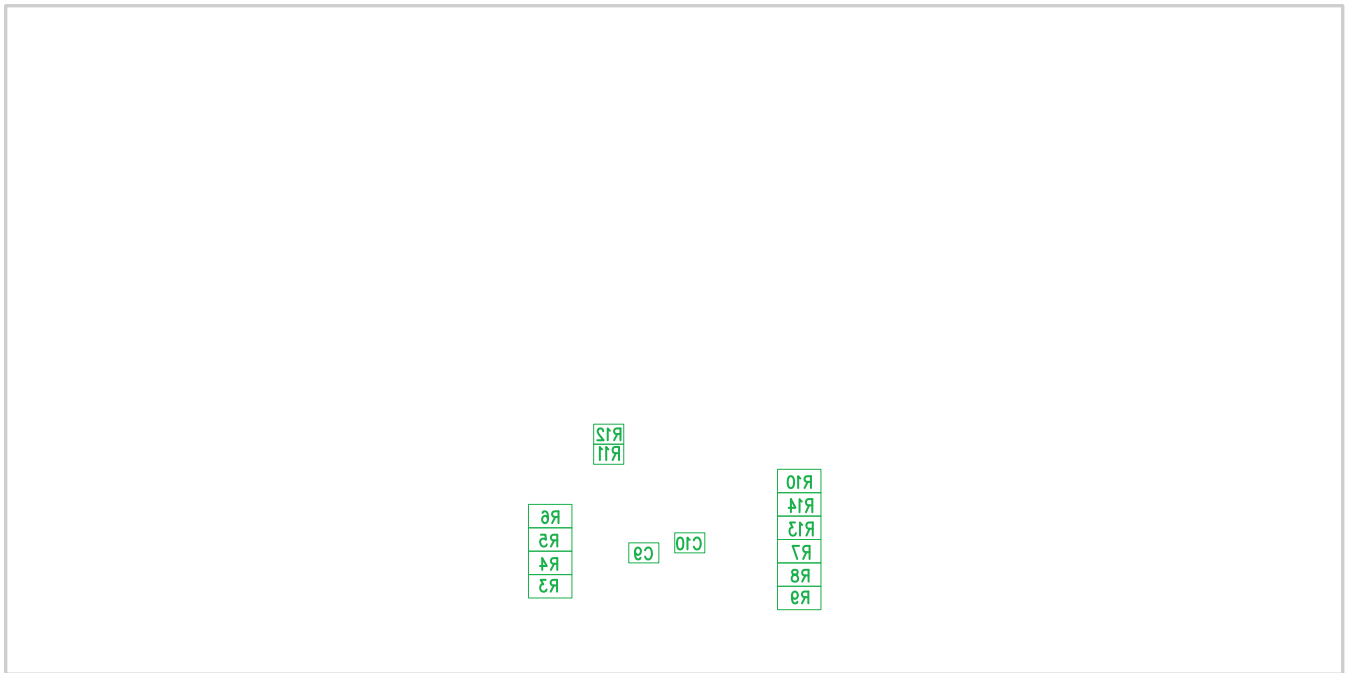


**Figure 7. Bottom Layer**





**Figure 8. Top Assembly**



**Figure 9. Bottom Layer**

**8 Bill of Materials**
**Table 4. LMZ3060xEVM-00x Bill of Materials**

-003	-002	-001	REF DES	DESCRIPTION	Part Number	MFR
1	1	1	C1	Capacitor, ceramic, 10 V, x5R, 10%, 47 $\mu$ F, 1210	GRM32ER61A476K	Murata
1	1	1	C2	Capacitor, ceramic, 6.3 V, x5R, 20%, 47 $\mu$ F, 1210	GRM32ER60J476M	Murata
1	1	1	C7	Capacitor, polymer, 10 V, 20%, 220 $\mu$ F, D3L	10TPE220ML	Sanyo
0	0	0	C8	Capacitor, polymer, 10 V, 20%, 220 $\mu$ F, D3L	10TPE220ML	Sanyo
1	1	1	C4	Capacitor, polymer, 6.3 V, 20%, 100 $\mu$ F, B2	6TPE100MPB	Sanyo
0	0	0	C3, C5, C6	Capacitor, ceramic, 0.1 $\mu$ F, 1210	Std	STD
0	0	0	10	Capacitor, ceramic, 0.01 $\mu$ F, 0402	STD	STD
2	2	2	J1-2	Header, male 2 x 5 pin, 100-mil spacing, 0.100 inch x 5 inch x 2 inch	PEC05DAAN	Sullins
1	1	1	R3	Resistor, chip, 1/16 W, 1%, 2.87 k $\Omega$ , 0603	STD	STD
1	1	1	R4	Resistor, chip, 1/16 W, 1%, 1.15 k $\Omega$ , 0603	STD	STD
1	1	1	R5	Resistor, chip, 1/16 W, 1%, 681 $\Omega$ , 0603	STD	STD
1	1	1	R6	Resistor, chip, 1/16 W, 1%, 464 $\Omega$ , 0603	STD	STD
1	1	1	R7	Resistor, chip, 1/16 W, 1%, 348 k $\Omega$ , 0603	STD	STD
1	1	1	R8	Resistor, chip, 1/16 W, 1%, 715 k $\Omega$ , 0603	STD	STD
1	1	1	R9	Resistor, chip, 1/16 W, 1%, 1.2 M $\Omega$ , 0603	STD	STD
1	1	1	R10	Resistor, chip, 1/16 W, 5%, 0 $\Omega$ , 0603	STD	STD
1	1	1	R13	Resistor, chip, 1/16 W, 1%, 174 k $\Omega$ , 0603	STD	STD
1	1	1	R14	Resistor, chip, 1/16 W, 1%, 113 k $\Omega$ , 0603	STD	STD
0	0	0	R1, R2, R11, R12	Resistor, chip, 1/16 W, 1%, 100 k $\Omega$ , 0402	Std	Std
2	2	2	TB1-2	Terminal block, 2 pin, 15 A, 5.1 mm, 0.40 inch x 0.35 inch	ED120/2DS	OST
8	8	8	TP1, TP2 TP8 TP10- TP14	Test point, white, thru hole, 5012, 0.125 inch x 0.125 inch	5012	Keystone
6	6	6	TP3-7 TP9	Test point, black, thru hole, 5011, 0.125 inch x 0.125 inch	5011	Keystone
0	0	1	U1	6-V input, 4-A Output Sync. Step-Down Converter with PWM, QFN	LMZ30604RKG	TI
0	1	0	U1	6-V input, 2-A Output Sync. Step-Down Converter with PWM, QFN	LMZ30604RKG	TI
1	0	0	U1	6-V input, 6-A Output Sync. Step-Down Converter with PWM, QFN	LMZ30604RKG	TI
1	1	1		PCB, 0.063 inch H x 1.9 inch L x 3.9 inch W	PWR059	ANY
2	2	2		Conn jumper shorting gold flash	SPC02SYAN	Sullins
4	4	4		Bump on hemisphere 0.44 inch x 0.20 inch clear, 0.440 inch Dia x 0.200 inch H	SJ-5303	3M

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## Revision History

<b>Changes from Original (July 2013) to A Revision</b>	<b>Page</b>
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- Updated [Figure 3](#) ..... 6
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NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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This Class A or B digital apparatus complies with Canadian ICES-003.

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##### Concerning EVMs Including Detachable Antennas

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1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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