Using the LP8555 Evaluation Module

User's Guide

Literature Number: SNVU299
FEBRUARY 2014

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About this Manual

This user's guide describes the module used to evaluate characteristics, operation, and use of the LP8555 high-efficiency LED backlight driver for tablet PCs. This document includes a schematic diagram, PCB layout, and bill of materials (BOM). Evaluation SW usage is also described.

How to Use This Manual

This document contains the following chapters:

- Chapter 1—Introduction
- Chapter 2—Description of the LP8555
- Chapter 3—Hardware Setup
- Chapter 4—Board Layout
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- Chapter 10—Programming Considerations
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Related Documentation from Texas Instruments

LP8555 datasheet SNVS857

DSBGA Package Application Note AN-1112 SNVA009

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user, at his own expense, will be required to take whatever measures may be required to correct this interference.

If You Need Assistance

Contact your local TI sales representative.

Introduction

The Texas Instruments LP8555EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LP8555 device. The LP8555EVM uses the LP8555 to drive up to 12 LED strings for LCD backlighting with high efficiency. Information about output voltage and current ratings of LP8555EVM can also be found in the device datasheet SNVS857.

In order to facilitate ease of testing and evaluation of this circuit, the EVM contains a TI MSP430 microprocessor to provide easy communication via USB. Power supply connection for the VDD, VDDIO, and test points for the each signal can be found on the EVM. Windows GUI is used to control I^2C registers of the device. A separate LED board can be used as a load, or it is possible to connect an LCD panel to the output connectors.

For evaluation purposes, the EVM has been tested over a 2.7-V to 20-V input voltage range. This voltage range is within the recommended operating range for input voltage of the LP8555. Users are cautioned to evaluate their specific operating conditions and choose components with the appropriate voltage ratings before designing this support circuitry into a final product.

Description of the LP8555

The LP8555 is a high-efficiency LED driver with integrated dual DC-DC boost converters. It has 12 high-precision current sinks that can be controlled by a PWM input signal, an I^2C master, or both.

Dual-boost configuration of LP8555 shares the load to two inductors and allows thinner overall solution size and better efficiency compared to single-boost solutions. 12 LED strings allow the driving of high number of LEDs with optimal efficiency since boost conversion ratio can be kept low.

The boost converter has adaptive output voltage control based on the LED current sink headroom voltages. This feature minimizes the power consumption by adjusting the voltage to lowest sufficient level in all conditions.

The LED string auto-detect function enables use of the same device in systems with 2 to 12 LED strings for maximum design flexibility. Proprietary Hybrid PWM and Current dimming mode enables additional system power savings. Phase-shift PWM allows reduced audible noise and smaller boost output capacitors. Flexible CABC support combines brightness level selections based on the PWM input and I^2C commands.

2.1 Features

- Dual High-Efficiency DC/DC Boost Converters
- 2.7-V to 20-V VDD Range
- 12 50-mA High-Precision LED Current Sinks With 12-Bit Brightness Control
- Adaptive LED Current Sink Headroom Controls for Maximum System Efficiency
- LED String Count Auto-Detection
- Phase-Shifted PWM Mode for Reduced Audible Noise
- PWM Input Duty-Cycle and/or I^2C-Register Brightness Control
- Hybrid PWM and Current Dimming for Higher LED Drive Optical Efficiency
- Flexible CABC Support
- EPROM, I^2C-Registers, or External Resistors for Configuration
- Improved Boost EMI Performance with Slew-Rate Control, Spread Spectrum, and Phase-Shifted Switching
- Extensive Fault Detection Schemes
- 36-pin DSBGA package, 2.478 mm x 2.478 mm x 0.6 mm, 0.4 mm pitch

2.2 Applications

- Tablet LCD Display LED Backlight

2.3 Typical Applications

In the following example all 12 channels are used with I²C brightness control. The PWM/INT terminal is used for interrupt signal, notifying the processor of possible fault conditions. LED current and PWM frequency are loaded from EPROM registers during the start-up sequence, and they can be changed with I²C writes, if needed, before turning on the backlight. Configuration registers can be set before the backlight is enabled, so special pre-set EPROM is not necessarily needed. Details on I²C registers and EPROM settings are seen in the Register Maps section .

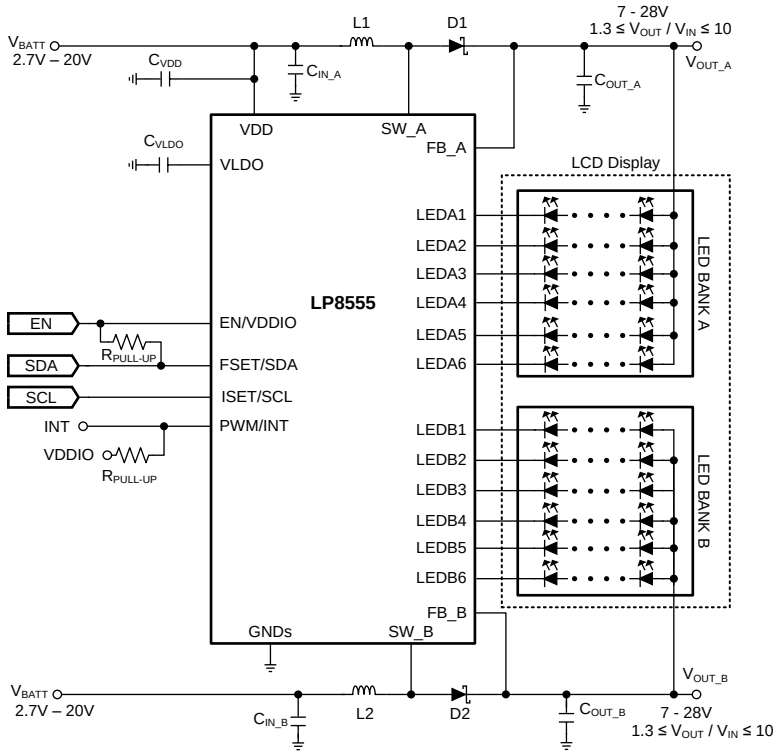


Figure 2-1. Application Example With 12 LED Strings, I²C Brightness Control

Figure 2-2 shows how the LP8555 can be configured for operating without I²C control. In this case, the only controls needed are PWM input for brightness control and EN for enabling and disabling device. PWM frequency is set with the R_{FSET} resistor, and LED current is set with the R_{ISET} resistor. All 12 channels are used in this example, but other configurations can be used instead. Details on I²C registers and EPROM settings are seen in Chapter 10. Since this configuration relies on pre-programmed EPROM for basic setup (although LED current and PWM frequency are set with resistors), special EPROM configuration is needed for this application.

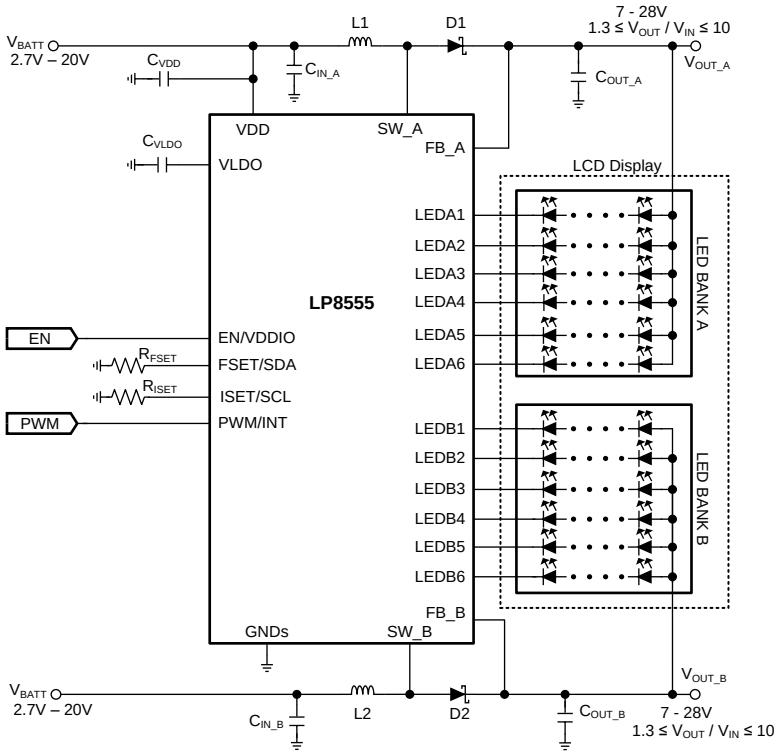


Figure 2-2. Application Example with 12 LED Strings and PWM Input Brightness Control

Figure 2-3 shows how the LED banks can have different LED configurations. Bank A has 4 active LED outputs, and Bank B has 5 active LED outputs. The LP8555 will automatically detect open outputs and adjust phase shifting for both sinks optimally. Control in this example is from I²C bus; the PWM/INT terminal is used for interrupt signal, notifying processor of possible fault conditions. Details on I²C registers and EPROM settings are seen in Chapter 10 .

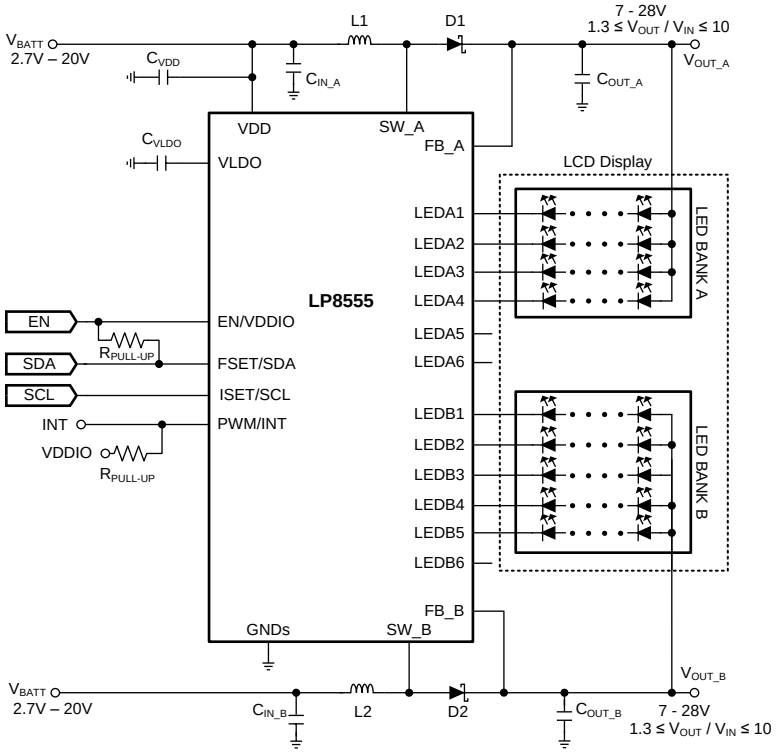


Figure 2-3. Application Example With Different LED Configurations on Each Bank

3.1 Connectors and Main Components On Board

Figure 3-1 shows connectors and main components on the board. Note that all jumpers are disconnected in this example picture; in typical use case jumpers must be set based on requirements.

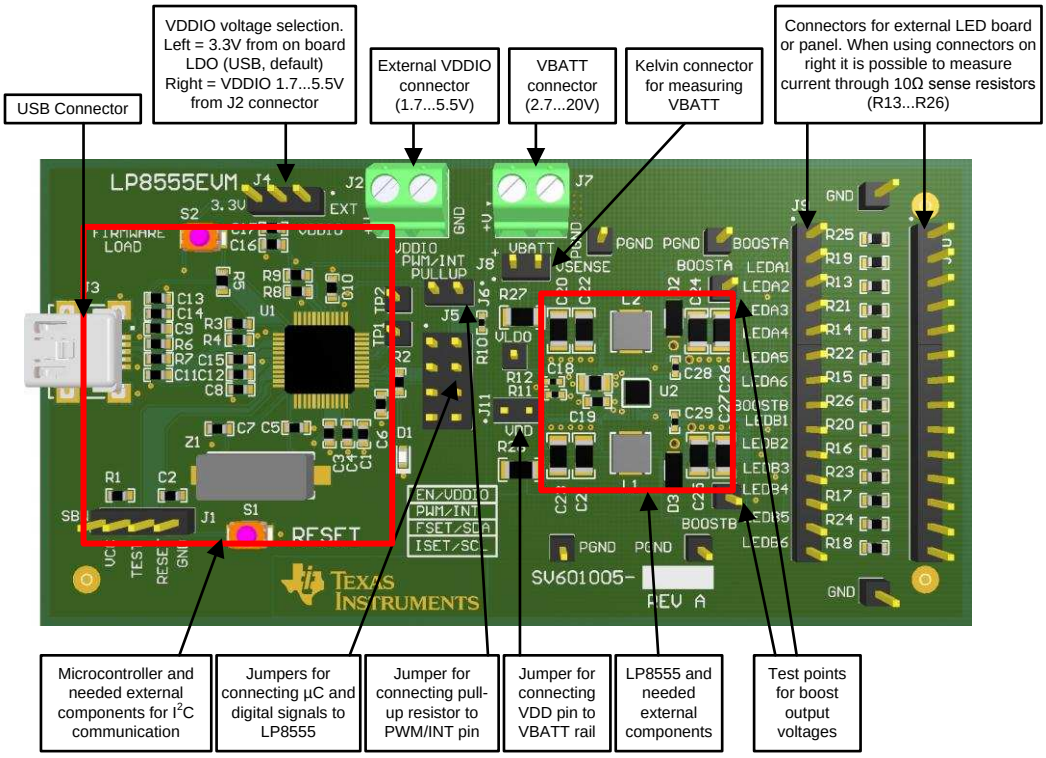


Figure 3-1. Evaluation Board Connectors and Setup

3.2 Power Supply

The device is designed to operate from an input voltage supply range between 2.7 V and 20 V. This input supply should be well regulated and able to withstand maximum input current and maintain stable voltage without voltage drop even at load transition condition (start-up or rapid brightness change). The resistance of the input supply rail should be low enough that the input current transient does not cause large enough drop in the LP8555 supply voltage that can cause false UVLO fault triggering. If the input supply is located more than a few inches from the LP8555, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. Depending on device EPROM configuration and usage case the boost converter is configured to operate optimally with certain input voltage range. Examples are seen in the Detailed Design Procedures in the LP8555 Datasheet. In applications other than that illustrated before, contacting your TI Sales Representative is recommended for confirmation of the compatibility of the use case, EPROM configuration, and input voltage range.

Board Layout

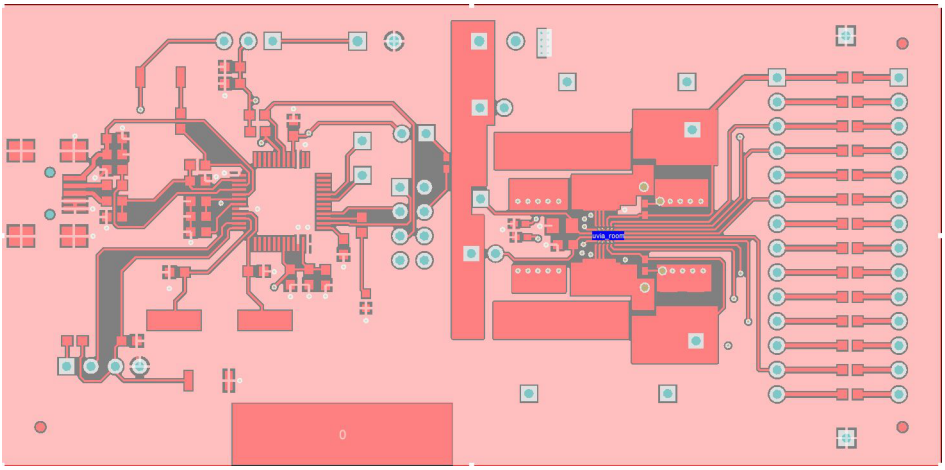


Figure 4-1. Layer 1 Top (Signal). Light Red Color = Top Copper Pour, Connected to GND

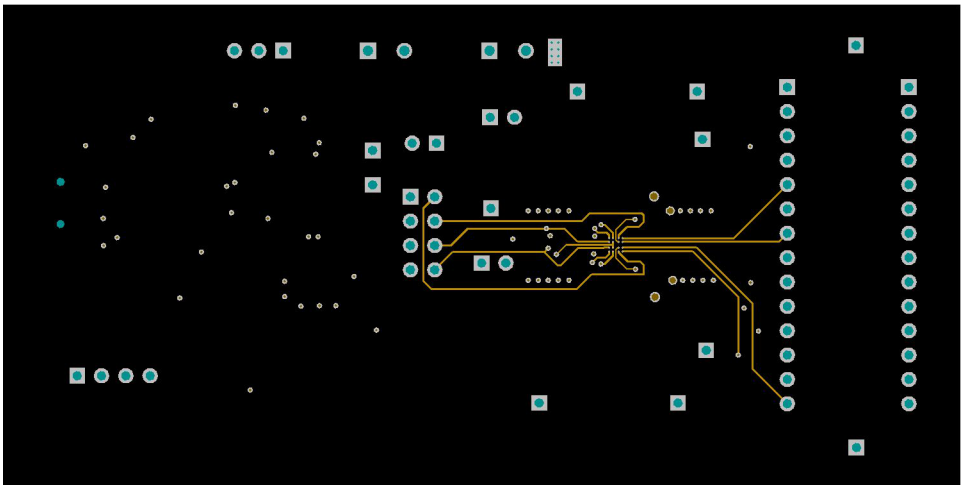


Figure 4-2. Layer 2 (GND / Signal)

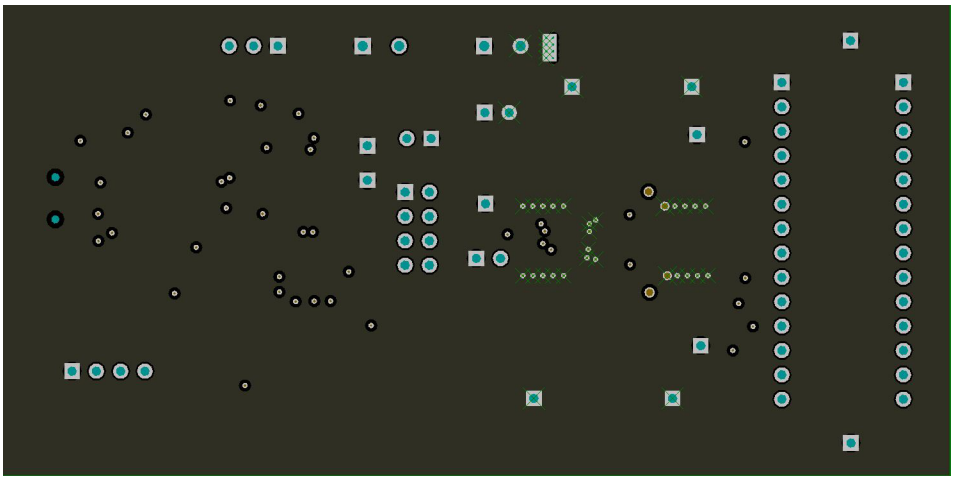


Figure 4-3. Layer 3 (PGND)

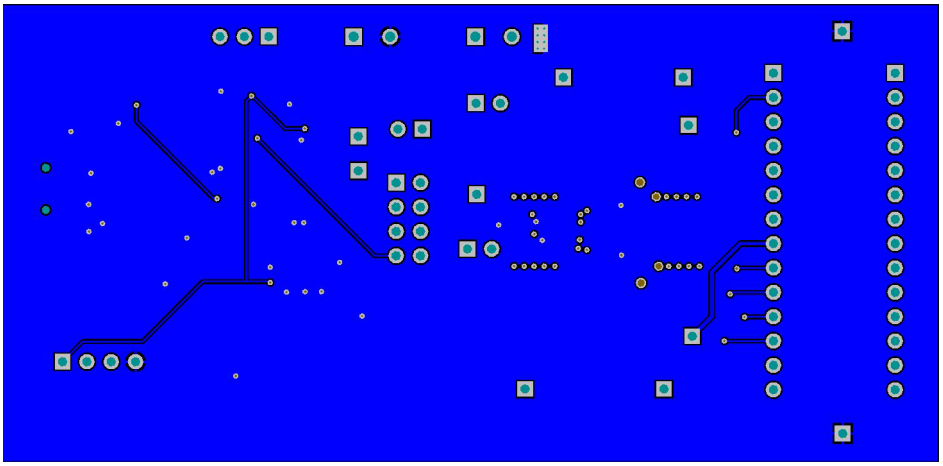


Figure 4-4. Layer 4 Bottom (Signal/GND Pour)

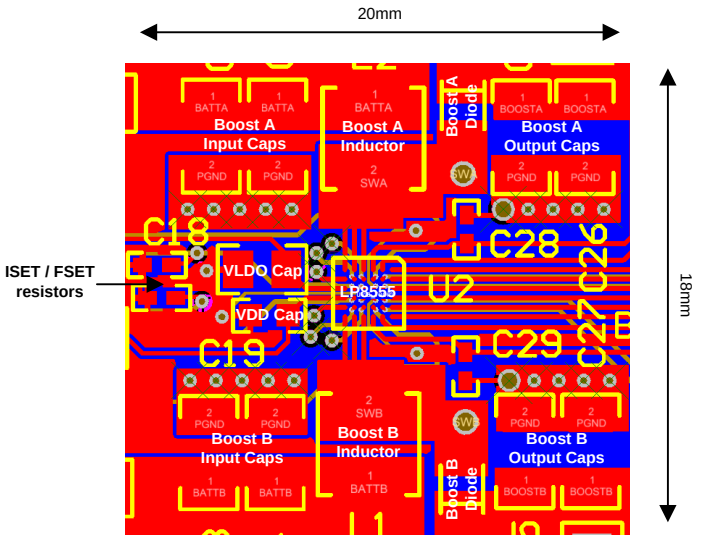


Figure 4-5. Close-up of the LP8555 and Main External Components Layout

Board Stackup

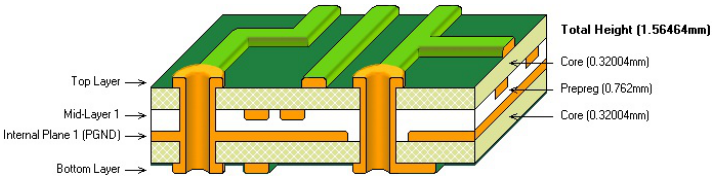


Figure 5-1. Evaluation Board Stackup

Details:

- 4-layer board FR4
- Top layer 1 - copper 35 µm
- Core 0.32 mm
- Internal Layer 2 - 18 µm
- Prepreg 0.762 mm
- Power Ground plane Layer 3 - 18 µm
- Core 0.32 mm
- Bottom Layer 4 - copper 35 µm
- MicroVias (between layers 1 and 2) filled
- Surface finish immersion gold

Power Sequences

The LP8555 has a dual-function EN/VDDIO terminal. It acts as enable for the chip as well as the supply/reference voltage for IO logic. When VDD voltage is present and above UVLO voltage level (2.6 V typ.), the device will start when the EN/VDDIO voltage is set above high threshold voltage (1.7 V typ.).

6.1 Start-up and Shutdown Sequences

Depending on brightness control mode the LP8555 can be started up and shut down differently. Below are explained typical start-up/shutdown sequences with corresponding timings for operation states. Diagrams have more details and illustrated waveforms for typical usage cases.

6.1.1 Start-up with PWM Input Brightness Control Mode (BRTMODE = 00b)

When VDD and EN/VDDIO are above min operational value, the LP8555 enters start-up mode. During start-up mode, an LDO is started, and EPROM values are loaded to registers. I^2C is available after the start-up sequence has ended.

In standby mode the device waits for the ON bit to go high to start the boost start-up sequence. Also, in standby mode the PWM input duty cycle measurement is active.

Once the ON bit is set to 1 (it can be also programmed to 1 by default in EPROM and no I^2C write is then needed for entering active mode), boost is started, and the device enters active mode with brightness set by PWM input duty cycle. If no brightness is set, the backlight stays off until two PWM pulses are received in the PWM input, or if PWM input is set high for more than 1/75 Hz (typ.) time. Boost starts initially to the level to the level set in VINIT registers, and after backlight is turned on, the adaptive control adjusts the voltage to get to the minimal headroom voltage.

6.1.2 Shutdown with PWM Input Brightness Control Mode (BRTMODE = 00b)

The backlight can be turned off by setting PWM input low or by writing ON bit low. After a 1/75 Hz timeout period in PWM input the backlight slopes down (if slope is enabled), and the boost is returned to the initial voltage level programmed to the EPROM. If the backlight is shut down with the ON bit, it shuts down immediately even if slopes are enabled and boost turns off as well. To enter standby mode where boost is disabled and the power consumption is minimal, the ON bit must be written to 0. If the PWMSB bit has been programmed to 1, the LP8555 enters standby mode when PWM input has been low for more than 50 ms even if the ON bit is high.

The device shuts down completely by setting EN/VDDIO and/or VDD to low state.

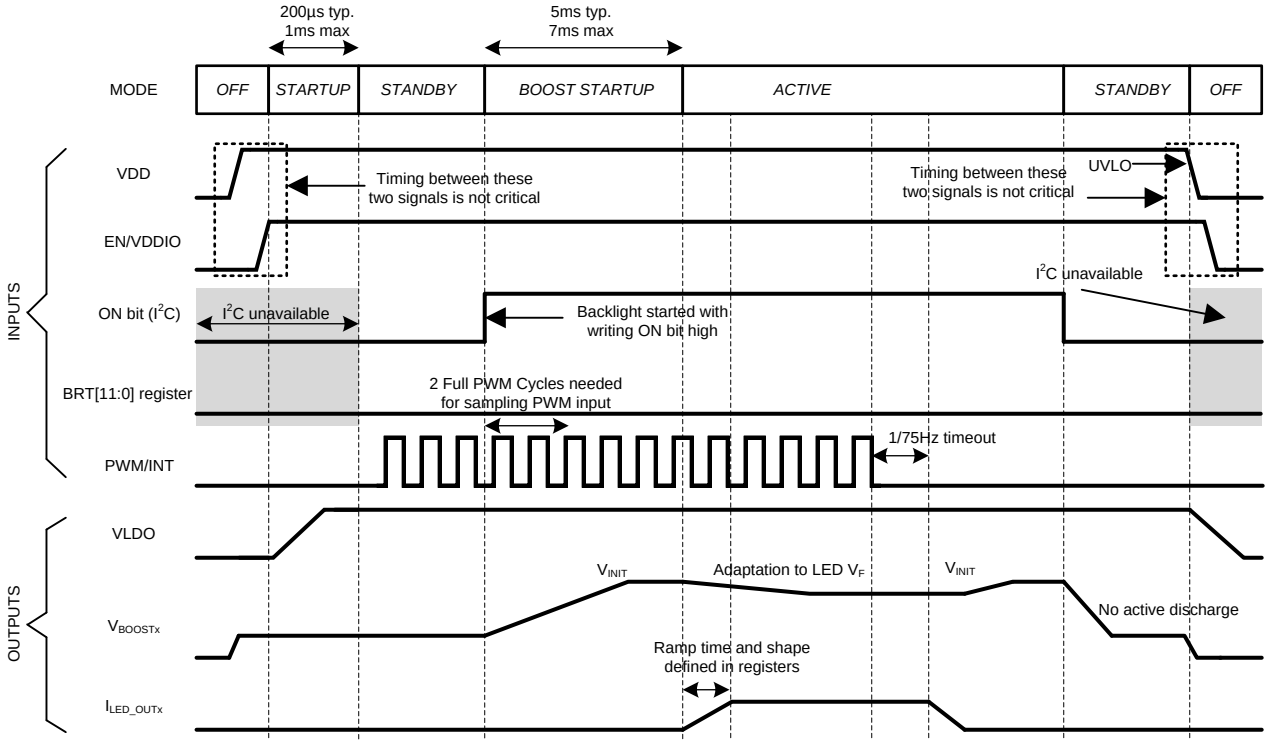


Figure 6-1. Start-up and Shutdown with PWM Input Control, ON bit = 0 in EPROM

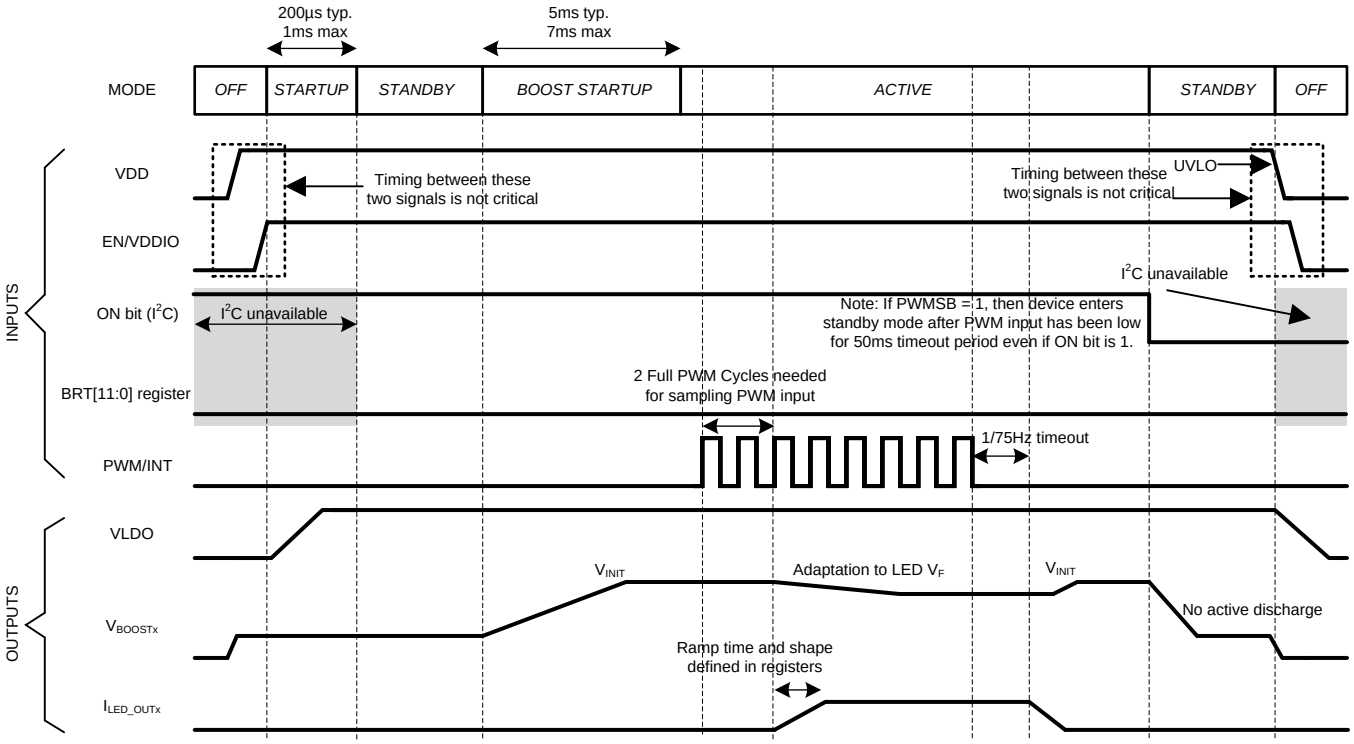


Figure 6-2. Start-up and Shutdown with PWM Input Control, ON bit = 1 in EPROM

6.1.3 Start-up with I²C Brightness Control Mode (BRTMODE = 01b)

When VDD and EN/VDDIO are above min operational value the LP8555 enters start-up mode. During start-up mode an LDO is started, and EPROM values are read. I²C is available after the start-up sequence has ended.

In standby mode the device waits for the ON bit to go high to start the boost start-up sequence. Also, in standby mode I²C is active, and brightness or other configuration registers can be written.

Once the ON bit is set to 1 (it can be also programmed to 1 by default in EPROM and no I²C write is then needed for entering active mode), boost is started, and device enters active mode with brightness set by I²C brightness registers. If no brightness is set, the backlight stays off until the brightness value is written to the I²C register(s). Boosts starts initially to the level set in VINIT registers, and after backlight is turned on, the adaptive control adjusts the voltage to get to the minimal headroom voltage.

6.1.4 Shutdown with I²C Brightness Control Mode (BRTMODE = 01b)

The backlight can be turned off by setting the ON bit low, or by writing brightness to 0. The backlight shuts down immediately if the ON bit is written low even if slope is enabled. If backlight is turned off by writing brightness to 0, brightness control does slope (if enabled), and the boost is returned to the initial voltage level programmed to EPROM. To enter standby mode where boost is disabled and the power consumption is minimal, the ON bit must be written to 0.

The device shuts down completely by setting EN/VDDIO and/or VDD to low state.

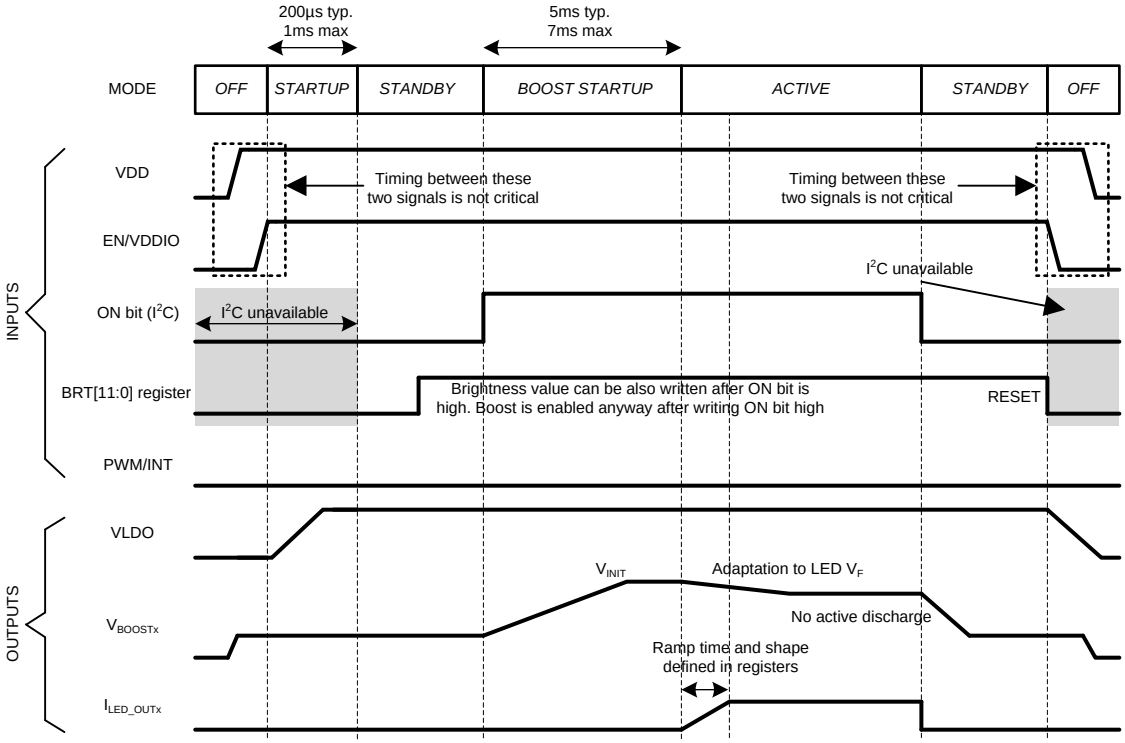


Figure 6-3. Start-up and Shutdown with I²C Brightness Control Mode

6.1.5 Start-up with I²C + PWM Input Brightness Control Mode (BRTMODE = 10 or 11b)

When VDD and EN/VDDIO are above min operational value, the LP8555 enters start-up mode. During start-up mode an LDO is started, and EPROM values are read. I²C is available after the start-up sequence has ended.

In standby mode the LP8555 waits for the ON bit to go high to start the boost start-up sequence. Also, in standby mode I²C registers can be written and PWM input duty cycle measurement is active.

Once the ON bit is set to 1 (it can be also programmed to 1 by default in EPROM and no I²C write is then needed for entering active mode), boost is started, and device enters active mode with brightness set by the PWM input duty cycle multiplied by I²C brightness register value. If no brightness is set, backlight stays off until I²C brightness register receives value and two PWM pulses are received in the PWM input, or if PWM input is set high for more than 1/75Hz time. Boost starts initially to the level to the level set in VINIT registers, and after backlight is turned on, the adaptive control adjusts the voltage to get to the minimal headroom voltage.

6.1.6 Shutdown with I²C + PWM Input Brightness Control Mode (BRTMODE = 10 or 11b)

The backlight can be turned off by setting ON bit low, or by setting brightness to 0 either by PWM input (same 1/75Hz timeout applies here as in PWM input control mode) or by I²C brightness register writes. The backlight shuts down immediately if the ON bit is written low, even if slope is enabled. If the backlight is turned off by setting brightness to 0, brightness control does slope (if enabled, depending on which input is used – see Brightness Control Modes in datasheet for details), and the boost is returned to the initial voltage level programmed to EPROM. To enter standby mode where boost is disabled and the power consumption is minimal, the ON bit must be written to 0.

The device shuts down completely by setting EN/VDDIO and/or VDD to low state.

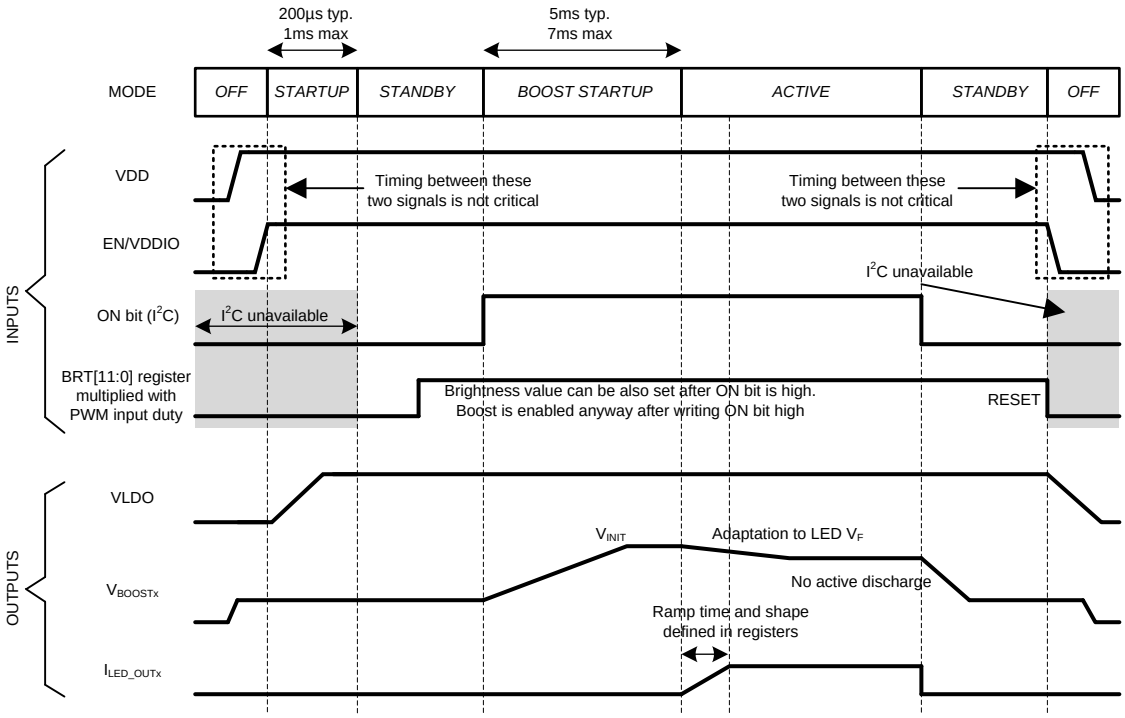
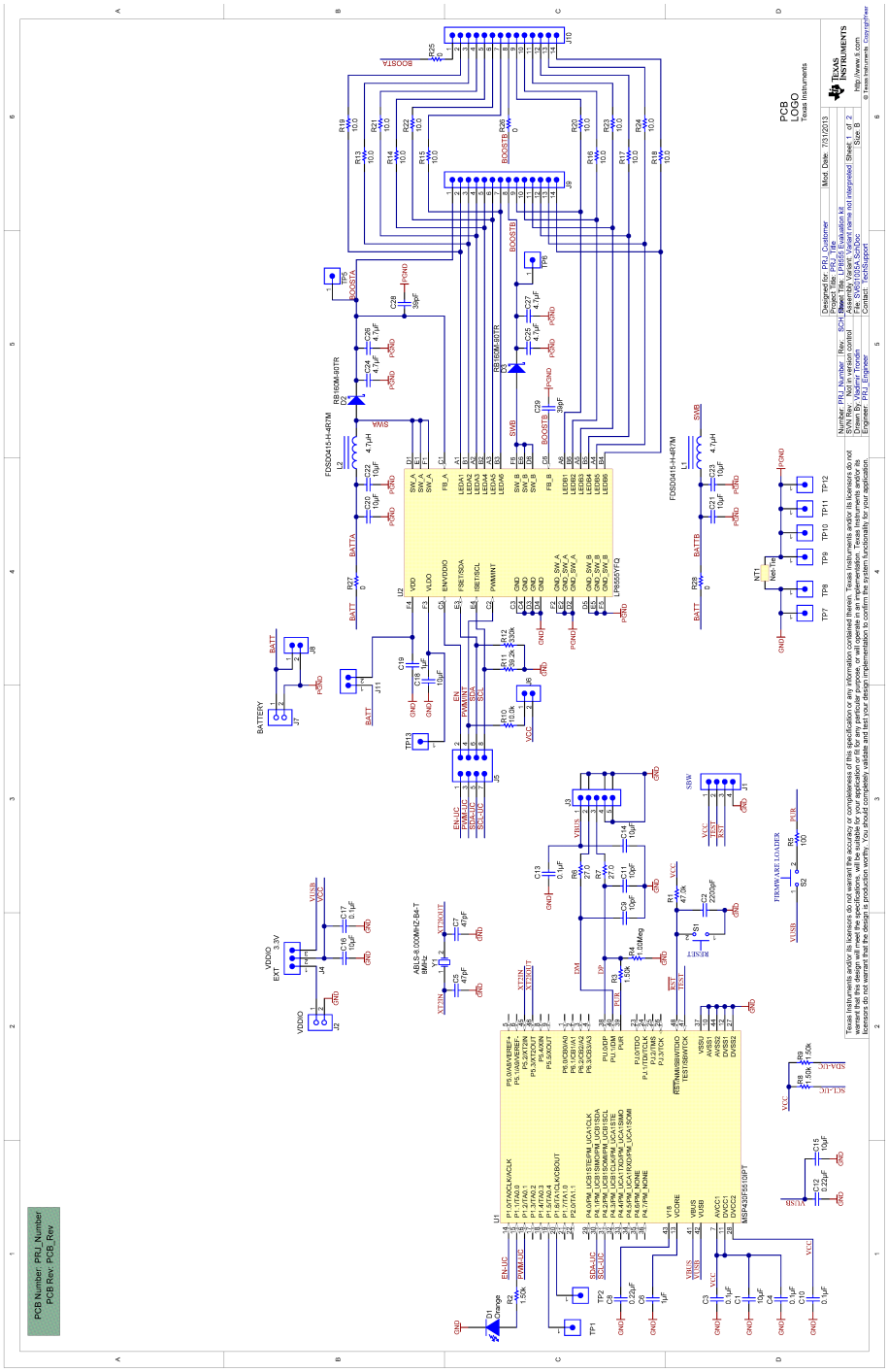


Figure 6-4. Start-up and Shutdown with I²C + PWM Input Brightness Control

Evaluation Board Schematic



Bill of Materials

The following is the bill of materials for the LP8555EVM:

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY.
PCB	Printed Circuit Board	Any	SV601005	1
C1, C14, C15, C16	CAP, CERM, 10uF, 10V, ±10%, C0G/NP0, 0603	TDK	C1608X5R1A106M	4
C2	CAP, CERM, 2200pF, 100V, ±5%, X7R, 0603	AVX	06031C222JAT2A	1
C3, C4, C10, C13, C17	CAP, CERM, 0.1uF, 50V, ±10%, X7R, 0603	MuRata	GRM188R71H104KA93D	5
C5, C7	CAP, CERM, 47pF, 100V, ±5%, C0G/NP0, 0603	MuRata	GRM1885C2A470JA01D	2
C6, C19	CAP, CERM, 1uF, 25V, ±10%, X7R, 0603	MuRata	GRM188R71E105KA12D	2
C8, C12	CAP, CERM, 0.22uF, 16V, ±10%, X7R, 0603	TDK	C1608X7R1C224K	2
C9, C11	CAP, CERM, 10pF, 50V, ±5%, C0G/NP0, 0603	TDK	C1608C0G1H100D	2
C18	CAP, CERM, 10uF, 10V, ±10%, X5R, 0805	MuRata	GRM21BR61A106KE19L	1
C20, C21, C22, C23	CAP, CERM, 10uF, 25V, ±10%, X7R, 1206	MuRata	GRM31CR71E106KA12L	4
C24, C25, C26, C27	CAP, CERM, 4.7uF, 50V, ±10%, X5R, 1206	MuRata	GRM319R61H475KA12	4
C28, C29	CAP, CERM, 39pF, 50V, ±5%, C0G/NP0, 0402	MuRata	GRM1555C1H390JA01D	2
D1	LED, Orange, SMD	Lite-On	LTST-C190KFKT	1
D2, D3	Diode Schottky, 90V, 1A	Rohm Semiconductor	RB160M-90TR	2
J1	Header, TH, 100mil, 4x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-104-07-G-S	1
J2, J7	Conn Term Block, 2POS, 3.81mm, TH	Phoenix Contact	1727010	2
J3	Conn Rcpt Mini USB2.0 Type B 5POS SMD	TE Connectivity	1734035-2	1
J4	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-103-07-G-S	1
J5	Header, TH, 100mil, 4x2, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-104-07-G-D	1
J6, J8, J11	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-102-07-G-S	3
J9, J10	Header, TH, 100mil, 14x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-114-07-G-S	2
L1, L2	Inductor, Shielded, 4.7uH, 2.1A, 0.1 ohm, SMD	Toko	FDSD0415-H-4R7M	2
R1	RES, 47.0k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-0747KL	1
R2, R3, R8, R9	RES, 1.50k ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-071K5L	4
R4	RES, 1.00Meg ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031M00FKEA	1
R5	RES, 100 ohm, 1%, 0.1W, 0603	Yageo America	RC0603FR-07100RL	1

DESIGNATOR	DESCRIPTION	MANUFACTURER	PART NUMBER	QTY.
R6, R7	RES, 27 ohm, 5%, 0.1W, 0603	Yageo America	RC0603FR-0727RL	2
R10	RES, 10.0k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040210K0FKED	1
R11	RES, 39.2k ohm, 1%, 0.063W, 0402	Vishay-Dale	CRCW040239K2FKED	1
R12	RES, 330k ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW0402330KJNED	1
R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24	RES, 10.0 ohm, 0.1%, 0.1W, 0603	Yageo America	RT0603BRD0710RL	12
R25, R26	RES, 0 ohm, 5%, 0.1W, 0603	Panasonic	ERJ-3GEY0R00V	2
R27, R28	RES, 0 ohm, 5%, 0.25W, 1206	Vishay-Dale	CRCW12060000Z0EA	2
S1, S2	Switch, Push Button, SMD	Alps	SKRKAEE010	2
TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13	Header, TH, 100mil, 1pos, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-101-07-G-S	9
U1		Texas Instruments	MSP430F5510IPTR	1
U2	High-efficiency LED Backlight Driver for Tablet PCs, YFQ0036AEAE	Texas Instruments	LP8555YFQR	1
Y1	Crystal, 8.000MHz, 18pF, SMD	Abracon Corporation	ABLS-8.000MHZ-B4-T	1

Evaluation Software

9.1 Setup

The LP8555 EVM is connected via USB to the computer. The EVM is controlled with special evaluation software (Windows™). An MSP430 microcontroller (µC) is used with the EVM to provide easy I^2C communication, external PWM control, and EN/VDDIO-terminal control with the LP8555 via USB. The EVM board µC and LP8555 VDDIO are powered by default via USB. VDD for LP8555 must be supplied with external power supply with a high enough current limit.

When the board is connected to a computer, Windows should recognize it automatically and start to install the driver. A “Found New Hardware” dialog box will prompt user to locate the missing driver. Select “No, not this time” and continue with “Next”. Select “Install from a list or specific location (Advanced)” to install the driver. Select the directory where the supplied TI_CDC_Virtual_Port driver is located. Windows should now install the driver, and the PC can then communicate with the EVM using a virtual COM port. If Windows cannot find the driver, the TI_CDC_Virtual_Port driver needs to be manually installed from the Device Manager. There should be a "USB OK" message on the status bar at the bottom of evaluation program, and the red LED should blink on the EVM when the board is recognized. If the board is not recognized, check the USB address from the Windows Control Panel. The USB address should always be less than or equal to 9 (from COM1 to COM9) (see Appendix A). Also switching to another USB port might solve the issue.

I^2C/PWM/EN communication can be controlled from an external source using pin headers on the EVM if needed. The test point for all of the signals is provided, but jumpers to the on-board µC must be removed if external source is used for control.

9.2 Usage

The LP8555 evaluation software helps user to control the evaluation hardware connected to the computer. The evaluation software consists of three sections: tab selection, register selection, and register control section. In the tab selection user can switch between the Pin Control, Brightness Control, LED Driver Control, Boost Control, Other, and History tabs. In the left-hand side of the evaluation program, the register view (see Figure 9-1) is always visible. From this view the user can see the register addresses, register names, and register values. The user can select the register that needs to be changed. The selected register is marked with a red X beside the register value. When the user selects the register, the selected register can be viewed in detail at the bottom of the evaluation software. This view tells the register address, register name, register default value, register bits, and current register value. The user can also read and write the register bits by pushing the RD-button (read) and WR-button (write).

In the **File** menu the user can save register settings to a file, or load ready-made register setups from a file to the LP8555 registers.

In the **Operation** menu the user can read register settings with 'Read Registers' from the LP8555 memory so that the GUI reflects the current state of the LP8555. 'Execute Macro' allows running sequence of register writes from file. In 'Direct control' the user can manually control registers by selecting address and data in hex format.

9.2.1 Pin Control Tab

From the "Pin Control" tab (see Figure 9-1) the user can control all the basic functions of the EVM, such as EN/VDDIO pin control, PWM input generation and I^2C interface settings:

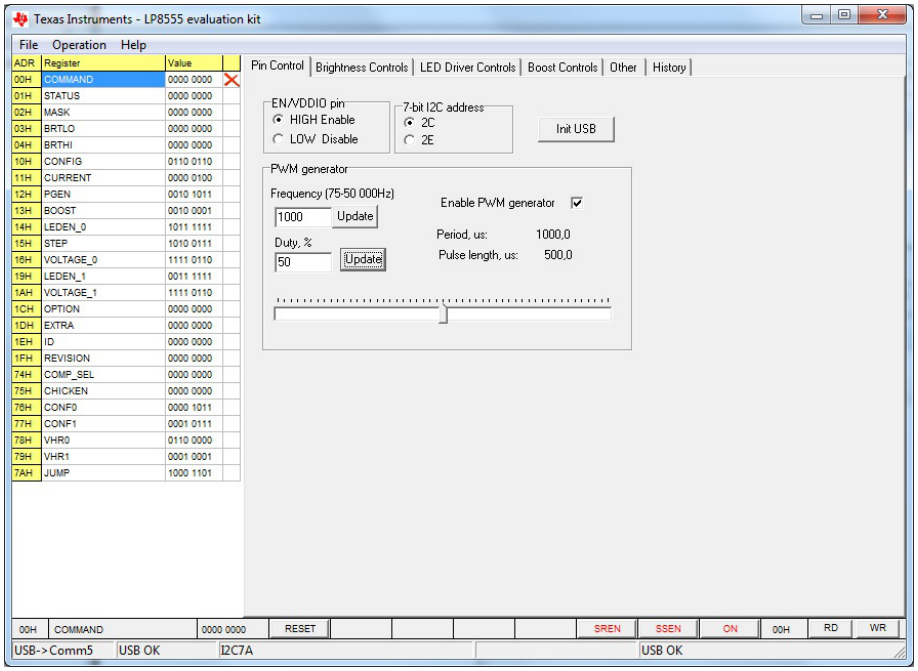


Figure 9-1. Main Window and Pin Control Tab

9.2.2 Brightness Controls Tab

From the "Brightness Controls" tab (see Figure 9-2) the user can control all the brightness control functions of the device. Note that Backlight Enable must be set to 0 to be able to change settings. Brightness can be changed any time.

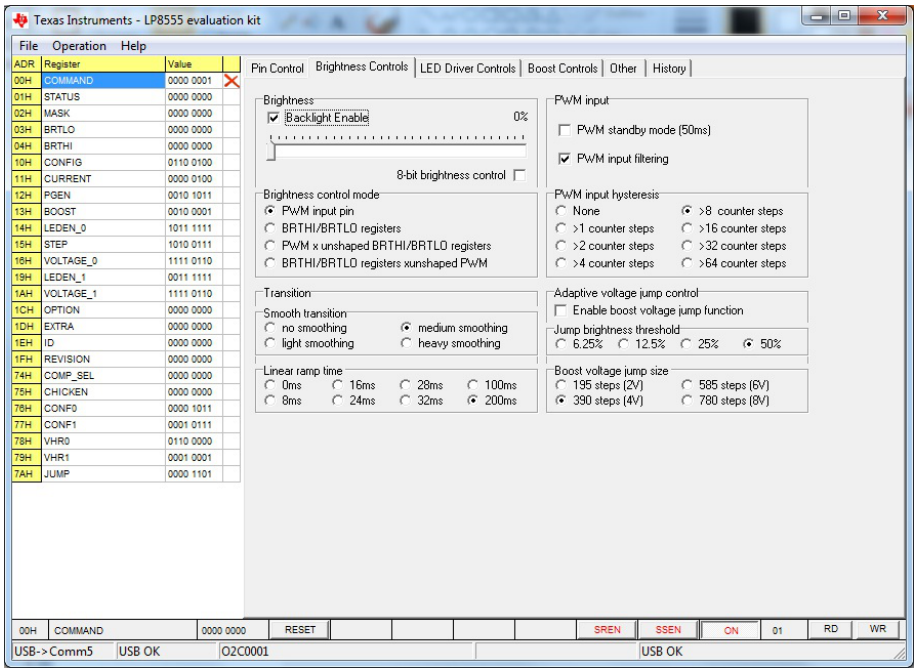


Figure 9-2. Brightness Controls Tab

9.2.3 LED Driver Controls Tab

From the "LED Driver Controls" tab (see Figure 9-3) the user can control all LED drivers of the device, such as LED Current, PWM frequency/mode, and number of strings. Note: backlight must be disabled to be able to change settings.

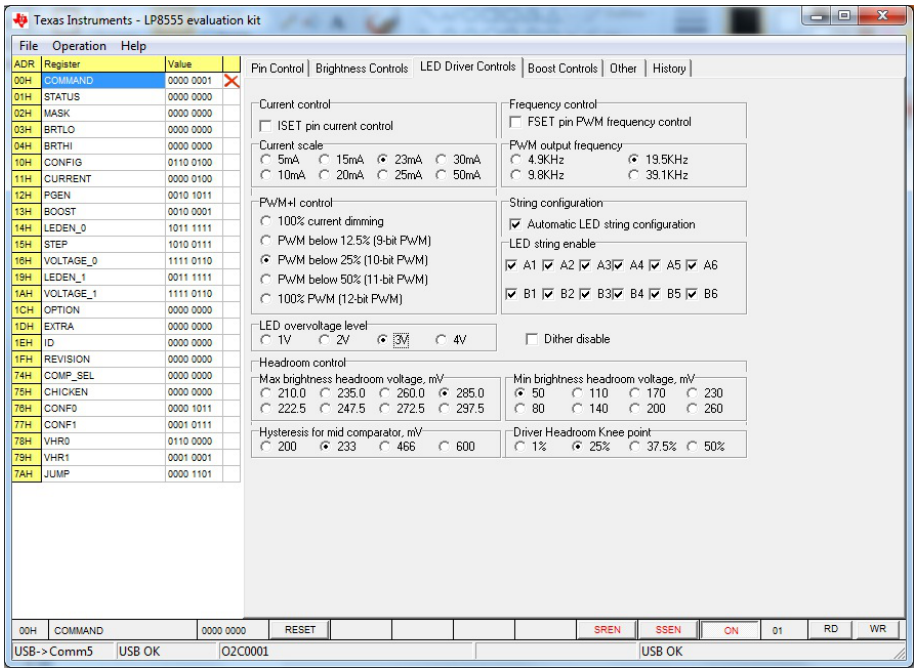


Figure 9-3. LED Driver Controls Tab

9.2.4 Boost Controls Tab

From the "Boost Controls" tab (see Figure 9-4) the user can control all the boost functions of the device, such as boost inductor current limit, initial voltage, and spread spectrum settings. Note: Backlight Enable must be set to 0 to be able to change settings. Although it is possible to change boost frequency with I^2C write to register, the frequency is not set precisely to correct value. To get accurate 500 kHz or 1 MHz it must be pre-programmed to EPROM in TI production line.

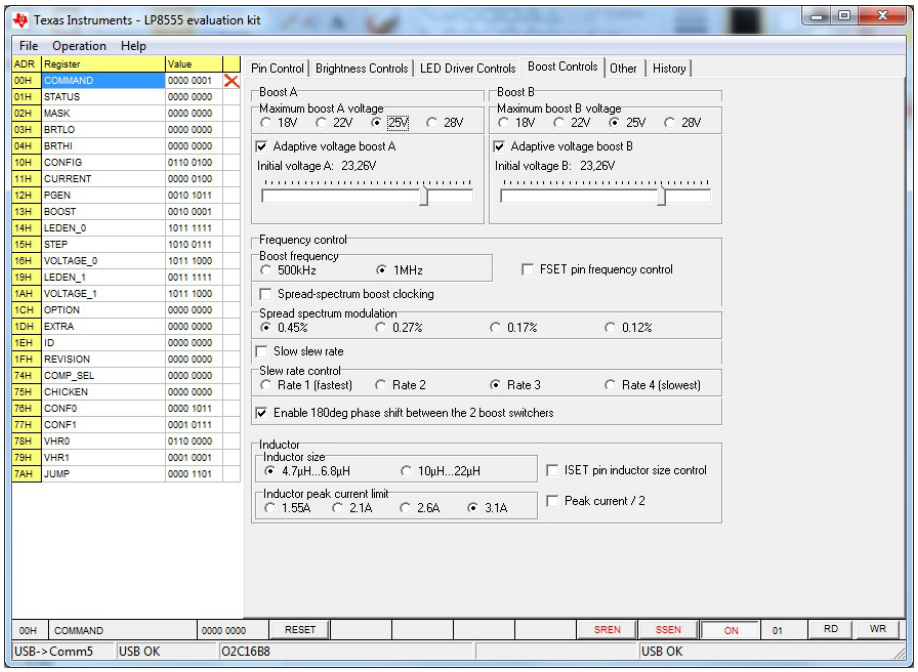


Figure 9-4. Boost Controls Tab

9.2.5 Other Tab

From the "Other" tab (see Figure 9-5) the user can control EPROM start-up behavior, ID, and status registers.

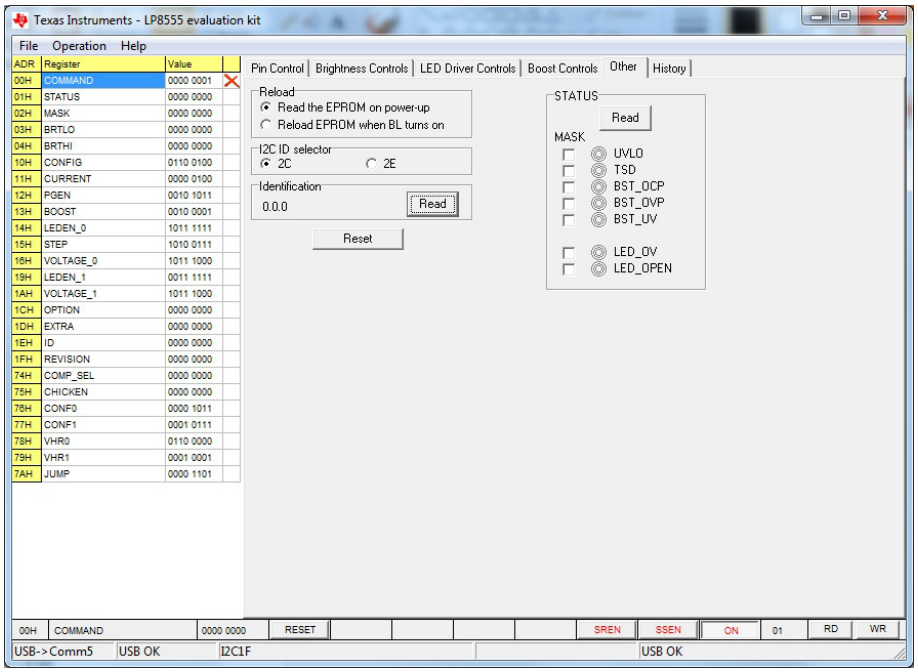


Figure 9-5. Other Tab

9.2.6 History Tab

The "History" tab (see Figure 9-6) provides information on the I²C writes used to configure/control the LP8555 device. This is a good way of finding out what writes/reads have been done. This can be used as a reference for developing software for real application.

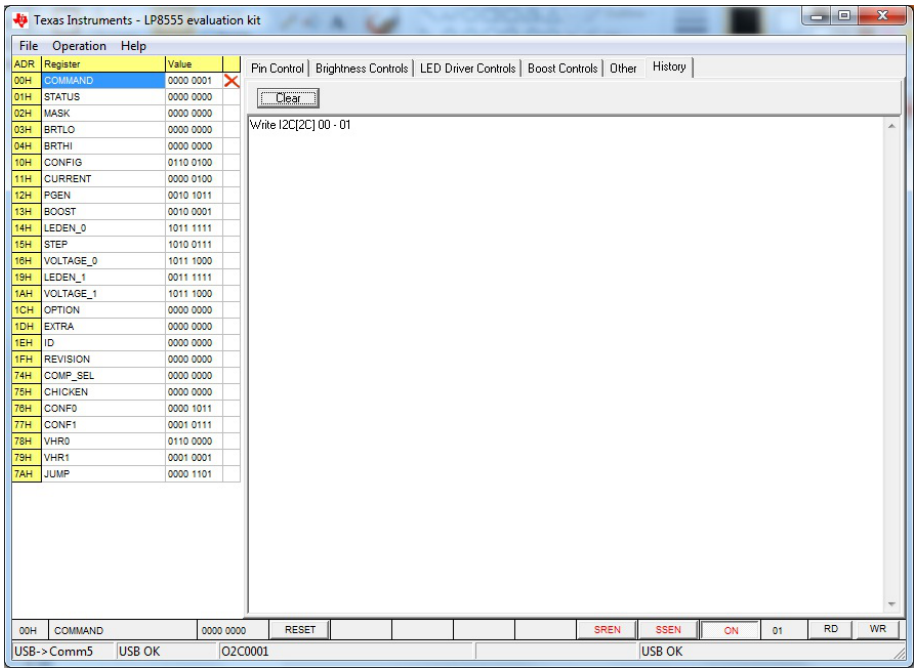


Figure 9-6. History Tab

LP8555 Programming Considerations

10.1 Register Maps

Register	Addr	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND	00h	RESET					SREN	SSEN	ON
STATUS	01h	LED_OPEN	LED_OV		BST_UV	BST_OVP	BST_OCP	TSD	UVLO
MASK	02h	LED_OPEN	LED_OV		BST_UV	BST_OVP	BST_OCP	TSD	UVLO
BRTLO	03h	BRT[3:0]							
BRTHI	04h	BRT[11:4]							
CONFIG	10h	PWMSB	PWMFILT	EN_BPHASE180		RELOAD	AUTO	BRTMODE	
CURRENT	11h	ISET					MAXCURR		
PGEN	12h	PFSET		THRESHOLD			PFREQ		
BOOST	13h							BIND	BFREQ
LEDEN_0	14h	OV		ENABLE_0					
STEP	15h	SMOOTH		PWM_IN_HYST			STEP		
VOLTAGE_0	16h	VMAX_0		ADAPT_0	VINIT_0				
LEDEN_1	19h			ENABLE_1					
VOLTAGE_1	1Ah	VMAX_1		ADAPT_1	VINIT_1				
OPTION	1Ch					OPTION			
EXTRA	1Dh	EXTRA							
ID	1Eh	ID_CUST				ID_CFG			
REVISION	1Fh	MAJOR				MINOR			
CONF0	76h	BOOST_IS_DIV2			ALTID	SRON		CURR_LIMIT	
CONF1	77h	FMOD_DIV							
VHR0	78h		VHR_SLOPE				VHR_VERT		
VHR1	79h			VHR_HYST				VHR_HORZ	
JUMP	7Ah	JEN				JTHR		JVOLT	

Some register fields are loaded from an internal EPROM (shaded above). This EPROM is programmed by TI during final test. This allows default values to be assigned. This feature is intended for applications where the I^2C interface is not used. With the exception of the ID fields, most EPROM based fields can be written via I^2C writes like a normal register field. There are limitations on certain configuration bits, their operation and can they be changed "on-the-fly". It is noted in the description of corresponding bit.

There is a restriction on register writes. The COMMAND, MASK, BRTLO, and BRTHI registers can be written at any time; however, the remaining registers will only accept writes when the COMMAND.ON bit is low. All registers can be read at any time.

Many registers contain empty bit locations. These blank areas are reserved for future use. As a general rule, when writing to a register any empty fields should be set to what ever value is read back from them and they should not be changed.

Default EPROM values are listed in datasheet.

10.1.1 COMMAND

Address: 0x00

D7	D6	D5	D4	D3	D2	D1	D0
RESET	—				SREN	SSEN	ON

Bits	Field	Type	Description
7	RESET	R/W	Write 1 to reset the device. This bit is self-cleaning and will always be 0 when read.
6:3	reserved	R/O	
2	SREN	R/W	0 = Slew rate limited disabled 1 = Enable slower boost gate drive slew rate. Reduces EMI energy in high frequencies and reduces boost efficiency.
1	SSEN	R/W	0 = Spread Spectrum Scheme disabled 1 = Enable spread-spectrum boost clocking. Spreads EMI spectrum spikes.
0	ON	R/W	Turn on the backlight. 0 = backlight off 1 = backlight on

The COMMAND.ON bit must be programmed to 1 in the EPROM for applications without I^2C access to the device. The COMMAND.SSEN bit may be updated at any time. It is not necessary for the backlight to be off when changing COMMAND.SSEN and/or COMMAND.SREN.

10.1.2 STATUS/MASK

Address: 0x01/0x02

D7	D6	D5	D4	D3	D2	D1	D0
DRV_FAULT	DRV_OV	—	BST_UV	BST_OVP	BST_OCP	TSD	UVLO

Bits	Field	Type	Description
7	LED_OPEN	R/O	An open/short condition was detected on one or more LED strings. Once set this bit will stay set until the STATUS register is read. An LED open/short condition will turn off the backlight when CONFIG.AUTO is 0.
6	LED_OV	R/O	An over-voltage condition was detected on one or more LED strings. Once set this bit will stay set until the STATUS register is read.
5	reserved	R/O	
4	BST_UV	R/O	The boost reported an under-voltage condition. Once set this bit will stay set until the STATUS register is read.
3	BST_OVP	R/O	The boost reported an over-voltage protection condition when the maximum allowed voltage is requested. Once set this bit will stay set until the STATUS register is read.
2	BST_OCP	R/O	The boost reported an under-voltage condition longer than 50 ms in time when the backlight on.
1	TSD	R/O	A thermal shutdown condition was detected. Once set this bit will stay set until the STATUS register is read. A thermal shutdown condition will turn off the backlight.
0	UVLO	R/O	An under-voltage lockout condition was detected. Once set this bit will stay set until the STATUS register is read. An under-voltage lockout condition will turn off the backlight.

Each fault bit of the STATUS register has a corresponding bit in the MASK register, which enables interrupts for the fault. For example, an interrupt will occur if the MASK.BST_UV and STATUS.BST_UV bits are both set. If a fault bit is cleared in the MASK register then that fault will not trigger an interrupt.

10.1.3 BRTLO

Address: 0x03

D7	D6	D5	D4	D3	D2	D1	D0
BRT[3:0]				—			

Bits	Field	Type	Description
7:4	BRT[3:0]	R/W	Least significant bits of the brightness level.
3:0	reserved	R/O	

10.1.4 BTHI

Address: 0x04

D7	D6	D5	D4	D3	D2	D1	D0
BRT[11:4]							

Bits	Field	Type	Description
7:0	BRT[11:4]	R/W	Most significant bits of the brightness level.

The brightness level can be updated with 8-bit precision or 12-bit precision. To make brightness level updates effective the internal brightness level is only updated when the BRTHI register is written. If the BRTHI register is written without a previous write to the BRTLO register, then the lower 4 bits of the internal 12-bit brightness will be synthesized from the BRTHI register value.

BRTLO	BRTHI	Brightness	Comments
write 0x95	write 0xFC	0xFC9	BRTLO[3:0] is ignored
write 0x10	write 0xDC	0xDC1	set to an exact 12-bit value
no write	write 0x8C	0x8C8	synthesize low order bits
no write	write 0x0C	0x0C0	synthesize low order bits
no write	write 0x00	0x000	0% brightness
no write	write 0xFF	0xFFF	100% brightness

10.1.5 CONFIG

Address: 0x10

D7	D6	D5	D4	D3	D2	D1	D0
PWMSB	PWMFILT	EN_BPHASE180	—	RELOAD	AUTO	BRTMODE	

Bits	Field	Type	Description
7	PWMSB	R/W	Enables PWM standby mode 0 = CONTROL.ON alone turns the backlight on/off 1 = turn off the backlight after 50 ms of PWM low
6	PWMFILT	R/W	0 = PWM input filter disabled 1 = Enable 50 ns glitch filter on PWM input.
5	EN_BPHASE180	R/W	0 = Boosts operate in same phase 1 = Enable 180° phase shift between the 2 boost switchers.
4	reserved	R/O	
3	RELOAD	R/W	Automatically re-read the EPROM at each turn-on. 0 = only read the EPROM upon power-up 1 = re-read the EPROM when the backlight turns on
2	AUTO	R/W	Automatic LED string configuration 0 = enable LED strings using just LEDEN.ENABLE 1 = disable all open LED strings
1:0	BRTMODE	R/W	Brightness mode 00 = PWM 01 = BRTHI/BRTLO registers 10 = PWM × unshaped BRTHI/BRTLO registers 11 = BRTHI/BRTLO registers × unshaped PWM

When the AUTO bit is set the LED configuration is done dynamically. When an OPEN/SHORT condition is detected on an LED string it will be removed, and PWM output phasing will be adjusted. Conversely, an LED string will be added back for operation if the LED string is not open.

The BRTMODE field selects how LED brightness is controlled. When BRTMODE is set to 00b the PWM terminal duty cycle controls the LED brightness. When BRTMODE is set to 01b the BRTLO and BRTHI registers will control the LED brightness. When the backlight is turned on the brightness level is reset to 0% and will automatically transition to the brightness value programmed in the BRTLO and BRTHI registers.

When the BRTMODE field is set to 00b, and the PWMSB bit is set to 1, the backlight will be turned off whenever the PWM terminal is held low for 50 ms. This will also put the device into its lowest power state. When the PWM terminal becomes active the backlight will automatically turn back on.

A 50 ns glitch filter will be applied to the PWM input signal when the PWMFILT bit is set to 1. When BRTMODE is set to 10b or 11b the LED brightness is controlled by both the PWM terminal duty cycle and the BRTLO and BRTHI registers.

When BRTMODE is set to 10b the PWM terminal duty cycle is routed through the smoothing function (controlled via the STEP register). The smoothed duty cycle is multiplied with the value from the BRTLO/BRTHI registers. Updates to the BRTLO/BRTHI registers have an immediate effect on the LED brightness, while PWM terminal duty cycle changes may be smoothed.

When BRTMODE is set to 11b the BRTLO/BRTHI register value is routed through the smoothing function. The smoothed brightness level is multiplied with the PWM terminal duty cycle. In this configuration PWM terminal duty cycle changes have an immediate effect on the LED brightness, while BRTLO/BRTHI register changes may be smoothed.

10.1.6 CURRENT

Address: 0x11

D7	D6	D5	D4	D3	D2	D1	D0
ISET	—				MAXCURR		

Bits	Field	Type	Description
7	ISET	R/W	0 = LED maximum current set with MAXCURR bits 1 = Set MAXCURR via the ISET/SCL terminal. This bit should only set to 1 as an EPROM default, writing to this bit "on-the-fly" does not have effect. Resistor values and their corresponding LED current setting is seen in Full-Scale LED Current section in datasheet.
6:3	reserved	R/O	
2:0	MAXCURR	R/W	Full-scale current (100% brightness). 000 = 5 mA 001 = 10 mA 010 = 15 mA 011 = 20 mA 100 = 23 mA 101 = 25 mA 110 = 30 mA 111 = 50 mA

The full-scale current can be configured into two different ways: EPROM or the ISET/SCL terminal. The ISET/SCL terminal resistor is automatically measured during start-up. The CURRENT.ISET bit is used to select between the maximum current value measured from the ISET/SCL terminal and the EPROM value. When the ISET bit is set to 1 the ISET/SCL terminal value is used; otherwise the EPROM value is used. Regardless of EPROM programming, the maximum current can always be configured from I^2C by clearing the CURRENT.ISET bit and configuring the CURRENT.MAXCURR field as needed.

When the CURRENT register is read via I^2C the MAXCURR field will contain the active full-scale current value. To read the EPROM value, the ISET bit must be set to 0. To read the ISET/SCL-terminal resistor value, the ISET bit must be set to 1 during start-up, which means it must be set in EPROM.

If the ISET/SCL terminal is grounded or floating the MAXCURR value will be set to 23 mA if ISET = 1.

10.1.7 PGEN

Address: 0x12

D7	D6	D5	D4	D3	D2	D1	D0
PFSET	—	THRESHOLD			PFREQ		

Bits	Field	Type	Description
7	PFSET	R/W	0 = PWM frequency is set with PFREQ register bits 1 = Set PFREQ via the FSET/SDA terminal. This bit should only be set to 1 as an EPROM default, writing to this bit "on-the-fly" does not have effect. Resistor values and their corresponding frequency settings are seen in Setting PWM Dimming Frequency section in datasheet.
6	reserved	R/O	0
5:3	THRESHOLD	R/W	Adaptive dimming threshold. PWM dimming is used below the threshold and current dimming is used above the threshold. 000 = 100% current dimming 101 = PWM below 25% (10-bit PWM) 111 = 100% PWM (12-bit PWM)
2:0	PFREQ	R/W	PWM output frequency 000 = 4.9 kHz 001 = 9.8 kHz 011 = 19.5 kHz 111 = 39.1 kHz

The output PWM frequency can be configured in two different ways: EPROM or the FSET terminal. The FSET terminal is always automatically measured. The PGEN.PFSET bit is used to select between the PWM frequency value measured from the FSET terminal and the EPROM value. When the PFSET bit is set to 1 the FSET terminal value is used; otherwise the EPROM value is used. Regardless of EPROM programming, the PWM frequency can always be configured from I^2C by clearing the PGEN.PFSET bit and configuring the PGEN.PFREQ field as needed.

Full 12-bit precision is achieved in all adaptive dimming thresholds and PWM output frequencies. When the PGEN register is read via I^2C the PFREQ field will contain the active PWM output frequency value. To read the EPROM value the PFSET bit must be set to 0. To read the R_{FSET} resistor value the PFSET bit must be set to 1.

If the FSET terminal is grounded or floating the PFREQ value will be set to 19.5 kHz.

10.1.8 BOOST

Address: 0x13

D7	D6	D5	D4	D3	D2	D1	D0
—		—		—		BIND	BFREQ

Bits	Field	Type	Description
7:6	reserved	R/W	
5:4	reserved	R/W	
3:2	reserved	R/W	
1	BIND	R/W	BIND bit is used to set boost inductor size. 0 = 4.7 µH … 6.8 µH 1 = 10 µH … 22 µH
0	BFREQ	R/W	Boost frequency (typical). This setting must be configured in EPROM, changing it with I^2C register write does not have desired effect. 0 = 500 kHz 1 = 1 MHz

10.1.9 LEDEN

Address: 0x14

D7	D6	D5	D4	D3	D2	D1	D0
OV		ENABLE[6:1]					

Bits	Field	Type	Description
7:6	OV	R/W	Set LED over-voltage level. 00 = 1 V 01 = 2 V 10 = 3 V 11 = 4 V
5:0	ENABLE	R/W	LED string enables for Bank A.

The ENABLE field configures the enabled LED strings. If the CONFIG.AUTO bit is 0 these LED strings will stay active when the backlight is on. If the CONFIG.AUTO bit is set, then an LED open/short condition will cause that LED string to be removed. A given LED string will never be enabled if the corresponding bit of the ENABLE field is set to 0. The OV field configures the threshold for detecting an LED overvoltage condition; which may occur when one or more LEDs are bypassed (shorted) within an LED string.

10.1.10 STEP

Address: 0x15

D7	D6	D5	D4	D3	D2	D1	D0
SMOOTH		PWM_IN_HYST				STEP	

Bits	Field	Type	Description
7:6	SMOOTH	R/W	Advanced Slope control. Filter strength for digital smoothing filter. 00 = no smoothing 01 = light smoothing 10 = medium smoothing 11 = heavy smoothing
5:2	PWM_IN_HYST	R/W	PWM input hysteresis 000 = None 001 = >1 LSB steps 010 = >2 LSB steps 011 = >4 LSB steps 100 = >8 LSB steps 101 = >16 LSB steps 110 = >32 LSB steps 111 = >64 LSB steps
2:0	STEP	R/W	Linear Sloping time (typical) 000 = 0 ms 001 = 8 ms 010 = 16 ms 011 = 24 ms 100 = 28 ms 101 = 32 ms 110 = 100 ms 111 = 200 ms

The STEP field controls the rate of brightness level changes. Brightness transitions have a fixed step time. The time required to complete a ramp between two levels is independent upon the difference between the starting and ending current levels. For example, when STEP is set to 110b a brightness transition between any brightness values will take 100 ms. The SMOOTH field controls the digital smoothing filter, Advanced Sloping. This filter behaves much like an RC filter. It can be used to remove the overshoot that appears to occur (for eye) on large brightness changes. The actual amount of smoothing is tailored for the STEP field setting. For example medium filter strength is higher for 100 ms ramp times than for 32 ms Linear Sloping times. This gives 32 possible brightness level ramping configurations.

The PWM detector over-samples the input PWM signal at 20 MHz. The accuracy of the duty-cycle measurement depends upon the frequency of the PWM signal. The maximum possible accuracy is 12-bit precision. To allow 12-bit precision the LP8555 must take at least 8192 samples.

$$\frac{20\ MHz}{2.44\ KHz} \approx 8192\ samples$$

0	2.4 kHz	4.8 kHz	9.6 kHz	19.5 kHz	39 kHz	78 kHz	156 kHz
12-bit	11-bit	10-bit	9-bit	8-bit	7-bit	6-bit	

When PWM-detector detects new PWM-value, it is effective only when it differs from previous value more than selected hysteresis. Hysteresis is selected with PWM_IN_HYST in register 0x15.

10.1.11 Brightness Transitions

STEP	SMOOTH	RAMP TIME (0 to 100%) (ms)
000	00	**0.0**
000	01	0.9
000	10	1.7
000	11	3.4
001	00	**8.2**
001	01	14.6
001	10	22.3
001	11	38.7
010	00	**16.0**
010	01	28.4
010	10	43.5
010	11	75.5
011	00	**24.2**
011	01	42.9
011	10	65.8
011	11	114.2
100	00	**27.9**
100	01	49.5
100	10	75.8
100	11	131.7
101	00	**32.0**
101	01	56.8
101	10	87.0
101	11	151.1
110	00	**102.0**
110	01	181.0
110	10	277.2
110	11	481.5
111	00	**204.8**
111	01	363.4
111	10	556.6
111	11	966.8

10.1.12 VOLTAGE_0

Address: 0x16

D7	D6	D5	D4	D3	D2	D1	D0
VMAX		ADAPT	VINIT				

Bits	Field	Type	Description
7:6	VMAX	R/W	Maximum boost voltage for Boost A (typical). 00 = 18V 01 = 22V 10 = 25V 11 = 28V
5	ADAPT	R/W	Enable adaptive headroom optimization.
4:0	VINIT	R/W	Initial boost voltage. When ADAPT is 0 the boost voltage will remain at the VINIT setting. The voltage range is from 7 V to 28 V; where 0x00 equals 7 V and 0x3F equals 28 V (typical).

The VOLTAGE_0.VMAX bit sets the maximum allowed boost voltage for Boost A. The boost control loop will never request a higher voltage than the VMAX value. When the VOLTAGE.ADAPT bit is set to 1 the boost voltage may vary from 7 V to the VMAX configured voltage.

VINIT (DEV)	Voltage (V)	VINIT (DEV)	Voltage (V)	VINIT (DEV)	Voltage (V)
0	7.00	11	14.45	22	21.91
1	7.68	12	15.13	23	22.58
2	8.35	13	15.8	24	23.26
3	9.03	14	16.48	25	23.94
4	9.71	15	17.16	26	24.61
5	10.39	16	17.84	27	25.29
6	11.06	17	18.52	28	25.97
7	11.74	18	19.2	29	26.65
8	12.42	19	19.87	30	27.32
9	13.09	20	20.55	31	28.00
10	13.77	21	21.23		

Example: For system where is 7 LEDs in series with 2.9V Vf. Target value for boost initial voltage would be: 7 x (2.9V + 0.1V) + 2V = 23V → VINIT = 24(DEC). 0.1V represents Vf variation of single LED, and 2V is worst case headroom. So it is desirable to set the initial voltage little higher than the actual Vf voltage to take the worst-case condition in consideration.

10.1.13 LEDEN1

Address: 0x19

D7	D6	D5	D4	D3	D2	D1	D0
—		ENABLE[6:1]					

Bits	Field	Type	Description
7:6	reserved	R/O	
5:0	ENABLE1	R/W	LED string enables for Bank B.

The ENABLE field configures the enabled LED strings. If the CONFIG.AUTO bit is 0 these LED strings will stay active when the backlight is on. If the CONFIG.AUTO bit is set, then an LED open/short condition will cause that LED string to be removed. A given LED string will never be enabled if the corresponding bit of the ENABLE field is set to 0. The OV field configures the threshold for detecting an LED overvoltage condition; which may occur when one or more LEDs are bypassed (shorted) within an LED string.

10.1.14 VOLTAGE1

Address: 0x1A

D7	D6	D5	D4	D3	D2	D1	D0
VMAX1		ADAPT1	VINIT1				

Bits	Field	Type	Description
7:6	VMAX	R/W	Maximum boost voltage for Boost B (typical). 00 = 18V 01 = 22V 10 = 25V 11 = 28V
5	ADAPT	R/W	Enable adaptive headroom optimization.
4:0	VINIT1	R/W	Initial boost voltage. When ADAPT is 0 the boost voltage will remain at the VINIT setting. The voltage range is from 7V to 28V; where 0x00 equals 7V and 0x3F equals 28V (typical).

The VOLTAGE1.VMAX bit sets the maximum allowed boost voltage for Boost B. The boost control loop will never request a higher voltage than the VMAX value. When the VOLTAGE.ADAPT bit is set to 1 the boost voltage may vary from 7V to the VMAX configured voltage.

VINIT (DEC)	Voltage (V)	VINIT (DEC)	Voltage (V)	VINIT (DEC)	Voltage (V)
0	7.00	11	14.45	22	21.91
1	7.68	12	15.13	23	22.58
2	8.35	13	15.8	24	23.26
3	9.03	14	16.48	25	23.94
4	9.71	15	17.16	26	24.61
5	10.39	16	17.84	27	25.29
6	11.06	17	18.52	28	25.97
7	11.74	18	19.2	29	26.65
8	12.42	19	19.87	30	27.32
9	13.09	20	20.55	31	28.00
10	13.77	21	21.23		

10.1.15 OPTION

Address: 0x1C

D7	D6	D5	D4	D3	D2	D1	D0
—				OPTION			

Bits	Field	Type	Description
7:4	reserved	R/O	
3:0	OPTION	R/O	Metal option identifier.

10.1.16 EXTRA

Address: 0x1D

D7	D6	D5	D4	D3	D2	D1	D0
EXTRA							

Bits	Field	Type	Description
7:0	EXTRA	R/W	User accessible extra identifier register

10.1.17 ID

Address: 0x0E

D7	D6	D5	D4	D3	D2	D1	D0
ID_CUST				ID_CFG			

Bits	Field	Type	Description
7:4	ID_CUST	R/W	TI Customer ID code.
3:0	ID_CFG	R/W	TI Configuration ID code.

The ID field is configured by TI when the EPROM is programmed.

10.1.18 REVISION

Address: 0x0F

D7	D6	D5	D4	D3	D2	D1	D0
MAJOR				MINOR			

Bits	Field	Type	Description
7:4	MAJOR	R/O	Major silicon revision.
3:0	MINOR	R/O	Minor silicon revision.

The REVISION register provides silicon revision information in case test SW needs to distinguish between different revisions of the device or later identification is needed. REVISION register content comes from read only metal register.

10.1.19 CONF0

Address: 0x76

D7	D6	D5	D4	D3	D2	D1	D0
BOOST_IS_DIV2	—		ALTID	SRON		CURR_LIMIT	

Bits	Field	Type	Description
7	BOOST_IS_DIV2	R/W	Divide inductor peak current by 2 0 = Normal operation 1 = Inductor currents divided by 2
6:5	reserved	R/W	
4	ALTID	R/W	I^2C Slave ID selector 0 = 2Ch 1 = 2Eh
3:2	SRON	R/W	Slowed boost slew rate. When COMMAND.SREN is set to 1 boost slew rate is controlled with this value.
1:0	CURR_LIMIT	R/W	Boost inductor peak current limit (typical). BOOST_IS_DIV2 sets which of the limits is used. 00 = 0.9A / 1.55A 01 = 1.2A / 2.1A 10 = 1.5A / 2.6A 11 = 1.8A / 3.1A

10.1.20 CONF1

Address: 0x77

D7	D6	D5	D4	D3	D2	D1	D0
FMOD_DIV		—		—		—	

Bits	Field	Type	Description
7:6	FMOD_DIV	R/W	Spread spectrum modulation frequency divisor. 00 = 0.45% 01 = 0.27% 10 = 0.17% 11 = 0.12%
5:0	reserved	R/W	

The FMOD_DIV field controls modulation frequency for spread spectrum clocking. The actual modulation frequency scales with the boost frequency.

BOOST Frequency (kHz)	FMOD_DIV = 00b (kHz)	FMOD_DIV = 01b (kHz)	FMOD_DIV = 10b (kHz)	FMOD_DIV = 11b (kHz)
1000	4.17	2.78	1.67	1.19
500	2.08	1.39	0.83	0.64

10.1.21 VHR0

Address: 0x78

D7	D6	D5	D4	D3	D2	D1	D0
—	VHR_SLOPE			—	VHR_VERT		

Bits	Field	Type	Description
7	reserved	R/O	
6:4	VHR_SLOPE	R/W	Typical headroom voltage at maximum current (50 mA) 000 = 210 mV 001 = 223 mV 010 = 235 mV 011 = 248 mV 100 = 260 mV 101 = 273 mV 110 = 285 mV 111 = 300 mV
3	reserved		
2:0	VHR_VERT	R/W	Typical minimum headroom voltage 000 = 50 mV 001 = 80 mV 010 = 110 mV 011 = 140 mV 100 = 170 mV 101 = 200 mV 110 = 230 mV 111 = 260 mV

10.1.22 VHR1

Address: 0x79

D7	D6	D5	D4	D3	D2	D1	D0
—		VHR_HYST		—		VHR_HORZ	

Bits	Field	Type	Description
7:6	reserved	R/O	
5:4	VHR_HYST	R/W	Typical hysteresis for the mid comparator threshold (above the low comparator threshold). 00 = 200 mV 01 = 233 mV 10 = 466 mV 11 = 600 mV
3:2	reserved	R/O	
1:0	VHR_HORZ	R/W	Percentage of full driver range (horizontal component) 00 = 1% 01 = 25% 10 = 37.5% 11 = 50%

10.1.23 JUMP

Address: 0x7A

D7	D6	D5	D4	D3	D2	D1	D0
JEN	—			JTHR		JVOLT	

Bits	Field	Type	Description
7	JEN	R/W	Enable boost voltage jumping on large brightness percentage increases.
6:4	reserved	R/O	
3:2	JTHR	R/W	Jump brightness percentage threshold. 00 = 6.25% 01 = 12.5% 10 = 25% 11 = 50%
1:0	JVOLT	R/W	Typical boost voltage jump size (10.26 mV/step) 00 = 195 steps (2V) 01 = 390 steps (4V) 10 = 585 steps (6V) 11 = 780 steps (8V)

The jump feature operates outside of the normal adaptive headroom loop. Whenever the brightness percentage instantaneously increases above the configured threshold the boost voltage is instructed to immediately jump up. This can be used in some rare cases where extremely fast boost reaction time to brightness changes is needed. The JTHR field configures the threshold and the JVOLT field configures the voltage increase. The requested boost voltage will never exceed the value set by the VOLTAGE.VMAX field.

PCB Layout Considerations

11.1 General Layout Guidelines

Figure 4-5 and Figure 11-1 show a layout recommendation for the LP8555. The figures are used for demonstrating the principle of good layout. This layout can be adapted to the actual application layout if/where possible. It is important that all boost components are close to the chip and the high-current traces should be wide enough. Principle of a PCB layout can be seen in LP8555 datasheet as well with external component selection guidance.

By placing the boost component on one side of the chip it is easy to keep the ground plane intact below the high-current paths. This way other chip terminals can be routed more easily without splitting the ground plane. If the chip is placed in the way of the boost current loops, the I^2C lines, LED lines, etc., cut the ground plane below the high-current paths, thus making the layout design more difficult. VDD and VLDO need to be as noise-free as possible. Place the bypass capacitors near the corresponding terminals and ground them to as noise-free ground as possible.

Here are some main points to help the PCB layout work:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close to the SW and SW_GND terminals as possible. Input and output capacitor grounds need to be close to each other and grounded to Power Ground.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents try to find the route with the minimum impedance, which is the route with the minimum loop area, not necessarily the shortest path. The minimum loop area is formed when return current flows just under the “positive” current route in the ground plane, if the ground plane is intact under the route. Traces from inner pads of the LP8555 need to be routed from below the part in the second layer so that the traces do not split the ground plane under the boost traces or components.
- The GND plane needs to be intact under the high-current boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Current loops when the boost switch is conducting and not conducting needs to be on the same direction in optimal case.
- Inductors should be placed so that the current flows in the same direction as in the current loops. Rotating an inductor 180 degrees changes current direction.
- Use separate “noisy” and “silent” grounds. A noisy ground is used for boost converter return current and a silent ground for more sensitive signals, like VDD and VLDO bypass capacitor grounding, as well as LP8555 GND connection.
- Boost output voltage to LEDs needs to be taken out “after” the output capacitors, not straight from the diode cathode.
- A small (for example, 39-pF) bypass capacitor should be placed close to the FB terminal.
- The VDD line should be separated from the high-current supply path to the boost converters to prevent high-frequency ripple affecting the chip behavior. A separate 1-µF bypass capacitor is used for the VDD line, and it is grounded to noise-free ground.
- Input and output capacitors need strong grounding (wide traces, vias to PGND plane).
- If two output capacitors are used, symmetrical layout should be used to obtain ideal capacitor function.
- If the output capacitance is too low, it can cause boost to become unstable on some loads; this increases EMI. DC-bias characteristics need to be obtained from the component manufacturer; it is not taken into account on component tolerance. 50-V X5R/X7R capacitors are recommended.

11.2 Principles of Good Layout

Figure 11-1 shows principles of good layout and component placement.

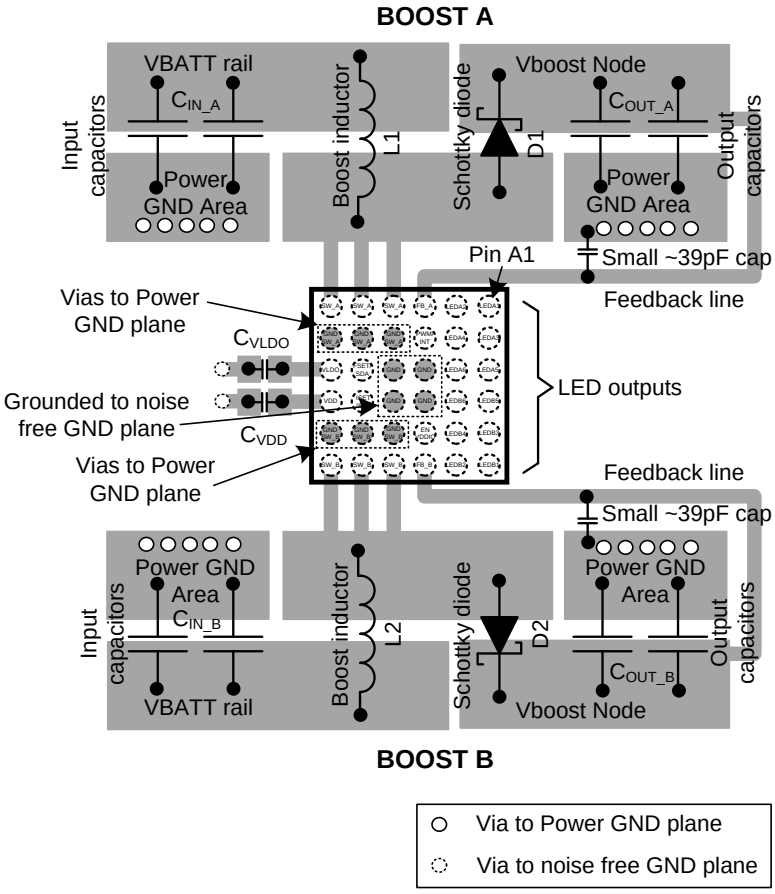


Figure 11-1. Principles of Good Layout

11.3 Recommended DSBGA Layout

See TI Application Note AN-1112 (SNVA009) for more information on die size package. Example below is 4 x 5 bump DSBGA, but same applies for 6 x 6 bump DSBGA.

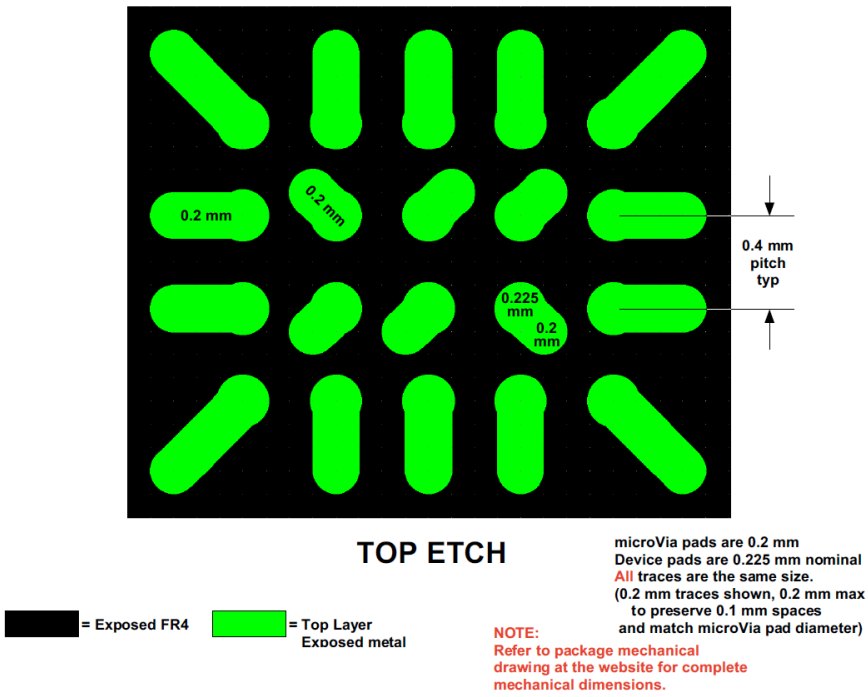


Figure 11-2. Top Etch

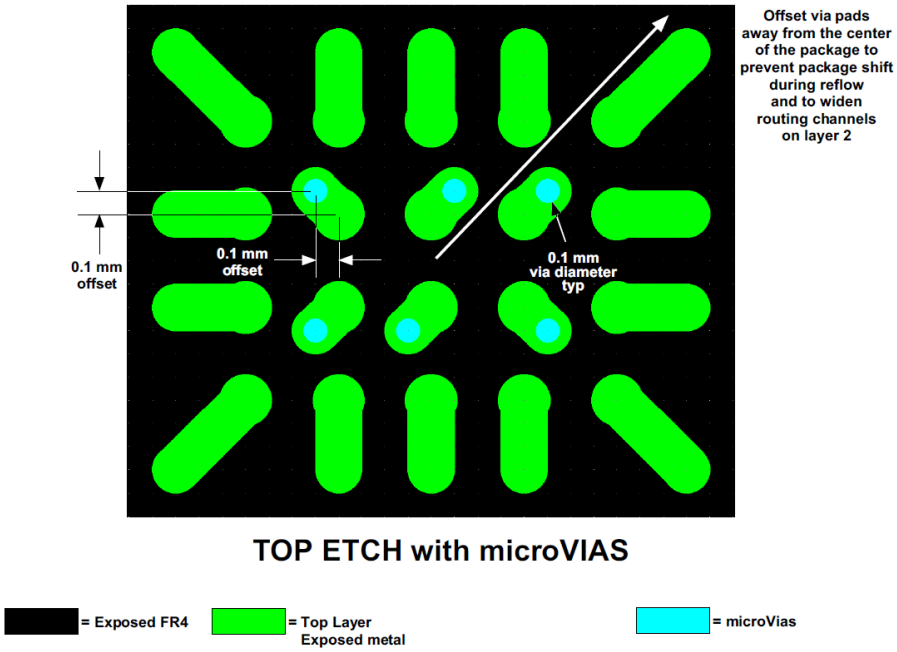


Figure 11-3. Top Etch with Micro Vias

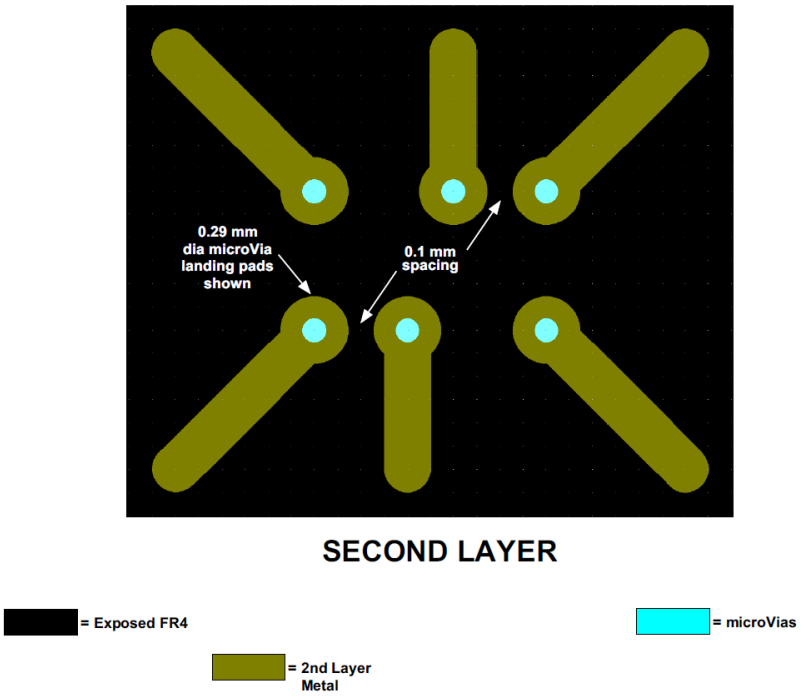


Figure 11-4. Second Layer

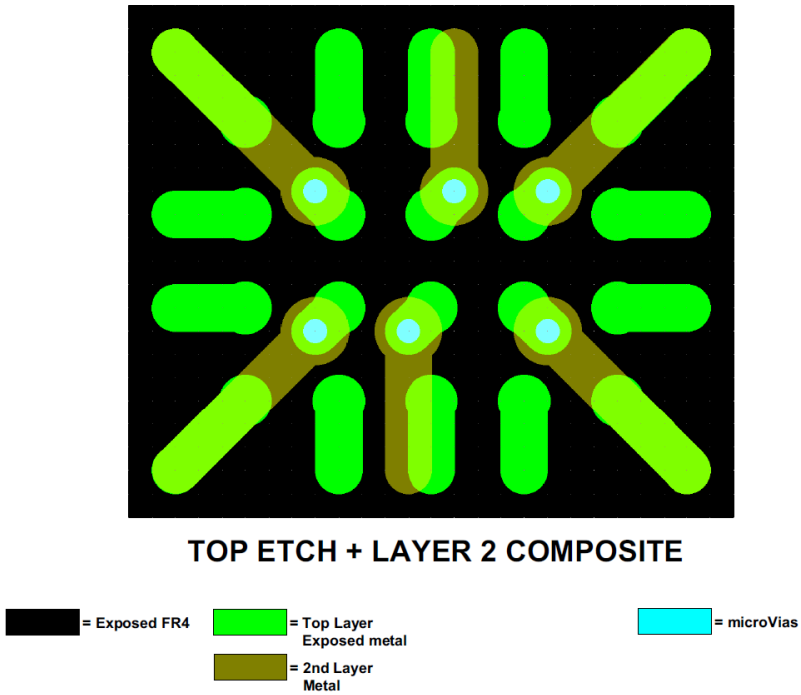


Figure 11-5. Top Etch + Layer 2 Composite

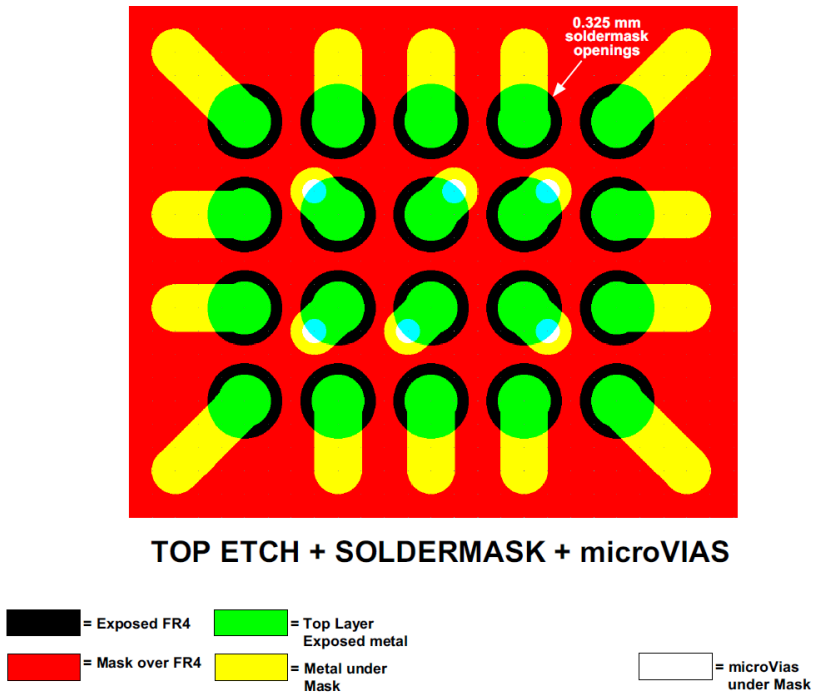


Figure 11-6. Top Etch + Soldermask + microVias

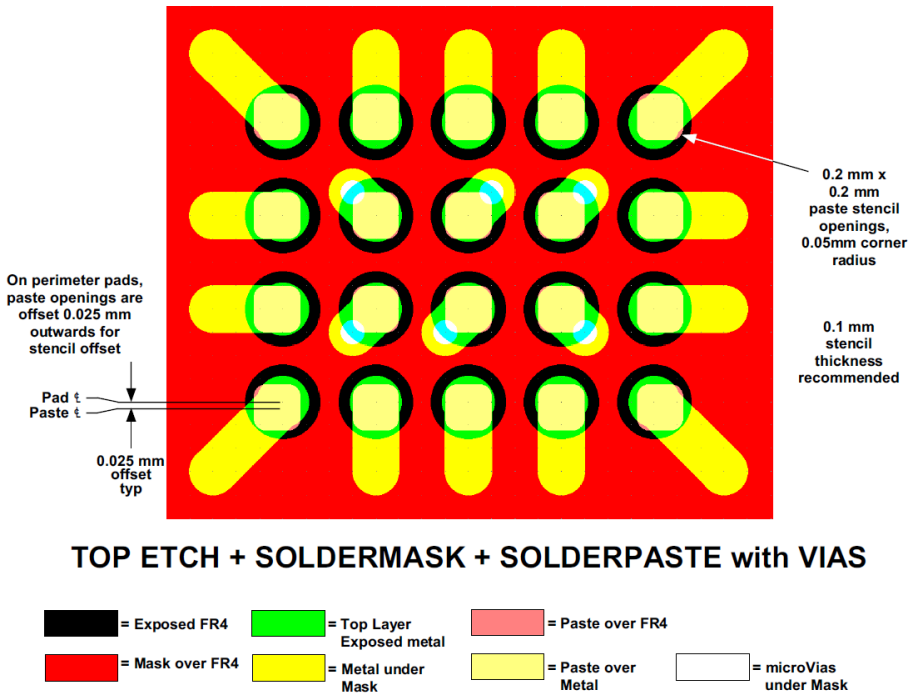


Figure 11-7. Top Etch + Soldermask + Solderpaste with Vias

Virtual COM Port Configuration

When the Virtual COM port number is bigger than 9, the evaluation program is not able to recognize the board. COM port number can be manually changed from Windows Device Manager. The below figures describe this sequence in Windows7. The Device Manager can be found from the Control Panel. Note that one may need to have Administrator rights to make the changes.

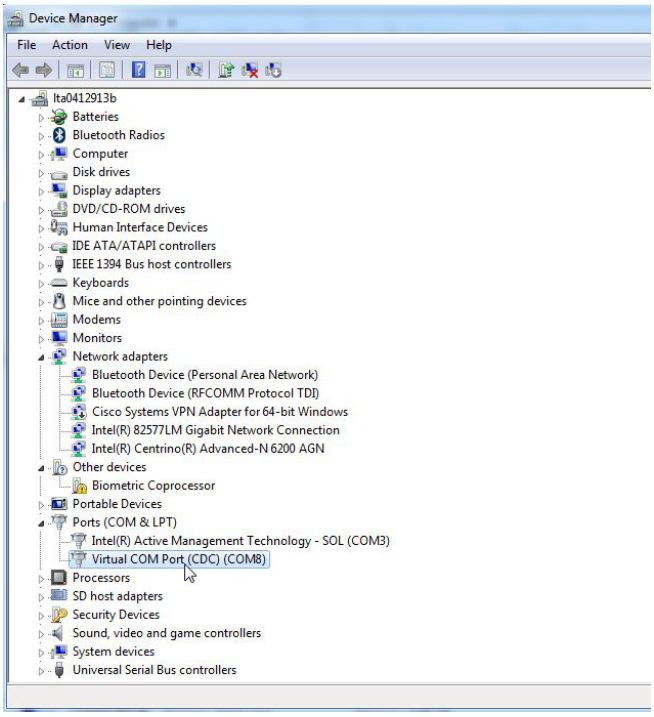


Figure A-1. Device Manager View. Select the Virtual COM Port

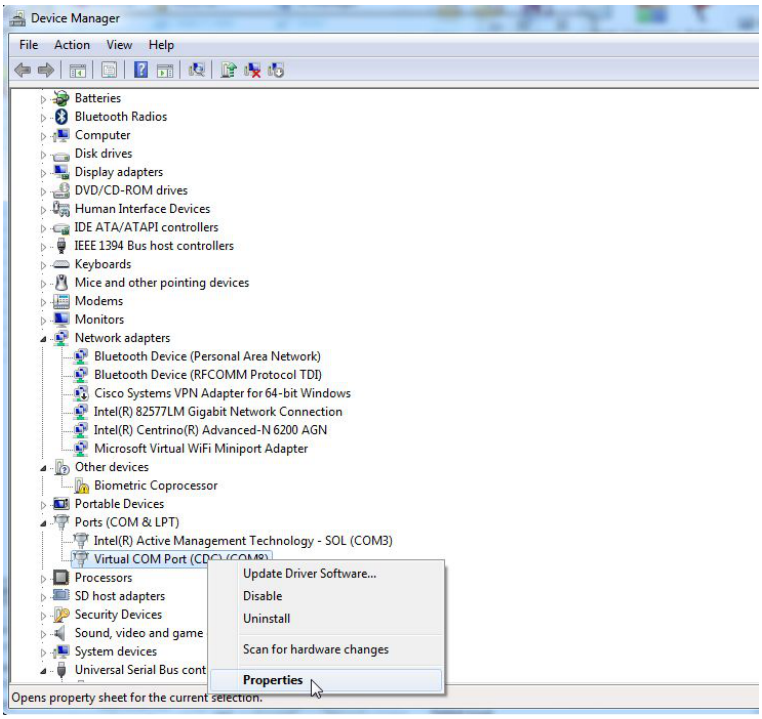


Figure A-2. Open Properties by Clicking Right Mouse Button on Virtual COM Port

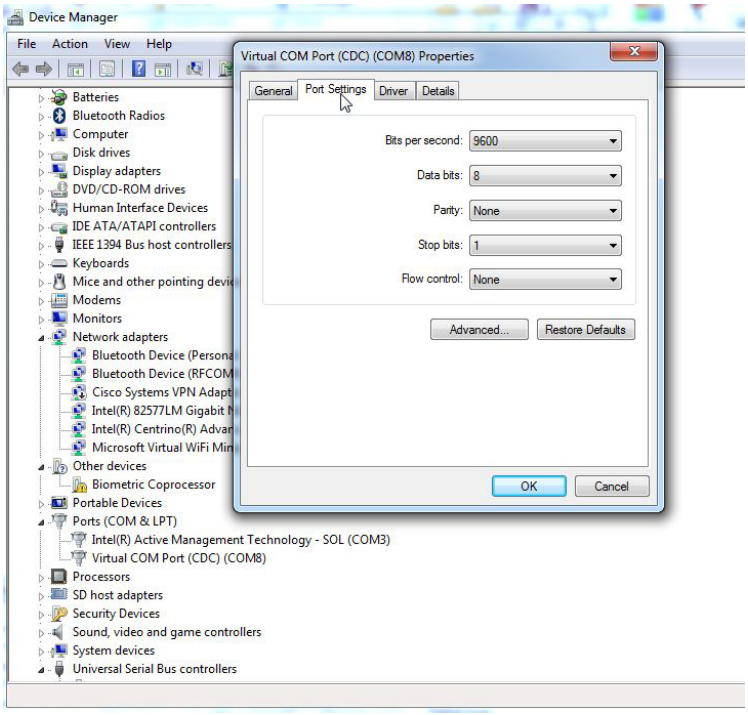


Figure A-3. Select Port Settings from the Virtual COM Port Properties

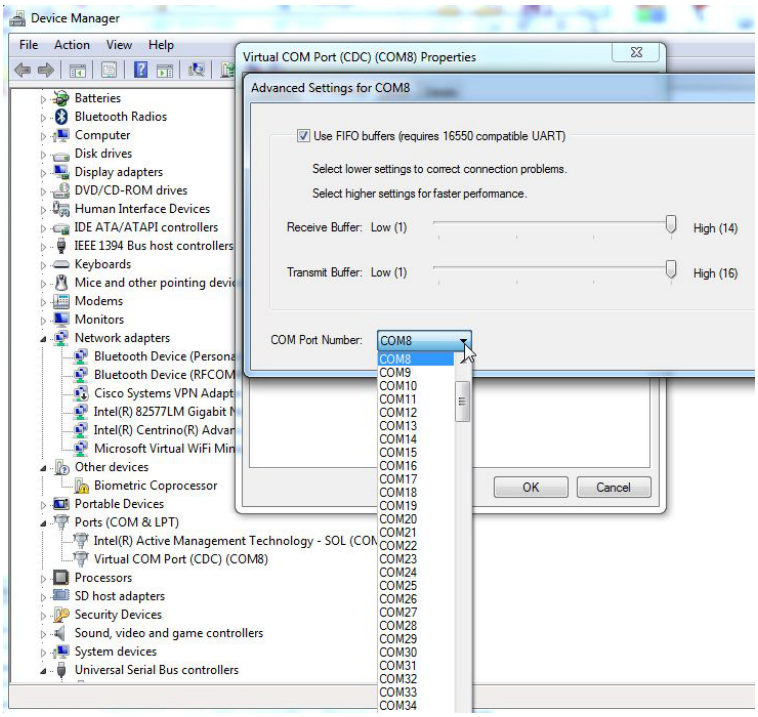


Figure A-4. Select Advanced from Virtual COM Port Properties and Select COM Port Number (9 or smaller)

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