LP87565C-Q1 Technical Reference Manual

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, LP87565CRNFRQ1.

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1 Introduction

This technical reference manual can be used as a reference for the LP87565C-Q1 default register bits after OTP memory download. This technical reference manual does not provide information about the electrical characteristics, external components. package, or the functionality of the device. For this information and the full register map, refer to the *LP8756x-Q1 Four-Phase 16-A Buck Converter With Integrated Switches* data sheet.

Table 1 lists the main OTP settings for power rails. lists the register bits loaded from OTP memory.

Table 1. Main OTP Settings for Power Rails

Description		Bit Name	LP87565CRNFRQ1 Value
Device identification	OTP configuration	OTP_ID	22h
BUCK0, BUCK1 (2-phase operation)	Output voltage	BUCK0_VSET	1150 mV
	Enable, EN pin, or I^2C register	EN_BUCK0, EN_PIN_CTRL0, BUCK0_EN_PIN_SELECT	EN1
	Force PWM	BUCK0_FPWM	Yes
	Force multiphase	BUCK0_FPWM_MP	No
	Peak current limit per phase	ILIM0, ILIM1	5 A
	Maximum load current	N/A	8 A
	Slew rate	BUCK0_SLEW_RATE	3.8 mV/µs
BUCK2, BUCK3 (2-phase operation)	Output voltage	BUCK2_VSET	1060 mV
	Enable, EN pin, or I^2C register	EN_BUCK2, EN_PIN_CTRL2, BUCK2_EN_PIN_SELECT	EN1
	Force PWM	BUCK2_FPWM	Yes
	Force multiphase	BUCK2_FPWM_MP	No
	Peak current limit per phase	ILIM2, ILIM3	5 A
	Maximum load current	N/A	8 A
	Slew rate	BUCK2_SLEW_RATE	3.8 mV/µs
Switching frequency		N/A	2 MHz
I^2C address		N/A	60h

2 Register Bits Loaded From OTP Memory

Table 2 lists the register bit values loaded from the OTP memory during device start-up.

Table 2. Summary of Registers Bits

Address	Register Name	Bit	LP87565CRNFRQ1 Value
0x01	OTP_REV	OTP_ID[7:0]	22h
0x02	BUCK0_CTRL1	EN_BUCK0	1h

Table 2. Summary of Registers Bits (continued)

Address	Register Name	Bit	LP87565CRNFRQ1 Value
0x02	BUCK0_CTRL1	EN_PIN_CTRL0	1h
0x02	BUCK0_CTRL1	BUCK0_EN_PIN_SELECT[1:0]	0h
0x02	BUCK0_CTRL1	BUCK0_FPWM	1h
0x02	BUCK0_CTRL1	BUCK0_FPWM_MP	0h
0x03	BUCK0_CTRL2	ILIM0[2:0]	7h
0x03	BUCK0_CTRL2	SLEW_RATE0[2:0]	4h
0x04	BUCK1_CTRL1	EN_BUCK1	1h
0x04	BUCK1_CTRL1	EN_PIN_CTRL1	1h
0x04	BUCK1_CTRL1	BUCK1_EN_PIN_SELECT[1:0]	0h
0x04	BUCK1_CTRL1	BUCK1_FPWM	1h
0x05	BUCK1_CTRL2	ILIM1[2:0]	7h
0x05	BUCK1_CTRL2	SLEW_RATE1[2:0]	4h
0x06	BUCK2_CTRL1	EN_BUCK2	1h
0x06	BUCK2_CTRL1	EN_PIN_CTRL2	1h
0x06	BUCK2_CTRL1	BUCK2_EN_PIN_SELECT[1:0]	0h
0x06	BUCK2_CTRL1	BUCK2_FPWM	1h
0x06	BUCK2_CTRL1	BUCK2_FPWM_MP	0h
0x07	BUCK2_CTRL2	ILIM2[2:0]	7h
0x07	BUCK2_CTRL2	SLEW_RATE2[2:0]	4h
0x08	BUCK3_CTRL1	EN_BUCK3	1h
0x08	BUCK3_CTRL1	EN_PIN_CTRL3	1h
0x08	BUCK3_CTRL1	BUCK3_EN_PIN_SELECT[1:0]	0h
0x08	BUCK3_CTRL1	BUCK3_FPWM	1h
0x09	BUCK3_CTRL2	ILIM3[2:0]	7h
0x09	BUCK3_CTRL2	SLEW_RATE3[2:0]	4h
0x0A	BUCK0_VOUT	BUCK0_VSET[7:0]	6Bh
0x0C	BUCK1_VOUT	BUCK1_VSET[7:0]	6Bh
0x0E	BUCK2_VOUT	BUCK2_VSET[7:0]	59h
0x10	BUCK3_VOUT	BUCK3_VSET[7:0]	59h
0x12	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	1h
0x12	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	0h
0x13	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	1h
0x13	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	0h
0x14	BUCK2_DELAY	BUCK2_SHUTDOWN_DELAY[3:0]	1h
0x14	BUCK2_DELAY	BUCK2_STARTUP_DELAY[3:0]	0h
0x15	BUCK3_DELAY	BUCK3_SHUTDOWN_DELAY[3:0]	1h
0x15	BUCK3_DELAY	BUCK3_STARTUP_DELAY[3:0]	0h
0x16	GPIO2_DELAY	GPIO2_SHUTDOWN_DELAY[3:0]	0h
0x16	GPIO2_DELAY	GPIO2_STARTUP_DELAY[3:0]	2h
0x17	GPIO3_DELAY	GPIO3_SHUTDOWN_DELAY[3:0]	0h
0x17	GPIO3_DELAY	GPIO3_STARTUP_DELAY[3:0]	2h
0x19	CONFIG	DOUBLE_DELAY	1h
0x19	CONFIG	CLKIN_PD	1h
0x19	CONFIG	EN4_PD	0h
0x19	CONFIG	EN3_PD	0h
0x19	CONFIG	TDIE_WARN_LEVEL	1h
0x19	CONFIG	EN2_PD	0h
0x19	CONFIG	EN1_PD	1h
0x21	TOP_MASK1	GPIO_MASK	1h
0x21	TOP_MASK1	SYNC_CLK_MASK	1h
0x21	TOP_MASK1	TDIE_WARN_MASK	0h

Table 2. Summary of Registers Bits (continued)

Address	Register Name	Bit	LP87565CRNFRQ1 Value
0x21	TOP_MASK1	I_LOAD_READY_MASK	1h
0x22	TOP_MASK2	RESET_REG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK1_PG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK1_ILIM_MASK	0h
0x23	BUCK_0_1_MASK	BUCK0_PG_MASK	1h
0x23	BUCK_0_1_MASK	BUCK0_ILIM_MASK	0h
0x24	BUCK_2_3_MASK	BUCK3_PG_MASK	1h
0x24	BUCK_2_3_MASK	BUCK3_ILIM_MASK	0h
0x24	BUCK_2_3_MASK	BUCK2_PG_MASK	1h
0x24	BUCK_2_3_MASK	BUCK2_ILIM_MASK	0h
0x28	PGOOD_CTRL1	PG3_SEL[1:0]	3h
0x28	PGOOD_CTRL1	PG2_SEL[1:0]	3h
0x28	PGOOD_CTRL1	PG1_SEL[1:0]	3h
0x28	PGOOD_CTRL1	PG0_SEL[1:0]	3h
0x29	PGOOD_CTRL2	EN_PG0_NINT	0h
0x29	PGOOD_CTRL2	PGOOD_SET_DELAY	0h
0x29	PGOOD_CTRL2	EN_PGFLT_STAT	0h
0x29	PGOOD_CTRL2	PGOOD_WINDOW	1h
0x29	PGOOD_CTRL2	PGOOD_OD	1h
0x29	PGOOD_CTRL2	PGOOD_POL	0h
0x2B	PLL_CTRL	PLL_MODE[1:0]	0h
0x2B	PLL_CTRL	EXT_CLK_FREQ[4:0]	13h
0x2C	PIN_FUNCTION	EN_SPREAD_SPEC	1h
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO3	1h
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO3	0h
0x2C	PIN_FUNCTION	EN_PIN_CTRL_GPIO2	1h
0x2C	PIN_FUNCTION	EN_PIN_SELECT_GPIO2	0h
0x2C	PIN_FUNCTION	GPIO3_SEL	1h
0x2C	PIN_FUNCTION	GPIO2_SEL	1h
0x2C	PIN_FUNCTION	GPIO1_SEL	0h
0x2D	GPIO_CONFIG	GPIO3_OD	1h
0x2D	GPIO_CONFIG	GPIO2_OD	0h
0x2D	GPIO_CONFIG	GPIO1_OD	1h
0x2D	GPIO_CONFIG	GPIO3_DIR	1h
0x2D	GPIO_CONFIG	GPIO2_DIR	1h
0x2D	GPIO_CONFIG	GPIO1_DIR	1h
0x2F	GPIO_OUT	GPIO3_OUT	1h
0x2F	GPIO_OUT	GPIO2_OUT	1h

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