TPS6565342-Q1 Technical Reference Manual

This document provides the register bit values for the one-time programmable (OTP) bits of the orderable part number, TPS6565342RHDRQ1 / TPS6565342RHDTQ1.

1 Introduction

This technical reference manual can be used as a reference for the TPS6565342-Q1 default register bits after OTP memory download. The TPS6565342-Q1 is designed for Radar applications, and is a part of two chip solution (TPS6565342-Q1 + TPS65313-Q1) to power the AWR1642 and AWR1843 radar chip.This technical reference manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the *TPS65653-Q1 Dual 3 A Buck Converters* data sheet.

2 OTP Memory Device Settings

This section lists all of the device settings that are downloaded from OTP memory.

Table 1 lists the device settings for I^2C and OTP revision ID values.

Table 1. Device Identification and I^2C Settings

	Description	Bit Name	TPS6565342-Q1
I^2C address			0x61
DEVICE_ID	Device specific ID code	DEVICE_ID	0x0
OTP_ID	Identification code for OTP version	OTP_ID	0x42

Table 2 lists the device settings for BUCK0 and BUCK1. The maximum allowed slew-rate for BUCKx depends on the output capacitance. Refer to the *TPS65653-Q1 Dual 3 A Buck Converters* data sheet for output capacitance boundary conditions.

Table 2. BUCK0 and BUCK1 OTP Settings

	Description	Bit Name	TPS6565342-Q1
	Buck phase configuration (2 single phase Bucks or combined 2 phase, denoted as 1+1 or 2-phase)		1+1
	Switching frequency		4 MHz
	Spread spectrum	EN_SPREAD_SPEC	Disabled
BUCK0	Output voltage	BUCK0_VSET	1.800 V
	Enable, EN-pin or I^2C register	BUCK0_EN_PIN_CTRL	EN-pin
	Control for BUCK0	BUCK0_EN	High
	Force PWM mode or auto mode	BUCK0_FPWM	Force PWM
	Peak current limit	BUCK0_ILIM	4 A
	Maximum load current limit	NA	3 A
	Slew rate	BUCK0_SLEW_RATE	3.8 mV/us
	Startup delay	BUCK0_ STARTUP_ DELAY	0 ms
	Shutdown delay	BUCK0_ SHUTDOWN_ DELAY	0 ms

Table 2. BUCK0 and BUCK1 OTP Settings (continued)

	Description	Bit Name	TPS6565342-Q1
BUCK1	Output voltage	BUCK1_VSET	1.000 V
	Enable, EN-pin or I²C register	BUCK1_EN_PIN_CTRL	EN-pin
	Control for BUCK1	BUCK1_EN	High
	Force PWM mode or auto mode	BUCK1_FPWM	Force PWM
	Peak current limit	BUCK1_ILIM	4 A
	Maximum load current limit	NA	3 A
	Slew rate	BUCK1_SLEW_RATE	3.8 mV/us
	Startup delay	BUCK1_ STARTUP_ DELAY	0 ms
	Shutdown delay	BUCK1_ SHUTDOWN_ DELAY	0 ms

Table 3 lists the device settings for GPIOs.

Table 3. EN, CLKIN and GPIO Pin Settings

	Description	Bit Name	TPS6565342-Q1
EN pin	EN pin pulldown resistor enable or disable	EN_PD	Disabled
CLKIN pin	CLKIN or GPO2 mode selection	CLKIN_PIN_SEL	CLKIN
	CLKIN pin pulldown resistor enable or disable (applicable for both CLKIN and GPO2 modes)	CLKIN_PD	Disabled
	Frequency of external clock when connected to CLKIN	EXT_CLK_FREQ	2 MHz
	Enable for the internal PLL. When PLL disabled, internal RC OSC is used	EN_PLL	Enabled
GPO	GPO output type (push-pull or open drain)	GPO_OD	OD
	Enable, EN-pin or I²C register	GPO_EN_PIN_CTRL	I2C
	Control for GPO	GPO_EN	Low
	Startup delay	GPO_ STARTUP_ DELAY	0 ms
	Shutdown delay	GPO_ SHUTDOWN_ DELAY	0 ms
GPO2	GPO2 output type (push-pull or open drain)	GPO2_OD	OD
	Enable, EN-pin or I²C register	GPO2_EN_PIN_CTRL	I2C
	Control for GPO2	GPO2_EN	Low
	Startup delay	GPO2_ STARTUP_ DELAY	0 ms
	Shutdown delay	GPO2_ SHUTDOWN_ DELAY	0 ms

Table 4 lists the device PGOOD settings.

Table 4. PGOOD OTP Settings

	Description	Bit Name	TPS6565342-Q1
Signals monitored by PGOOD	BUCK0 output voltage	EN_PGOOD_BUCK0	Yes
	BUCK1 output voltage	EN_PGOOD_BUCK1	Yes
	Thermal warning	EN_PGOOD_TWARN	Yes
PGOOD mode selections	PGOOD thresholds for BUCK0, BUCK1 (Undervoltage / Window (undervoltage and overvoltage))	PGOOD_WINDOW_BUCK	Window
	PGOOD operating mode (detecting UNUSUAL situations / detecting UNVALID situations)	PGOOD_MODE	Detecting UNVALID situations
	PGOOD signal mode (status / latched until fault source read)	PG_FAULT_GATES_PGOOD	Status
	PGOOD output mode (push-pull or open drain)	PGOOD_OD	OD
	PGOOD polarity (active high/ active low)	PGOOD_POL	Active High

Table 5 lists the device protection settings.

Table 5. Protections OTP Settings

	Description	Bit Name	TPS6565342-Q1
Protections	Thermal warning level (125°C or 137°C)	TDIE_WARN_LEVEL	137°C
	Input overvoltage protection	NA	Enabled

Table 6 lists the device settings for interrupts. When an interrupt from an event is unmasked, an interrupt is generated on the nINT pin.

Table 6. Interrupt Mask Settings

	Interrupt event	Bit Name	TPS6565342-Q1
General	PGOOD pin changing active to inactive	PGOOD_INT_MASK	Masked
	Sync clock appears or disappears	SYNC_CLK_MASK	Masked
	Thermal warning	TDIE_WRN_MASK	Masked
	Load measurement ready	I_MEAS_MASK	Masked
	Register reset	RESET_REG_MASK	Masked
BUCK0	Buck0 PGood active	BUCK0_PGR_MASK	Masked
	Buck0 PGood inactive	BUCK0_PGF_MASK	Masked
	Buck0 current limit	BUCK0_ILIM_MASK	Unmasked
BUCK1	Buck1 PGood active	BUCK1_PGR_MASK	Masked
	Buck1 PGood inactive	BUCK1_PGF_MASK	Masked
	Buck1 current limit	BUCK1_ILIM_MASK	Unmasked

3 Power-up and Power Down Sequence

This section shows the power-up and power-down sequence for the device. The power-up and power-down delays for each rail are shown in Figure 1.

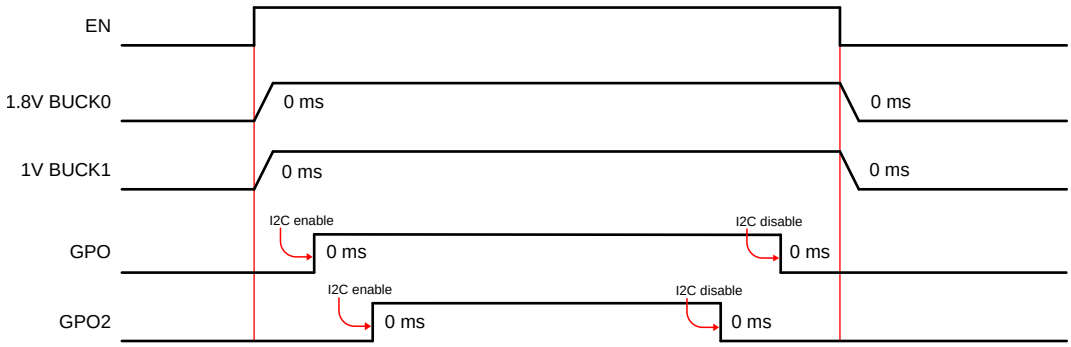


Figure 1. TPS6565342-Q1 Power-up and Power Down Sequence

4 Register Bits Loaded From OTP Memory

Table 7 lists the register bit values loaded from the OTP memory during device start-up.

Table 7. Summary of Control Registers

Address	Register Name	Bit	TPS6565342-Q1 Value
0x00	DEV_REV	DEVICE_ID[1:0]	0x0
0x01	OTP_REV	OTP_ID[7:0]	0x42
0x02	BUCK0_ CTRL_1	BUCK0_FPWM	0x1
0x02	BUCK0_ CTRL_1	BUCK0_ EN_PIN_CTRL	0x1
0x02	BUCK0_ CTRL_1	BUCK0_EN	0x1
0x03	BUCK0_ CTRL_2	BUCK0_ILIM[2:0]	0x5
0x03	BUCK0_ CTRL_2	BUCK0_SLEW_RATE[2:0]	0x4
0x04	BUCK1_ CTRL_1	BUCK1_FPWM	0x1
0x04	BUCK1_ CTRL_1	BUCK1_ EN_PIN_CTRL	0x1
0x04	BUCK1_ CTRL_1	BUCK1_EN	0x1
0x05	BUCK1_ CTRL_2	BUCK1_ILIM[2:0]	0x5
0x05	BUCK1_ CTRL_2	BUCK1_SLEW_RATE[2:0]	0x4
0x06	BUCK0_ VOUT	BUCK0_VSET[7:0]	0xB1
0x07	BUCK1_ VOUT	BUCK1_VSET[7:0]	0x4D
0x0C	BUCK0_ DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	0x0
0x0C	BUCK0_ DELAY	BUCK0_STARTUP_DELAY[3:0]	0x0
0x0D	BUCK1_ DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	0x0
0x0D	BUCK1_ DELAY	BUCK1_STARTUP_DELAY[3:0]	0x0
0x10	GPO_ DELAY	GPO_SHUTDOWN_DELAY[3:0]	0x0
0x10	GPO_ DELAY	GPO_STARTUP_DELAY[3:0]	0x0
0x11	GPO2_ DELAY	GPO2_SHUTDOWN_DELAY[3:0]	0x0
0x11	GPO2_ DELAY	GPO2_STARTUP_DELAY[3:0]	0x0
0x12	GPO_ CTRL	GPO2_OD	0x1
0x12	GPO_ CTRL	GPO2_ EN_PIN_CTRL	0x0
0x12	GPO_ CTRL	GPO2_EN	0x0
0x12	GPO_ CTRL	GPO_OD	0x1
0x12	GPO_ CTRL	GPO_ EN_PIN_CTRL	0x0
0x12	GPO_ CTRL	GPO_EN	0x0
0x13	CONFIG	STARTUP_DELAY_SEL	0x0
0x13	CONFIG	SHUTDOWN_DELAY_SEL	0x0
0x13	CONFIG	CLKIN_PIN_SEL	0x1
0x13	CONFIG	CLKIN_PD	0x0
0x13	CONFIG	EN_PD	0x0
0x13	CONFIG	TDIE _WARN _LEVEL	0x1
0x13	CONFIG	EN_ SPREAD _SPEC	0x0
0x14	PLL_CTRL	EN_PLL	0x1
0x14	PLL_CTRL	EXT_CLK_FREQ[4:0]	0x1
0x15	PGOOD_CTRL_1	PGOOD_POL	0x0
0x15	PGOOD_CTRL_1	PGOOD_OD	0x1
0x15	PGOOD_CTRL_1	PGOOD_WINDOW_BUCK	0x1
0x15	PGOOD_CTRL_1	EN_PGOOD_BUCK1	0x1
0x15	PGOOD_CTRL_1	EN_PGOOD_BUCK0	0x1
0x16	PGOOD_CTRL_2	EN_PGOOD_TWARN	0x1
0x16	PGOOD_CTRL_2	PG_FAULT_GATES_PGOOD	0x0
0x16	PGOOD_CTRL_2	PGOOD_MODE	0x1
0x20	TOP_ MASK_1	PGOOD_ INT_MASK	0x1

Table 7. Summary of Control Registers (continued)

Address	Register Name	Bit	TPS6565342-Q1 Value
0x20	TOP_ MASK_1	SYNC_CLK _MASK	0x1
0x20	TOP_ MASK_1	TDIE_WARN_MASK	0x1
0x20	TOP_ MASK_1	I_MEAS_ MASK	0x1
0x21	TOP_ MASK_2	RESET_ REG_MASK	0x1
0x22	BUCK_MASK	BUCK1_PGF_MASK	0x1
0x22	BUCK_MASK	BUCK1_PGR_MASK	0x1
0x22	BUCK_MASK	BUCK1_ ILIM_ MASK	0x0
0x22	BUCK_MASK	BUCK0_PGF_MASK	0x1
0x22	BUCK_MASK	BUCK0_PGR_MASK	0x1
0x22	BUCK_MASK	BUCK0_ ILIM_ MASK	0x0

Mechanical, Packaging, and Orderable Information

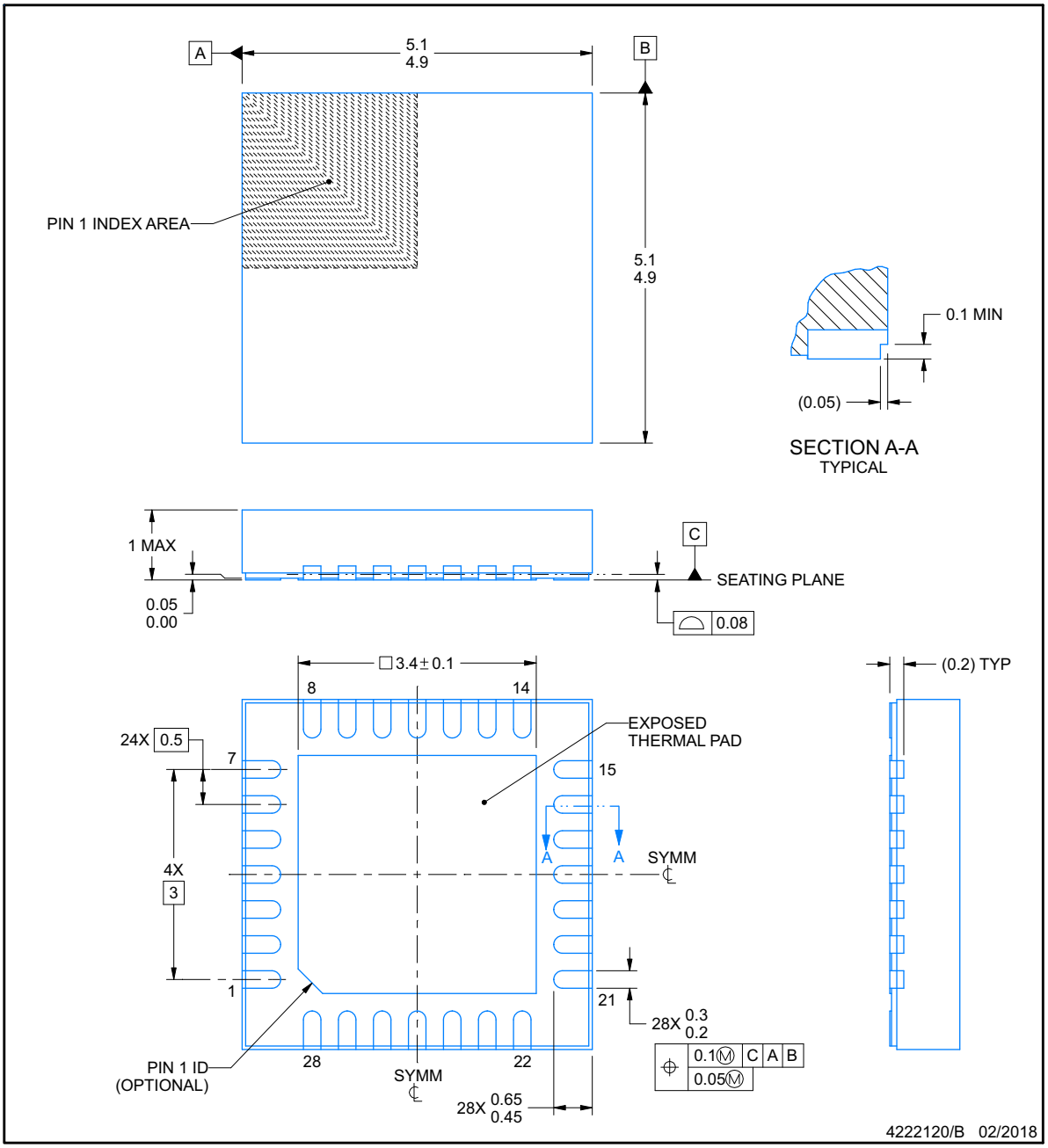
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RHD0028W

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



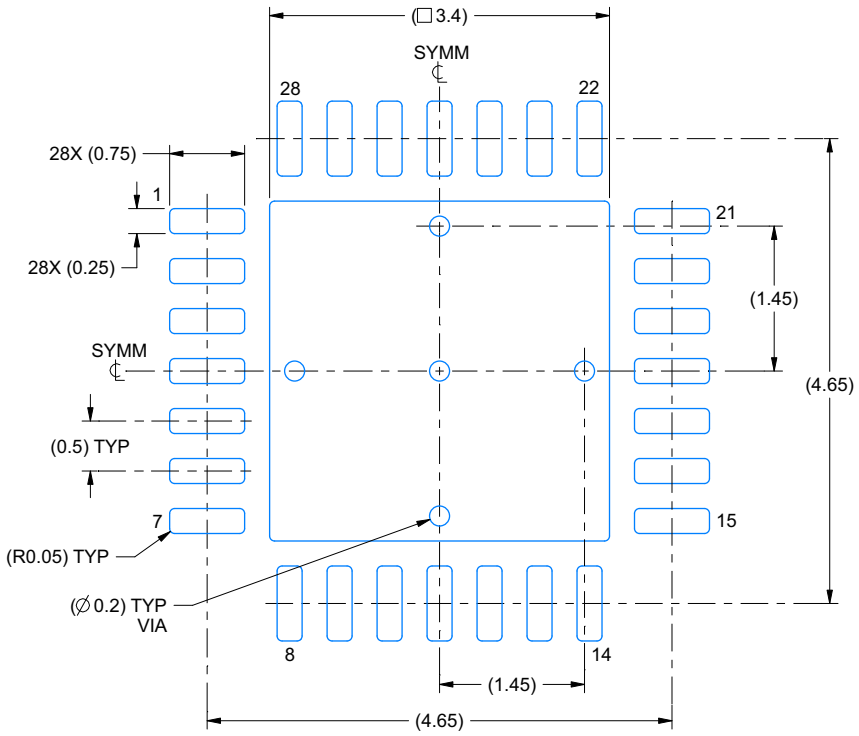
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

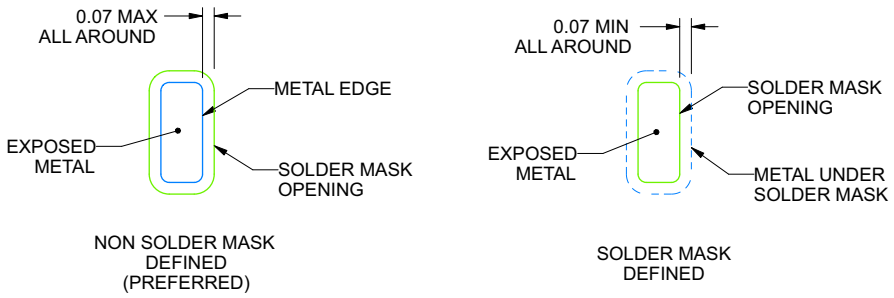
EXAMPLE BOARD LAYOUT

RHD0028W **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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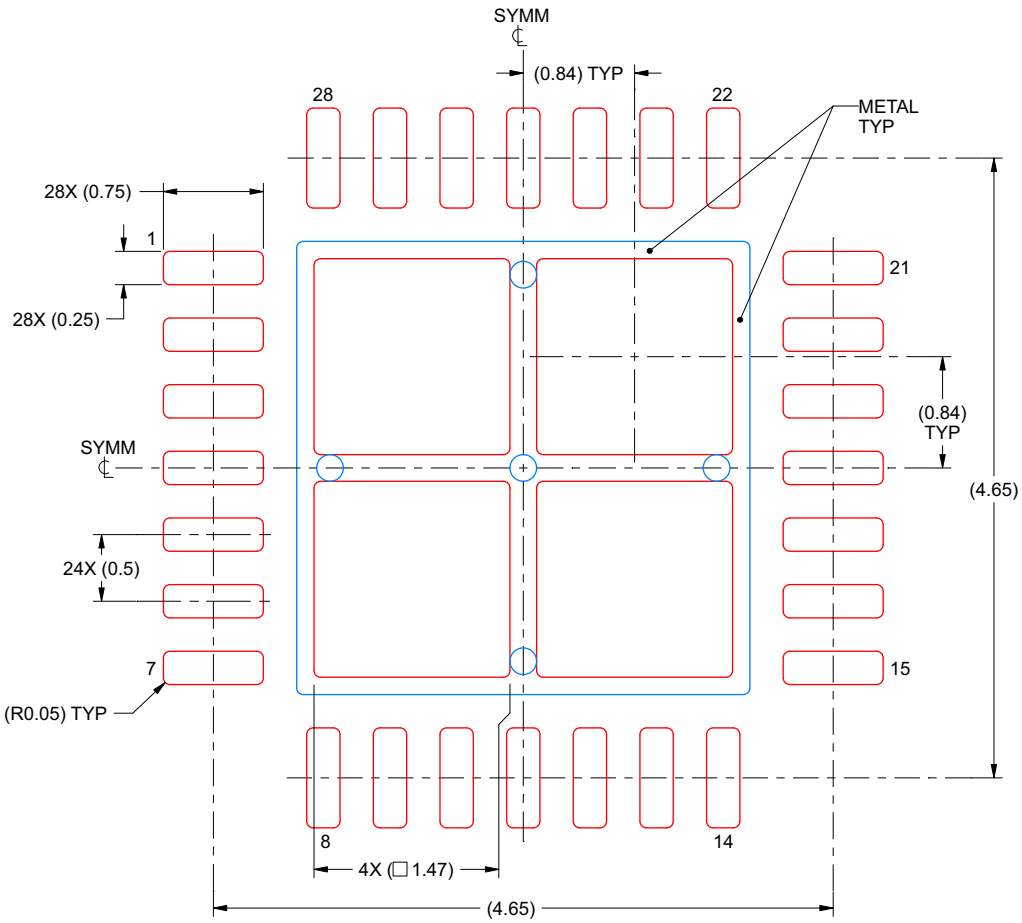
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RHD0028W **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
75% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222120/B 02/2018

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
TPS6565342RHDRQ1	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS65653 42RHDQ1
TPS6565342RHDTQ1	ACTIVE	VQFN	RHD	28	250	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	TPS65653 42RHDQ1

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

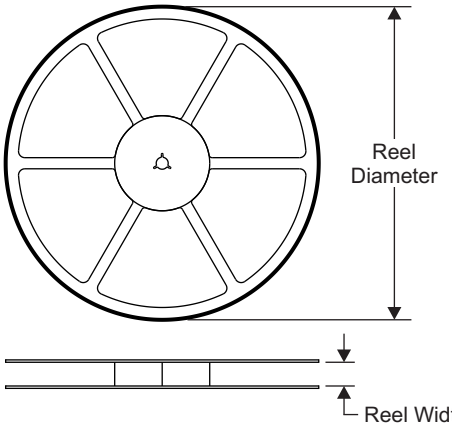
(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

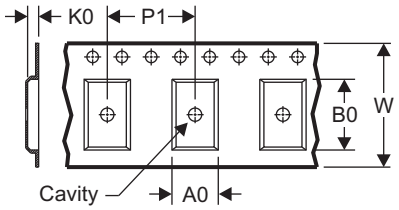
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

1.1 Tape and Reel Information

REEL DIMENSIONS

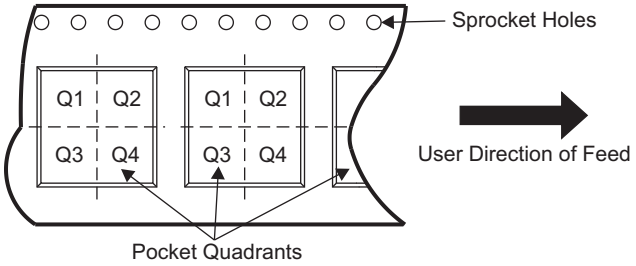


TAPE DIMENSIONS



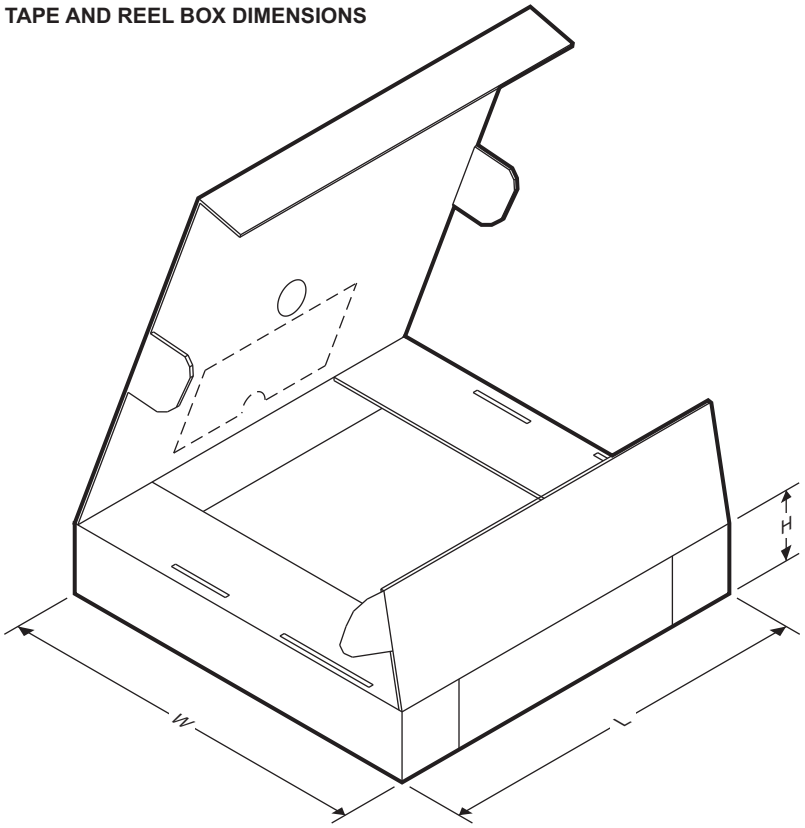
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS6565342RHDRQ1	VQFN	RHD	28	3000	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2
TPS6565342RHDTQ1	VQFN	RHD	28	250	330.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS6565342RHDRQ1	VQFN	RHD	28	3000	370.0	355.0	55.0
TPS6565342RHDTQ1	VQFN	RHD	28	250	370.0	355.0	55.0

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