EVM User's Guide: HSEC180ADAPEVM

HSEC Adapter Board

Description

This evaluation module is a 180-pin High Speed Edge Card (HSEC) adapter for TI C2000 System-On-Module (SOM) platforms, allowing for SOM-based platforms to have backwards compatibility with C2000 HSEC-based EVMs. The HSEC180ADAPEVM connects 180 pins from the SOM board to HSEC pins for use with legacy C2000 HSEC Docking Stations, such as the TMDSHSECDOCK. The HSEC180ADAPEVM also features two DP83826 10/100-Mbps Industrial Ethernet PHYs for evaluating EtherCAT® functionality on C2000 Microcontroller SOM platforms.

Features

- Standard 180-pin HSEC interface
- Compatibility with XDS110ISO-EVM for emulation
- 2x DP83826 10/100-Mbps Industrial Ethernet PHY with 2x RJ-45 Ethernet jacks
- Fast Serial Interface (FSI) header
- ADC filtering and ESD protection for dedicated Analog HSEC pins

1 Evaluation Module Overview

1.1 Introduction

This technical user's guide describes the hardware architecture of the HSEC Adapter Board, an adapter board for the SOM module built around the F28P65x MCU. The HSEC Adapter allows the user to interface with EtherCAT, FSI, JTAG, and other interfaces. This 180-pin Edge connector is intended to provide a well-filtered, robust design capable of working in most environments. The HSEC board is used with a docking station for powering up the SOM board. The XDS110 adapter board also can be interfaced with the SOM board with the help of the HSEC board. The HSEC Adapter Board has two RJ45 connectors for interfacing of EtherCAT, FSI header, and Emulation and DAC connector. The embedded emulation logic allows for emulation and debugging using standard development tools such as Code Composer Studio™ from TI.

Note

This evaluation board is a preproduction release and has several known issues that must not be copied into a production system.

1.2 Kit Contents

The following items are included in the HSEC180ADAPEVM kit:

- HSEC180ADAPEVM PCB
- Quick Start Guide

1.3 Specification

The HSEC180ADAPEVM is designed to expand on the capabilities of the F28P65x and F29H85x controlSOM EVMs, allowing a user to explore the full functionality of these microcontrollers. The SOM to HSEC adapter board can be treated as a good reference design for the F28P65x and F29H85x interfaces, but is not intended to be a complete customer design. Full compliance to safety, EMI/EMC, and other regulations are left to the designer of the system.

1.3.1 Functional Block Diagram

The functional block diagram of the HSEC adapter Board is shown below.

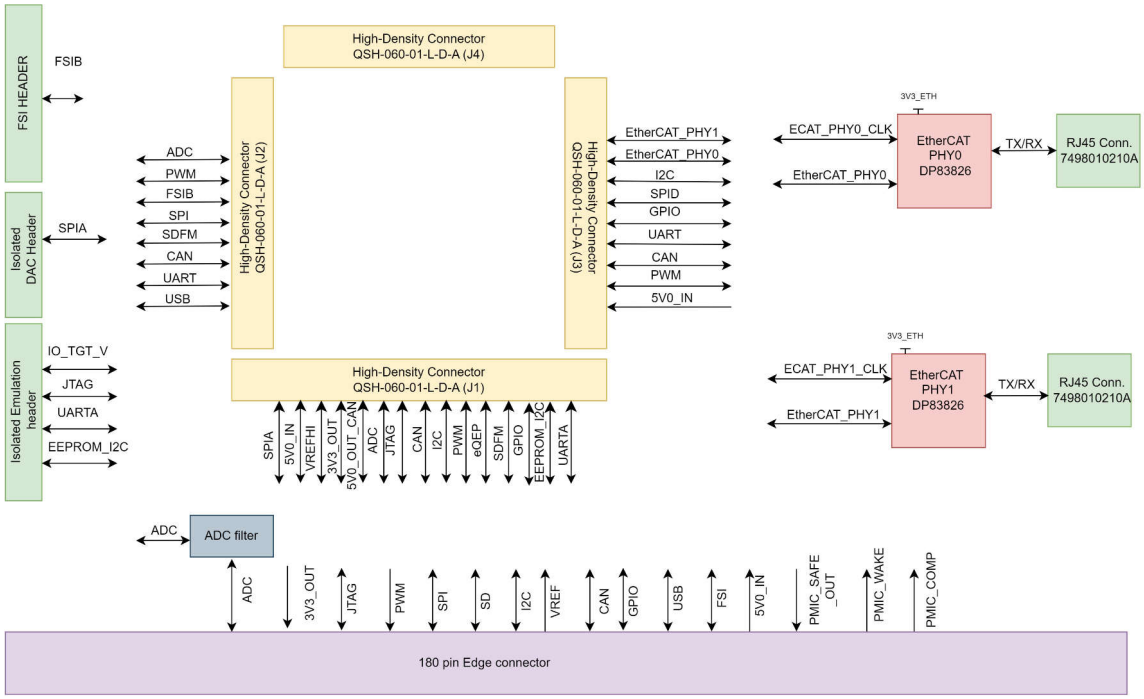


Figure 1-1. Block Diagram

1.3.2 Component Identification

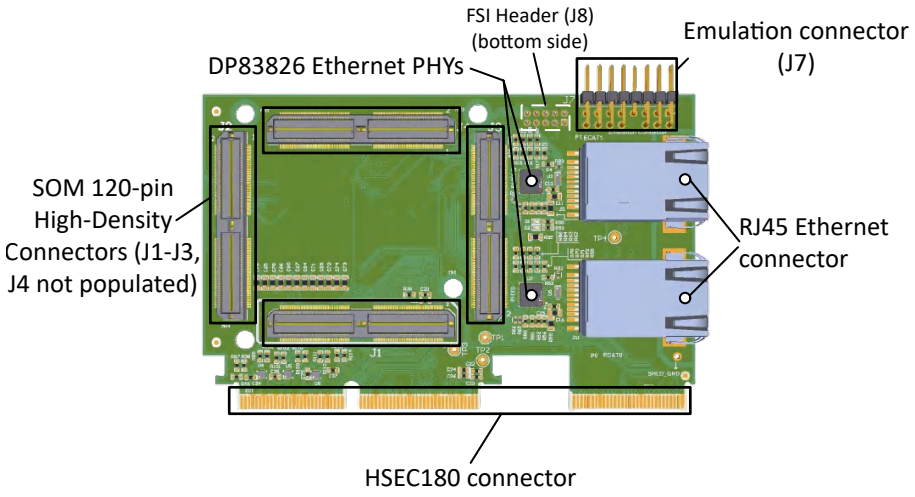


Figure 1-2. HSEC180ADAPEVM Component Identification

2 Hardware

2.1 System Description

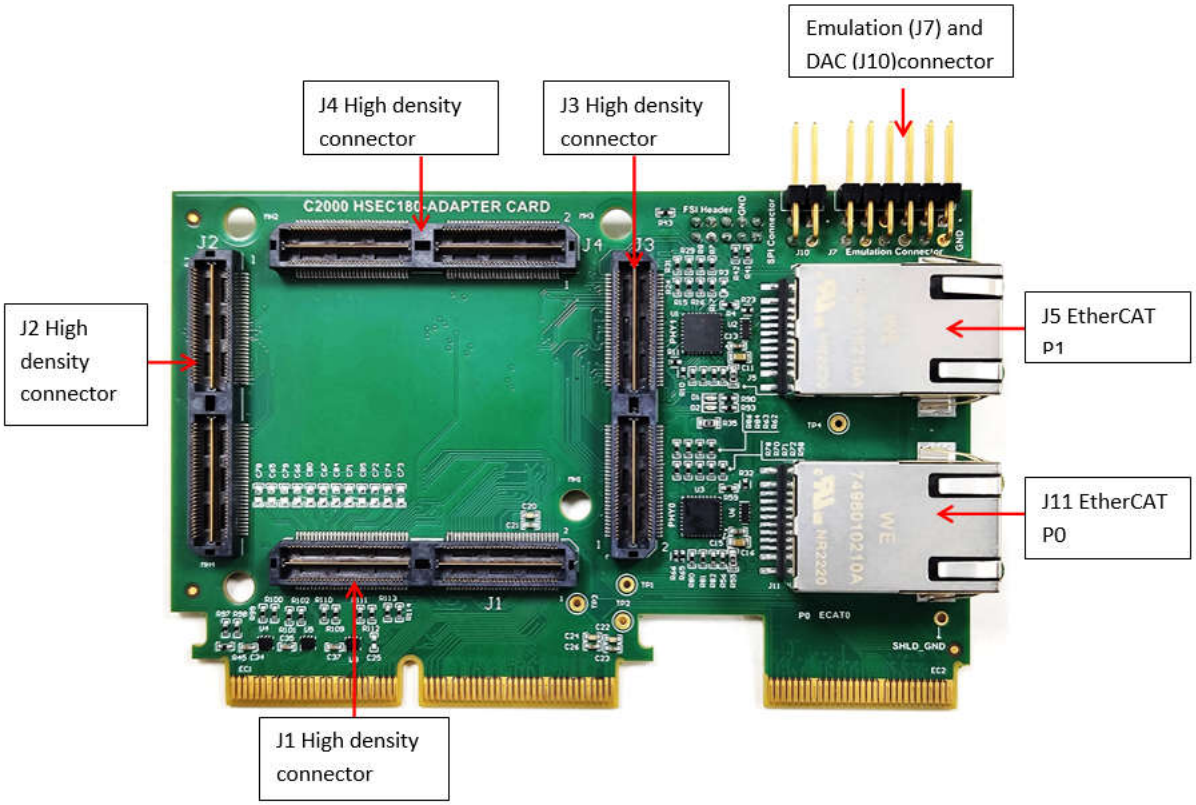


Figure 2-1. PCBA Top Side

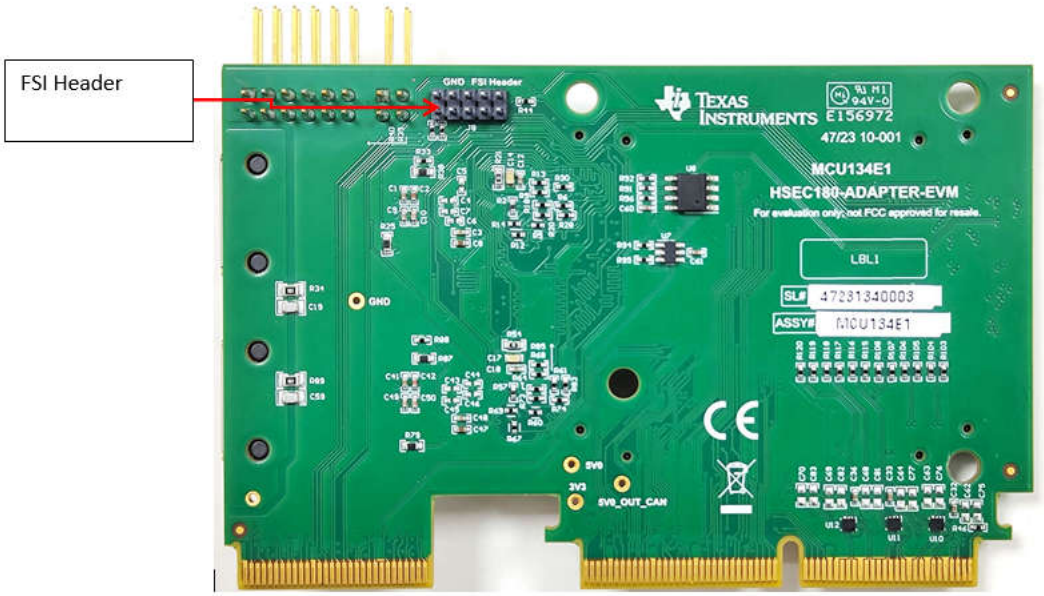


Figure 2-2. PCBA Bottom Side

2.1.1 Key Features

The HSEC Adapter board is a development platform that enables users to evaluate and develop industrial applications for Texas Instrument's C2000 F28P65x SOM board.

The following sections discuss the adapter board's key features.

2.1.1.1 Power Supply

HSEC adapter board utilizes the power from the SOM board provided by the PMIC to supply the EtherCAT PHYs and EEPROM and other components on the board.

The figure below shows the distribution of power to various.

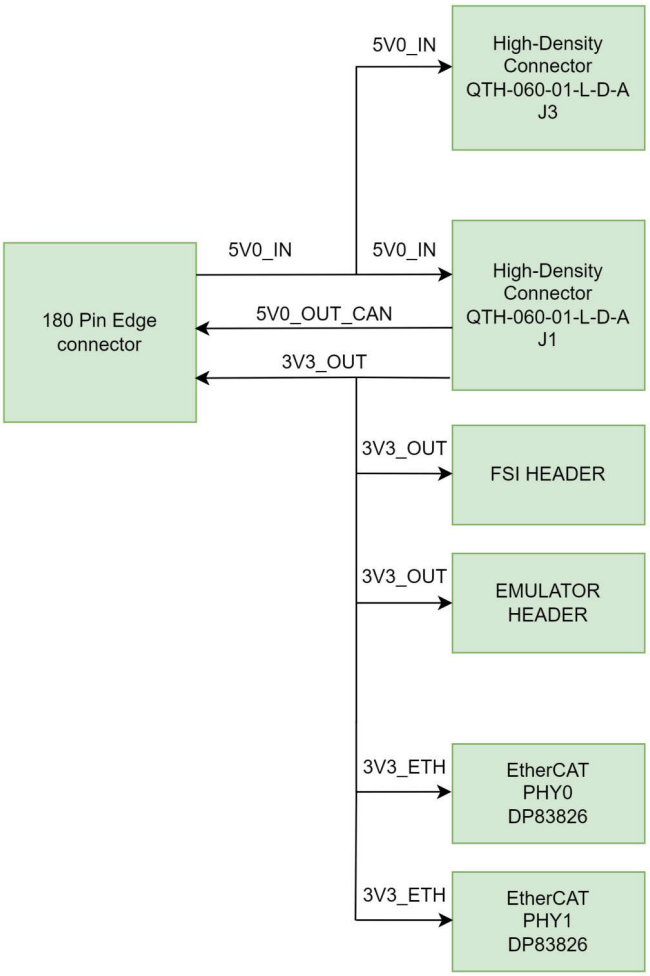


Figure 2-3. Power Tree

The following sections describe the power distribution network topology that supplies the HSEC board, supporting components, and reference voltages.

The HSEC adapter board is the input 5V source for the SOM board which is provided by the docking station. The 5V is then transferred as input to the SOM through a high-density connector, which utilizes this input to generate the powers that go to the HSEC board through a high-density connector. The HSEC adapter board gets 3V3 input from the PMIC and this is the input for the EtherCAT PHY's and EEPROM.

2.1.1.2 Memory

- 16KB Inter-Integrated Circuit (I2C) EEPROM

2.1.1.3 JTAG Emulator

- Supports 12-pin JTAG connection from external emulator.

2.1.1.4 Supported Interfaces and Peripherals

- 2x EtherCAT ports supporting 10/100 Mbps data rate on two connectors (RJ45).

2.1.1.5 Expansion Connectors/Headers to Support Application-specific Add-On Boards

- FSI header for FSI interface.
- DAC connector for interfacing DAC on XDS110 board.
- 4x High-density connector for interfacing with the SOM board.
- A 180-pin edge connector is used to connect the board with the docking station which gives the power to the system.

2.1.1.6 ADC

- ADC Clamping – ADC inputs are clamped by protection diodes.
- Anti-Aliasing Filters – Noise filters (small RC filters) can be easily added on ADC input pins.

2.1.2 Important Usage Notes:

2.1.2.1 Electrostatic Discharge (ESD) Compliance

Components installed on the product are sensitive to Electrostatic Discharge (ESD). TI recommends this product be used in ESD controlled environment. This can include a temperature or humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

2.1.2.2 IO Cable Length

The maximum length of all the IO cables must not exceed 3 meters.

2.1.3 Power ON/OFF Procedures

Power to the HSEC is provided through an external power supply to the docking station which is connected to the HSEC adapter board through finger edge pins.

2.1.3.1 Power-On Procedure

1. Connect the HSEC adapter board with the SOM board through High-density connectors J1, J2, J3, J4.
2. Connect the setup with SOM and HSEC with the docking station and attach the type C USB cable to the docking station.
3. Connect the other end of the Type-C cable to the source or Type-C source device (such as a Laptop computer).
4. Visually inspect that LED1 and LED2 are illuminated.
5. XDS110JTAG and DAC are routed to the emulation connector and DAC connector J7 and J10 respectively.

2.1.3.2 Power-Off Procedure

1. Disconnect the Type C Cable from the Laptop or Type C source.
2. Remove the USB Type-C cable from the SKEVM.

2.1.3.3 Power Test Points

Test points for each power input/output on the board are mentioned in Table 2-1.

Table 2-1. Power Test Points

Sl #	Power Supply	Test Point	Voltage
1	5V0_IN	TP1	5
2	3V3_OUT	TP2	3.3
3	5V0_OUT_CAN	TP3	5
4	IO_TGT_V	J7A.1	3.3
5	3V3_ETH	R35	3.3

2.1.4 Peripheral and Major Component Description

The following sections provide an overview of the different interfaces and circuits on the HSEC Adapter board.

2.1.4.1 Clocking

The Clock architecture of the HSEC Adapter board is shown below.

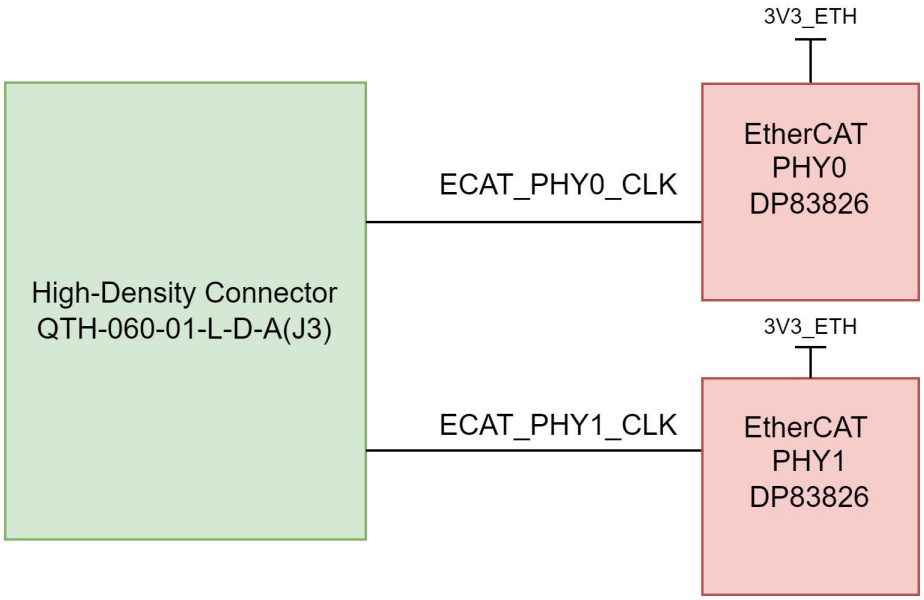


Figure 2-4. Clock Architecture

A clock generator of part number LMK1C1103PWR is used in SOM to drive the 25MHz clock to two EtherCATPHYs, and F28P65x MCU Clock. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides four 25MHz LVCMOS clock outputs. The clock signal for EtherCAT PHYs is routed from SOM to High-density connector.

2.1.4.2 EtherCAT Interface

The HSEC adapter board provides two EtherCAT interfaces for the SOM module which is going to connect with the High-density connector through the two RJ45 connectors with integrated magnetics. PHY DP83826 is configured as Enhanced mode which supports 10/100Mbps speed. Both the EtherCAT ports use a common MDIO Bus to communicate with the external PHY Transceiver.

Two Single port RJ45 Connectors Mfr Part# 7498010210A from Link-PP are used on the board for Ethernet 10/100 Connectivity. RJ45 Connectors have integrated magnetics and LEDs for indicating 100BASE-T link as well as receive or transmit activity.

Features of the DP83826:

- TX latency: 40ns, RX latency: 170ns
- Two selectable pin modes ENHANCED mode, BASIC mode
- Low power consumption of less than 160 mW
- Single, 3.3V power supply
- MAC interfaces: MII, RMII
- I/O voltages: 1.8V or 3.3V

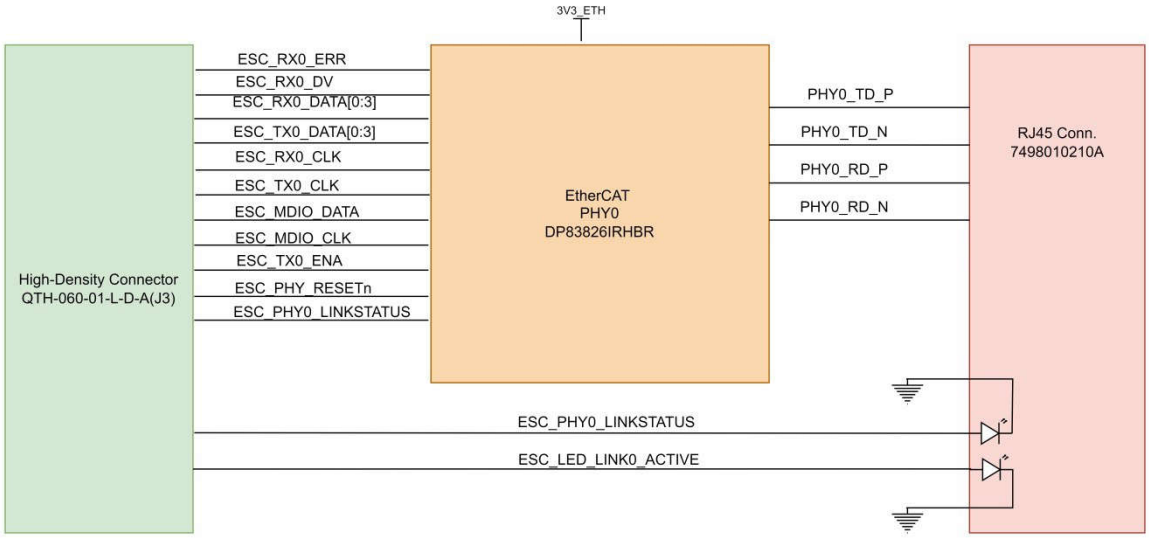


Figure 2-5. EtherCAT PHY0

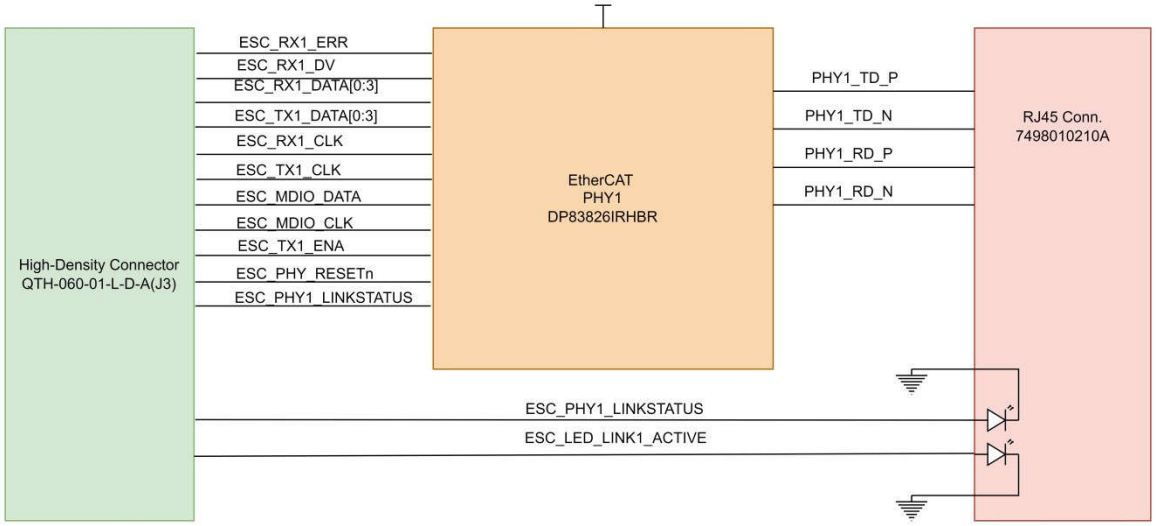


Figure 2-6. EtherCAT PHY1

2.1.4.2.1 DP83826 PHY Strapping Configuration

The DP83826 PHY uses two-level configurations based on resistor strapping which generate two distinct voltage ranges. The PHY Address strapping is provided for PHY0 to set address -000 and for the PHY1 to set address 001.

Table 2-2 shows the default values of the boot strap configurations.

Table 2-2. EtherCAT PHY Strap Value

Strap Setting	Pin Name	Strap Function	Value of Strap Function	Description
PHY address	LED0	PHY_ADD0	0/1	PHY0Address:000 PHY1 Address: 001
	CRS/LED3	PHY_ADD1	0	
	COL/LED2	PHY_ADD2	0	
MAC Mode selection	RX_D2	MAC Mode selection	1	RMII MAC mode

Table 2-2. EtherCAT PHY Strap Value (continued)

Strap Setting	Pin Name	Strap Function	Value of Strap Function	Description
RMII MAC Mode	TX_CLK	Controller/peripheral mode selection	0	RMII controller mode
	RX_D3	RMII_CRS_DV/ RMII_RX_DV	0	RMII_CRS_DV
Auto negotiation	RX_D1	auto MDIX enable/ disable	0	auto MDIX enable
	RX_D0	auto-negotiation enable/disable	0	auto-negotiation enable
	RX_DV	MDIX/MDI	0	MDIX
CLKOUT/LED1	RX_ER	CLKOUT 25MHz on Pin 31 LED1 on Pin 31	1	LED1 on Pin 31
Odd Nibble Detection	CLKOUT/LED1	Odd Nibble Detection disabled/enabled	0	Odd Nibble Detection disabled

2.1.4.3 Power

2.1.4.3.1 Power Requirement

HSEC Adapter board is powered through the 180-pin edge connector. For powering of the HSEC Adapter board, plug with the docking station and mount the SOM module. The HSEC adapter board transfers the input 5V0 voltage from the docking station to the SOM board. The SOM board has the PMIC, which provides the various powers required for the HSEC board and SOM board.

2.1.4.3.2 Power Input

The HSEC adapter board is the intermediate board to transfer the input 5V0 voltage to the SOM from docking station. The input source for the HSEC is from the 180-pin edge connector. The SOM board provides the 3V3 voltages which required for the various peripherals in the HSEC board.

Figure 2-7 shows the power architecture of the HSEC adapter board.

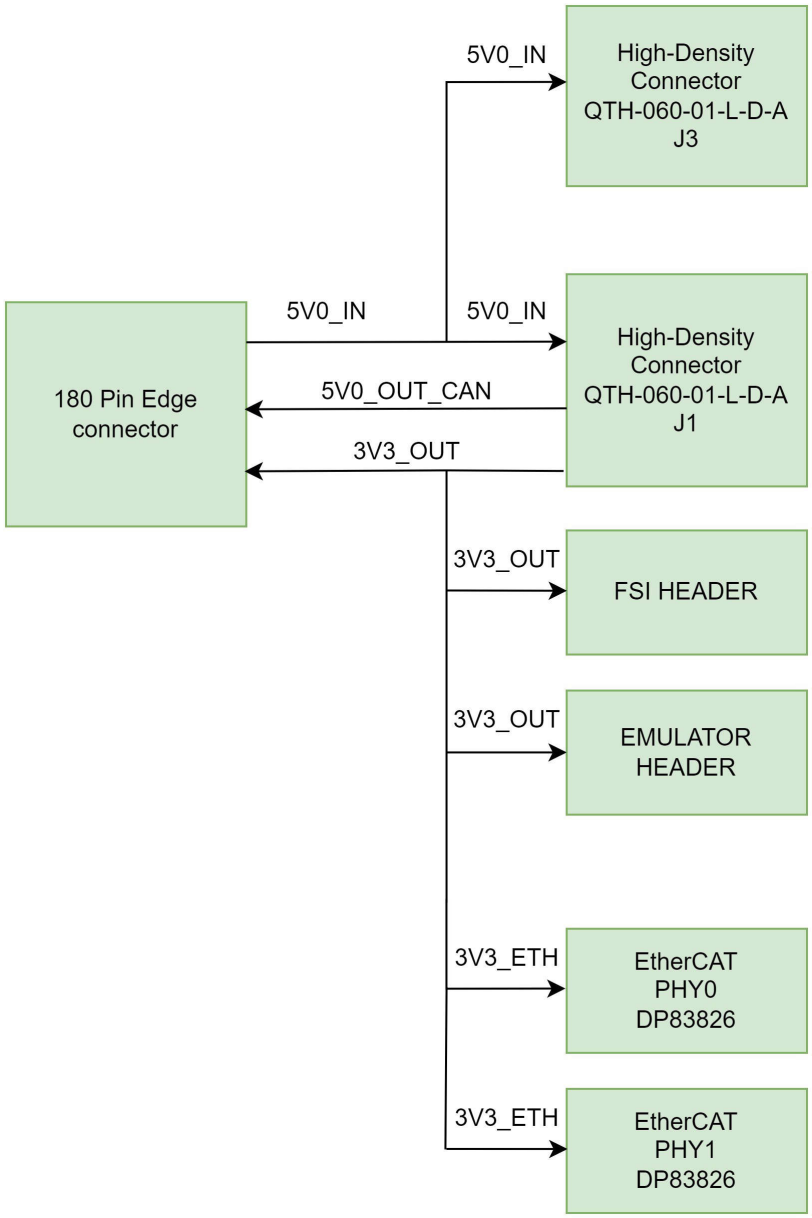


Figure 2-7. Power Architecture

2.1.4.4 Emulator Connector (TSW-106-16-G-D) and DAC Connector (TSW-102-16-G-D)

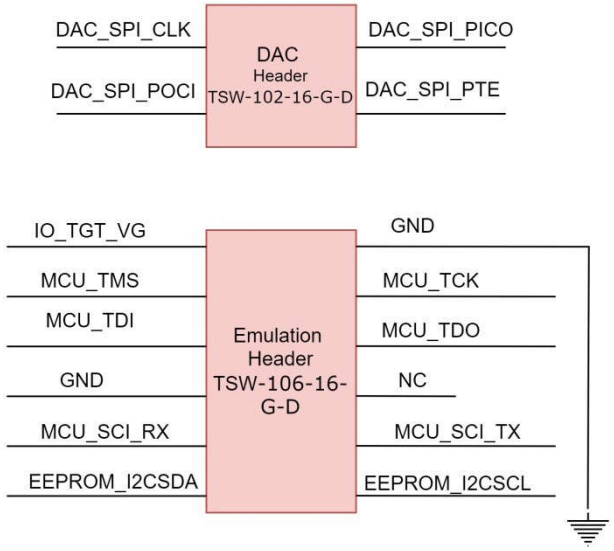


Figure 2-8. Isolated Signal from XDS110 Board Mating Connector

Find Table 2-3 and Table 2-4 for the connector pins details with the interfaced signal names.

Table 2-3. 4 Pin DAC Connector

Pin No	Signal	Pin No	Signal
1	DAC_SPI_CLK	2	DAC_SPI_PICO
3	DAC_SPI_POCI	4	DAC_SPI_PTE

Table 2-4. 12 Pin Emulator Connector

Pin No	Signal	Pin No	Signal
1	IO_TGT_V	2	GND
3	MCU_TMS	4	MCU_TCK
5	MCU_TDI	6	MCU_TDO
7	GND	8	NC
9	MCU_SCI_RX	10	MCU_SCI_TX
11	EEPROM_I2CSDA	12	EEPROM_I2CSCL

2.1.4.4.1 TSW-106-16-G-D

The TSW-106-16-G-D is a Mating part for SSW-106-02-G-D-RA connector on the isolated section of XDS110 boards. The connector supports I2C, UART and JTAG Interfaces.

2.1.4.4.2 TSW-102-16-G-D

The TSW-102-16-G-D is a mating part for SSW-102-02-G-D-RA connector on the isolated section of XDS110 boards. The connector supports SPI signals.

2.1.4.5 FSI Header

Figure 2-9 shows the FSI header connection to the High-density connector.

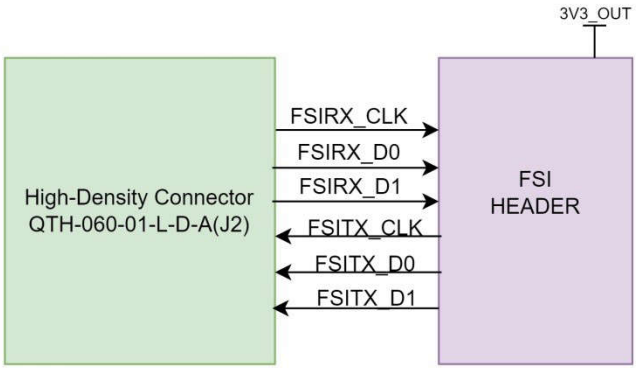


Figure 2-9. FSI Header

2.1.4.6 High Density Connector

There are four High density connectors in the HSEC Adapter Board which are referenced as J1, J2, J3 and J4.

J1 Connector

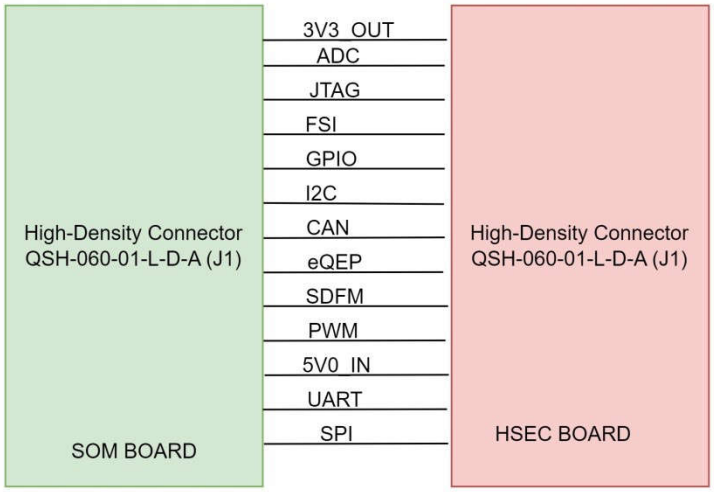


Figure 2-10. J1 Connector

J1 connector supports the ADC (Analog to Digital Converter), FSI (Fast serial interface), eQEP (Enhanced quadrature encoder plus), SDFM (Sigma Delta Filter Module), I2C, JTAG, CAN, PWM, SPI, UART, and GPIO signals. Also, the HSEC Adapter board get the 3V3 supply from the J1 connector.

J2 Connector

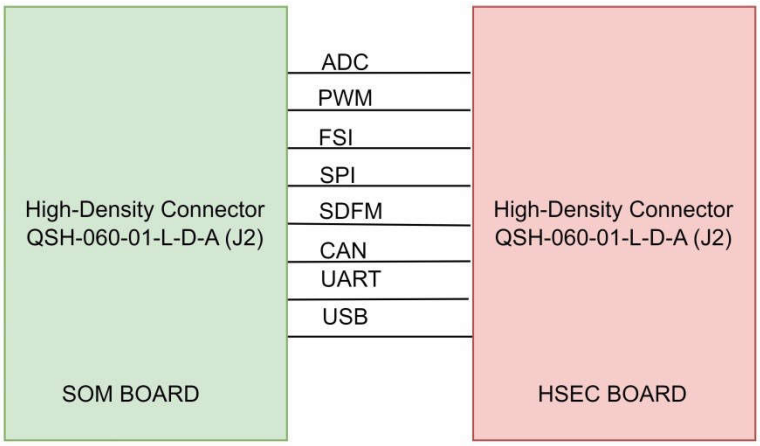


Figure 2-11. J2 Connector

J2 connector supports the ADC (Analog to digital converter), FSI (Fast serial interface), SDFM (Sigma Delta Filter), PWM, SPI, CAN, UART, and USB signals.

J3 Connector

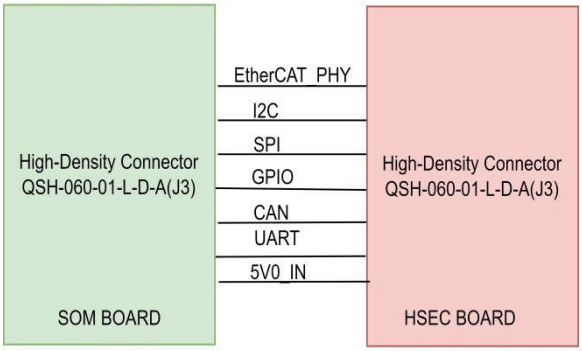


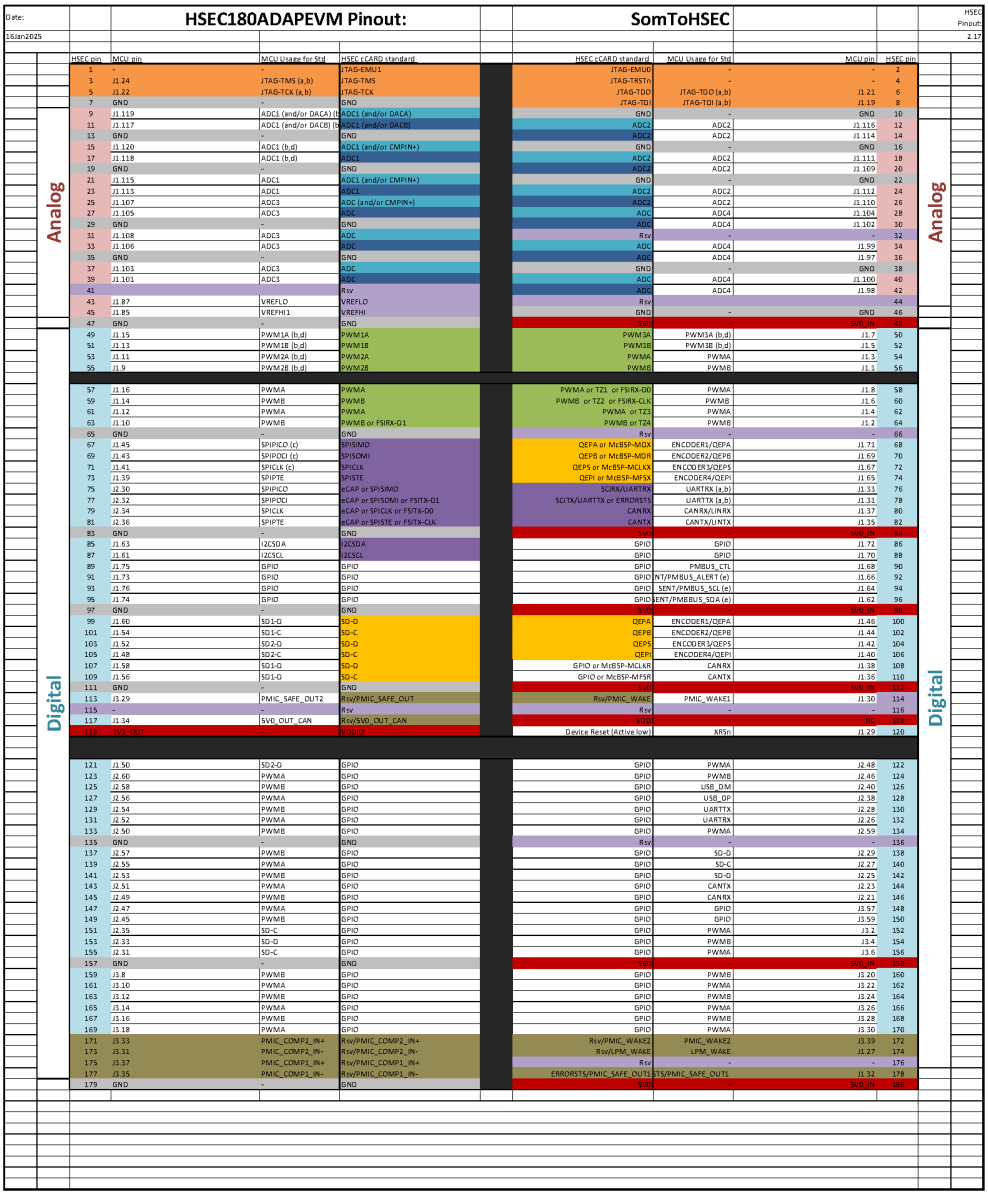
Figure 2-12. J3 Connector

J3 connector supports the SPI, CAN, I2C, GPIO, UART and EtherCAT PHY. Also, HSEC module gets the power from the J3 connector.

2.1.4.6.1 180-pin HSEC Edge Connector

The 180-pin HSEC edge connector provides the power to the SOM, which is going to connect with the HSEC through a high-density connector. For powering and validating various interfaces the 180-pin edge connector is mated with the docking station (TMDSHSECDOCK). The interfaces like SPI, I2C, UART, FSI, JTAG, ADC can be validated through the docking station pins.

Refer to the image below for the connector pins details with the interfaced signal names.



Date:		HSEC180ADAPEVM Pinout:				SomToHSEC				HSEC Pinout:
16Jan2025										2.17
	HSEC pin	MCU pin	MCU Usage for Std	HSEC cCARD standard		HSEC cCARD standard	MCU Usage for Std	MCU pin	HSEC pin	
Analog	1	-	-	JTAG-EMU1		JTAG-EMU0	-	-	2	Analog
	3	J1.24	JTAG-TMS (a,b)	JTAG-TMS		JTAG-TRSTn	-	-	4	
	5	J1.22	JTAG-TCK (a,b)	JTAG-TCK		JTAG-TDO	JTAG-TDO (a,b)	J1.21	6	
	7	GND	-	GND		JTAG-TDI	JTAG-TDI (a,b)	J1.19	8	
	9	J1.119	ADC1 (and/or DACA) (b	ADC1 (and/or DACA)		GND	-	GND	10	
	11	J1.117	ADC1 (and/or DACB) (b	ADC1 (and/or DACB)		ADC2	ADC2	J1.116	12	
	13	GND	-	GND		ADC2	ADC2	J1.114	14	
	15	J1.120	ADC1 (b,d)	ADC1 (and/or CMPIN+)		GND	-	GND	16	
	17	J1.118	ADC1 (b,d)	ADC1		ADC2	ADC2	J1.111	18	
	19	GND	-	GND		ADC2	ADC2	J1.109	20	
	21	J1.115	ADC1	ADC1 (and/or CMPIN+)		GND	-	GND	22	
	23	J1.113	ADC1	ADC1		ADC2	ADC2	J1.112	24	
	25	J1.107	ADC3	ADC (and/or CMPIN+)		ADC2	ADC2	J1.110	26	
	27	J1.105	ADC3	ADC		ADC	ADC4	J1.104	28	
	29	GND	-	GND		ADC	ADC4	J1.102	30	
	31	J1.108	ADC3	ADC		Rsv	-	-	32	
	33	J1.106	ADC3	ADC		ADC	ADC4	J1.99	34	
	35	GND	-	GND		ADC	ADC4	J1.97	36	
	37	J1.103	ADC3	ADC		GND	-	GND	38	
	39	J1.101	ADC3	ADC		ADC	ADC4	J1.100	40	
	41			Rsv		ADC	ADC4	J1.98	42	
	43	J1.87	VREFLO	VREFLO		Rsv			44	
	45	J1.85	VREFH1	VREFHI		GND	-	GND	46	
	47	GND	-	GND		5V0	-	5V0_IN	48	
	49	J1.15	PWM1A (b,d)	PWM1A		PWM3A	PWM3A (b,d)	J1.7	50	
	51	J1.13	PWM1B (b,d)	PWM1B		PWM3B	PWM3B (b,d)	J1.5	52	
	53	J1.11	PWM2A (b,d)	PWM2A		PWM4	PWM4A	J1.3	54	
	55	J1.9	PWM2B (b,d)	PWM2B		PWM5	PWM5	J1.1	56	
Digital	57	J1.16	PWM4	PWM4		PWM4 or TZ1 or FSIRX-D0	PWM4	J1.8	58	Digital
	59	J1.14	PWM5	PWM5		PWM5 or TZ2 or FSIRX-CLK	PWM5	J1.6	60	
	61	J1.12	PWM4	PWM4		PWM4 or TZ3	PWM4	J1.4	62	
	63	J1.10	PWM5	PWM5 or FSIRX-D1		PWM5 or TZ4	PWM5	J1.2	64	
	65	GND	-	GND		Rsv	-	-	66	
	67	J1.45	SPIPICO (c)	SPISIMO		QEPA or McBSP-MDX	ENCODER1/QEPA	J1.71	68	
	69	J1.43	SPIPOCI (c)	SPISOMI		QEPB or McBSP-MDR	ENCODER2/QEPB	J1.69	70	
	71	J1.41	SPICLK (c)	SPICLK		QEPS or McBSP-MCLKX	ENCODER3/QEPS	J1.67	72	
	73	J1.39	SPIPTE	SPISTE		QEPI or McBSP-MFSX	ENCODER4/QEPI	J1.65	74	
	75	J2.30	SPIPICO	eCAP or SPISIMO		SCIRX/UARTRX	UARTRX (a,b)	J1.33	76	
	77	J2.32	SPIPOCI	eCAP or SPISOMI or FSITX-D1		SCITX/UARTTX or ERROrSTS	UARTTX (a,b)	J1.31	78	
	79	J2.34	SPICLK	eCAP or SPICLK or FSITX-D0		CANRX	CANRX/LINRX	J1.37	80	
	81	J2.36	SPIPTE	eCAP or SPISTE or FSITX-CLK		CANTX	CANTX/LINTX	J1.35	82	
	83	GND	-	GND		5V0	-	5V0_IN	84	
	85	J1.63	I2CSDA	I2CSDA		GPIO	GPIO	J1.72	86	
	87	J1.61	I2CSCL	I2CSCL		GPIO	GPIO	J1.70	88	
	89	J1.75	GPIO	GPIO		GPIO	PMBUS_CTL	J1.68	90	
	91	J1.73	GPIO	GPIO		GPIO	NT/PMBUS_ALERT (e)	J1.66	92	
	93	J1.76	GPIO	GPIO		GPIO	SENT/PMBUS_SCL (e)	J1.64	94	
	95	J1.74	GPIO	GPIO		GPIO	ENT/PMBUS_SDA (e)	J1.62	96	
	97	GND	-	GND		5V0	-	5V0_IN	98	
	99	J1.60	SD1-D	SD-D		QEPA	ENCODER1/QEPA	J1.46	100	
	101	J1.54	SD1-C	SD-C		QEPB	ENCODER2/QEPB	J1.44	102	
	103	J1.52	SD2-D	SD-D		QEPS	ENCODER3/QEPS	J1.42	104	
	105	J1.48	SD2-C	SD-C		QEPI	ENCODER4/QEPI	J1.40	106	
	107	J1.58	SD1-D	SD-D		GPIO or McBSP-MCLKR	CANRX	J1.38	108	
	109	J1.56	SD1-D	SD-C		GPIO or McBSP-MFSR	CANTX	J1.36	110	
	111	GND	-	GND		5V0	-	5V0_IN	112	
	113	J3.29	PMIC_SAFE_OUT2	Rsv/PMIC_SAFE_OUT		Rsv/PMIC_WAKE	PMIC_WAKE1	J1.30	114	
	115	-		Rsv		Rsv	-	-	116	
	117	J1.34	5V0_OUT_CAN	Rsv/5V0_OUT_CAN		VPU		NC	118	
	119	3V3_OUT		3V3IO		Device Reset (Active low)	XRSn	J1.29	120	
	121	J1.50	SD2-D	GPIO		GPIO	PWM4	J2.48	122	
	123	J2.60	PWM4	GPIO		GPIO	PWM8	J2.46	124	
	125	J2.58	PWM8	GPIO		GPIO	USB_DM	J2.40	126	
	127	J2.56	PWM4	GPIO		GPIO	USB_DP	J2.38	128	
	129	J2.54	PWM8	GPIO		GPIO	UARTTX	J2.28	130	
	131	J2.52	PWM4	GPIO		GPIO	UARTRX	J2.26	132	
	133	J2.50	PWM8	GPIO		GPIO	PWM4	J2.59	134	
	135	GND	-	GND		Rsv	-	-	136	
	137	J2.57	PWM8	GPIO		GPIO	SD-D	J2.29	138	
	139	J2.55	PWM4	GPIO		GPIO	SD-C	J2.27	140	
	141	J2.53	PWM8	GPIO		GPIO	SD-D	J2.25	142	
	143	J2.51	PWM4	GPIO		GPIO	CANTX	J2.23	144	
	145	J2.49	PWM8	GPIO		GPIO	CANRX	J2.21	146	
	147	J2.47	PWM4	GPIO		GPIO	GPIO	J3.57	148	
	149	J2.45	PWM8	GPIO		GPIO	GPIO	J3.59	150	
	151	J2.35	SD-C	GPIO		GPIO	PWM4	J3.2	152	
	153	J2.33	SD-D	GPIO		GPIO	PWM8	J3.4	154	
	155	J2.31	SD-C	GPIO		GPIO	PWM4	J3.6	156	
	157	GND	-	GND		5V0	-	5V0_IN	158	
	159	J3.8	PWM8	GPIO		GPIO	PWM8	J3.20	160	
	161	J3.10	PWM4	GPIO		GPIO	PWM4	J3.22	162	
	163	J3.12	PWM8	GPIO		GPIO	PWM8	J3.24	164	
	165	J3.14	PWM4	GPIO		GPIO	PWM4	J3.26	166	
	167	J3.16	PWM8	GPIO		GPIO	PWM8	J3.28	168	
	169	J3.18	PWM4	GPIO		GPIO	PWM4	J3.30	170	
	171	J3.33	PMIC_COMP2_IN+	Rsv/PMIC_COMP2_IN+		Rsv/PMIC_WAKE2	PMIC_WAKE2	J3.39	172	
	173	J3.31	PMIC_COMP2_IN-	Rsv/PMIC_COMP2_IN-		Rsv/LPM_WAKE	LPM_WAKE	J1.27	174	
	175	J3.37	PMIC_COMP1_IN+	Rsv/PMIC_COMP1_IN+		Rsv	-	-	176	
	177	J3.35	PMIC_COMP1_IN-	Rsv/PMIC_COMP1_IN-		ERRORSTS/PMIC_SAFE_OUT1	STS/PMIC_SAFE_OUT1	J1.32	178	
	179	GND	-	GND		5V0		5V0_IN	180	

2.1.4.7 Use Case for HSEC Adapter Board

2.1.4.7.1 Case 1: Isolated XDS110 on HSEC Adapter, SOM ,Baseboard

SOM plugs into the HSEC adapter (through 4 High-density connectors J1, J2, J3, J4), 180-pin edge connector (EC1 & EC2) of HSEC adapter plugs into the docking station and XDS110 isolated connector (J3 & J4) plugs vertically into Emulation header (J7) and DAC header (J10) of HSEC adapter board.

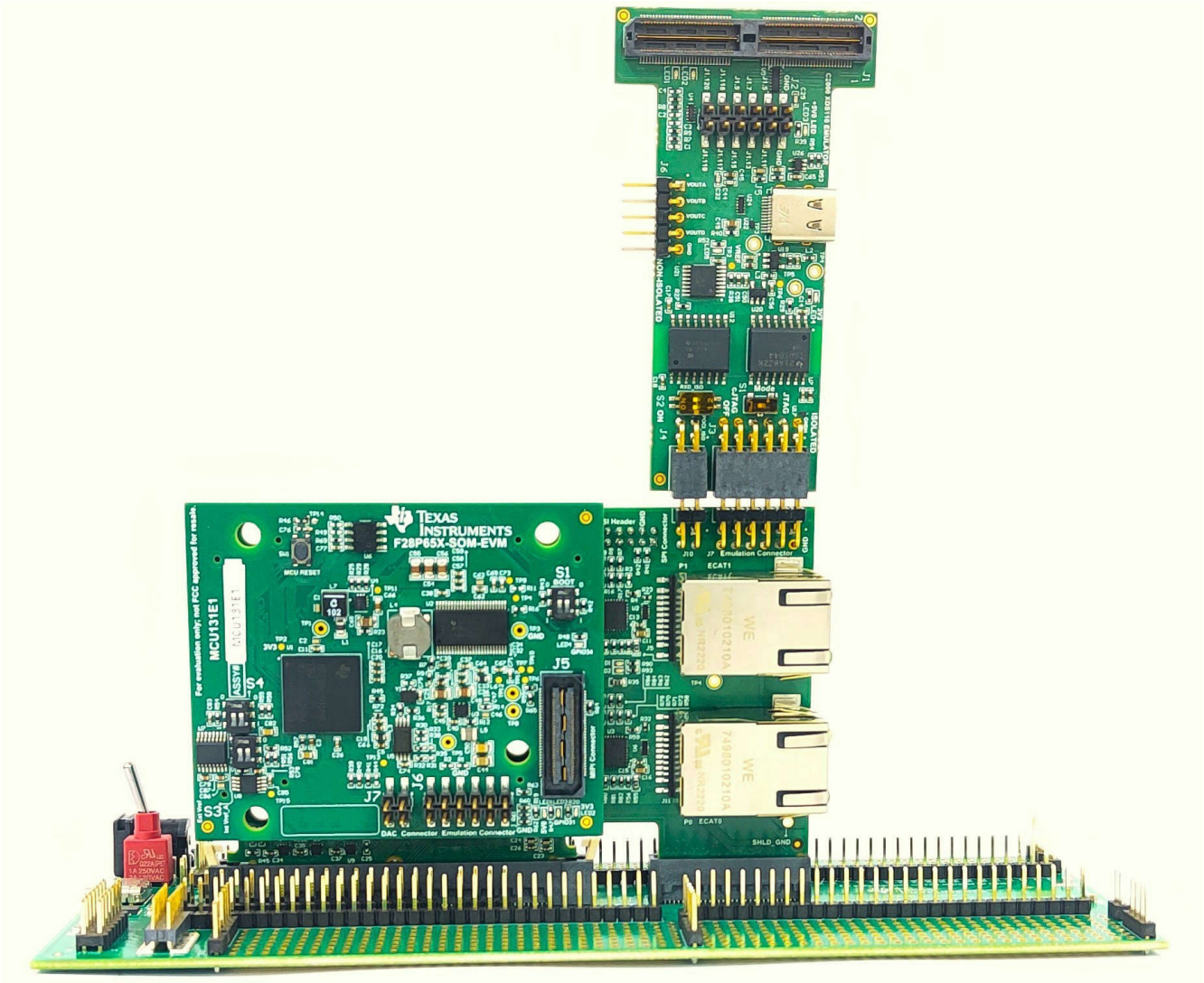


Figure 2-13. Isolated XDS110 on HSEC Adapter + SOM

2.1.4.7.2 Case 2: HSEC Adapter, Isolated XDS110 on SOM, Baseboard

SOM plugs into the HSEC adapter (through 4 High-density connectors J1, J2, J3, J4), 180-pin edge connector (EC1 & EC2) of HSEC adapter plugs into the docking station and XDS110 isolated connector (J3 & J4) plugs horizontally into Emulation header (J6) and DAC header (J7) of SOM.

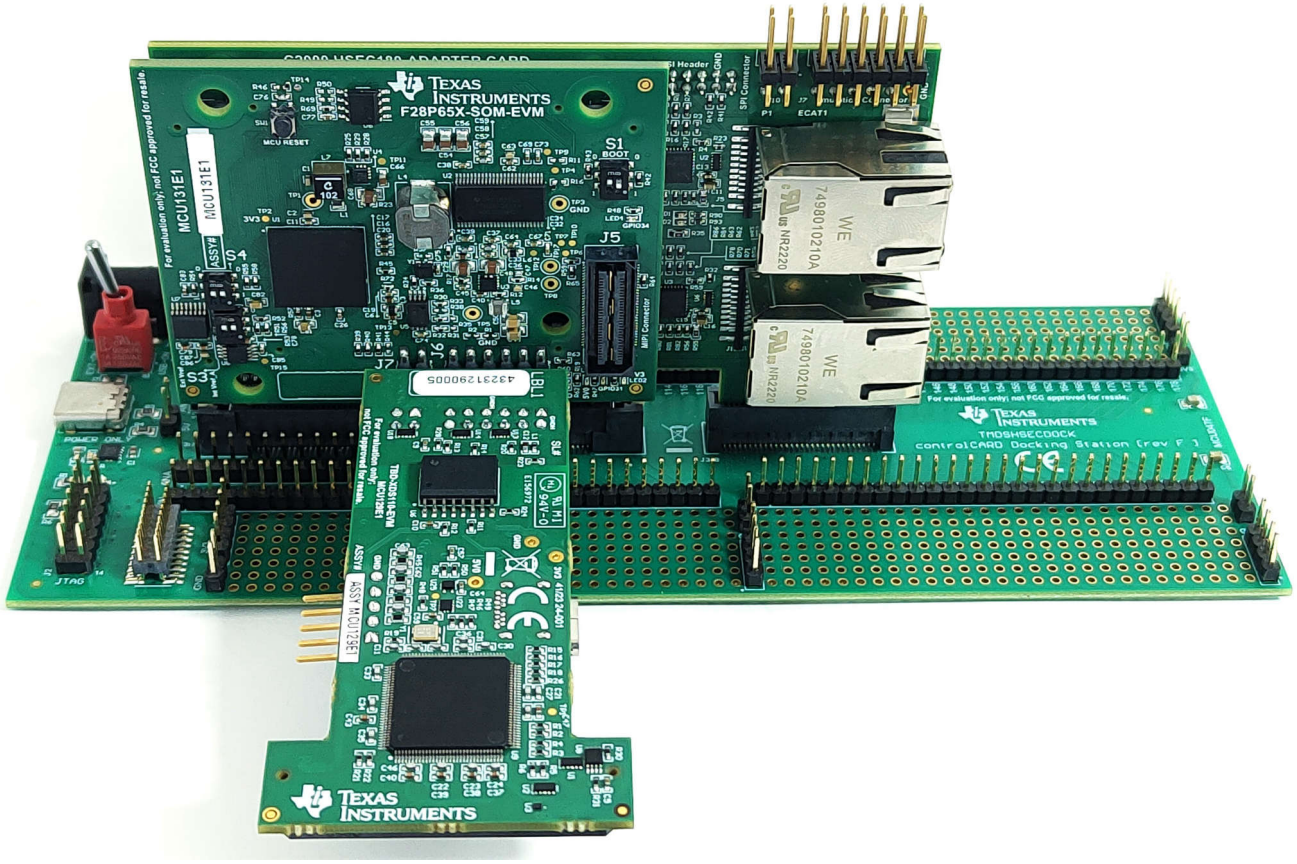


Figure 2-14. HSEC Adapter and Isolated XDS110 on SOM

3 Hardware Design Files

The HSEC180ADAPEVM design files can be found on the EVM tool page.

4 Additional Information

4.1 Known Hardware or Software Issues

This section describes the known exceptions to the EVM functional specification (advisories). This section also contains EVM usage notes. Usage notes describe situations where the EVM's behavior may not match the presumed or documented behavior.

4.1.1 EVM Usage Notes

Incorrect Silkscreen Labeling for POCI and PICO Pins

Revisions Affected: All

Pin 14 of the Emulator Header (J7) is incorrectly labeled as POCI on the PCB silkscreen. The correct label for this pin is PICO.

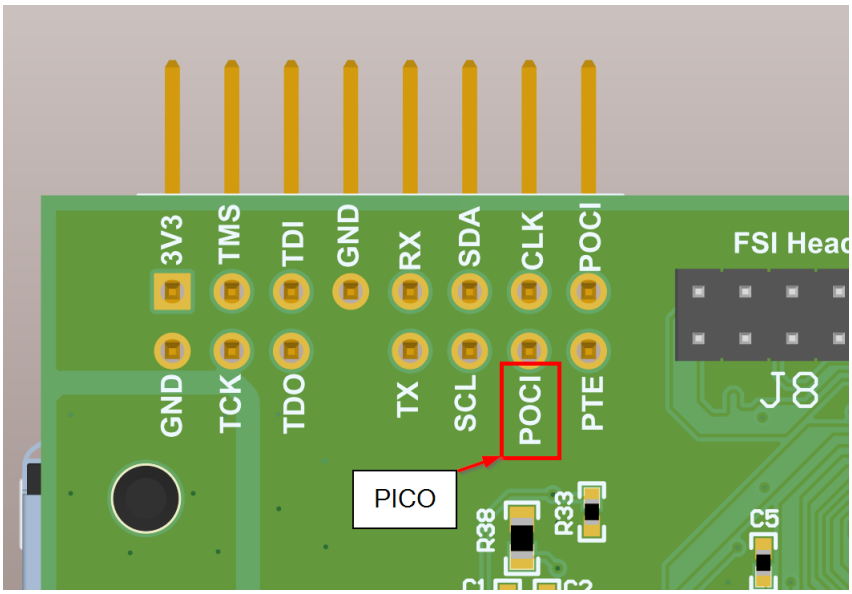


Figure 4-1. Emulation Header Silkscreen Correction

4.2 Trademarks

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 24, 2024 to January 28, 2025 (from Revision * (June 2024) to Revision A (January 2025)) **Page**

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NOTE:

EXPOSURE TO ELECTROSTATIC DISCHARGE (ESD) MAY CAUSE DEGREDATION OR FAILURE OF THE EVALUATION KIT; TI RECOMMENDS STORAGE OF THE EVALUATION KIT IN A PROTECTIVE ESD BAG.

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3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

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