Application Note

TMS570LC-SEP Single Event Latch-Up (SEL) Radiation Report

ABSTRACT

The purpose of this study is to characterize the effects of heavy-ion irradiation on the single-event latch-up (SEL) performance of the TMS570LC4357-SEP, Arm® Cortex®-R based microcontroller. Heavy-ions with an LET_{eff} of 48 MeV-cm^2/mg were used to irradiate the devices with a fluence of 1 x 10^7 ions/cm^2. The results demonstrate that TMS570LC4357-SEP is SEL-free up to LET_{eff} of 48 MeV-cm^2/mg at 125°C.

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1 Introduction

The TMS570LC4357-SEP is a high-performance Arm Cortex-R based microcontroller which has on-chip diagnostic features including: dual CPUs in lockstep, Built-In Self-Test (BIST) logic for CPU, the N2HET coprocessors, and for on-chip SRAMs; ECC protection on the L1 caches, L2 flash, and SRAM memories. The device also supports ECC or parity protection on peripheral memories and loopback capability on peripheral I/Os.

The device integrates two Arm Cortex-R5F floating-point CPUs, operating in lockstep, which offer an efficient 1.66 DMIPS/MHz, and can run up to 300 MHz providing up to 498 DMIPS. The device supports the big-endian [BE32] format.

With integrated safety features and a wide choice of communication and control peripherals, the TMS570LC4357-SEP device is an ideal solution for high-performance real-time control applications with safety critical requirements

Table 1-1. Overview Information (1)

Description	Device Information
TI Part Number	TMS570LC4357-SEP
Device Function	Arm Cortex-R based microcontroller
Package	337 GWT (nFBGA)
Technology	12F021.M7C
Exposure Facility	Radiation Effect Facility, Cyclotron Institute, Texas A&M University
Heavy Ion Fluence per Run	1 x 10^6 - 1 x 10^7 ions/cm^2
Irradiation Temperature	125°C (for SEL testing)

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2 SEE Mechanisms

The primary single-event effect (SEE) event of interest in the TMS570LC4357-SEP is the destructive single-event latch-up (SEL). From a risk/impact point of view, the occurrence of an SEL is potentially the most destructive SEE event, and the biggest concern for space applications. The 12F021 (CMOS) process node was used for the TMS570LC4357-SEP. CMOS circuitry introduces a potential for SEL susceptibility. SEL can occur if excess current injection caused by the passage of an energetic ion is high enough to trigger the formation of a parasitic cross-coupled PNP and NPN bipolar structure (formed between the p-sub and n-well and N+ and P+ contacts). The parasitic bipolar structure initiated by a single-event creates a high-conductance path (inducing a steady-state current that is typically orders-of-magnitude higher than the normal operating current) between the power and ground that persists (is "latched") until power is removed, or until the device is destroyed by the high-current state. The process modifications applied for the SEL-mitigation were sufficient, as the TMS570LC4357-SEP exhibited no SEL with heavy-ions up to an LET_{eff} of 48 MeV-cm^2/mg at a fluence of 1 x 10^7 ions/cm^2 and a chip temperature of 125°C.

This study was performed to evaluate the SEL effects with a bias voltage of VCCAD = 5.25 V; VCCIO = 3.6 V; VCC(core) = 1.32 V supply voltages. Heavy (^{47}Ag) ions with LET_{eff} of 48 MeV-cm^2/mg were used to irradiate the devices. Flux of 10^5 ions/s-cm^2 and fluence of 10^7 ions/cm^2 were used during the exposure at 125°C temperature.

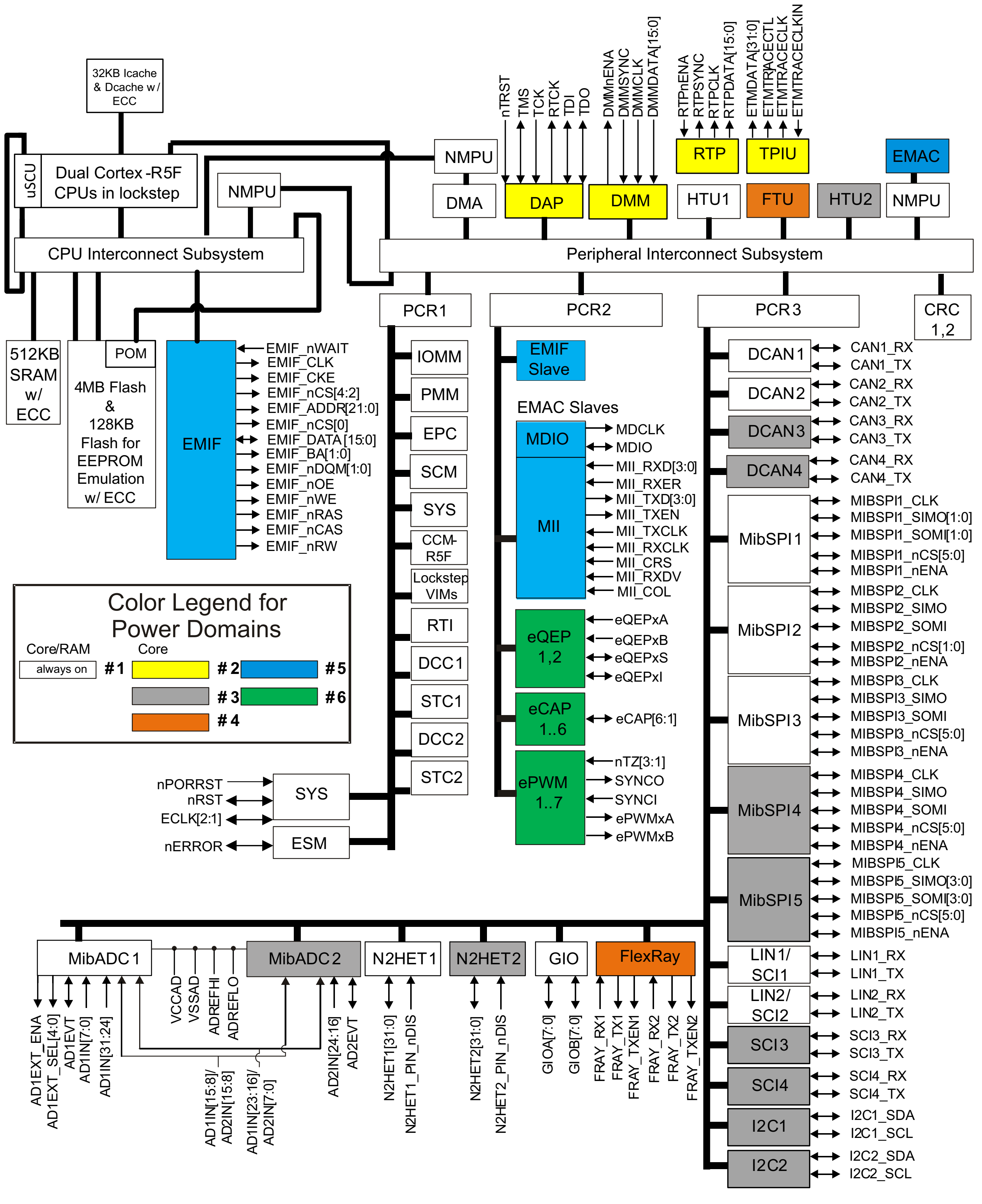

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Figure 2-1. Functional Block Diagram of the TMS570LC4357-SEP

3 Test Device Information

The TMS570LC4357-SEP is packaged in a 337-pin (GWT) BGA terminal grid array. Figure 3-1 shows the I/O-signal and Power-Supply definitions for the package, and Table 3-1 shows the power supply bias during the SEL heavy ion testing.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	
19	VSS	VSS	TMS	N2HET1 [10]	MIBSPI5 NCS[0]	MIBSPI1 SIMO[0]	MIBSPI1 NENA	MIBSPI5 CLK	MIBSPI5 SIMO[0]	N2HET1 [28]	DMM_DATA[0]	DCAN3RX	AD1EVT	AD1IN[15] / AD2IN[15]	AD1IN[22] / AD2IN[06]	AD1IN [06]	AD1IN[11] / AD2IN[11]	AD2IN[24]	VSSAD	19
18	VSS	TCK	TDO	nTRST	N2HET1 [08]	MIBSPI1 CLK	MIBSPI1 SOMI[0]	MIBSPI5 NENA	MIBSPI5 SOMI[0]	N2HET1 [0]	DMM_DATA[1]	DCAN3TX	AD1IN[24]	AD1IN[08] / AD2IN[08]	AD1IN[14] / AD2IN[14]	AD1IN[13] / AD2IN[13]	AD1IN [04]	AD1IN [02]	AD2IN[24]	18
17	TDI	nRST	EMIF_ADDR[21]	EMIF_nWE	MIBSPI5 SOMI[1]	DMM_CLK	MIBSPI5 SIMO[3]	MIBSPI5 SIMO[2]	N2HET1 [31]	EMIF_nCS[3]	EMIF_nCS[2]	EMIF_nCS[4]	EMIF_nCS[0]	AD1IN[25]	AD1IN [05]	AD1IN [03]	AD1IN[10] / AD2IN[10]	AD1IN [01]	AD1IN[09] / AD2IN[09]	17
16	RTCK	FRAY TXEN1	EMIF_ADDR[20]	EMIF_BA[1]	MIBSPI5 SIMO[1]	DMM_nENA	MIBSPI5 SOMI[3]	MIBSPI5 SOMI[2]	DMM_SYNC	N2HET2 [08]	N2HET2 [09]	N2HET2 [10]	N2HET2 [11]	AD1IN[26]	AD1IN[23] / AD2IN[07]	AD1IN[12] / AD2IN[12]	AD1IN[19] / AD2IN[03]	ADREFLO	VSSAD	16
15	FRAYRX1	FRAYTX1	EMIF_ADDR[19]	EMIF_ADDR[18]	ETM DATA[06]	ETM DATA[05]	ETM DATA[04]	ETM DATA[03]	ETM DATA[02]	ETM DATA[16] / EMIF_DATA[0]	ETM DATA[17] / EMIF_DATA[1]	ETM DATA[18] / EMIF_DATA[2]	ETM DATA[19] / EMIF_DATA[3]	AD1IN[27]	AD1IN[28]	AD1IN[21] / AD2IN[05]	AD1IN[20] / AD2IN[04]	ADREFHI	VCCAD	15
14	N2HET1 [26]	nERROR	EMIF_ADDR[17]	EMIF_ADDR[16]	ETM DATA[07]	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	VCCIO	VCCIO	VCCIO	AD1IN[29]	AD1IN[30]	AD1IN[18] / AD2IN[02]	AD1IN [07]	AD1IN [0]	14
13	N2HET1 [17]	N2HET1 [19]	EMIF_ADDR[15]	N2HET2 [04]	ETM DATA[12] / EMIF_BA[0]	VCCIO								VCCIO	ETM DATA[01]	AD1IN[31]	AD1IN[17] / AD2IN[01]	AD1IN[16] / AD2IN[0]	AD2IN[16]	13
12	ECLK	N2HET1 [04]	EMIF_ADDR[14]	N2HET2 [05]	ETM DATA[13] / EMIF_nOE	VCCIO		VSS	VSS	VCC	VSS	VSS		VCCIO	ETM DATA[0]	MIBSPI5 NCS[3]	AD2IN[19]	AD2IN[18]	AD2IN[17]	12
11	N2HET1 [14]	N2HET1 [30]	EMIF_ADDR[13]	N2HET2 [06]	ETM DATA[14] / EMIF_nDQM[1]	VCCIO		VSS	VSS	VSS	VSS	VSS		VCCPLL	ETM TRACE CTL	AD2IN[20]	AD2IN[21]	AD2IN[22]	AD2IN[23]	11
10	DCAN1TX	DCAN1RX	EMIF_ADDR[12]	ePWM1B	ETM DATA[15] / EMIF_nDQM[0]	VCC		VCC	VSS	VSS	VSS	VCC		VCC	ETM TRACE CLKOUT	AD2EVT	MIBSPI1 NCS[4]	MIBSPI3 NCS[0]	GIOB[3]	10
9	N2HET1 [27]	FRAY TXEN2	EMIF_ADDR[11]	ePWM1A	ETM DATA[08] / EMIF_ADDR[5]	VCC		VSS	VSS	VSS	VSS	VSS		VCCIO	ETM TRACE CLKIN	MDCLK	MIBSPI1 NCS[5]	MIBSPI3 CLK	MIBSPI3 NENA	9
8	FRAYRX2	FRAYTX2	EMIF_ADDR[10]	N2HET2[1]	ETM DATA[09] / EMIF_ADDR[4]	VCCP		VSS	VSS	VCC	VSS	VSS		VCCIO	ETM DATA[31] / EMIF_DATA[15]	N2HET2 [23]	MII_TXD [0]	MIBSPI3 SOMI	MIBSPI3 SIMO	8
7	LIN1RX	LIN1TX	EMIF_ADDR[9]	N2HET2 [2]	ETM DATA[10] / EMIF_ADDR[3]	VCCIO								VCCIO	ETM DATA[30] / EMIF_DATA[14]	N2HET2 [22]	MII_TX_CLK	N2HET1 [09]	nPORRST	7
6	GIOA[4]	MIBSPI5 NCS[1]	EMIF_ADDR[8]	N2HET2 [0]	ETM DATA[11] / EMIF_ADDR[2]	VCCIO	VCCIO	VCCIO	VCCIO	VCC	VCC	VCCIO	VCCIO	VCCIO	ETM DATA[29] / EMIF_DATA[13]	N2HET2 [21]	MII_RX_DV	N2HET1 [05]	MIBSPI5 NCS[2]	6
5	GIOA[0]	GIOA[5]	EMIF_ADDR[7]	EMIF_ADDR[1]	ETM DATA[20] / EMIF_DATA[4]	ETM DATA[21] / EMIF_DATA[5]	ETM DATA[22] / EMIF_DATA[6]	FLTP2	FLTP1	ETM DATA[23] / EMIF_DATA[7]	ETM DATA[24] / EMIF_DATA[8]	ETM DATA[25] / EMIF_DATA[9]	ETM DATA[26] / EMIF_DATA[10]	ETM DATA[27] / EMIF_DATA[11]	ETM DATA[28] / EMIF_DATA[12]	N2HET2 [20]	MII_RX_ER	MIBSPI3 NCS[1]	N2HET1 [02]	5
4	N2HET1 [16]	N2HET1 [12]	EMIF_ADDR[6]	EMIF_ADDR[0]	MII_TXEN	MDIO	MII_TXD [3]	N2HET1 [21]	N2HET1 [23]	N2HET2 [15]	N2HET2 [16]	N2HET2 [17]	N2HET2 [18]	N2HET2 [19]	EMIF_nCAS	MII_RXCLK	MII_RXD [0]	MII_CRS	MII_COL	4
3	N2HET1 [29]	N2HET1 [22]	MIBSPI3 NCS[3]	N2HET2 [12]	N2HET1 [11]	MIBSPI1 NCS[1]	MIBSPI1 NCS[2]	GIOA[6]	MIBSPI1 NCS[3]	EMIF_CLK	EMIF_CKE	N2HET1 [25]	N2HET2 [7]	EMIF_nWAIT	EMIF_nRAS	MII_RXD [1]	MII_RXD [2]	MII_RXD [3]	N2HET1 [06]	3
2	VSS	MIBSPI3 NCS[2]	GIOA[1]	N2HET2 [13]	N2HET2 [3]	GIOB[2]	GIOB[5]	DCAN2TX	GIOB[6]	GIOB[1]	KELVIN_GND	GIOB[0]	N2HET1 [13]	N2HET1 [20]	MIBSPI1 NCS[0]	MII_TXD [2]	TEST	N2HET1 [1]	VSS	2
1	VSS	VSS	GIOA[2]	N2HET2 [14]	GIOA[3]	GIOB[7]	GIOB[4]	DCAN2RX	N2HET1 [18]	OSCIN	OSCOUT	GIOA[7]	N2HET1 [15]	N2HET1 [24]	MII_TXD [1]	N2HET1 [7]	NHET1 [03]	VSS	VSS	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	

Figure 3-1. TMS570LC4357-SEP Pinout Diagram

Table 3-1. TMS570LC4357-SEP SEL Voltage Bias Table

Supply	Bias
VCCAD	5.25 V
VCCIO	3.6 V
VCC (core)	1.32 V
VSS	GND

4 Irradiation Facility and Setup

The heavy ion species used for the SEE studies on this product were provided and delivered by the TAMU Cyclotron Radiation Effects Facility [3] using a superconducting cyclotron and advanced electron cyclotron resonance (ECR) ion source. Ion beams are delivered with high uniformity over a 1-inch diameter, circular cross section area for the in-air station. Uniformity is achieved by means of magnetic defocusing. The intensity of the beam is regulated over a broad range spanning several orders of magnitude. For the bulk of these studies, ion fluxes between 10^4 and 10^5 ions/s-cm^2 were used to provide heavy ion fluences between 10^6 and 10^7 ions/cm^2. For these experiments, Silver (^{47}Ag) ions were used. Ion beam uniformity for all tests was in the range of 91% to 98%.

5 SEL Results

During SEL characterization, the device was heated using forced hot air, maintaining the IC temperature at 125°C. The temperature was monitored by means of a K-type thermocouple attached as close to the IC as possible. The species used for the SEL testing was a silver (^{47}Ag) ion with an angle-of-incidence of 0° for an LET_{eff} = 48 MeV-cm^2/mg. The kinetic energy in the vacuum for this ion is 1.634 GeV (15-MeV/amu line). A flux of approximately 10^5 ions/cm^2-s and a fluence of approximately 10^7 ions/cm^2 were used for {two} runs. The supply voltages are supplied externally at the recommended maximum voltage setting noted in Table 3-1. Run duration to achieve this fluence was approximately {2} minutes.

Table 5-1. TMS570LC4357-SEP SEL Conditions

#Runs	Distance (mm)	Temperature (°C)	Ion	Angle	Flux (ions.cm^2/mg)	Fluence (#ions/cm^2)	LET_{eff} (MeV.cm2/mg)
{2}	40	125	^{47}Ag	0°	1.00E+05	1.00E+07	48

Figure 5-1 shows plots of the power supply current over time. No SEL events were observed for any of the runs.

$$\{\sigma SEL \le 3.67\} \times 10–7\ \text{cm}^2 \text{ for } LET_{EFF} = 48\ \text{MeV-cm}^2\text{/mg and } T = 125°\text{C} \tag{1}$$

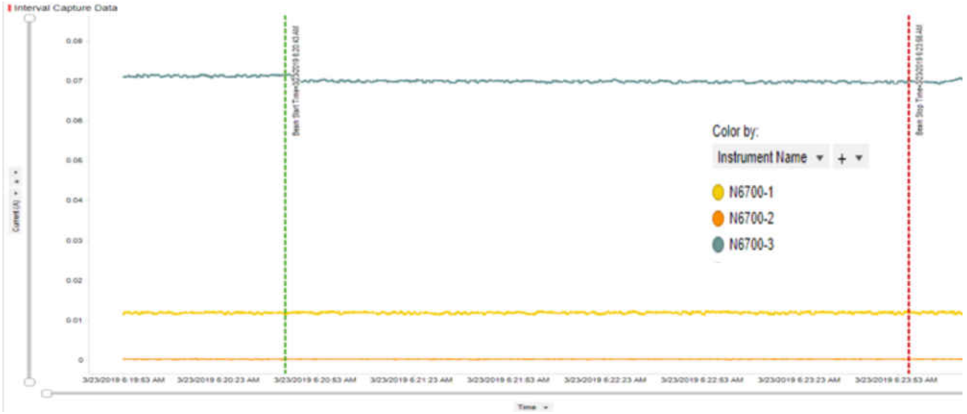

Figure 5-1. TMS570LC4357-SEP SEL Plot of all Three Power Supplies, ^{47}Ag With 0° Angle, LET_{eff} = 48MeV

Supply	Bias
VCCAD	5.25 V
VCCIO	3.6 V
VCC(core)	1.32 V

No significant increases in current consistent with a latch-up event were detected Pre and Post Beam.

6 Summary

Radiation effects of Radiation Tolerant TMS570LC4357-SEP, Arm Cortex-R based microcontroller was studied. This device did not exhibit latch-up to LET_{eff} = 48 MeV-cm^2/mg and T = 125°C.

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