TMS470R1A64

TMS470 Microcontrollers

Silicon Errata

Silicon Initial Revision

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Contents

1 Known Design Marginality/Exceptions to Functional Specifications

The following is a list of advisories on modules in the K version of silicon. Documentation may differ from the user guide or data sheet. The advisory reference number is shown first (i.e.; ADM#1), followed by a description and any known workarounds. The reference numbers may not always be sequential for this device.

Modules include the following:

> Clock control module (CCM)
>
> Direct memory access controller (DMA)
>
> Flash pump (FP)
>
> Flash wrapper (FW)
>
> High-end timer (HET)
>
> Real-time interrupt (RTI)
>
> Standard CAN controller (SCC)
>
> Serial communication interface (SCI)
>
> Serial peripheral interface (SPI)
>
> Zero-pin phase-locked loop (ZPLL)

Advisory C2SI#27	After Error Not Waiting for EOF Time

Description: After an error, the transmitter goes to idle transmission state and waits for new data to output. If it gets new data AND the bus is HIGH, then it will attempt to output the new data without waiting for the correct EOF time.

Workaround: None

Advisory CCM#1	ICLK Not 50% Duty Cycle

Description: The ICLK signal output from the CCM is not a 50% duty cycle signal when the SYSCLK–to–ICLK divide ratio is odd and 3 or above. This output affects the SCI and SPI modules.

Workaround: None

Advisory FP#7	*VNV Voltage Adjusted to Set 0xA Step to −7.86V*

Description: This is to improve yield and reduce erase time. No functional impact or changes to software.

Workaround: None

Advisory FW#3	*Configuration Mode Required for Sleep or Standby*

Description: The configuration mode must be set to enter sleep or standby modes.

Workaround: The documentation (literature number SPNU213) has been updated to reflect this requirement.

Advisory FW#13	*Fails Initial Read of 0x0−0x7 in Pipeline Mode*

Description: Immediately after entering pipeline mode, a data read of location 0x04 immediately following a data read of location 0x0 will cause 0x04 to read as all 0's.

Workaround: Perform a dummy data read of any location other than zero or four immediately after entering pipeline mode. The documentation (literature number SPNU213) has been updated to reflect this requirement.

Advisory FW#14	*Wait States Must Be Set From Highest to Lowest*

Description: Wait states must be set by bank from highest to lowest wait states. Otherwise, if the higher number of wait states is written last, this value will apply to all banks.

Workaround: Set the wait states in each bank by first writing to the bank requiring the most wait states and proceeding last to the bank requiring the least wait states. The documentation (literature number SPNU213) has been updated to reflect this requirement.

Advisory FW#17	*Access to Non-Existing Bank Hangs CPU*

Description: If all banks are in sleep or standby mode and an access to a nonexisting bank is performed, the CPU will hang.

Workaround: Make sure the decoder MFBAH/L0 and MFBAH/L1 registers are set so that an access to a nonexisting memory bank will generate an illegal access exception. The documentation (literature number SPNU213) has been updated to reflect this requirement.

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| **Advisory HET#15** | *Auto Read Clear Malfunction* |

Description: The HET Auto Read Clear feature does not always work properly. Specifically, the data field of instruction X is NOT cleared if the following conditions are BOTH true at the same time:

1. The 64-bit CPU read access happens in the two HET time slots exactly PRECEDING the time slot Y in which instruction X is executed.

2. Instruction X only changes its data field (in time slot Y). Example: Instruction X is an ECNT instruction, which just detected an edge.

The malfunction does NOT occur if the data field of instruction X does not change, since then 2) is not true.

Workaround: See above.

| **Advisory HET#16** | *No PWM With MCMP* |

Description: MCMP causes a constant signal instead of a PWM if both of the following conditions are met:

1. Consecutive compare match in every LRP for order = reg_ge_data (only when [data=0]).

2. The high resolution delay (in number of SYSCLK cycles) is equal to the time slot the MCM is executed.

Workaround: Replace each MCMP with a two instruction sequence: ECMP and MOV32.

| **Advisory RTI#3** | *Tap Interrupt When Clearing Counter* |

Description: Write accesses to the RTICNTR register will clear the CNTR (21 bit counter), which causes a Tap interrupt if the corresponding bit switches from a 1 to a 0.

Workaround: Disable the RTI before changing the RTICNTR value.

| **Advisory RTI#4** | *Tap Interrupt When Clearing Counter in Suspend Mode* |

Description: Write accesses to the RTICNTR register will clear the CNTR (21 bit counter), which causes a Tap interrupt if the corresponding bit switches from a 1 to a 0 when the suspend signal is asserted. This is the same problem as RTI#3, however, on the initial fix of RTI#3, the case where the suspend signal is asserted because of an emulator breakpoint was not considered. This problem occurs when the emulator has set a breakpoint on one of the instructions closely following the instruction that writes to the counter.

Workaround: None

Advisory SCC#4	*Delayed Frame Error*

Description: This nonconformance is classified as nonserious and does not have any impact on proper communication and inter-operability with other nodes. Because of the proposed update of the ISO-WD-16485 CAN Test specification (2001–05–31), the SCC on this device has a nonconformance to the Bosch CAN specification and the ISO-11898 standard as described below.

If the following conditions are met, the CAN does not perform a resynchronization as it is expected to.

Conditions:

1.   The node must be transmitter.
2.   The node must transmit a dominant bit.
3.   The dominant bit must be sampled back as recessive.
4.   A recessive–to–dominant edge must be detected after the sample point.

But because the recessive sampling of the bit transmitted as dominant is also an error, an error frame will be transmitted at the beginning of the following bit.

Therefore, the effect of the no-conformance is a delay of this error frame. The maximum for this delay is 5 (max(SJW) + 1 Tq) time quanta.

Workaround: None

Advisory SCC#5	*Pins Are High Impedance in Low Power Mode*

Description: Regardless of how the CANSTX or CANSRX pins are configured, they become general purpose inputs when entering low power mode.

Workaround: If the pin is not driven externally, which is usually the case with the CANSTX pin, an external pull-up or pull-down resistor should be added to avoid consuming extra current in low power mode.

Advisory SCC#6	*CANSRX Must be High During Self-Test*

Description: The CANSRX pin must be high during self-test.

Workaround: The CANSRX pin is usually driven high by the bus transceiver. As long as there is no bus activity during the self-test, this is not a problem. If nothing is driving the CANSRX pin, it can be configured as a digital output and set high during the self-test.

Advisory SCC#7	*Abort Acknowledge Bit Not Set After Transmission Request Reset*

Description:

After aborting a message using the Transmission Request Reset (TRR) register bit, there are some rare instances where the TRR bit will clear without setting the Abort Acknowledge (AA) bit.

For the rare instance to occur, all three of the following conditions must exist:

1. The current message has a message error or lost arbitration. This message does not need to have the same mailbox number as the TRR bit mailbox discussed in condition 2.

2. The TRS bit of the same mailbox as the TRR mailbox must be set from either this current message, before the current message and still pending, or just set.

3. The TRR bit must be set in the exact ICLK cycle were the wrapper state machine is in IDLE for one cycle. (One ICLK before or after and the condition will not occur). This IDLE state can occur just after the current message. It can also occur just a few ICLKs after setting the TRS bit of any mailbox after the current message (point 1 above).

If these conditions occur, then the TRR and TRS bits for the mailbox will clear t_{clr} ICLKs after the TRR bit is set where:

$$t_{clr} = ((16-mailbox\_number)*2)+3 \qquad \textbf{ICLK cycles}$$

The TA and AA bits will not be set if this condition occurs. Normally, either the TA or AA bit sets after TRR bit goes to 0.

Workaround:

When this problem occurs, the TRR and TRS bits will clear within t_{clr} ICLK cycles. To check for this condition, first disable the interrupts. Check the TRR bits' t_{clr} ICLK cycles after setting the TRR bits to make sure that they are still set. A set TRR bit indicates the problem did not occur. If TRR is cleared, then perhaps it was the normal end of a message and the TA or AA bits are set. Check both the TA and AA bits. If they are both 0, then the conditions did occur. Handle the condition as the interrupt service routine would, except that the AA bit does not need clearing now. If the TA or AA bit is set, then the normal interrupt routine will happen when the interrupt is re-enabled.

Advisory SPI#1	*Slave Baud Rate Setting*

Description:

When the SPI is operated in slave mode, the SPI clock must be configured to a baud rate as close to the master's baud rate as possible. If the baud rate is too slow, the enable signal will not be generated in time to keep the master from sending additional data. If the baud rate is too fast, the slave will capture the data before the last bit is shifted in.

Workaround:

The documentation (literature number SPNU195) has been updated to reflect this requirement.

Advisory SPI#2	*Clearing, Setting SPI EN Bit Does Not Clear Internal Flag*

Description: Clearing and then setting the SPI EN bit does not clear an internal flag that indicates valid data is in the SPI data register. This could lead to an inadvertent overrun error. The software should do a dummy read of SPIBUF after setting the SPIEN bit to clear the internal flag.

Workaround: The documentation (literature number SPNU195) has been updated to reflect this requirement.

Advisory ZPLL#1	*Clock Corruption When Changing Multiplier*

Description: All interrupt requests coming to the CIM module must be disabled when changing between multiply-by-4 and multiply-by-8.

Workaround: Disable the interrupt request at the peripheral source if possible.

Advisory ZPLL#2	*High Halt Current*

Description: There is a high IDDQ current consumption because of an incorrect tie-off of internal unused signals.

Workaround: None

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