

# **Migrating from TMS320C5515/05 to TMS320C5535/34/33/32**

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## **ABSTRACT**

This document provides the minimum changes required to migrate from TMS320C5515/05 to TMS320C5535/34/33/32. Enhancements or new features of the TMS320C5535/34/33/32 devices that do not affect migrating from the TMS320C5515/05 devices will also be briefly mentioned in this document.

All efforts have been made to provide a comprehensive list of changes. An update will be provided if additional changes are identified.

The TMS320C5515/05 devices will henceforth be referred to as C5515/05 in this document. The TMS320C5535/34/33/32 devices will henceforth be referred to as C5535/34/33/32 in this document.

More information on the C5535/34/33/32 DSP can be found in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Fixed-Point Digital Signal Processors Data Manual* (literature number [SPRS737](#)).

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## 1 Overview

The following table shows the major differences between the two devices. Peripherals that are not included in the table have no changes.

**Table 1. Device Differences**

	<b>C5535/34/33/32</b>	<b>C5515/05</b>
Max CPU Speed (PLL output)	50 MHz at 1.05 V 50/100 MHz at 1.3 V	60/75 MHz at 1.05 V 100/120 MHz at 1.3 V 150 MHz at 1.4 V (only C5505)
On-chip Memory	C5535	320KB
	C5534	256KB
	C5533	128KB
	C5532	64KB
USB_LDO	C5535, C5534, and C5533	C5515
DSP_LDO	C5535 and C5534	C5515
Bootloader	Boot both encrypted and unencrypted images from 16-bit SPI EEPROM, 24-bit SPI serial flash, I2C EEPROM, SD/SDHC/eMMC/moviNAND, UART, and USB	Boot both encrypted and unencrypted images from NAND, NOR, 16-bit SPI EEPROM, 24-bit SPI serial flash, I2C EEPROM but only encrypted images from SD/SDHC/MMC/eMMC, and USB
Pins and Peripherals	144-pin BGA (ZHH Suffix) No EMIF support	196-pin BGA (ZCH Suffix) EMIF Support
FFT Coprocessor (C5535 only)	HWA FFT API Address 00fefe9c _hwafft_br 00fefeb0 _hwafft_8pts 00feff9f _hwafft_16pts 00ff00f5 _hwafft_32pts 00ff03fe _hwafft_64pts 00ff0593 _hwafft_128pts 00ff07a4 _hwafft_256pts 00ff09a2 _hwafft_512pts 00ff0c1c _hwafft_1024pts	HWA FFT API Address 0x00ff6cd6 _hwafft_br 0x00ff6cea _hwafft_8pts 0x00ff6dd9 _hwafft_16pts 0x00ff6f2f _hwafft_32pts 0x00ff7238 _hwafft_64pts 0x00ff73cd _hwafft_128pts 0x00ff75de _hwafft_256pts 0x00ff77dc _hwafft_512pts 0x00ff7a56 _hwafft_1024pts

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## 2 Operating Conditions

### 2.1 Operating Voltages and CPU Speeds

**Table 2. Operating Voltages and CPU Speeds for C5535/34/33/32 and C5515/05**

Supply Pins	C5535/34/33/32		C5515/05	
	CV <sub>DD</sub>	1.05 V	50 MHz	1.05 V
1.3 V		50/100 MHz	1.3 V	100/120 MHz
N/A		N/A	1.4 V	150 MHz (C5505 only)
All other power domains	No changes			

**Table 3. On-Chip RAM Availability**

On-Chip RAM	Device				
	C5535	C5534	C5533	C5532	C5515/05
320KB	x <sup>(1)</sup>	- <sup>(2)</sup>	-	-	x
256KB	x	x	-	-	x
128KB	x	x	x	-	x
64KB	x	x	x	x	x

<sup>(1)</sup> x — Supported

<sup>(2)</sup> - — Not supported

## 3 Low-Dropout Regulators (LDOs)

**Table 4. LDO Availability**

LDO	Device					
	C5535	C5534	C5533	C5532	C5515	C5505
ANA_LDO	x <sup>(1)</sup>	x	x	x	x	x
USB_LDO	x	x	x	- <sup>(2)</sup>	x	-
DSP_LDO	x	x	-	-	x	-

<sup>(1)</sup> x — Supported

<sup>(2)</sup> - — Not supported

For the 50-MHz devices, DSP\_LDO must be programmed to 1.05 V to match the core voltage, CV<sub>DD</sub>, for proper operation after reset. This is because DSP\_LDO is enabled to 1.3 V when coming out of reset.

## 4 Pin and Package Considerations

### 4.1 Package

The C5535/34/33/32 uses the 144-pin, 12x12 mm, Green (Pb-free and environmentally friendly) ZHH package. For more information, see the *TMS320C5535*, *TMS320C5534*, *TMS320C5533*, *TMS320C5532 Data Manual* (literature number [SPRS737](#)). The C5515/05 uses the 196-pin, 10x10 mm, Green (Pb-free and environmentally friendly) ZCH package.

### 4.2 Pin Compatibility

Due to differences between the C5535/34/33/32 and C5515/05 packages, they are **not** pin-to-pin compatible.

### 4.3 Peripheral Changes

**Table 5. Peripheral Availability**

Peripheral	Device				
	C5535	C5534	C5533	C5532	C5515/05
USB	x <sup>(1)</sup>	x	x	- <sup>(2)</sup>	x
LCD Interface	x	-	-	-	x
HWA FFT	x	-	-	-	x
SAR ADC	x	-	-	-	x

<sup>(1)</sup> x — Supported

<sup>(2)</sup> - — Not supported

## 4.4 Pin Maps

Figure 1 through Figure 4 show the pin maps of the C5535/34/33/32 devices.

P	V <sub>SS</sub>	LCD_D[4]/ GP[14]	LCD_D[6]/ GP[16]	TRST	LCD_D[8]/ I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	LCD_D[7]/ GP[17]	LCD_D[10]/ I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	LCD_D[11]/ I2S2_DX/ GP[27]/ SPI_TX	LCD_D[13]/ UART_CTS/ GP[29]/ I2S3_FS	LCD_D[14]/ UART_RXD/ GP[30]/ I2S3_RX	V <sub>SS</sub>
N	TDO	LCD_RW/ WRB/SPI_ CS2	TCK	LCD_D[0]/ SPI_RX	LCD_D[3]/ GP[13]	TMS	LCD_D[5]/ GP[15]	DV <sub>DDIO</sub>	CV <sub>DD</sub>	LCD_D[9]/ I2S2_FS/ GP[19]/ SPI_CS0	DV <sub>DDIO</sub>	LCD_D[12]/ UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV <sub>DDIO</sub>
M	EMU1	LCD_CS1_E1/ SPI_CS1	DV <sub>DDIO</sub>	DV <sub>DDIO</sub>	LCD_RS/ SPI_CS3	CV <sub>DD</sub>	V <sub>SS</sub>	SD0_CLK/ I2S0_CLK/ GP[0]	CV <sub>DD</sub>	SD0_CMD/ I2S0_FS/ GP[1]	LCD_D[15]/ UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	LCD_CS0/ E0/SPI_CS0	EMU0	LCD_EN/ RDB/ SPI_CLK	DV <sub>DDIO</sub>	V <sub>SS</sub>					V <sub>SS</sub>	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	LCD_D[1]/ SPI_TX	TDI	V <sub>SS</sub>	V <sub>SS</sub>							CV <sub>DD</sub>	RSV1	USB_VDD1P3	USB_VSS1P3
J	SD0_D0/ I2S0_DX/ GP[2]	LCD_D[2]/ GP[12]	XF									USB_VSSA1P3	V <sub>SS</sub>	USB_DM
H	RSV10	CV <sub>DD</sub>	V <sub>SS</sub>									USB_VDDA1P3	USB_VSSA3P3	USB_DP
G	RSV9	RSV12	CV <sub>DD</sub>									USB_VDDA3P3	USB_VDDPLL	USB_R1
F	RSV8	CV <sub>DD</sub>	V <sub>SS</sub>									USB_VSSREF	USB_VSSPLL	USB_VDD1P3
E	RSV7	RSV11	V <sub>SS</sub>	V <sub>SS</sub>							V <sub>SS</sub>	USB_VDD1P3	USB_VDDOSC	USB_MXI
D	CLK_SEL	RESET	CV <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>					V <sub>SS</sub>	CV <sub>DD</sub>	USB_VSSOSC	USB_LD00	USB_MXO
C	CLKIN	INT0	DV <sub>DDRTC</sub>	SCL	V <sub>SSRTC</sub>	DV <sub>DDIO</sub>	V <sub>DDA_PLL</sub>	V <sub>SS</sub>	V <sub>SSA_ANA</sub>	BG_CAP	CV <sub>DD</sub>	V <sub>SS</sub>	DSP_LDO_ EN	LDOI
B	INTT	V <sub>SS</sub>	V <sub>SS</sub>	CV <sub>DDRTC</sub>	CV <sub>DDRTC</sub>	V <sub>SSA_ANA</sub>	V <sub>DDA_ANA</sub>	GPAIN1	ANA_LD00	LDOI	RSV5	RSV3	RSV6	LDOI
A	V <sub>SSA_PLL</sub>	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	GPAIN0	GPAIN2	GPAIN3	RSV4	RSV0	DSP_LD00	V <sub>SS</sub>
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

Figure 1. C5535 Pin Map

P	V <sub>SS</sub>	GP[14]	GP[16]	TRST	I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	GP[17]	I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	I2S2_DX/ GP[27]/ SPI_TX	UART_CTS/ GP[29]/ I2S3_FS	UART_RXD/ GP[30]/ I2S3_RX	V <sub>SS</sub>
N	TDO	SPI_CS2	TCK	SPI_RX	GP[13]	TMS	GP[15]	DV <sub>DDIO</sub>	CV <sub>DD</sub>	I2S2_FS/ GP[19]/ SPI_CS0	DV <sub>DDIO</sub>	UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV <sub>DDIO</sub>
M	EMU1	SPI_CS1	DV <sub>DDIO</sub>	DV <sub>DDIO</sub>	SPI_CS3	CV <sub>DD</sub>	V <sub>SS</sub>	SD0_CLK/ I2S0_CLK/ GP[0]	CV <sub>DD</sub>	SD0_CMD/ I2S0_FS/ GP[1]	UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	SPI_CS0	EMU0	SPI_CLK	DV <sub>DDIO</sub>	V <sub>SS</sub>					V <sub>SS</sub>	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	SPI_TX	TDI	V <sub>SS</sub>	V <sub>SS</sub>							CV <sub>DD</sub>	RSV1	USB_VDD1P3	USB_VSS1P3
J	SD0_D0/ I2S0_DX/ GP[2]	GP[12]	XF									USB_VSSA1P3	V <sub>SS</sub>	USB_DM
H	RSV10	CV <sub>DD</sub>	V <sub>SS</sub>									USB_VDDA1P3	USB_VSSA3P3	USB_DP
G	RSV9	RSV12	CV <sub>DD</sub>									USB_VDDA3P3	USB_VDDPLL	USB_R1
F	RSV8	CV <sub>DD</sub>	V <sub>SS</sub>									USB_VSSREF	USB_VSSPLL	USB_VDD1P3
E	RSV7	RSV11	V <sub>SS</sub>	V <sub>SS</sub>							V <sub>SS</sub>	USB_VDD1P3	USB_VDDOSC	USB_MXI
D	CLK_SEL	RESET	CV <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>					V <sub>SS</sub>	CV <sub>DD</sub>	USB_VSSOSC	USB_LDOO	USB_MXO
C	CLKIN	INT0	DV <sub>DDRTC</sub>	SCL	V <sub>SSRTC</sub>	DV <sub>DDIO</sub>	V <sub>DDA_PLL</sub>	V <sub>SS</sub>	V <sub>SSA_ANA</sub>	BG_CAP	CV <sub>DD</sub>	V <sub>SS</sub>	DSP_LDO_ EN	LDOI
B	INT1	V <sub>SS</sub>	V <sub>SS</sub>	CV <sub>DDRTC</sub>	CV <sub>DDRTC</sub>	V <sub>SSA_ANA</sub>	V <sub>DDA_ANA</sub>	NC	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V <sub>SSA_PLL</sub>	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	NC	NC	NC	RSV4	RSV0	DSP_LDOO	V <sub>SS</sub>
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

**Figure 2. C5534 Pin Map**

P	V <sub>SS</sub>	GP[14]	GP[16]	TRST	I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	GP[17]	I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	I2S2_DX/ GP[27]/ SPI_TX	UART_CTS/ GP[29]/ I2S3_FS	UART_RXD/ GP[30]/ I2S3_RX	V <sub>SS</sub>
N	TDO	SPI_CS2	TCK	SPI_RX	GP[13]	TMS	GP[15]	DV <sub>DDIO</sub>	CV <sub>DD</sub>	I2S2_FS/ GP[19]/ SPI_CS0	DV <sub>DDIO</sub>	UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV <sub>DDIO</sub>
M	EMU1	SPI_CS1	DV <sub>DDIO</sub>	DV <sub>DDIO</sub>	SPI_CS3	CV <sub>DD</sub>	V <sub>SS</sub>	SD0_CLK/ I2S0_CLK/ GP[0]	CV <sub>DD</sub>	SD0_CMD/ I2S0_FS/ GP[1]	UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	SPI_CS0	EMU0	SPI_CLK	DV <sub>DDIO</sub>	V <sub>SS</sub>					V <sub>SS</sub>	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_VBUS
K	SPI_TX	TDI	V <sub>SS</sub>	V <sub>SS</sub>							CV <sub>DD</sub>	RSV1	USB_VDD1P3	USB_VSS1P3
J	SD0_D0/ I2S0_DX/ GP[2]	GP[12]	XF									USB_VSSA1P3	V <sub>SS</sub>	USB_DM
H	RSV10	CV <sub>DD</sub>	V <sub>SS</sub>									USB_VDDA1P3	USB_VSSA3P3	USB_DP
G	RSV9	RSV12	CV <sub>DD</sub>									USB_VDDA3P3	USB_VDDPLL	USB_R1
F	RSV8	CV <sub>DD</sub>	V <sub>SS</sub>									USB_VSSREF	USB_VSSPLL	USB_VDD1P3
E	RSV7	RSV11	V <sub>SS</sub>	V <sub>SS</sub>							V <sub>SS</sub>	USB_VDD1P3	USB_VDDOSC	USB_MXI
D	CLK_SEL	RESET	CV <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>					V <sub>SS</sub>	CV <sub>DD</sub>	USB_VSSOSC	USB_LDOO	USB_MXO
C	CLKIN	INT0	DV <sub>DDRTC</sub>	SCL	V <sub>SSRTC</sub>	DV <sub>DDIO</sub>	V <sub>DDA_PLL</sub>	V <sub>SS</sub>	V <sub>SSA_ANA</sub>	BG_CAP	CV <sub>DD</sub>	V <sub>SS</sub>	DSP_LDOO <sup>(1)</sup> EN	LDO1
B	INT1	V <sub>SS</sub>	V <sub>SS</sub>	CV <sub>DDRTC</sub>	CV <sub>DDRTC</sub>	V <sub>SSA_ANA</sub>	V <sub>DDA_ANA</sub>	NC	ANA_LDOO	LDO1	RSV5	RSV3	RSV6	LDO1
A	V <sub>SSA_PLL</sub>	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	NC	NC	NC	RSV4	RSV0	DSP_LDOO <sup>(2)</sup>	V <sub>SS</sub>
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

- (1) DSP\_LDOO is not supported on the TMS320C5533. An external power supply is used to provide power to CV<sub>DD</sub>, DSP\_LDOO\_EN should be tied to LDO1, and DSP\_LDOO should be left unconnected. The RESET pin must be asserted appropriately for device initialization after power up.
- (2) DSP\_LDOO is not supported on the TMS320C5533. For proper device operation, this pin must be left connected. DSP\_LDOO can be enabled to provide a regulated 1.3- or 1.05-V output only to the internal POR to support the RTC-only mode. For more information, see the *RTC Only Mode* section in the *TMS320C5535, TMS320C5534, TMS320C5533, TMS320C5532 Data Manual* (literature number [SPRS737](#)).

**Figure 3. C5533 Pin Map**

P	V <sub>SS</sub>	GP[14]	GP[16]	TRST	I2S2_CLK/ GP[18]/ SPI_CLK	SD0_D1/ I2S0_RX/ GP[3]	SD0_D3/ GP[5]	GP[17]	I2S2_RX/ GP[20]/ SPI_RX	SD1_D1/ I2S1_RX/ GP[9]	I2S2_DX/ GP[27]/ SPI_TX	UART_CTS/ GP[29]/ I2S3_FS	UART_RXD/ GP[30]/ I2S3_RX	V <sub>SS</sub>
N	TDO	SPI_CS2	TCK	SPI_RX	GP[13]	TMS	GP[15]	DV <sub>DDIO</sub>	CV <sub>DD</sub>	I2S2_FS/ GP[19]/ SPI_CS0	DV <sub>DDIO</sub>	UART_RTS/ GP[28]/ I2S3_CLK	SD0_D2/ GP[4]	DV <sub>DDIO</sub>
M	EMU1	SPI_CS1	DV <sub>DDIO</sub>	DV <sub>DDIO</sub>	SPI_CS3	CV <sub>DD</sub>	V <sub>SS</sub>	SD0_CLK/ I2S0_CLK/ GP[0]	CV <sub>DD</sub>	SD0_CMD/ I2S0_FS/ GP[1]	UART_TXD/ GP[31]/ I2S3_DX	SD1_D3/ GP[11]	SD1_D0/ I2S1_DX/ GP[8]	SD1_CLK/ I2S1_CLK/ GP[6]
L	SPI_CS0	EMU0	SPI_CLK	DV <sub>DDIO</sub>	V <sub>SS</sub>					V <sub>SS</sub>	SD1_CMD/ I2S1_FS/ GP[7]	SD1_D2/ GP[10]	RSV2	USB_V <sub>BUS</sub>
K	SPI_TX	TDI	V <sub>SS</sub>	V <sub>SS</sub>							CV <sub>DD</sub>	RSV1	USB_V <sub>DD1P3</sub>	USB_V <sub>SS1P3</sub>
J	SD0_D0/ I2S0_DX/ GP[2]	GP[12]	XF									USB_V <sub>SSA1P3</sub>	V <sub>SS</sub>	USB_DM
H	RSV10	CV <sub>DD</sub>	V <sub>SS</sub>									USB_V <sub>VDDA1P3</sub>	USB_V <sub>SSA3P3</sub>	USB_DP
G	RSV9	RSV12	CV <sub>DD</sub>									USB_V <sub>VDDA3P3</sub>	USB_V <sub>DDPLL</sub>	USB_R1
F	RSV8	CV <sub>DD</sub>	V <sub>SS</sub>									USB_V <sub>SSREF</sub>	USB_V <sub>SSPLL</sub>	USB_V <sub>DD1P3</sub>
E	RSV7	RSV11	V <sub>SS</sub>	V <sub>SS</sub>						V <sub>SS</sub>		USB_V <sub>DD1P3</sub>	USB_V <sub>DDOSC</sub>	USB_MXI
D	CLK_SEL	RESET	CV <sub>DD</sub>	V <sub>SS</sub>	V <sub>SS</sub>				V <sub>SS</sub>	CV <sub>DD</sub>	USB_V <sub>SSOSC</sub>	USB_LDOO <sup>(1)</sup>	USB_MXO	
C	CLKIN	INT0	DV <sub>DDRTC</sub>	SCL	V <sub>SSRTC</sub>	DV <sub>DDIO</sub>	V <sub>VDDA_PLL</sub>	V <sub>SS</sub>	V <sub>SSA_ANA</sub>	BG_CAP	CV <sub>DD</sub>	V <sub>SS</sub>	DSP_LDOO <sub>EN</sub> <sup>(2)</sup>	LDOI
B	INT1	V <sub>SS</sub>	V <sub>SS</sub>	CV <sub>DDRTC</sub>	CV <sub>DDRTC</sub>	V <sub>SSA_ANA</sub>	V <sub>VDDA_ANA</sub>	NC	ANA_LDOO	LDOI	RSV5	RSV3	RSV6	LDOI
A	V <sub>SSA_PLL</sub>	CLKOUT	RTC_CLKOUT	SDA	WAKEUP	RTC_XO	RTC_XI	NC	NC	NC	RSV4	RSV0	DSP_LDOO <sup>(3)</sup>	V <sub>SS</sub>
	1	2	3	4	5	6	7	8	9	10	11	12	13	14

- (1) USB\_LDOO is not supported on the TMS320C5532. For proper device operation, this pin must be left unconnected.
- (2) DSP\_LDOO is not supported on the TMS320C5532. An external power supply is used to provide power to CV<sub>DD</sub>. DSP\_LDOO\_EN should be tied to LDOI, and DSP\_LDOO should be left unconnected. The RESET pin must be asserted appropriately for device initialization after power up.
- (3) DSP\_LDOO is not supported on the TMS320C5532. For proper device operation, this pin must be left connected. DSP\_LDOO can be enabled to provide a regulated 1.3- or 1.05-V output only to the internal POR to support the RTC-only mode. For more information, see the *RTC Only Mode* section in the *TMS320C5535*, *TMS320C5534*, *TMS320C5533*, *TMS320C5532 Data Manual* (literature number [SPRS737](#)).

Shaded pins are not supported on this device. To ensure proper device operation, these pins must be hooked up properly. For more information, see the *Unsupported USB 2.0 Terminal Functions* section in the *TMS320C5535*, *TMS320C5534*, *TMS320C5533*, *TMS320C5532 Data Manual* (literature number [SPRS737](#)).

**Figure 4. C5532 Pin Map**



## 5 Bootloader

The C5535/34/33/32 bootloader includes the following changes to support new features:

- Adds unencrypted boot image from SD/SDHC/eMMC/moviNAND, UART, and USB
- Supports reauthoring for 16-bit SPI EEPROM, I2C EEPROM, and SD/SDHC/eMMC/moviNAND
- Does not support NOR, NAND, and MMC

See the *Boot Sequence* section in the *TMS320C5535*, *TMS320C5534*, *TMS320C5533*, *TMS320C5532 Data Manual* (literature number [SPRS737](#)) for details.

## Revision History

<b>Changes from Original (November, 2011) to A Revision</b>	<b>Page</b>
• Changed description of <u>DSP_LDO_EN</u> pin .....	7
• Added description of DSP_LDOO pin .....	7
• Added description of USB_LDOO pin .....	8
• Added description of <u>DSP_LDO_EN</u> pin .....	8
• Added description of DSP_LDOO pin .....	8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

## IMPORTANT NOTICE

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