Application Note

Jacinto 7 Display Subsystem Overview

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ABSTRACT

This application report summarizes TDA4VM and DRA829V SoCs' display subsystem capabilities.

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Trademarks

1 Introduction

Jacinto 7 TDA4VM and DRA829V processors [1, 2] Display Sub-System (DSS) provides the logic to output video frames stored in the memory to the external display interfaces. The DSS performs multi-layer composition for the display output and supports a set of industry standard display interfaces to drive wide range of display panel resolutions. For the complete DSS feature-set, see the *DRA829/TDA4VM Technical Reference Manual* [3].

2 Jacinto 7 Display Subsystem Overview

The DSS is a flexible composition-enabled display subsystem, that supports multiple high resolution display outputs. The DSS supports a multi-layer blending and transparency for each of its display outputs. The DSS block diagram is shown in Figure 2-1.

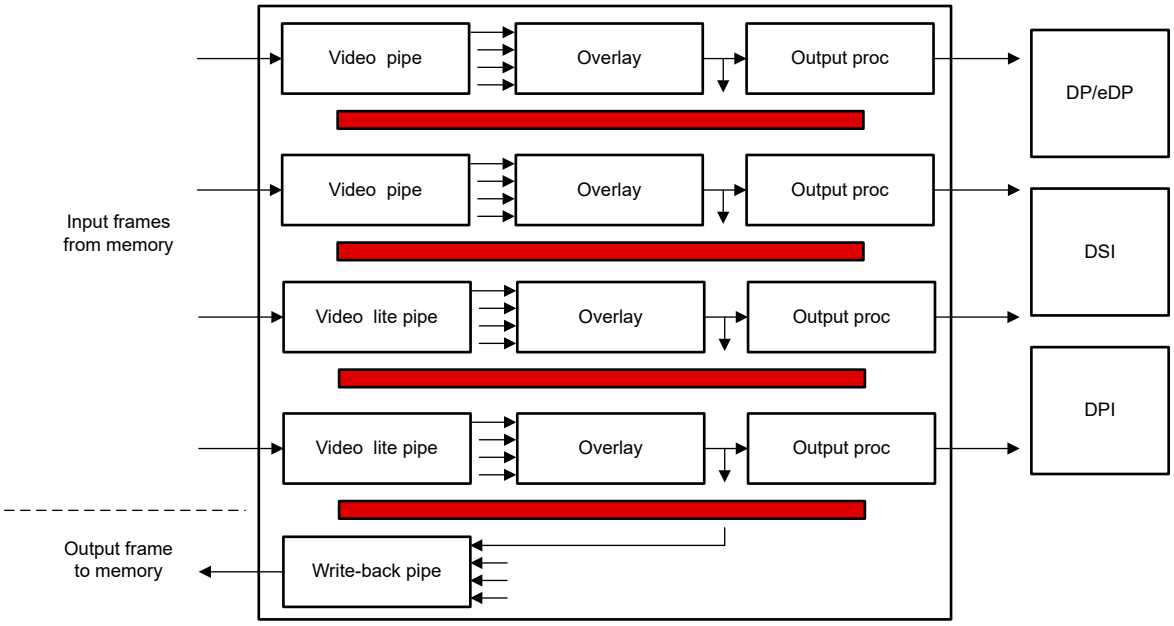

Figure 2-1. TDA4 / DRA829V Display Subsystem Architecture

The DSS is divided into blocks that are connected internally and high-level features that are summarized in the next sections.

2.1 Video (Input) Pipelines

- 4x input display pipes enable up to 4 concurrent displays
  - 2x Video pipelines and 2x Video Lite pipelines
- Each pipe supports 10-bit width for HDR video
- Input RGB and YUV source pixel formats
- 4K x2K (UHD) resolution support
- Flexible line-buffer enables >4K line width for wide/short displays (8Kx1k)
- 2x Video Pipelines support upscaling and downscaling
  - Programmable poly-phase filter (scaler)
  - Independent horizontal and vertical re-sampling: up-sampling (up to x16) and down-sampling (down to x0.25)
- Color Space Conversion
- Programmable VC1 range mapping
- Programmable Brightness/Contrast/Hue/Saturation
- Programmable Gamma Correction LUT
- Luma Key generation

2.2 Writeback Pipeline

- One Write-back pipeline can be used to store composited image to memory for additional blending or for transmission over other interfaces (PCIe, Eth.)
- Destination RGB and YUV pixel formats
- Programmable poly-phase filter (scaler) with up and down-scaling

2.3 Overlay Manager

- On-the-Fly Composition enables alpha blending on up to 4 input pipelines
- Transparency color key (source and destination)
- Alpha blending support: Embedded pixel alpha (ARGB and RGBA), global pixel, and combination of global pixel and pixel alpha
- Z-order programmable (full flexibility)
- Color Processing per pipe supports gamma correction, color space conversion, BCHS control, output dithering, scaling

2.4 Output Processing

- 12-bit output processing pipeline
- Fully programmable Color Space Conversion matrix to serve as color phase rotation (CPR)
- Brightness/Contrast/Saturation control
- Gamma Correction

2.5 Output Display Interfaces

DSS supports multiple display output interfaces: DP/eDP, DSI and DPI.

2.5.1 Embedded Display Port (eDP)

- Compliance with VESA Display Port (DP) 1.3 (with 1.4 DSC/FEC support) specification
- Compliance with VESA embedded Display Port (eDP) 1.4 specification
- Static configuration of either DP or eDP mode
- Single Stream Transport (SST)
- Multiple Stream Transport (MST)
  - Up to 4 video and up to 1 audio sources
  - Support for up to 25 GBps throughput (equivalent to approximately 4K + 2xFHD streams) use case
- The DP (Physical Layer) SERDES and Aux PHY modules support
  - DP1.3 HBR3 and eDP1.4a HBR3 throughput
  - 1, 2, or 4 lanes at 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps per lane
  - Hot Plug Detect (HPD) for connection detection and interrupt from sink

2.5.2 MIPI Display Serial Interface (DSI)

- Compliance with MIPI DSI v1.3.1 protocol specification and previous specifications
- Programmable display resolutions with maximum clock rate not exceeding the total available bandwidth over 4MPix @60fps
  - Supporting resolutions up to 2560x1440 @60fps (2.5K)
- The MIPI DSI (Physical Layer) D-PHY module supports:
  - Compliance with MIPI D-PHY 1.2 physical layer interface specification and features
  - 1, 2 or 4 data lanes, in addition to clock signaling
  - Maximum data rate up to 2.5 Gbps per data lane
- It supports up to 4 x 2.5 Gbps D-PHY data lanes in a single-link configuration and handles the byte lane mapping per use case (1, 2, 3, or 4-lanes)

2.5.3 Display Parallel Interface (DPI)

- Support for resolutions to FHD (1920x1080 @ 60fps)
- 24-bit or 16-bit MIPI DPI 2.0
- BT.656 and BT.1120

2.6 Safety Support

- Enhanced safety features. Entire display subsystem is designed for ASIL-B.
- DSS supports the following safety check regions to implement the safety as shown in Figure 2-2.
  - Input pipelines: One safety check region at the output of each video pipeline.
  - Output ports: Up to four sub-regions within the active video output area of the final display output of each video port.
- Each safety check region supports
  - Data correctness check: To verify intended data is shown correctly on the display.
  - Freeze frame detection: To notify a possible frame freeze, when there is no change in the display frame over a multiple frame periods.
- Display pipe and Display management isolation enables virtualization via separate virtual machine ownership per pipe.
  - Each data pipe and corresponding control registers are segmented on separate 64K firewall-protected regions.
  - Each data overlay and output processing control registers are segmented on separate 64K firewall-protected regions.

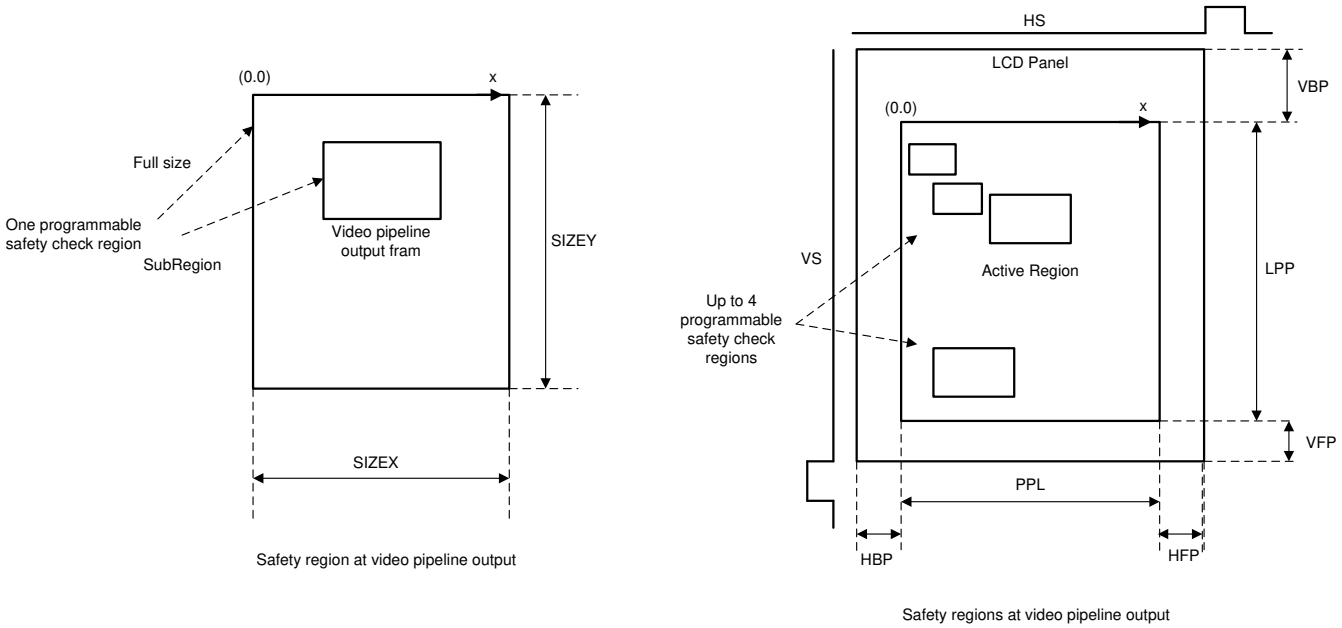

Figure 2-2. Display Subsystem Input and Output Frame Region Safety Checker

3 Display Subsystem Use-case Examples

3.1 3-Display Configuration

Figure 3-1 shows example of 3-display use-case: 1x4K or Wide 8K, 1x2.5K and 1x1080p.

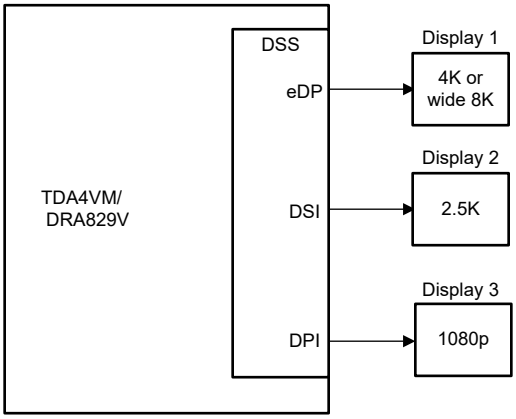

Figure 3-1. 3-Display Configuration

With Multi-Stream Transport mode, the eDP interface can drive multiple displays through daisy chaining. Such an example is shown below where eDP drives 1x4K, and 2x1080 displays.

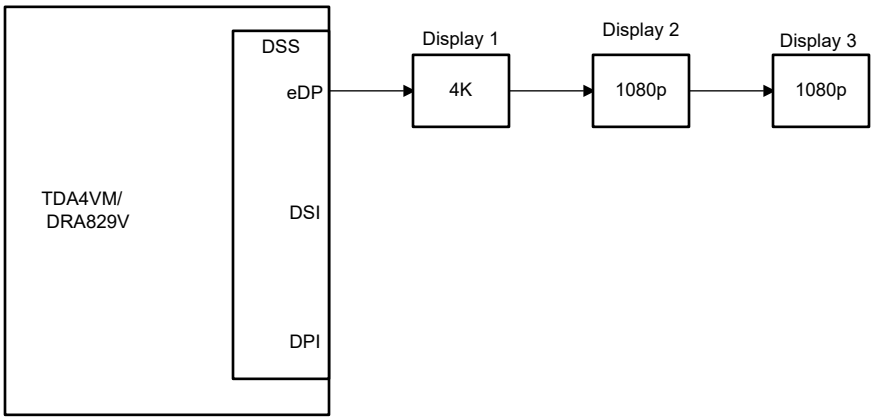

Figure 3-2. Multi-Display Support With eDP

4 TDA4VM/DRA829V Hardware Display Support

TDA4VM/DRA829V evaluation module (J721EXCPXEVM) [4] enables following display outputs as shown in Figure 4-1.

- DP out to DP connector
- DSI out to
  - DSI connector
  - DSI-to-FPD-Link IV to Fakra connector
- DPI out to expansion connector (to Audio and display expansion card)
  - DPI-to-HDMI converter to HDMI connector
  - DPI--to-FPD-LinkIII to Fakra connector

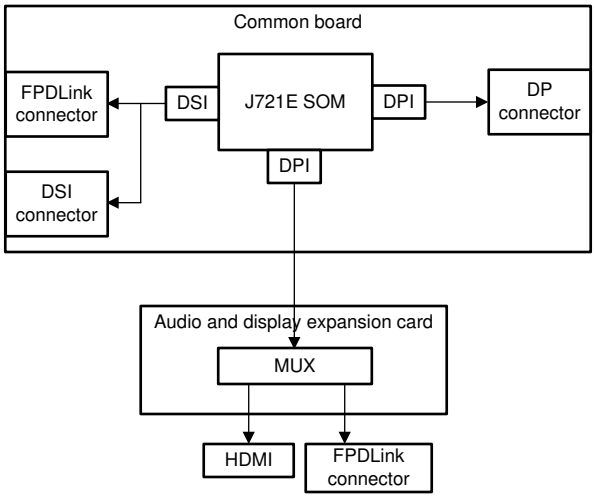

Figure 4-1. TDA4VM/DRA829V EVM Multi-Display Support

5 Display Subsystem Software Architecture

Linux and QNX processor SDKs and PSDK RTOS for TDA4xx /DRA8xx SoCs [5] support DSS driver.

5.1 Linux DSS Architecture

Linux DSS software architecture including GPU support and Windowing system support is shown in Figure 5-1.

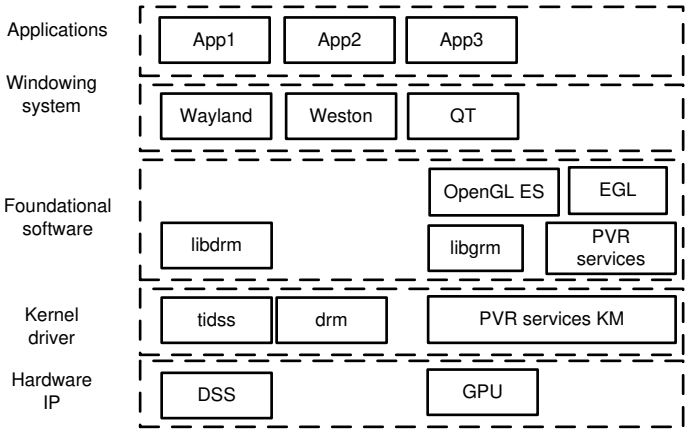

Figure 5-1. Linux DSS and GPU Architecture

DSS software support details can be found as part of SDK documentation at: https://software-dl.ti.com/jacinto7/esd/processor-sdk-linux-jacinto7/08_00_00_08/exports/docs/linux/Foundational_Components/Graphics/Graphics_and_Display.html#display

5.2 QNX Software Architecture

DSS driver on QNX SDK can be supported through the QNX Screen Graphics Subsystem. Architecture details can be found on qnx.com at: http://www.qnx.com/developers/docs/7.1/#com.qnx.doc.screen/topic/manual/cscreen_about.html

5.3 RTOS-Based DSS Support

In addition to Linux and QNX HLOS, DSS driver is supported on RTOS running on R5F core. For more information, see the PSDK RTOS package as part of TDA4VM/DRA829V SDK release [5].

6 References

1. TDA4VM product page
2. DRA829V product page
3. Texas Instruments: *DRA829/TDA4VM Technical Reference Manual*
4. TDA4VM/DRA829 Evaluation Module (https://www.ti.com/tool/J721EXCPXEVM)
5. Software Development Kit for TDA4VM/DRA829 Jacinto Processors

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