

Application Note

Sitara™ AM62x Benchmarks



Andrew Shutzberg

ABSTRACT

This application report contains benchmarks for the AM62x family of devices.

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1 Introduction

These benchmarks are measured on the Cortex®-A53 cores. For updated benchmarks see [Performance Guide section](#) and the [HMI and 3D Out Of Box Demo](#) in the Processor SDK for AM62x. The benchmarks have been run on the AM62x processor, comprised of a Quad-Core 64-bit Arm®-Cortex A53 microprocessor, Single-core Arm Cortex-R5F MCU and an Arm Cortex-M4F MCU. The key parameters of the evaluation board are 1.2GHz clock speed for the Cortex-A53 cores, and a 16-bit wide DDR4 at a speed of 1600MT/s.

2 Processor Core Benchmarks

This section contains benchmarks contained within an Arm Cortex processor core. Synthetic benchmarks included are for example Dhrystone and CoreMark-Pro. Math function benchmarks include functions such as linear algebra and fast fourier transforms (FFT).

2.1 Dhrystone

Dhrystone is a core-only benchmark that runs from warm L1 caches in all modern processors. Dhrystone scales linearly with clock speed. The score calculated by normalizing the time the benchmark takes the loop to run by the reference 1 MIPS machine score of 1757. Even though the benchmark was introduced in 1984 by Reinhold P. Weicker, Dhrystone still gets used in embedded processing. To further normalize to DMIPS/MHz/core as the score scales linearly with clock speed is common. For standard Arm cores, the DMIPS/MHz is identical to the same compiler and flags. Dhrystone is a single core benchmark; a simple sum of multiple cores running the benchmark in parallel is sometimes used. The aggregate score for AM62 with four A53 cores at 1.2GHz (14228 DMIPS).

Table 2-1. Dhrystone Benchmarks

	Cortex-A53 (1.2GHz)
Dhrystones	6250000
DMIPS ¹	3557
DMIPS/MHz each core	3
Compiler and flags	GCC 9.2 -march=ARMv8 -O3
Operating System	Linux 5.10 (2021 LTS)

2.2 CoreMark®-Pro

CoreMark-Pro tests the entire processor, adding comprehensive support for multicore technology, a combination of integer and floating-point workloads, and data sets for utilizing larger memory subsystems. The components of CoreMark-Pro utilizes all levels of cache with an up to 3MB data memory footprint. Many, but not all of the tests, are also using pthreads to allow utilization of multiple cores. The score scales with the number of cores but is always less than linear (dual core score is less than 2x single core).

CoreMark-Pro must not be confused with the smaller CoreMark which, like Dhrystone, is a microbenchmark contained in L1 caches of a modern processor.

Table 2-2. CoreMark®-Pro Results

	Arm Cortex-A53	Core Performance Ratio ²
Single Core	795	1.00
Dual Core	1330	1.67
Quad Core	2030	2.55

¹ Dhrystones normalized by dividing by 1757 reference for 1MIPS

² Compared to Single Core CoreMark®-Pro Result

2.3 Fast Fourier Transform

Fast Fourier Transform (FFT) is a multiply accumulate heavy building block in many applications. A 1024-point single precision floating point complex FFT execution time is shown in [Table 2-3](#). The Arm Cortex-A53 benchmark uses the implementation from Ne10 library, which leverages the Advanced SIMD or NEON acceleration of Cortex A53.

Table 2-3. NE10 CFFT Benchmark

	1024 pt float CFFT Execution Time (single thread / core)
Arm Cortex-A53 (1.2GHz)	23 microseconds

2.4 Cryptographic Benchmarks

The AM62x Linux SDK includes an openssl cryptographic library that can be used by applications. The library is also used by some HTTPS, ssh, and netconf implementations to get access to optimized implementation of cryptographic functions. For the highest performance, the higher-level interface provided by the EVP library needs to be used. A set of selected benchmarks of software observed performance run on AM62x is shown in [Table 2-4](#). Command run was `openssl speed -elapsed -evp <cryptographic mode> -multi 4`. This is utilizing all four A53 cores using four threads.

Table 2-4. Symmetric Cryptography and Secure Hash in Mbit/s

	Frame Size (bytes)					
	16	64	256	1024	8192	16384
aes-128-gcm	2080	5944	11300	14772	16084	16128
aes-256-gcm	1956	5453	9966	12684	13668	13720
aes-128-ctr	215	481	1815	6181	21258	25584
sha256	14	58	227	868	5144	8193
sha512	14	57	203	655	1717	1932
chacha20-poly1305	1196	2550	5101	5824	6154	6173

Further quad A53 core benchmarks for public key cryptography are shown in [Table 2-5](#). Tests can be run with command `openssl speed -elapsed <algorithm> -multi 4`.

Table 2-5. Public Key Cryptography Benchmarks

RSA	size	512	1024	2048	3072	4096
	sign/second	13469	2892	443	146	65
	verify/second	166015	57372	16521	7646	4382
ECDSA	curve	nistp224	nistp256	nistp521	nistk233	nistb233
	sign/second	927	4075	185	706	690
	verify/second	1468	6735	260	378	370

3 Compute and Memory System Benchmarks

This section contains benchmarks involving the Arm Cortex processor core and the memory system of the System-on-Chip (SoC). Synthetic benchmarks included are for example LMBench.

3.1 Memory Bandwidth and Latency

STREAM and a subset of LMBench are benchmarks to measure achieved memory bandwidth and latency from software.

3.1.1 LMBench

LMBench is a suite of microbenchmarks for processor cores and operating system primitives. The memory bandwidth and latency related tests are most relevant for modern embedded processors. The results vary a little (< 10%) run to run.

LMBench benchmark *bw_mem* measures achieved memory copy performance. The parameter *cp* does an array copy and *bcopy* parameter uses the runtime glibc version of *memcpy()* standard function. The glibc uses a highly optimized implementation that utilizes, for example, SIMD resulting in higher performance. The size parameter equal to or smaller than the cache size at a given level measures the achievable memory bandwidth from software doing a typical for loop or *memcpy()* type operation. Typical use is for external memory bandwidth calculation. The bandwidth is calculated as byte read and written counts as 1, which is roughly half of STREAM copy result. The measured bandwidth and the efficiency compared to theoretical wire rate is shown in [Table 3-1](#). The wire rate used is the DDR MT/s rate times the width divided by two (read and write making up a copy both consume the bus). The benchmark further allows creating parallel threads with *-P* parameter. To get the maximum multicore memory bandwidth, create the same amount of threads as there are cores available for the operating system, which is 4 for AM62x Linux (*-P 4*).

Table 3-1. LMBench Results

	Description	Arm Cortex-A53, DDR4-1600MT/s-16 Bit	DDR4 Efficiency
<i>bw_mem -P 2 8M bcopy</i>	<i>quad core, glibc memcpy</i>	1222MB/s	76%
<i>bw_mem 8M bcopy</i>	<i>single core, glibc memcpy</i>	887MB/s	55%
<i>bw_mem -P 4 8M cp</i>	<i>quad core, inline copy loop</i>	731MB/s	46%
<i>bw_mem 8M cp</i>	<i>single core, inline copy loop</i>	590MB/s	37%

LMBench benchmark *lat_mem_rd* is used to measure the observed memory access latency for external memory (DDR4 & LPDDR4 on AM62x) and cache hits. The two arguments are the size of the transaction (64 in [Table 3-2](#)) and the stride of the read (512). These two values are selected to measure the latency to caches and external memory, not the processor data prefetchers or other speculative execution. For access patterns, the prefetching works, but this benchmark is most useful to measure the case when prefetching does not. The left column is the size of the data access pattern in megabytes, right column is the round trip read latency in nanoseconds. As a summary for Arm Cortex-A53 read latency to:

- L1D is 2.5ns
- L2 latency is 11.5ns
- For access to DDR4-1600, latency is 209ns
- For access to LPDDR4-1600, latency is 218ns

Table 3-2. LMBench Benchmarks for DDR4 and LPDDR4

DDR4-1600:	LPDDR4-1600:
<pre> root@am62xx-evm:~ #lat_mem_rd 64 512 "stride=512 0.00049 2.503 0.00098 2.504 0.00195 2.503 0.00293 2.503 0.00391 2.503 0.00586 2.503 0.00781 2.504 0.01172 2.503 0.01562 2.503 0.02344 2.520 0.03125 2.562 0.04688 7.673 0.06250 8.980 0.09375 10.190 0.12500 10.772 0.18750 11.374 0.25000 11.675 0.37500 11.969 0.50000 12.784 0.75000 140.541 1.00000 179.407 1.50000 192.142 2.00000 197.091 3.00000 202.542 4.00000 205.342 6.00000 207.528 8.00000 208.155 12.00000 209.024 16.00000 209.193 24.00000 209.510 32.00000 209.754 48.00000 209.919 64.00000 209.947 </pre>	<pre> root@am62xx-lp-evm:~ #lat_mem_rd 64 512 "stride=512 0.00049 2.404 0.00098 2.404 0.00195 2.404 0.00293 2.404 0.00391 2.404 0.00586 2.404 0.00781 2.404 0.01172 2.404 0.01562 2.404 0.02344 2.404 0.03125 4.658 0.04688 7.361 0.06250 8.649 0.09375 9.829 0.12500 10.425 0.18750 10.902 0.25000 11.206 0.37500 19.735 0.50000 45.997 0.75000 142.079 1.00000 192.943 1.50000 211.722 2.00000 214.697 3.00000 216.157 4.00000 217.630 6.00000 217.874 8.00000 218.525 12.00000 218.666 16.00000 218.752 24.00000 218.732 32.00000 218.727 48.00000 218.696 64.00000 218.854 </pre>

3.1.2 STREAM

STREAM is a microbenchmark for measuring data memory system performance without any data reuse. STREAM is designed to miss on caches and exercise the data prefetcher and speculative accesses. STREAM uses double precision floating point (64 bit), but, in most modern processors, the memory access is the bottleneck. The four individual scores are copy, scale as in multiply by constant, add two numbers, and triad for multiply accumulate. For bandwidth, a byte read counts as one and a byte written counts as one resulting in a score that is double the bandwidth LMBench. The measured bandwidth and the efficiency compared to theoretical wire rate is shown in [Table 3-3](#). The wire rate used is the DDR MT/s rate times the width. To get overall maximum achieved throughput the command used is `stream -M 16M -P 4-N 10`, which means two parallel threads and 10 iterations.

Table 3-3. Stream Benchmarks

	DDR4-1600MT/s-16-Bit Bandwidth	DDR4-1600MT/s-16-Bit Efficiency
copy	2448MB/s	77%
scale	2372MB/s	74%
add	2491MB/s	78%
triad	2493MB/s	78%

3.2 Critical Memory Access Latency

This section provides round-trip read latency measurements for processors in AM62x to various memory destinations in the system. The measurements were made on the AM62x platform using bare-metal silicon verification tests. The tests execute on A53, M4F and R5F processors out of LPDDR4. Each test includes a loop of 8192 iterations to read a total of 32 KiB of data. The number of cycles for each access were counted and divided by the respective processor clock frequency to obtain latency time. [Table 3-4](#) shows the average latency results.

Table 3-4. Critical Memory Access Latency of A53, R5F WKUP, and M4F MCU

Memory	Arm-Cortex-A53 (Avg ns)	Arm-Cortex-R5F WKUP (Avg ns)	Arm-Cortex-M4F MCU (Avg ns)
LPDDR4	219	228	350
OCSRAM MAIN	127	70	170
R5F WKUP TCM	104	2.5	180
M4F MCU TCM	263	233	10

Tests were done at 0.75V VDD_CORE, 1.25Ghz A53 cores, 400MHz R5F core, 400MHz M4F cores, and 1600MT/s LPDDR4. Tightly-Coupled Memory, or TCM, is RAM that is directly attached to an ARM Cortex core. ARM architecture provides a local internal low latency path and also allows external access to the memory through SoC bus infrastructure.

3.3 UDMA: DDR to DDR Data Copy

This section provides test results and observations for DDR to DDR block copy, using the Normal Capacity (NC) UDMA channel, detailed in [Table 3-5](#).

Table 3-5. UDMA Channel Class

	Description
Normal Capacity (NC)	Provides baseline amount of descriptor and TR prefetch and Tx/Rx control and data buffering. An excellent choice for most peripheral transfers which are communicating with on-chip memories and DDR. With a buffer size of 192B, this FIFO depth allows for 3 read transactions, of 64B data bursts, per flight.

The following measurements are collected using bare-metal silicon verification tests on A53 executing out of DDR. Transfer descriptors and rings in DDR. Tests were done at 0.75V VDD_CORE, 1.25Ghz A53 cores, and 1600MT/s LPDDR4. Transfer sizes range from 1KiB to 512KiB.

Table 3-6. UDMA: DDR to DDR Block Copy

Buffer Size (KiB)	NC Channel Bandwidth (MiB/s)	NC Channel Latency (µs)
1	77.02	12.68
2	143.61	13.60
4	207.45	18.83
8	302.46	25.83
16	360.36	43.36
32	413.03	75.66
64	444.93	140.47
128	461.85	270.65
256	470.79	531.02
512	475.26	1052.05

The transfer capacity and latency of the NC UDMA channel, for buffer sizes up to 512 KiB, is shown in [Table 3-6](#).

4 Graphics Processing Unit Benchmarks

The 3D graphics core on AM62x have specifications as shown in [Table 4-1](#).

Table 4-1. AM62x GPU Specifications

Vendor	Imagination Technologies
GPU Core	AXE-1-16M
Pixel Fillrate (Mpixels/sec)	500
GFLOPS	8
3D API	OpenGL ES 3.1

4.1 GImark2 and Kanzi

These results were gathered from the GImark2 and Kanzi performance tests as shown in [Table 4-2](#) and [Table 4-3](#).

Table 4-2. GImark2 Results

Test	Score
glmark2-es2-drm --off-screen	57

Table 4-3. Kanzi Results

Test	Score
Screen Resolution	1920 x 1080
Digital Cockpit	101
Car Shading	50
Fast Cluster	244

4.2 GFXBench5

The results were gathered from the GFXBench5 performance tests as shown in [Table 4-4](#).

Table 4-4. GFXBench5 Results

Test	FPS
Manhattan Off-screen	1.53
Trex Off-screen	2.75
Egypt Off-screen	8.47

5 Summary

The benchmark document is a standard collateral that is published with releasing a new Texas Instruments embedded processor. This report captures various performance metrics of the AM62x device family, including processor core, compute and memory, and GPU benchmarks. Instructions on how to reproduce each experiment are included with the results.

6 References

- [CoreMark-Pro](#)
- STREAM McCalpin, John D. "STREAM: Sustainable Memory Bandwidth in High Performance Computers", a continually updated technical report (1991-2007), available at: <http://www.cs.virginia.edu/stream/>
- [Ne10 math library](#)
- [hosted models at tensorflow.org](#)
- [OpenSSL](#)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (October 2024) to Revision B (December 2024)	Page
• Changed unit typo to <i>Ghz</i> from <i>Hhz</i>	6

Changes from Revision * (July 2022) to Revision A (October 2024)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document.....	2
• Updated Section 1	2
• Added Section 2.4	3
• Updated Section 3.1.1	4
• Updated Section 3.1.2	6

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