*Application Note*

# *AM263 to AM263P Migration Overview*

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**ABSTRACT**

This application note describes the differences between the Texas Instruments AM263 and AM263P microcontrollers to provide details on the new features offered with AM263P and what needs to be considered when migrating from AM263 to AM263P. Both hardware and software changes are covered for the purpose of application migration. This document provides a comprehensive list of feature differences between the two devices. However, these details are kept at a feature level and specific information about the performance or usage of each feature should be found in the device-specific data sheets, technical reference manuals, or software user guides. Features that are identical between the devices are not included outside of the *Device Comparison* table.

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# 1 Feature Differences Between AM263 and AM263P

Device Comparison provides a feature-level comparison between the super set AM2634 and AM263P4 devices.

**Table 1-1. Device Comparison**

| Features | Reference Name | AM2634 | AM263P4 |
|---|---|---|---|
| **Processors and Accelerators** | | | |
| Arm Cortex-R5F | R5FSS | 4 | 4 |
| Trigonometric Math Unit | TMU | No | Yes |
| Hardware Security Module | HSM | Yes | Yes |
| Crypto Accelerators | Security | Yes | Yes |
| **Program and Data Storage** | | | |
| On-Chip Shared Memory (RAM) | OCSRAM | Grade N: 1 MB<br>Grade O/P: 2 MB | Grade N: 2 MB<br>Grade O/P: 3 MB |
| R5F Tightly Coupled Memory (TCM) | TCM | Up to 256KB(9) | Up to 512kB(10) |
| General-Purpose Memory Controller | GPMC | 4MB | None |
| **Peripherals** | | | |
| Modular Controller Area Network Interface | MCAN | 4 | 8 |
| Full CAN-FD Support | MCAN | 4 | 8 |
| General-Purpose I/O | GPIO | Up to 139 | Up to 140 |
| Serial Peripheral Interface | SPI | 5 | 8 |
| Universal Asynchronous Receiver and Transmitter | UART | 6 | 6 |
| Local Interconnect Network | LIN | 5 | 5 |
| Inter-Integrated Circuit Interface | I2C | 4 | 4 |
| Analog-to-Digital Converter | ADC | 3(1) or 5(2) | 3(3) or 5(4) |
| Resolver (ADC12B3M) | RDC | None | 0(7) or 2(8) |
| | ADC | None | 0(7) or 2(8) |
| Comparator Modules | CMPSS | 12(1) or 20(2) | 12(3) or 20(4) |
| Digital-to-Analog Converter | DAC | 1 | 1 |
| Programmable Real-Time Unit Subsystem(5) | PRU-ICSS | 0 or 1 | 0 or 1 |
| Industrial Communication Subsystem Support(6) | PRU-ICSS | Optional | Optional |
| Gigabit Ethernet Interface | CPSW | 2 | 1(8) or 2(7) |
| Multi-Media Card/Secure Digital Interface | MMCSD | 1 | 1 |
| Enhanced High-Resolution Pulse-Width Modulator Module | EHRPWM | 16(1) or 32(2) | 16(3) or 32(4) |
| Enhanced Capture Module | ECAP | 5(1) or 10(2) | 8(3) or 16(4) |
| Enhanced Quadrature Encoder Pulse Module | EQEP | 2(1) or 3(2) | 2(3) or 3(4) |
| Sigma Delta Filter Module | SDFM | 1(1) or 2(2) | 1(3) or 2(4) |
| Fast Serial Interface | FSI | 4x FSI_RX + 4x FSI_TX | 4x FSI_RX + 4x FSI_TX |
| Quad / Octal SPI Flash Interface | QSPI / OSPI | QSPI | OSPI(11) |
| Real Time Interrupt | RTI | 4 | 8 |
| Windowed Watchdog Timer | WWDT | 4 | 4 |

(1) Standard Analog configuration for AM263 contains 3x ADC, 16x EHRPWM, 5x eCAP, 2x EQEP, 1x SDFM, 12x CMPSS
(2) Enhanced Analog configuration for AM263 contains 5x ADC, 32x EHRPWM, 10x eCAP, 3x EQEP, 2x SDFM, 20x CMPSS
(3) Standard Analog configuration for AM263P contains 3x ADC, 16x EHRPWM, 8x eCAP, 2x EQEP, 1x SDFM, 12x CMPSS
(4) Enhanced Analog configuration for AM263P contains 5x ADC, 32x EHRPWM, 16x eCAP, 3x EQEP, 2x SDFM, 20x CMPSS
(5) Programmable Real-Time Unit Subsystem is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, M, or N. Refer to the Device Datasheet for a Nomenclature Description table for definition of all feature codes.
(6) Industrial Communication Subsystem Support is available when selecting an orderable part number that includes a feature code of D, E, F, K, L, M, or N. Refer to the Device Datasheet for a Nomenclature Description table for definition of all feature codes.
(7) Applies to devices in the ZCZ-C Package only and have a Special Features code of C. Refer to the Device Datasheet for a Nomenclature Description table for definition of all feature codes.
(8) Applies to devices in the ZCZ-S Package only and have a Special Features code of F or S. Refer to the Device Datasheet for a Nomenclature Description table for definition of all feature codes.
(9) Each R5FSS cluster supports 128-KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 128-KB of TCM memory, while in Dual-Core mode, each core may only utilize its designated half (64-KB TCM).
(10) Each R5FSS cluster supports 256-KB of Tightly-Coupled Memory (TCM). When configured as Single-Core or Lockstep operating mode, individual cores can utilize the entire 256-KB of TCM memory, while in Dual-Core mode, each core may only utilize its designated half (128-KB TCM).

(11) The Octal SPI (OSPI) Flash Interface for AM263P devices can support Quad SPI (QSPI) Flash devices. The differences between the AM263 QSPI and AM263P OSPI interfaces are covered in Section 2.4.

# 2 Feature Differences for System Consideration

This section outlines the differences and additions to modules when moving from AM263 to AM263P.

## 2.1 New Features in AM263P

This section is to outline new peripheral additions to AM263P.

### 2.1.1 Resolver Peripheral

Certain variants of the AM263P comes with a Resolver peripheral that provide two Resolver to Digital Converters (RDC) with dedicated ADCs. This feature is included in AM263P devices available in the ZCZ-S package and has a special feature code of F or S. For details about feature codes, see the *Device Naming Convention table* in the device-specific data sheet.

The Resolver to Digital Converter can process incoming digital data from ADCs to estimate the angle of the rotor and the angular velocity. The RDC is able to generate excitation sine PWM at frequencies of 5/10/20 KHz (with configurable amplitude and phase) and synchronizes sampling across sine/cosine channels. Offset, gain, and phase corrections, demodulation, and angle and/or velocity outputs are done at the same rate as the excitation frequency. The RDC also provides safety diagnostics and observational data for the application that can be used for safety improvements.

If the resolvers are not used, it is possible to configure the asssociated dedicated SAR ADCs into general purpose ADCs that have four channels each with 12-bit resolution and 3 MSPS sample rate. These ADC modules also do not have an associated comparator subsystem.

#### *2.1.1.1 Migration From Software to Hardware Resolver*

For AM263 devices, the five ADC modules (12-bit / 4 MSPS) with comparator subsystems can be leveraged to implement a software-based Resolver system.

With AM263P's integrated Resolver peripheral, two additional ADC modules (12-bit / 3 MSPS, no comparator subsystem) have been added to directly interface with it. This is in addition to the same five ADC modules with comparator subsystems that remain available. These added ADC modules can be used to interface to two parallel hardware resolver channels. The Resolver subsystem then hardware synchronizes precisely to the motor control PWM signal to enable the optimization of the motor control loop delay.

### 2.1.2 Trigonometric Math Unit

Each R5F core for all AM263P devices comes with a Trigonometric Math Unit (TMU). This hardware accelerator extends the capabilities of the R5F by speeding up the execution of common trigonometric and arithmetic operations. Table 2-1 provides a list of the available instructions in the TMU.

**Table 2-1. List of Implemented Instructions in the TMU**

| Instruction Name | Description |
|---|---|
| SINPUF32 | Returns the SINE of Input value |
| COSPUF32 | Returns the COSINE of Input value |
| ATANPUF32 | Returns the ATAN of Input value |
| QUADF32 | Returns the quadrant value and the ratio of X and Y inputs which are provided as per unit values. |
| IEXP2F32 | Returns inverse exponent of input value |
| LOG2F32 | Returns base-2 logarithm of input value |

### 2.1.3 Remote L2 Cache

Each R5F core for all AM263P devices now has an integrated Remote L2 (RL2) Cache controller that can be used to reserve system memory to cache data. As it uses system memory, the RAM comes with EEC protection. The memory is structured to support 4096 lines of cache support at a line size of 32 bytes. The cache lines are software programmable and can support sizes of 8, 16, 32, 64, or 128kB.

The primary use case for this feature is to cache system data that is typically stored in flash memory into the SoC memory system to improve the processing performance. As the RL2 uses system memory, there are access protections that must be configured to guard its contents so no system data is altered by mistake. For more information, see the *AM263P Technical Reference Manual*.

## 2.2 Memory Subsystem Differences

AM263P comes with three changes to the memory module. The first is an increase in available Tightly-Coupled Memory (TCM) from 64kB to 256kB. The second is an increase in total on-chip RAM (SRAM) from 2MB to 3MB.

The final change is the addition of a Remote L2 (RL2) cache for external memory, programmable up to 128kB per CPU core. This RL2 cache allows users to cache the system flash into the SoC memory system. For full details on this feature, see the *Remote L2 Cache* subchapter of the *AM263P Technical Reference Manual*.

## 2.3 CONTROLSS Module Differences

### 2.3.1 ADC Feature Differences and Additions

AM263Px uses the Type-4 ADC Post-Processing Block (PPB). This enables the following additional features compared to the AM263x Type-3 ADC PPB:

- External Channel Selection – Two ADCxEXTMUX signals are provided for each ADC module. These can be used with an external analog mux to control the channel select to route multiple analog signals to a single ADC channel.
- Repeater Block – Enables fixed amounts of repeated conversions that can be used for oversampling, undersampling, phase delay, and sample spreads.
- Oversampling - The hardware additions in the PPB that support averaging and min/max sample detection are available when oversampling. These can be used for applications like peak detection and outlier removal.
- Synchronization – Sync inputs from either hardware or software allow for the PPBs on different ADC modules to be synchronized.
- Global Software Trigger – This can be used to trigger multiple ADC SOC conversions with a single bit write from the *CONTROLSS_GLOBAL_CTRL* register.

### 2.3.2 ADC Safety Tile Additions

AM263Px adds 12x ADC Safety Tiles and 1x ADC Safety Event Aggregator to support redundant sampling which enables safety checker functionality. The safety tiles allow for ADC conversion results from multiple ADC modules to be compared against each other for consistency. The event aggrerator tracks the results of each check and can generate trip events for overflow events and measurements that exceed the programmed tolerance.

### 2.3.3 ADC_R Module Addition

To support the Resolver peripheral in AM263P devices, two additional SAR ADC modules, ADC_R0 and ADC_R1, have been added. In applications where the Resolver is not utilized, these ADCs can be configured and used as general purpose ADCs. Each has four channels with 12-bit resolution. The most notable differences between ADC_R0-1 versus ADC0-4 is that the maximum sample for ADCR0-1 is 3 MSPS compared to 4 MSPS for ADC0-4 and that ADCR0-1 does not contain the comparator subsystem that is part of each ADC0-4 module. These additional ADCs benefit from all the Type-4 ADC Post Processing Block improvements that are a part of the AM263P ADC0-4 modules.

## 2.4 QSPI/OSPI Module Differences

AM263P devices come with an Octal SPI (OSPI) interface that replaces the Quad SPI (QSPI) interface from AM263 devices. With this new interface, it is possible to connect to both Octal and Quad-SPI flash memories. To connect to OSPI flash memory cells, the interface supports four additional data lines, an additional chip select, and the DQS pin that can be used as a data strobe or loopback clock input. It also includes two reset outputs for external SPI devices and an input for external ECC failure indication.

There is also a significant change in operation regarding data access. The AM263 QSPI interface uses a Serial Flash Interface (SFI) memory-mapped block to handle addressing and data access and this interface was limited to a maximum size of 8MB for external flash support. In comparison, the new AM263P OSPI peripheral does not use a memory-mapped interface block and instead handles direct and indirect data accesses through a data target interface. With this change, the upper limit on memory addresses has been increased to 128 MB.

Due to the differences in data accesses between these interfaces, they are not software compatible and any AM263-to-AM263P migration would require software updates for the QSPI/OSPI interface even if the AM263P OSPI bus is only used as a QSPI bus.

A high-level table of feature differences between these interfaces is provided below. For further details, see the device-specific Technical Reference Manuals.

| Feature | AM263 Quad SPI | AM263P Octal SPI |
|---|---|---|
| # of Data Lines | 4 | 8 |
| # of Chip Select Lines | 1 | 2 |
| External Device Reset | N/A | Yes, 2 outputs |
| Data Strobe | N/A | Yes |
| ECC Fail Indicator | N/A | Yes, 1 input |
| Data Access | Data access through the SFI memory-mapped interface only | Direct and indirect access supported |
| Maximum External Flash Supported Per Chip Select | 8 MB | 128 MB |
| **opTI Flash Support** | | |
| XIP | No | Yes |
| Boot Acceleration | No | Yes |
| FOTA Acceleration | No | Yes |

## 2.5 Hardware Security Module Differences

AM263P devices come with two changes to the Hardware Security Module (HSM). The first is that the dedicated RAM for the HSM is increased from 192kB on AM263 devices to 256kB on AM263P devices.

Second, the HSM Watchdog Timer (WDT) is enabled by default in AM263P devices. With this change, the default clock source for the HSM WDT has been changed to RCCLK10M and the default timeout is set to 25 milliseconds.

## 2.6 Hardware Differences

### 2.6.1 Sourcing VPP With ANALDO

With AM263P, it is possible to use the ANALDO output to connect to the VPP rail to source VPP without the need for an external LDO. By taking advantage of this added functionality, BOM costs can be reduced by removing the VPP LDO from the hardware design.

Figure 2-1 illustrates how the connection can be made. For boards that need to support AM263 devices, a path can be added to support the LDO as necessary.

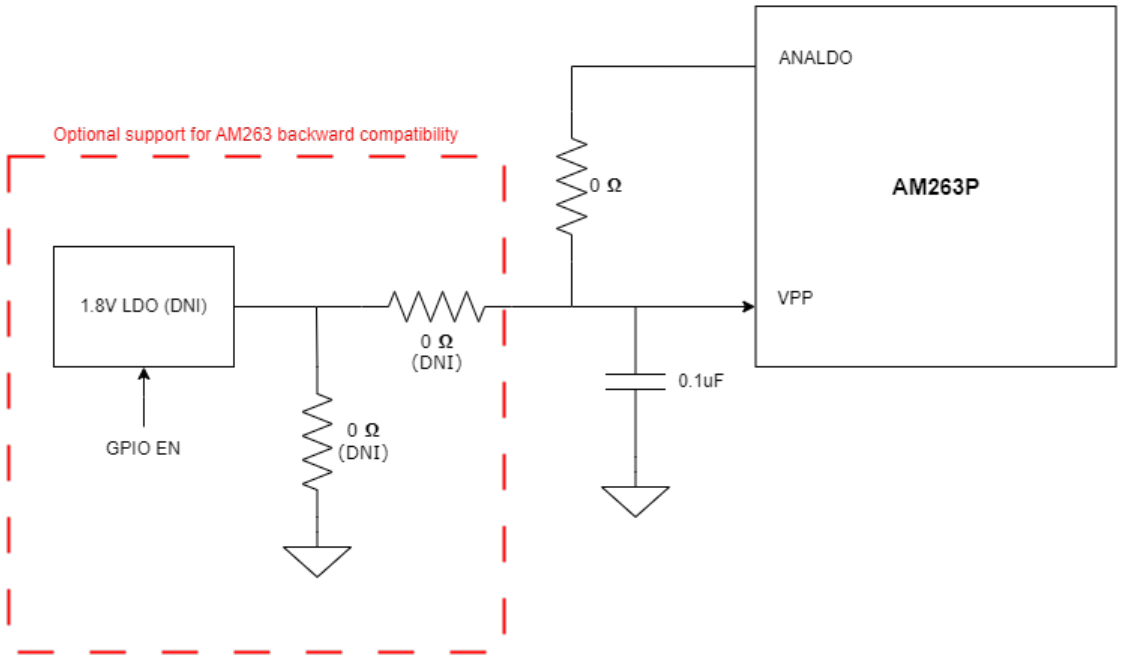


**Figure 2-1. Example Schematic**

## 3 Software Changes Between AM263 and AM263P SDK

| Component | AM263 | AM263P |
|---|---|---|
| ADC | IP Type 3<br>Driver v1 | New hardware feature now supports IP Type 4.<br>SDK includes drivers (v2), documentation, unit test, and examples in SDK for the new additions with Type 4.<br>Type 4 additions include the following:<br>• DMA trigger (added feature)<br>• SOC Trigger (added feature)<br>• Trigger Repeater block (new feature set)<br>• PPB Aggregator (new feature set)<br>• External Channel Selection<br>• Open Short Detection (new feature) |
| ADC Safety,<br>ADC Safety Aggr | N/A | New hardware feature.<br>SDK includes driver (v0), documentation, unit test, and examples for the following features:<br>• Comparison against any 2 selected results across most ADC modules with the exception of the the 3MSPS or ADC-R modules.<br>• Usage of interrupts when one or more threshold reaches occur across all the ADC Safety Tiles |
| Resolver | N/A | New hardware feature.<br>SDK includes driver (v0), documentation, unit test, and examples for the following features:<br>• Sequencer modes to support single motor single core, single motor lockstep core, and dual motor dual core configurations.<br>• Demonstration of a safety diagnostics feature.<br>Software implementation of Track2 loop is included with the provided examples. |

| Component | AM263 | AM263P |
|---|---|---|
| Sigma Delta Filter Module (SDFM) | IP Type 2.1<br>Driver v0 | No hardware changes.<br>Additional SDK examples provided:<br>• Workaround for SDFM Digital Filter interrupt reassertion issue<br>• SDFM-ECAP loopback example |
| SoC driver - ControlSS CTRL | N/A | New hardware feature.<br>SDK includes driver, documentation, unit test, and examples for the following features:<br>• Dynamic clock gating<br>• How to configure the EPWM to use WLINK |
| Trip and Sync XBAR | N/A | New hardware feature.<br>SDK includes driver, documentation, unit test, and examples for the following features:<br>• New XBARs - EXTCHSEL, EQEP SOCAB XBAR, new groups to XBARs<br>• XBAR clock gating |
| Opti-Flash<br>• FLC<br>• RL2<br>• RAT | N/A | New hardware feature.<br>SDK includes driver (v0), documentation, unit test, and examples for the following features:<br>• RL2 example for how to configure the new feature<br>• FLC example for early CAN response |
| OSPI | QPSI | New hardware feature.<br>SDK includes driver (v0), documentation, unit test, and examples for the following features:<br>• Flash Diagnostics Example<br>• Flash DMA Example<br>• Flash IO Example<br>• Use of two chip select pins<br>QSPI is also supported with FLASH API which internally uses OSPI, however this requires software updates when transitioning from AM263 to AM263P. |
| SBL OSPI | SBL QSPI | SBL-OSPI is provided for AM263P |
| eXecute In Place (XIP) support | N/A | New hardware feature.<br>Enabling XIP functionality does not require dedicated drivers.<br>With XIP functionality offered in AM263P, it is possible to change the boot flow on a per application basis to leverage XIP. |
| Firmware Over the Air Update (FOTA) | N/A | New hardware feature.<br>SDK includes driver (v0), documentation, and unit test. |
| On The Fly Encryption and Authentication (OTFA) | N/A | New hardware feature.<br>SDK includes driver (v0), documentation, and unit test |
| Smart Placement | N/A | New compiler support.<br>This has been developed because Sitara Microcontrollers have different levels of memory with varying latency between the core and peripherals.<br>Smart placement distributes functions and other linker-placed objects across different memories by assigning critically based on the frequency of use to minimize perform degradation.<br>This new feature is available for other Sitara Microcontroller SoCs in addition to AM263P once released. |
| Function-call Based Layout | N/A | New compiler support.<br>This feature is part of Smart Placement and is geared towards improving the performance of key usage for boot acceleration. However, this can be applied to any startup code.<br>It operates by grouping startup code functions and data in execution order into address regions that can be programmed using a Fast Local Copy (FLC) hardware accelerator.<br>This new feature will be available for other Sitara Microcontroller SOCs in addition to AM263P once released. |

# 4 List of Errata Fixes in AM263P

Table 4-1 contains a comprehensive list of Errata items from AM263 and outlines in which issues are fixed in either Rev 1.1 of AM263 or Rev 1.0 of AM263P. Full details for the errata items are provided in AM263x Sitara™ Microcontroller Silicon Revision 1.0A, 1.1.

**Table 4-1. AM263/AM263P Errata Fixes**

| Module | Description | Silicon Revisions Affected | | |
|---|---|---|---|---|
| | | AM263x | | AM263P |
| | | 1.0A | 1.1 | 1.0 |
| CLOCKS | i2324 — No synchronizer present between GCM and GCD status signals | Present | Present | Present |
| QSPI | i2364 — QSPI: Access to address beyond 8MB is not supported in mem map mode | Present | Present | New OSPI module can support addresses beyond 8MB |
| VDDA | i2348 — VDDA1V8 Static Power leakage | Present | Fixed | Fixed |
| ADC | i2346 — ADC result has Error when switching between odd and even channels | Present | Fixed | Fixed |
| ADC | i2347 — VREF current consumption of ADC is random at powerup | Present | Fixed | Fixed |
| ADC | i2349 — ADC VrefHi Loading increase in powerdown | Present | Fixed | Fixed |
| CONTROLSS | i2352 — CONTROLSS-SDFM: Dynamically Changing Threshold Settings (LLT, HLT), Filter Type, or COSR Settings Will Trigger Spurious Comparator Events | Present | Present | Present |
| CONTROLSS | i2353 — CONTROLSS-SDFM: Dynamically Changing Data Filter Settings (Such as Filter Type or DOSR) Will Trigger Spurious Data Acknowledge Events | Present | Present | Present |
| CONTROLSS | i2354 — CONTROLSS-SDFM: Two Back-to-Back Writes to SDCPARMx Register Bit Fields CEVT1SEL, CEVT2SEL, and HZEN Within Three SD-Modulator Clock Cycles can Corrupt SDFM State Machine, Resulting in Spurious Comparator Events | Present | Present | Present |
| CONTROLSS | i2355 — CONTROLSS-ADC: DMA Read of Stale Result | Present | Present | Fixed |
| CONTROLSS | i2356 — CONTROLSS-ADC: Interrupts may Stop if INTxCONT (Continue-to-Interrupt Mode) is not Set | Present | Present | Present |
| CONTROLSS | i2357 — CONTROLSS-ePWM: An ePWM Glitch can Occur if a Trip Remains Active at the End of the Blanking Window | Present | Present | Present |
| CONTROLSS | i2358 — CONTROLSS-ePWM: Trip Events Will Not be Filtered by the Blanking Window for the First 3 Cycles After the Start of a Blanking | Present | Present | Present |
| CONTROLSS | i2359 — CONTROLSS-CMPSS:Prescaler counter behaviour different from spec when DACSOURCE is made 0 or reconfigured as 1 | Present | Present | Present |
| CONTROLSS | i2405 — Race condition OUTPUT_XBAR and PWM_XBAR resulting in event miss | Present | Present | Present |
| CPSW | i2345 — CPSW: Ethernet Packet corruption occurs if CPDMA fetches a packet which spans across memory banks | Present | Present | Present |
| CPSW | i2401 — Host Timestamps Cause CPSW Port to Lock up | Present | Present | Present |
| CPSW | i2402 — Ethernet to Host Checksum Offload does not work | Present | Present | Fixed |
| CPSW | i2329 — MDIO interface corruption (CPSW and PRU-ICSS) | Present | Fixed | Fixed |
| CRC | i2386 — CRC 8-bit data width and CRC8-SAE-J1850 and CRC8-H2F possible use in CAN module is not supported | Present | Present | Fixed |
| DCC | i2395 — DCC Module Frequency Comparison can Report Erroneous Results | Present | Present | Fixed |
| GPMC | i2313 — GPMC: Sub-32-bit read issue with NAND and FPGA/FIFO | Present | Present | Not Applicable |
| M4 ROM | i2403 — SBL redundant boot image feature not supported on HSSE devices | Not Applicable | Present | Not Applicable |
| MBOX | i2404 — Race condition in mailbox registers resulting in events miss | Present | Present | Present |
| McSPI | i2350 — McSPI data transfer using EDMA in ‘ABSYNC’ mode stops after 32 bits transfer | Present | Present | Fixed |
| MSS_CTRL | i2392 — Race condition in mem-init capture registers resulting in events miss | Present | Present | Present |
| MSS_CTRL | i2394 — Race condition in interrupt and error aggregator capture registers resulting in events miss | Present | Present | Present |

**Table 4-1. AM263/AM263P Errata Fixes (continued)**

| Module | Description | Silicon Revisions Affected | | |
|---|---|---|---|---|
| | | AM263x | | AM263P |
| | | 1.0A | 1.1 | 1.0 |
| R5FSS | i2374 — PBIST fails if clock frequency of R5SS_CORE_CLK is not same as R5FSS_CLK_SELECTED frequency | Present | Present | Present |
| SDFM | i2375 — SDFM module event flags (SDIFLG.FLTx_FLG_CEVTx) do not get set again if the comparator event is still active and digital filter path (using SDCOMPxCTL.CEVTxDIGFILTSEL) is being selected | Present | Present | Fixed |
| UART | i2310 — USART: Erroneous triggering of timeout interrupt | Present | Present | Present |
| UART | i2311 — USART: Spurious DMA Interrupts | Present | Present | Present |

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