

# Custom DDR Memory Mapping for Vision Applications on Jacinto™ SoCs



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## Introduction

The Jacinto family of SoCs from Texas Instruments (TI) is designed to support a wide range of automotive DL applications, offering powerful processing capabilities for vision and inference tasks. To facilitate development, TI provides an EVM for users to prototype, test, and validate use cases. The EVM comes with a predefined DDR configuration; users have the flexibility to choose any size DDR that is designed for specific DL requirements. The SDK released by TI for the SoCs includes memory maps and DDR configuration settings tailored to the EVM. However, for users using custom boards, adjust settings to match the custom DDR setup.

This application brief focuses on the necessary changes to vision application memory mapping, guiding customers through the process of modifying the memory configuration to establish compatibility with a custom hardware setup.

The DDR sizes on the EVM for various SOC are as shown in [Table 1](#).

**Table 1. DDR Sizes on the EVM for Various SOC**

SOC	DDR Size (GB)
J721E	4
J721s2	16
J722s	8
J742s2	32
J784s4	32
J7200	4

## Guidelines for Custom DDR Sizes Over 2GB Differing from EVM

The DDR memory is mapped to the SOC so that the first 2GB of the memory lies in the lower bank (for example, the 32-bit address starts from 0x80000000 to 0xFFFFFFFF) and the rest of the DDR memory is mapped to the upper bank (for example, the 64-bit address 0x880000000 to [SOC Total DDR Size]).

Refer to [Table 2](#) if a board has a DDR of size less than or greater than that of the EVM (but greater than 2GB).

**Table 2. Modify the vision\_apps Memory Map**

SOC	Guide
J721E	Texas Instruments, <a href="#">8.9. Understanding and updating SDK memory map for J721E — Processor SDK RTOS J721E developer notes</a>
J722s	Texas Instruments, <a href="#">9.6. Understanding and updating SDK memory map for J722S — Processor SDK RTOS J722S developer notes</a>
J721s2	Texas Instruments, <a href="#">9.9. Understanding and updating SDK memory map for J721S2 — Processor SDK RTOS J721S2 developer notes</a>
J784s4	Texas Instruments, <a href="#">9.9. Understanding and updating SDK memory map for J784S4 developer notes</a>

[Table 2](#) elaborates on the method to modify the vision\_apps memory map for customer use-cases.

Additionally, changes are required in the bootloader, U-boot, and underlying HLOS based on the boot flow of the user. Refer the below FAQ to understand the modifications involved here in such cases.

Texas Instruments, [\[FAQ\] TDA4VM/TDA4VL/TDA4AL/TDA4VH/DRA821: How can we make the Jacinto SDK compatible for device variants?](#), E2E forum

### Guidelines for Custom DDR Sizes Less Than 2GB

If the board has a DDR of size less than 2GB, modify the memory map so that the upper 64-bit region of the DDR is unused by any core. Per the default SDK memory map, the typical local heap and scratch regions for the C7x core are found in the upper region, along with the physical memory mapping of DDR\_SHARED\_MEM.

Follow the below steps for modifying custom DDR sizes less than 2GBs

1. Move the local heap and scratch regions of C7x cores to the lower 2 GB region.
2. Verify that the MMU mapping in the C7x core maps local heap and scratch regions to the physical address, such as a 32-bit address, and not to the virtual address.
3. Confirm that the DDR\_SHARED\_MEM\_PHYS\_ADDR and DDR\_SHARED\_MEM\_ADDR point to the same address and are the same size.
4. For J784s4, change the order of the MMU mapping for non-cacheable heap and scratch regions for C7x so that the J784s4 comes after the MAIR7 mapping to prevent overwriting.

Follow the above modifications and instructions mentioned in the previous section to implement memory mapping.

### Sample Memory Maps for SoCs Using Only Lower 2GB Regions

[Table 3](#) is the modified python script to cater a 2GB DDR to run the vision\_apps application. The python script is tested on SDK 10.0 for all SOCs. Replace the python script in the path `_${PSDKRA}/vision_apps/platform/${SOC}/rtos/gen_linker_mem_map.py` and execute the same to generate the updated memory map.

Apply the below patch in the path in `_${PSDKRA}/vision_apps/` and follow the instructions in the [Table 2](#) to achieve memory mapping.

**Table 3. Links to Modified Python Scripts**

SOC	Python Script	Additional Patches
J721E	Texas Instruments, <a href="#">gen_linker_mem_map.py</a>	Texas Instruments, <a href="#">2GB_config.patch</a>
J721s2	Texas Instruments, <a href="#">gen_linker_mem_map.py</a>	Texas Instruments, <a href="#">2GB_config.patch</a>
J784s4	Texas Instruments, <a href="#">gen_linker_mem_map.py</a>	Texas Instruments, <a href="#">2GB_config.patch</a>

The same approach extends to the other SOCs.

### Conclusion

This application brief provides a sample of 2GB DDR configuration, but the same is extendable by modifying the region sizes per use case. Use the default memory map in the SDK as a reference for custom boards with DDR of size greater than 2GB and use this application note as a reference for custom boards with a DDR size 2GB or less.

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