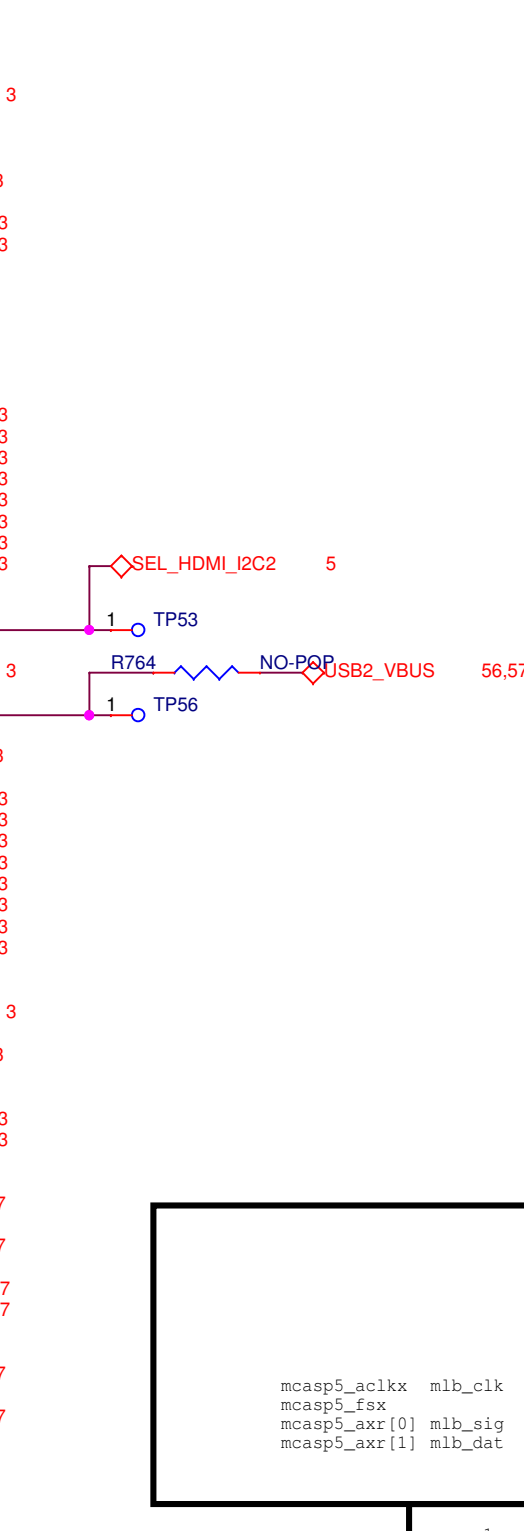
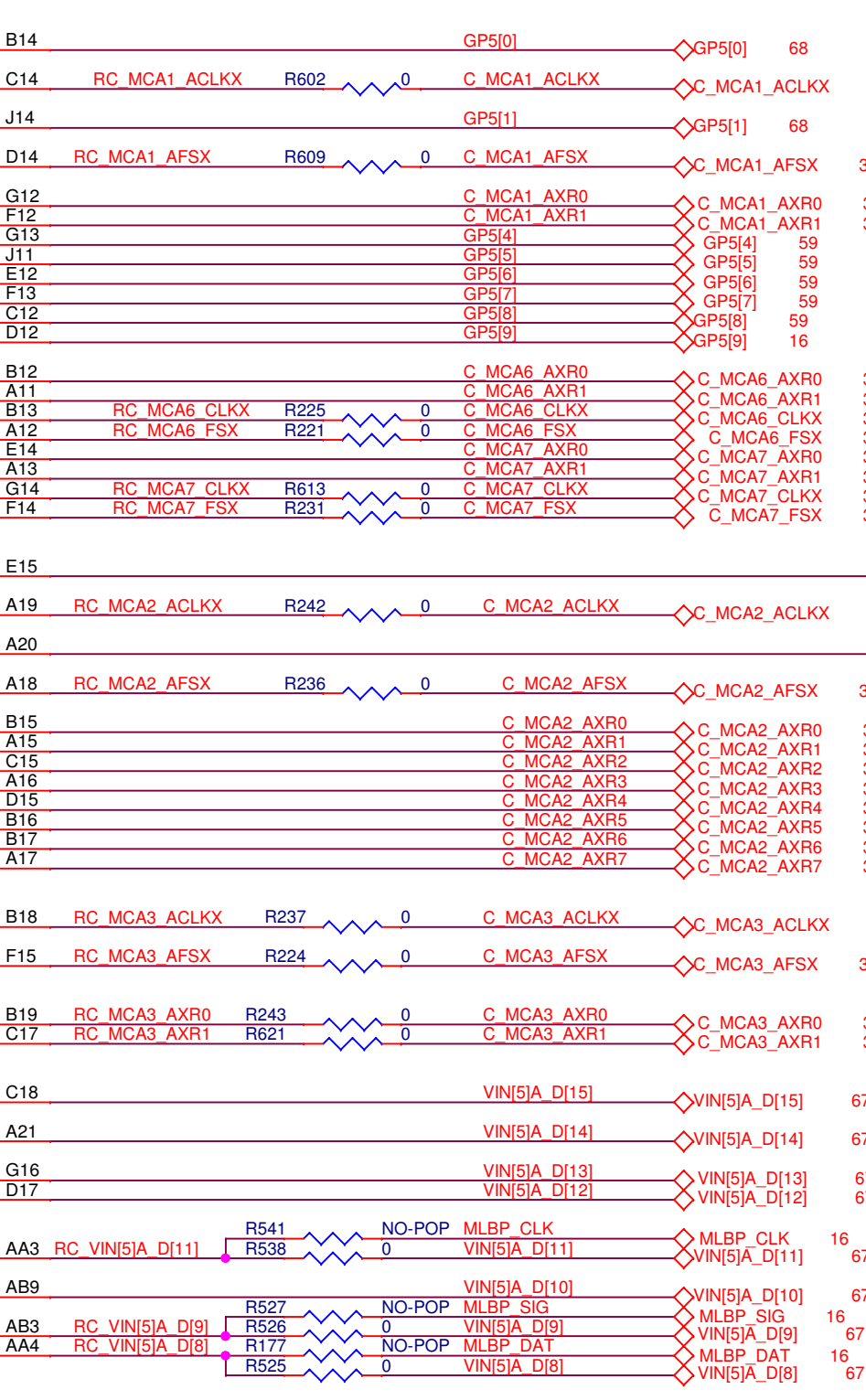
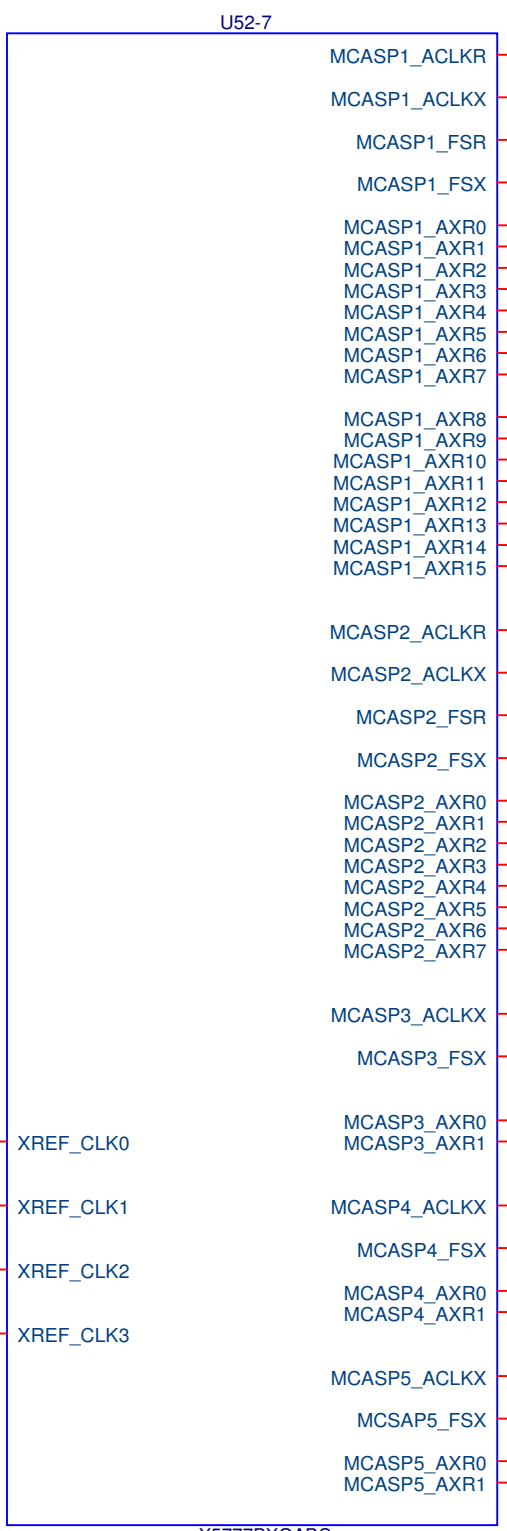



```

gpio5_4 mcaspl_axr[2]
gpio5_5 mcaspl_axr[3]
gpio5_6 mcaspl_axr[4]
gpio5_7 mcaspl_axr[5]
gpio5_8 mcaspl_axr[6]
gpio5_9 mcaspl_axr[7]
gpio5_10 mcaspl_axr[8]
gpio5_11 mcaspl_axr[9]
gpio5_12 mcaspl_axr[10]
gpio4_17 mcaspl_axr[11]
gpio4_18 mcaspl_axr[12]
gpio6_4 mcaspl_axr[13]
gpio6_5 mcaspl_axr[14]
gpio6_6 mcaspl_axr[15]

```



```

mcasp1_axr[8] mcaspl6_axr[0] vin6a_d[15]
mcasp1_axr[9] mcaspl6_axr[1] vin6a_d[14]
mcasp1_axr[10] mcaspl6_aclkx vin6a_d[13]
mcasp1_axr[11] mcaspl6_fsx vin6a_d[12]
mcasp1_axr[12] mcaspl7_axr[0] vin6a_d[11]
mcasp1_axr[13] mcaspl7_axr[1] vin6a_d[10]
mcasp1_axr[14] mcaspl7_aclkx vin6a_d[9]
mcasp1_axr[15] mcaspl7_fsx vin6a_d[8]

```

```

mcasp1_axr[12] mcaspl7_axr[0] vin6a_d[11]
mcasp1_axr[13] mcaspl7_axr[1] vin6a_d[10]
mcasp1_axr[14] mcaspl7_aclkx vin6a_d[9]
mcasp1_axr[15] mcaspl7_fsx vin6a_d[8]

```

```

mcasp2_aclkx vin6a_d[7]
mcasp2_fsx vin6a_d[6]
mcasp2_aclkr
mcasp2_fsr
mcasp2_axr[0]
mcasp2_axr[1]
mcasp2_axr[2] vin6a_d[5]
mcasp2_axr[3] vin6a_d[4]
mcasp2_axr[4]
mcasp2_axr[5]
mcasp2_axr[6]
mcasp2_axr[7]

```

```

mcasp3_aclkx vin6a_d[3]
mcasp3_fsx vin6a_d[2]
mcasp3_axr[0] vin6a_d[1]
mcasp3_axr[1] vin6a_d[0]

```

```

mcasp4_aclkx vin5a_d[15]
mcasp4_fsx vin5a_d[14]
mcasp4_axr[0] vin5a_d[13]
mcasp4_axr[1] vin5a_d[12]
McASP5
mcasp5_aclkx vin5a_d[11]
mcasp5_fsx vin5a_d[10]
mcasp5_axr[0] vin5a_d[9]
mcasp5_axr[1] vin5a_d[8]

```

```

mcasp1_aclkx vin6a_fld0
mcasp1_fsx vin6a_de0
mcasp1_aclkr
mcasp1_fsr
mcasp1_axr[0] vin6a_vsync0
mcasp1_axr[1] vin6a_hsync0

```

```

xref_clk2 mcaspl_ahclkx

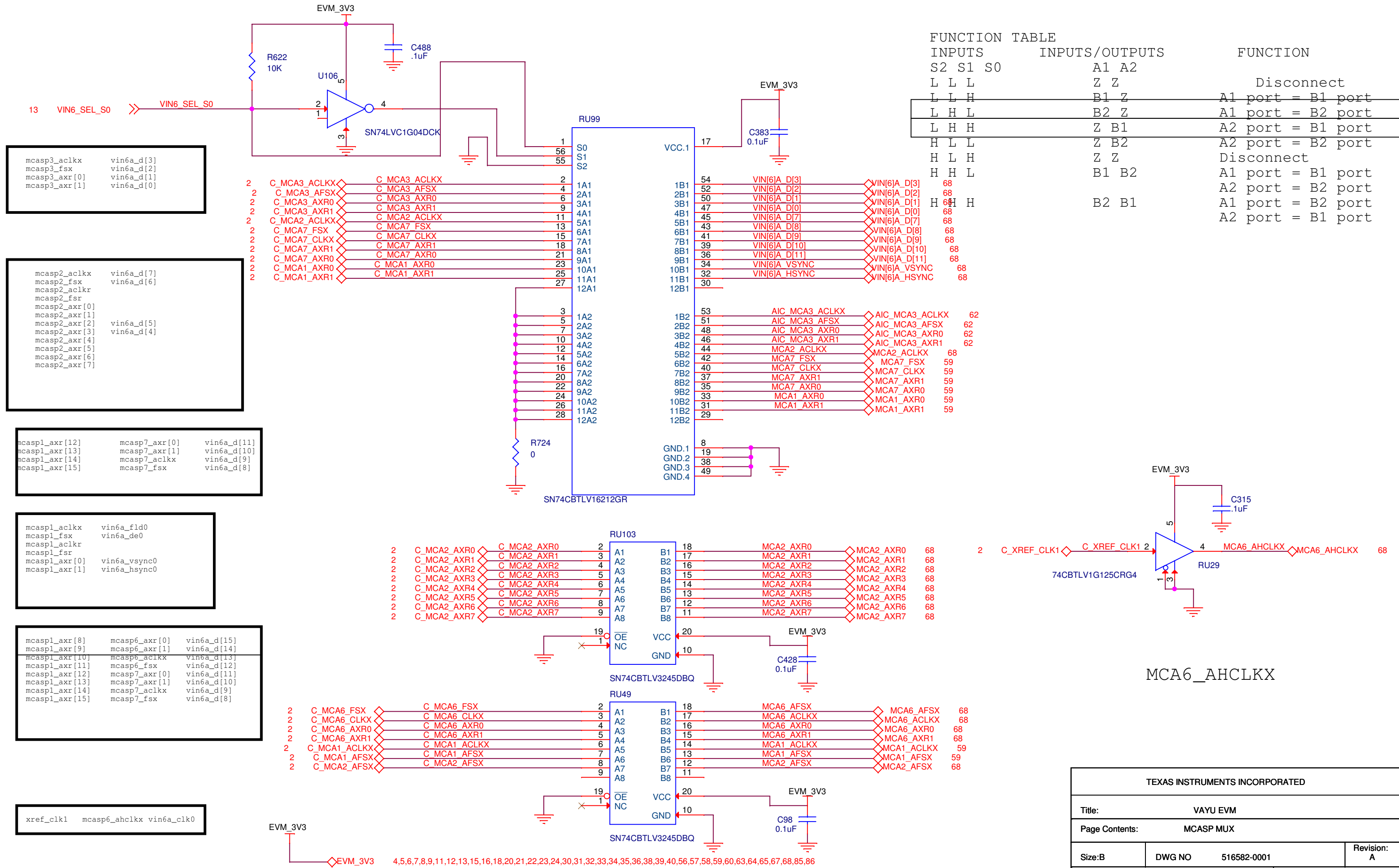
```

```

xref_clk1 mcaspl6_ahclkx vin6a_clk0

```

TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		VAYU McASP	
Size: B	DWG NO	516582-0001	Revision: C
Date: Tuesday, January 12, 2016	Sheet 2 of	89	



FUNCTION TABLE			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port
H	H	H	B2	B1	A2 port = B1 port

```

mcasp3_aclkx  vin6a_d[3]
mcasp3_fsx    vin6a_d[2]
mcasp3_axr[0] vin6a_d[1]
mcasp3_axr[1] vin6a_d[0]

```

```

mcasp2_aclkx  vin6a_d[7]
mcasp2_fsx    vin6a_d[6]
mcasp2_aclkr
mcasp2_fsr
mcasp2_axr[0]
mcasp2_axr[1]
mcasp2_axr[2]  vin6a_d[5]
mcasp2_axr[3]  vin6a_d[4]
mcasp2_axr[4]
mcasp2_axr[5]
mcasp2_axr[6]
mcasp2_axr[7]

```

```

mcasp1_axr[12]  mcasp7_axr[0]  vin6a_d[11]
mcasp1_axr[13]  mcasp7_axr[1]  vin6a_d[10]
mcasp1_axr[14]  mcasp7_aclkx  vin6a_d[9]
mcasp1_axr[15]  mcasp7_fsx    vin6a_d[8]

```

```

mcasp1_aclkx  vin6a_fld0
mcasp1_fsx    vin6a_de0
mcasp1_aclkr
mcasp1_fsr
mcasp1_axr[0]  vin6a_vsync0
mcasp1_axr[1]  vin6a_hsync0

```

```

mcasp1_axr[8]  mcasp6_axr[0]  vin6a_d[15]
mcasp1_axr[9]  mcasp6_axr[1]  vin6a_d[14]
mcasp1_axr[10] mcasp6_aclkx  vin6a_d[13]
mcasp1_axr[11] mcasp6_fsx    vin6a_d[12]
mcasp1_axr[12] mcasp7_axr[0]  vin6a_d[11]
mcasp1_axr[13] mcasp7_axr[1]  vin6a_d[10]
mcasp1_axr[14] mcasp7_aclkx  vin6a_d[9]
mcasp1_axr[15] mcasp7_fsx    vin6a_d[8]

```

```

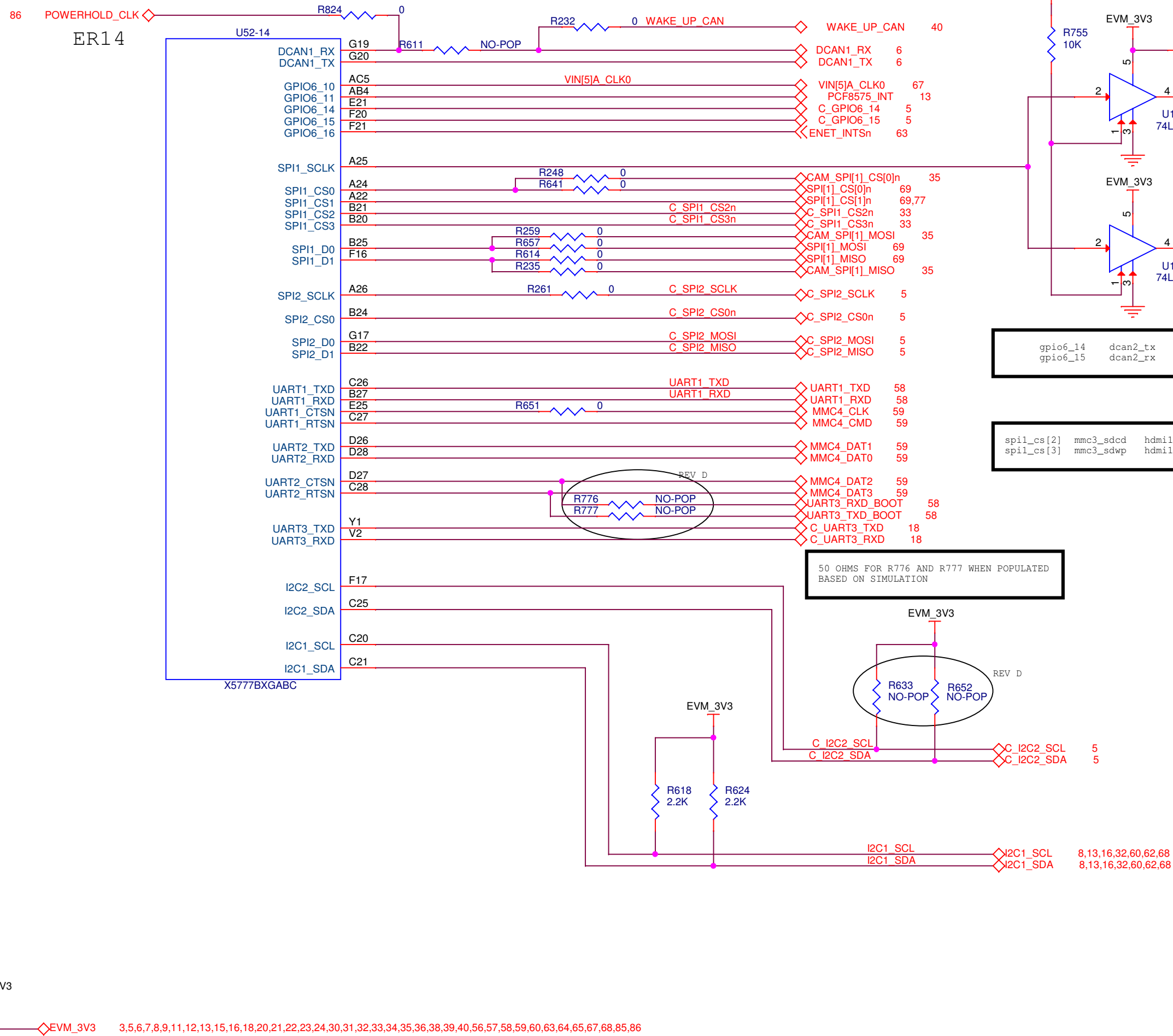
xref_clk1  mcasp6_ahclkx  vin6a_clk0

```

Pin	Signal	Pin	Signal	Pin	Signal
2	C_MCA2_AXR0	2	MCA2_AXR0	18	MCA2_AXR0
2	C_MCA2_AXR1	3	MCA2_AXR1	17	MCA2_AXR1
2	C_MCA2_AXR2	4	MCA2_AXR2	16	MCA2_AXR2
2	C_MCA2_AXR3	5	MCA2_AXR3	15	MCA2_AXR3
2	C_MCA2_AXR4	6	MCA2_AXR4	14	MCA2_AXR4
2	C_MCA2_AXR5	7	MCA2_AXR5	13	MCA2_AXR5
2	C_MCA2_AXR6	8	MCA2_AXR6	12	MCA2_AXR6
2	C_MCA2_AXR7	9	MCA2_AXR7	11	MCA2_AXR7

Pin	Signal	Pin	Signal	Pin	Signal
2	C_MCA6_FSX	2	MCA6_FSX	18	MCA6_FSX
2	C_MCA6_CLKX	3	MCA6_CLKX	17	MCA6_CLKX
2	C_MCA6_AXR0	4	MCA6_AXR0	16	MCA6_AXR0
2	C_MCA6_AXR1	5	MCA6_AXR1	15	MCA6_AXR1
2	C_MCA1_ACLKX	6	MCA1_ACLKX	14	MCA1_ACLKX
2	C_MCA1_AFSX	7	MCA1_AFSX	13	MCA1_AFSX
2	C_MCA2_AFSX	8	MCA2_AFSX	12	MCA2_AFSX
2	C_MCA2_AFSX	9	MCA2_AFSX	11	MCA2_AFSX

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: MCASP MUX			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 3 of 89	



gpio6_14 dcan2_tx
gpio6_15 dcan2_rx

spi1_cs[2] mmc3_sdc d hdmil_hpd
spi1_cs[3] mmc3_sdwp hdmil_cec

spi2_sclk uart3_rxd
spi2_d[1] uart3_txd
spi2_d[0] uart3_ctsn
spi2_cs[0] uart3_rtsn

uart1_ctsn mmc4_clk
uart1_rtsn mmc4_cmd

uart2_rxd mmc4_dat[0]
uart2_txd mmc4_dat[1]
uart2_ctsn mmc4_dat[2]
uart2_rtsn mmc4_dat[3]

i2c2_sda hdmil_ddc_scl
i2c2_scl hdmil_ddc_sda

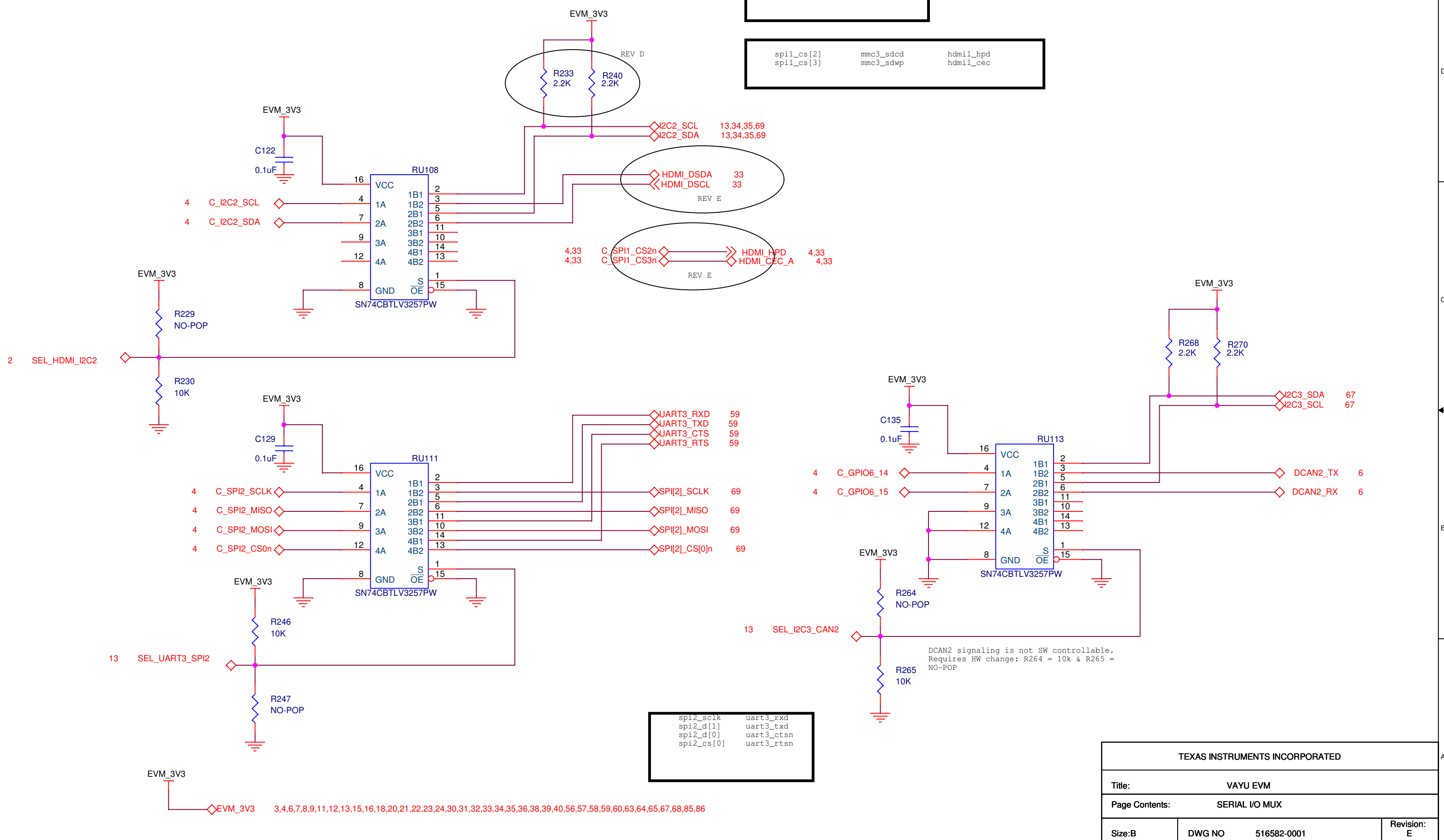
50 OHMS FOR R776 AND R777 WHEN POPULATED
BASED ON SIMULATION

EVM_3V3 3,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85,86

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: SERIAL I/O			
Size: B	DWG NO	516582-0001	Revision: D
Date: Tuesday, January 12, 2016		Sheet 4 of 89	

i2c2_sda	hdmi1_ddc_scl
i2c2_scl	hdmi1_ddc_sda

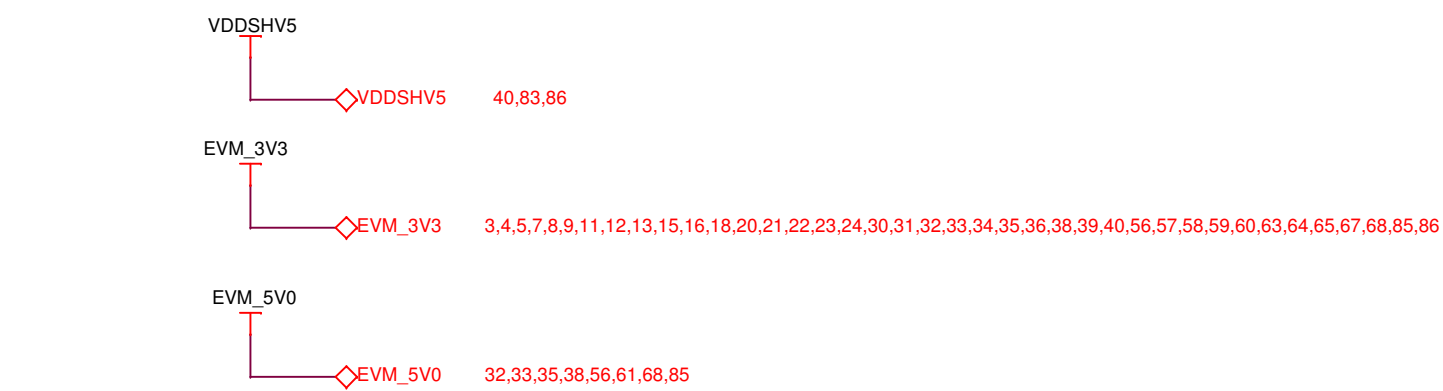
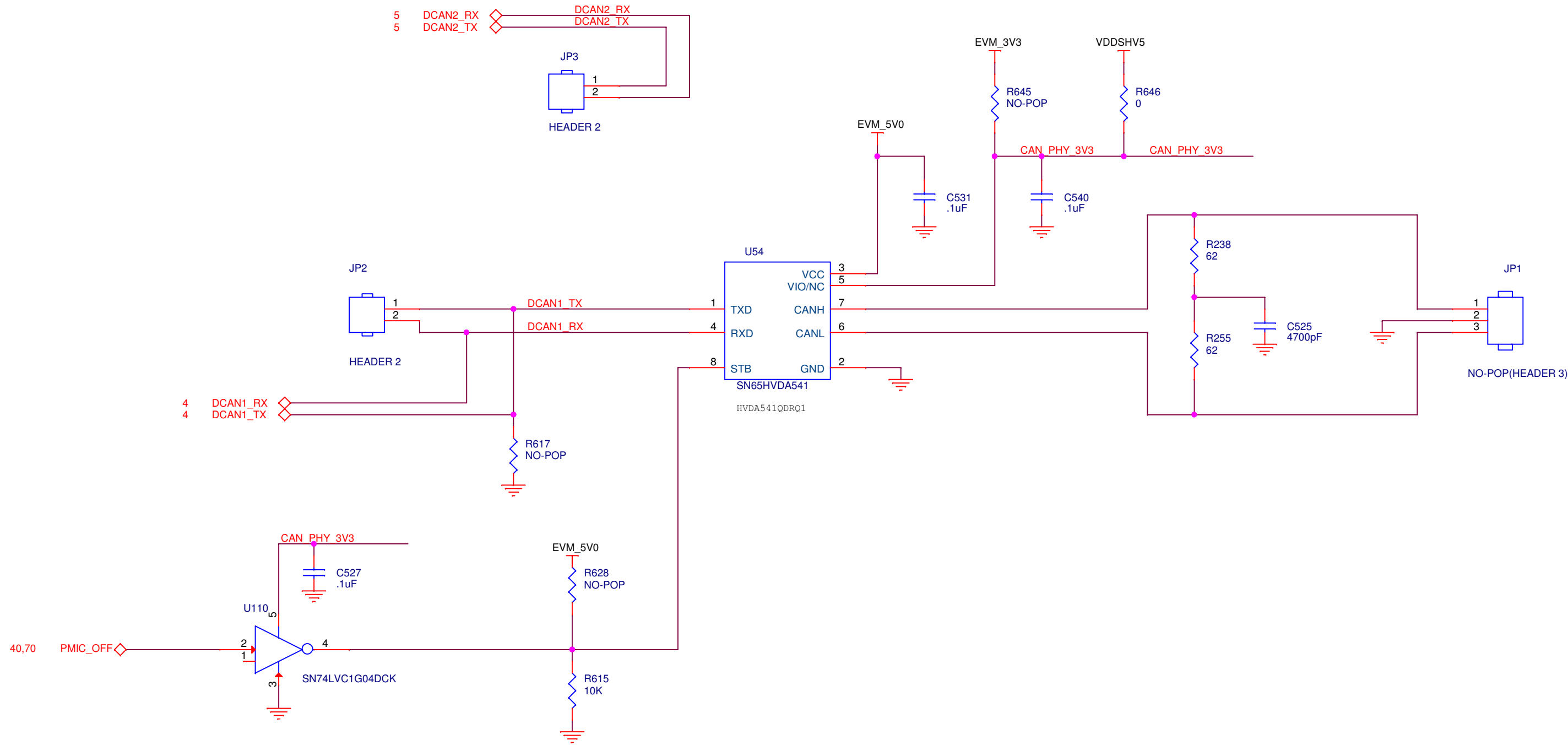
spi1_cs[2]	mmc3_sdccl	hdmi1_hpd
spi1_cs[3]	mmc3_sdwp	hdmi1_cec



spi2_sclk	uart3_rxd
spi2_d[1]	uart3_txd
spi2_d[0]	uart3_ctsn
spi2_cs[0]	uart3_rtsn

DCAN2 signaling is not SW controllable. Requires HW change: R264 = 10k & R265 = NO-POP

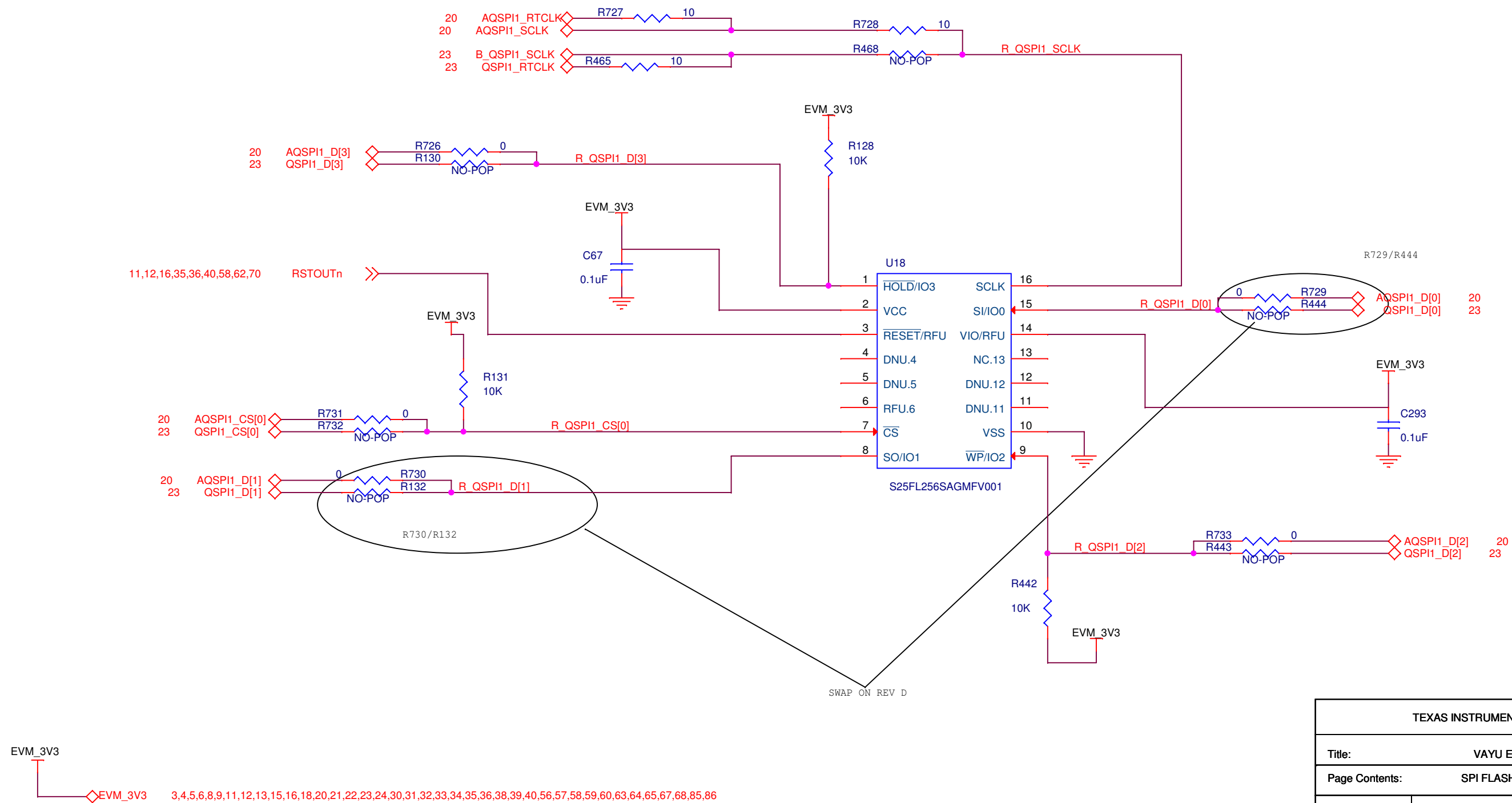
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: SERIAL I/O MUX			
Size: B	DWG NO	516582-0001	Revision: E
Date: Tuesday, January 12, 2016	Sheet 5 of 89		



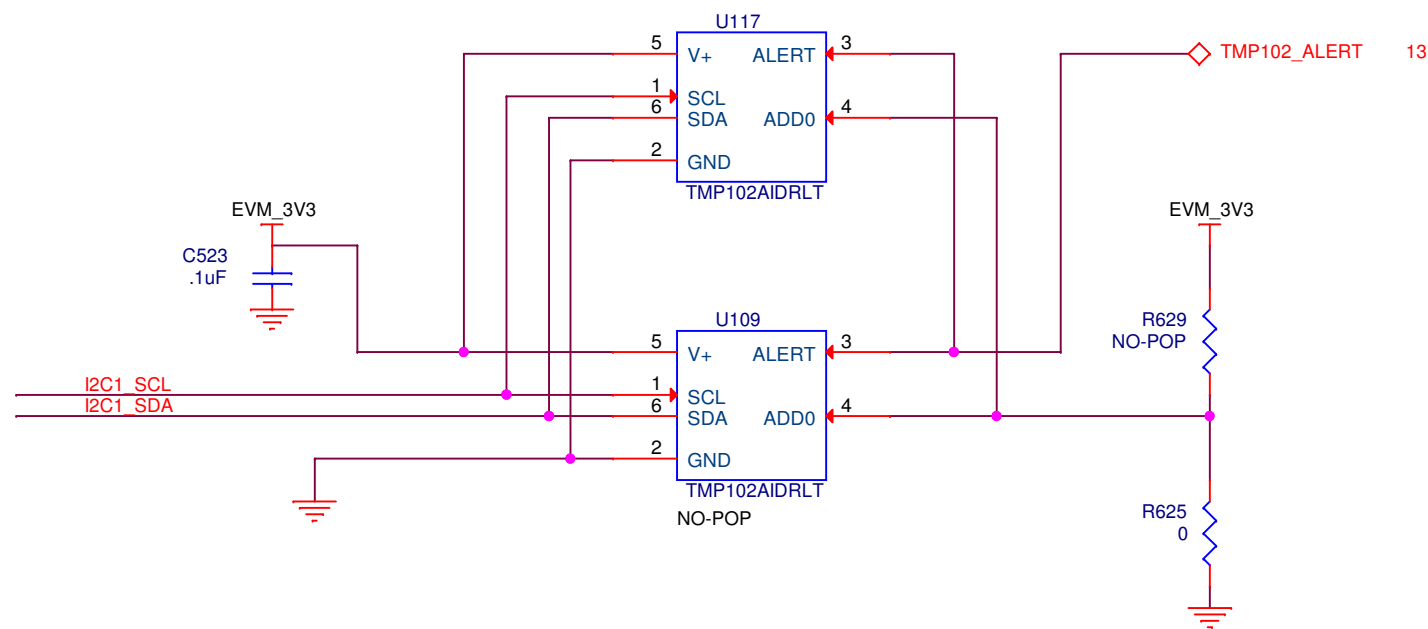
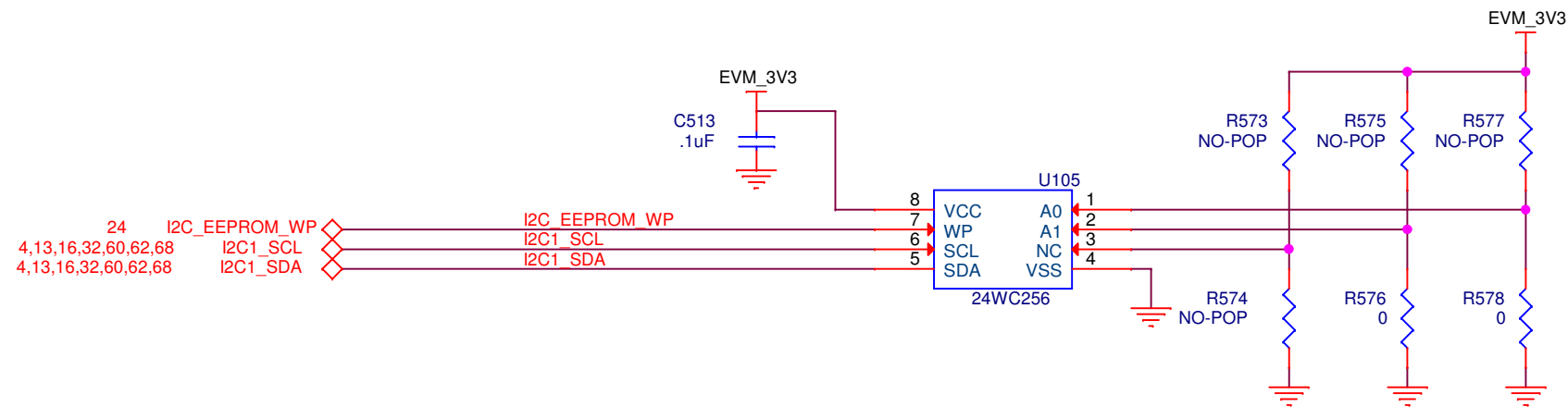
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: CAN CONNECTORS			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 6 of 89	

ROUTE THE FOLLOWING SIGNALS AS A GROUP
 WITH A NET LENGTH LESS THEN 2.75
 INCHES AND 60ps OF SKEW. PLACE THE
 DUAL RESISTOR CLOSE TOGETHER NEAR THE
 PIN OF THE FLASH.

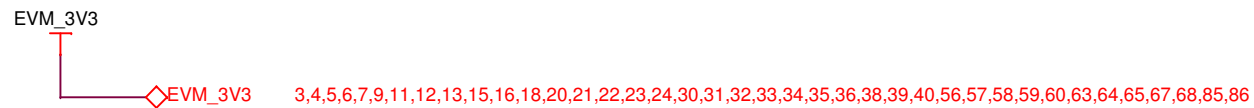
AQSPI1_SCLK
 AQSPI1_RTCLK
 AQSPI1_CS[0]
 AQSPI1_D[0]
 AQSPI1_D[1]
 AQSPI1_D[2]
 AQSPI1_D[3]



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: SPI FLASH			
Size: B	DWG NO	516582-0001	Revision: D2
Date: Tuesday, January 12, 2016		Sheet 7 of 89	



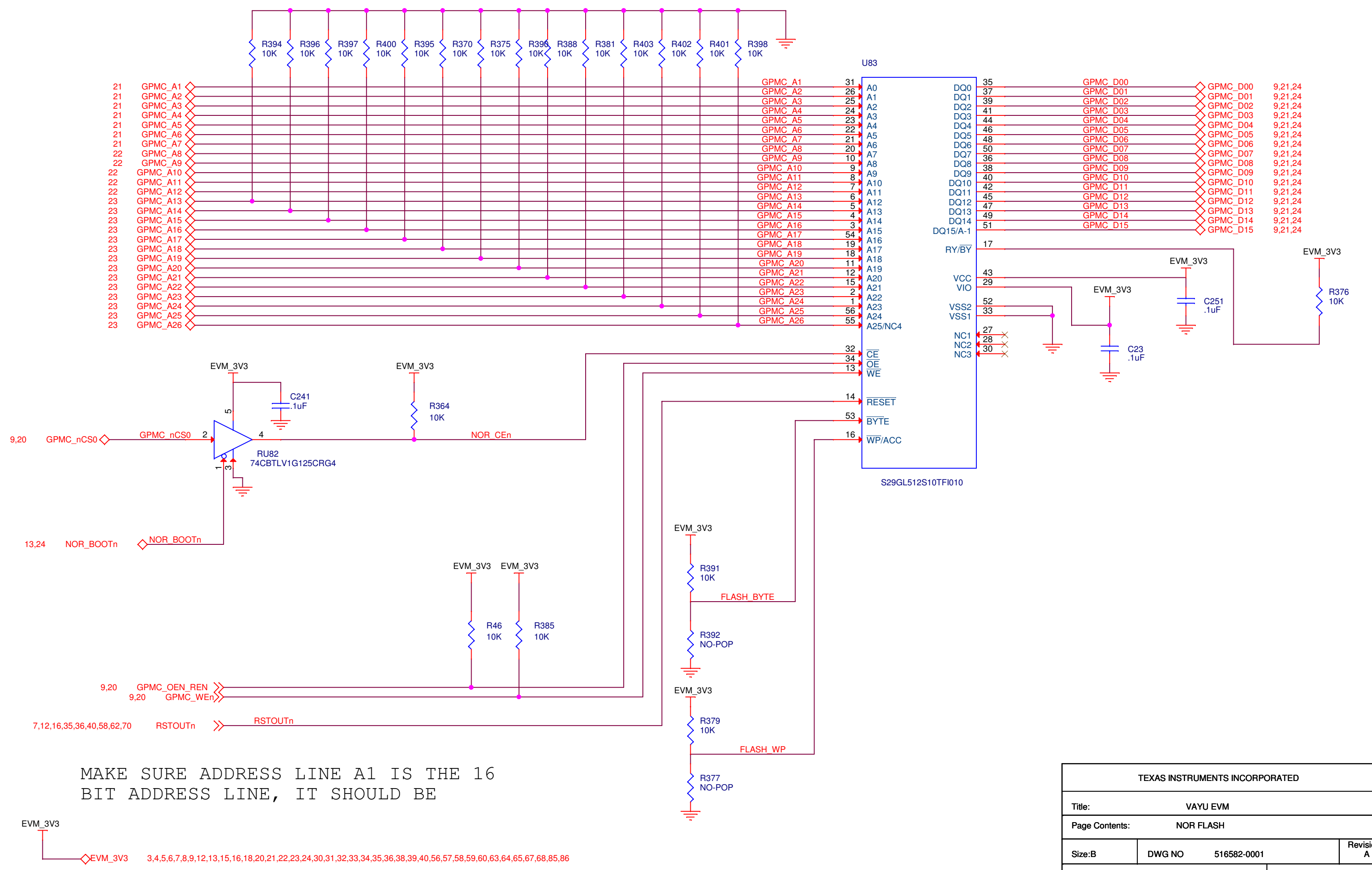
PLACE TEMP SENSOR CLOSE TO PROCESSOR



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EEPROM/TEMP SENSOR			
Size: B	DWG NO	516582-0001	Revision: B
Date: Tuesday, January 12, 2016		Sheet 8 of 89	

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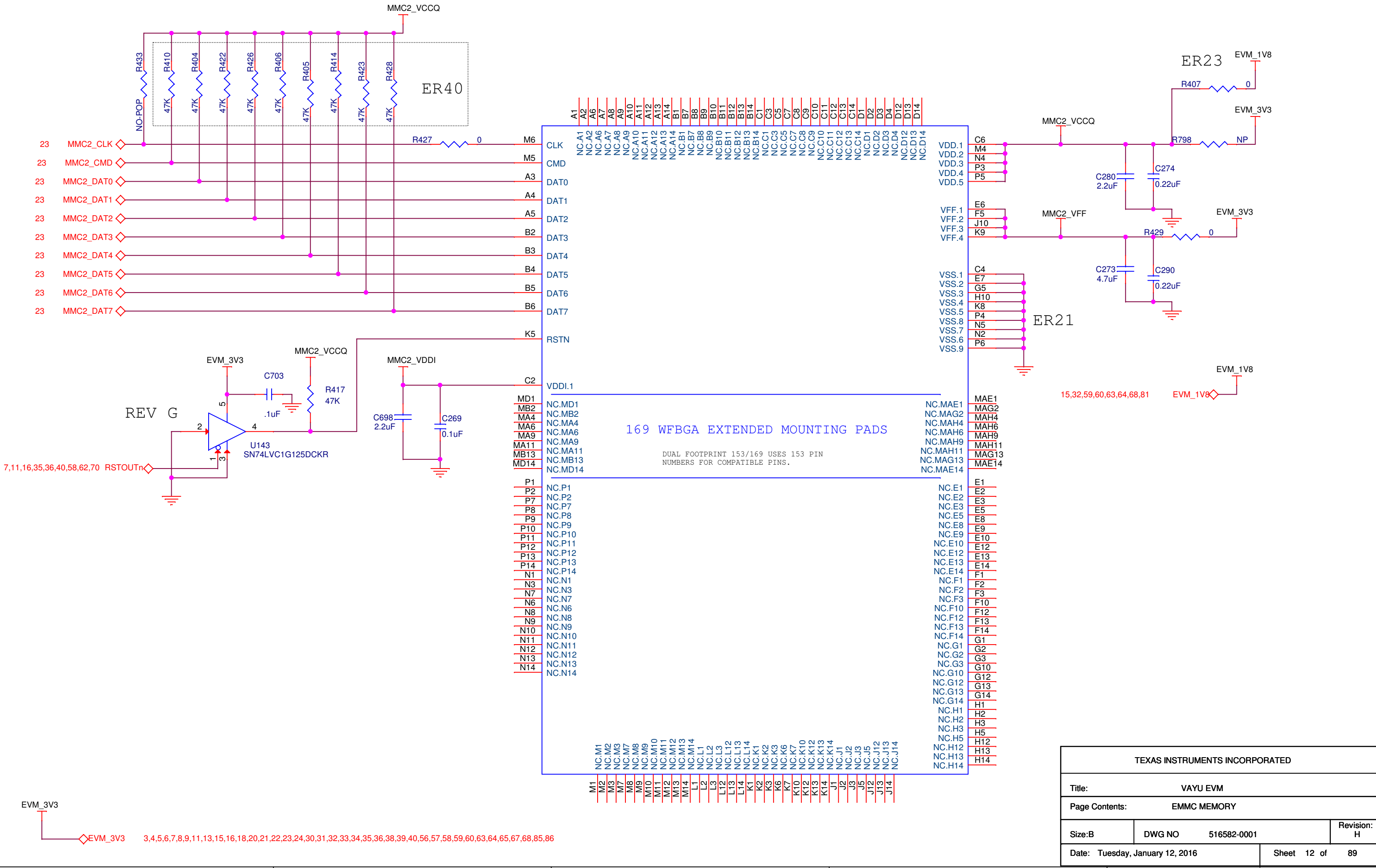
TEXAS INSTRUMENTS INCORPORATED		
Title: VAYU EVM		
Page Contents: HPC TOOL		
Size: B	DWG NO 516582-0001	Revision: A
Date: Thursday, October 01, 2015	Sheet 10 of	89



MAKE SURE ADDRESS LINE A1 IS THE 16 BIT ADDRESS LINE, IT SHOULD BE

EVM_3V3 3,4,5,6,7,8,9,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85,86

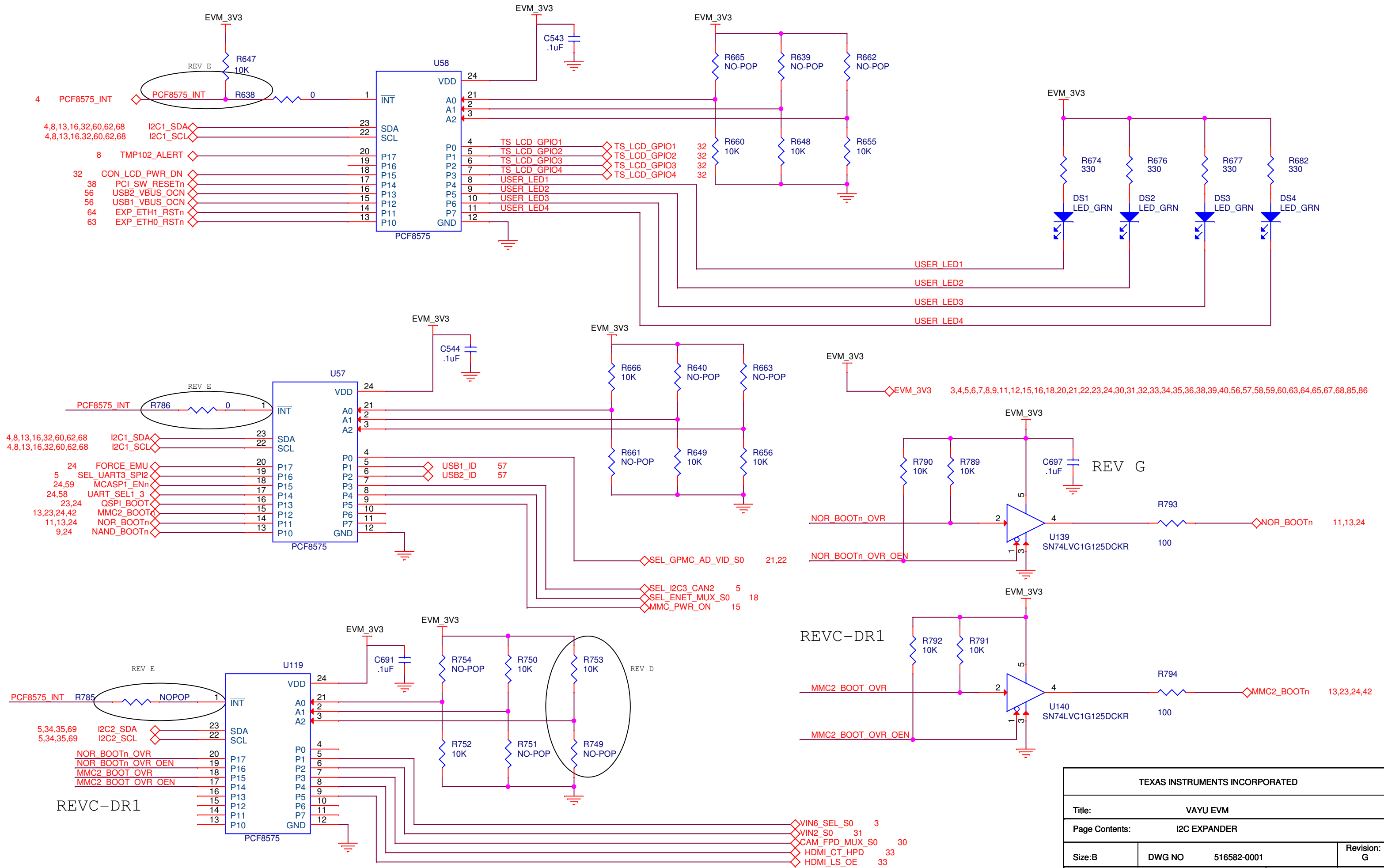
TEXAS INSTRUMENTS INCORPORATED		
Title: VAYU EVM		
Page Contents: NOR FLASH		
Size: B	DWG NO 516582-0001	Revision: A
Date: Tuesday, January 12, 2016	Sheet 11 of	89



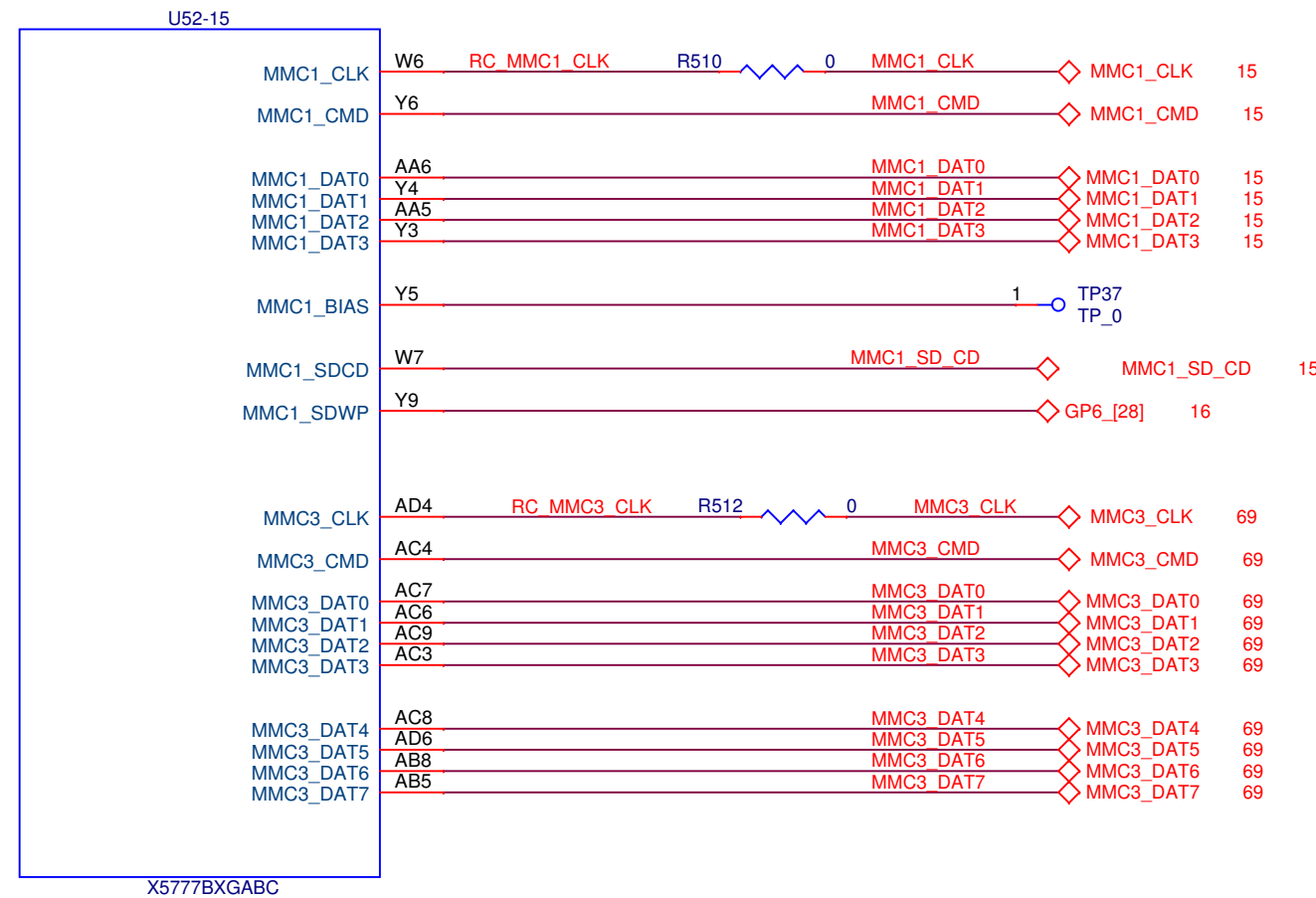
169 WFBGA EXTENDED MOUNTING PADS

DUAL FOOTPRINT 153/169 USES 153 PIN NUMBERS FOR COMPATIBLE PINS.

TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		EMMC MEMORY	
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016	Sheet	12 of	89



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: I2C EXPANDER			
Size: B	DWG NO	516582-0001	Revision: G
Date: Tuesday, January 12, 2016		Sheet 13 of 89	

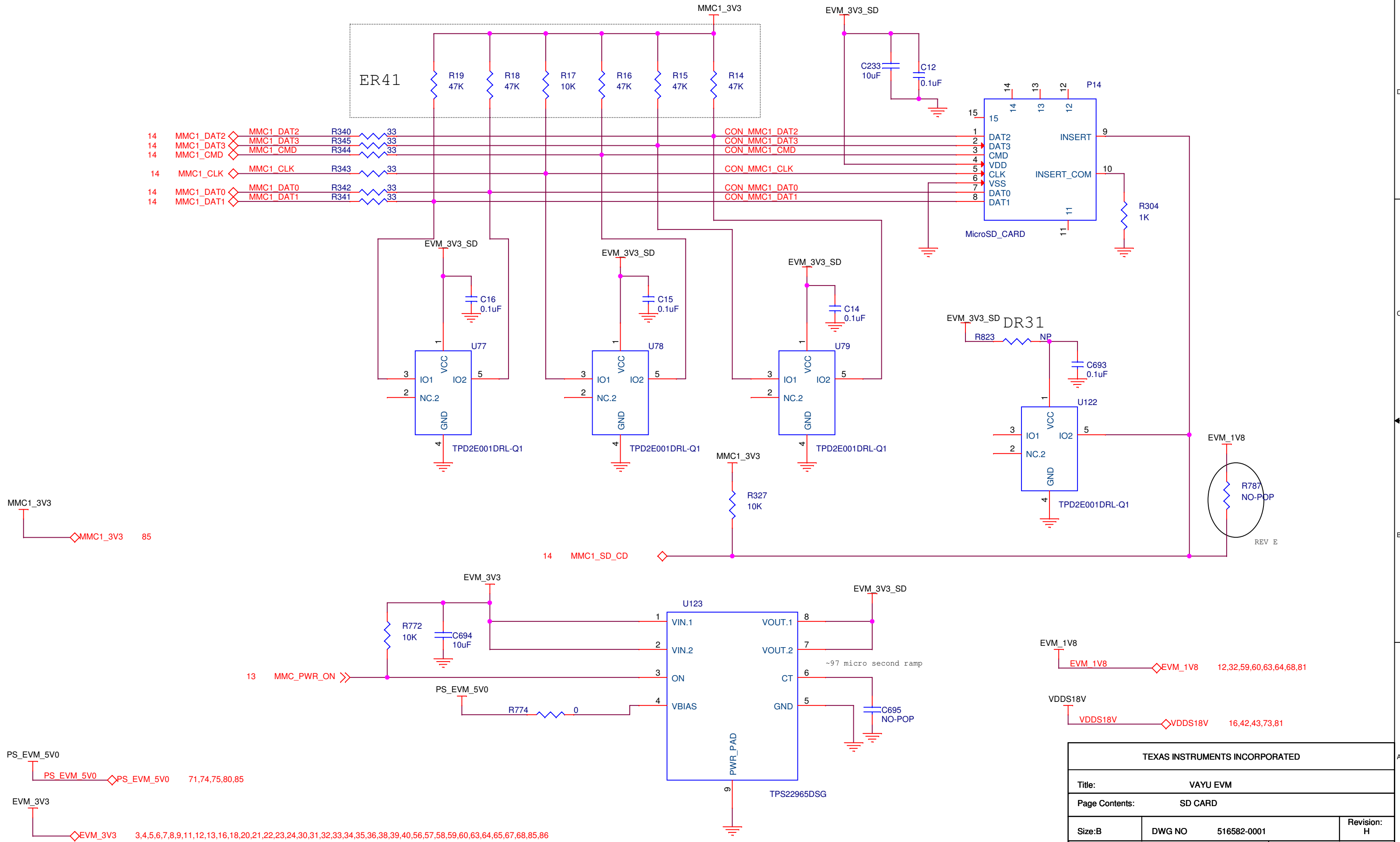


```

mmc3_clk      vin5a_d[7]
mmc3_cmd      vin5a_d[6]
mmc3_dat[0]   vin5a_d[5]
mmc3_dat[1]   vin5a_d[4]
mmc3_dat[2]   vin5a_d[3]
mmc3_dat[3]   vin5a_d[2]
mmc3_dat[4]   vin5a_d[1]
mmc3_dat[5]   vin5a_d[0]
mmc3_dat[6]   vin5a_hsync0
mmc3_dat[7]   vin5a_vsync0

```

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: MMC INTERFACE			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016	Sheet	14 of	89



MMC1_3V3 85

MMC1_SD_CD 14

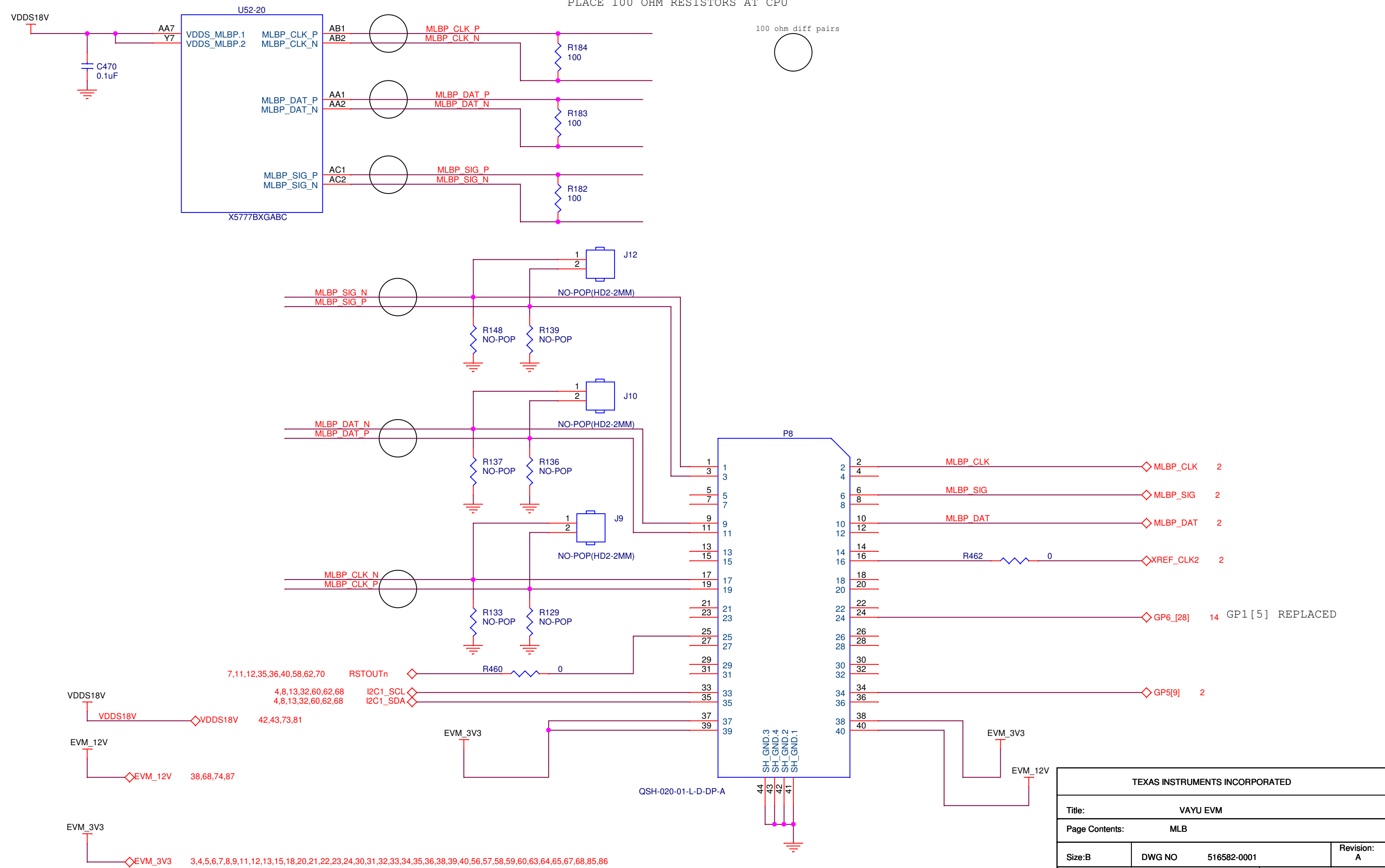
PS_EVM_5V0 71,74,75,80,85

EVM_3V3 3,4,5,6,7,8,9,11,12,13,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85,86

EVM_1V8 12,32,59,60,63,64,68,81

VDDS18V 16,42,43,73,81

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: SD CARD			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 15 of 89	



PLACE 100 OHM RESISTORS AT CPU

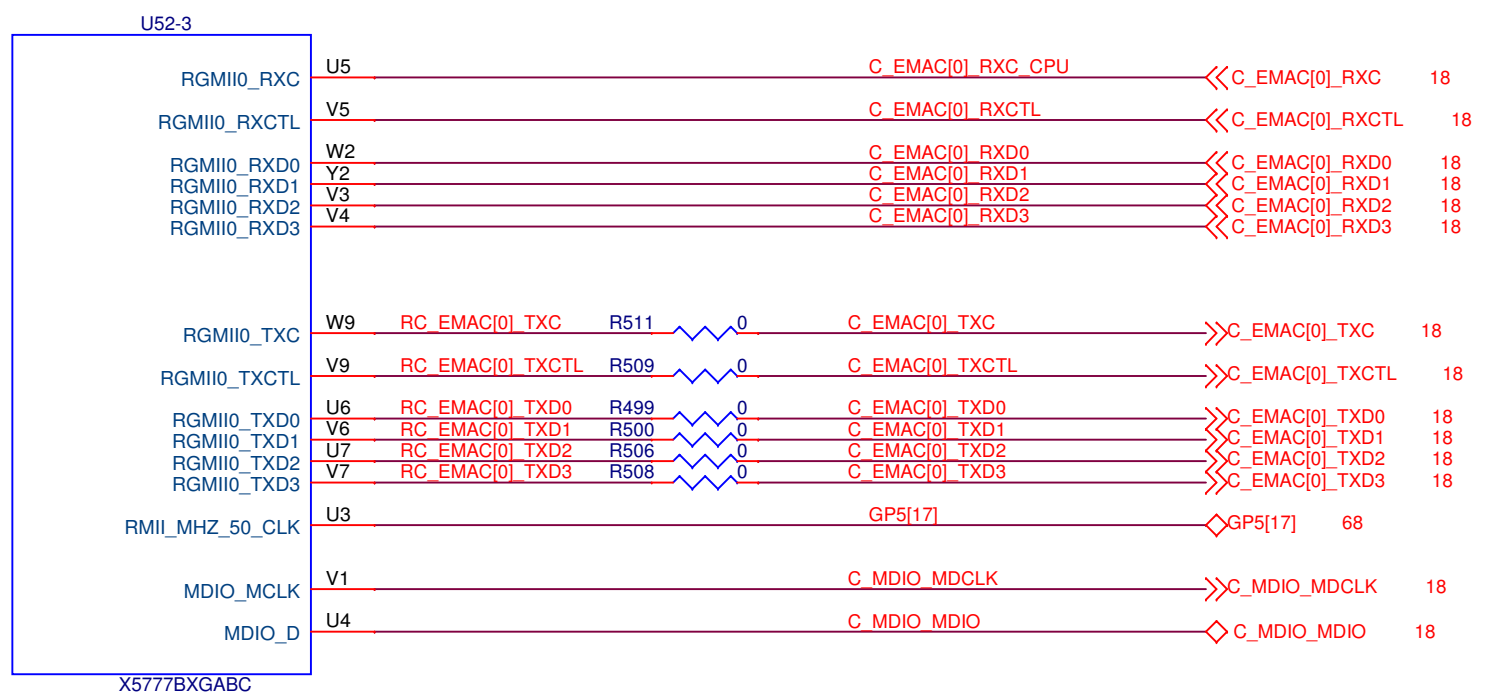
100 ohm diff pairs

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: MLB			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 16 of	89

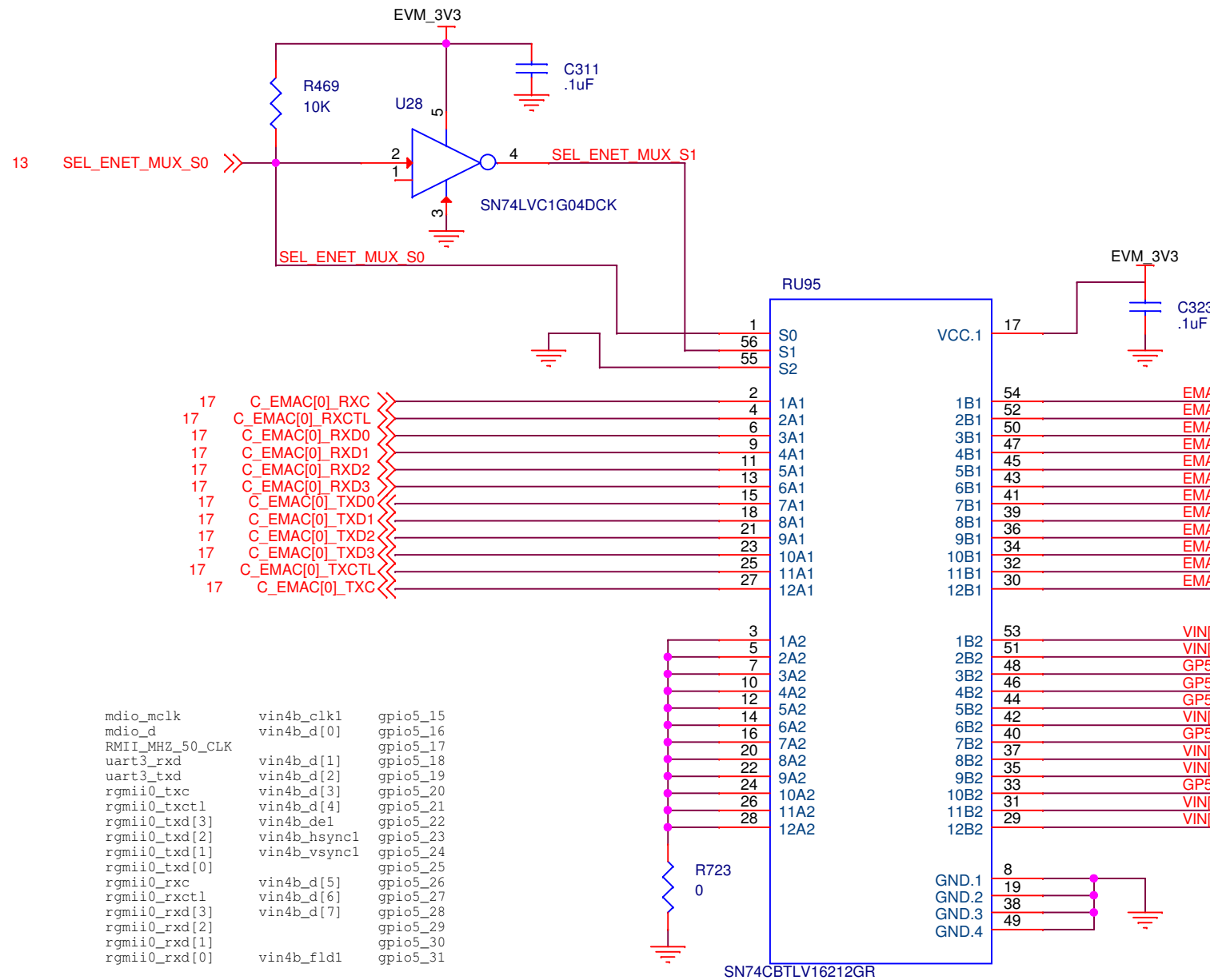

```

mdio_mclk      vin4b_clk1
mdio_d         vin4b_d[0]
RMII_MHZ_50_CLK
uart3_rxd     vin4b_d[1]
uart3_txd     vin4b_d[2]
rgmii0_txc    vin4b_d[3]
rgmii0_txctl  vin4b_d[4]
rgmii0_txd[3] vin4b_de1
rgmii0_txd[2] vin4b_hsync1
rgmii0_txd[1] vin4b_vsync1
rgmii0_txd[0]
rgmii0_rxc    vin4b_d[5]
rgmii0_rxctl  vin4b_d[6]
rgmii0_rxd[3] vin4b_d[7]
rgmii0_rxd[2]
rgmii0_rxd[1]
rgmii0_rxd[0] vin4b_fld1

```



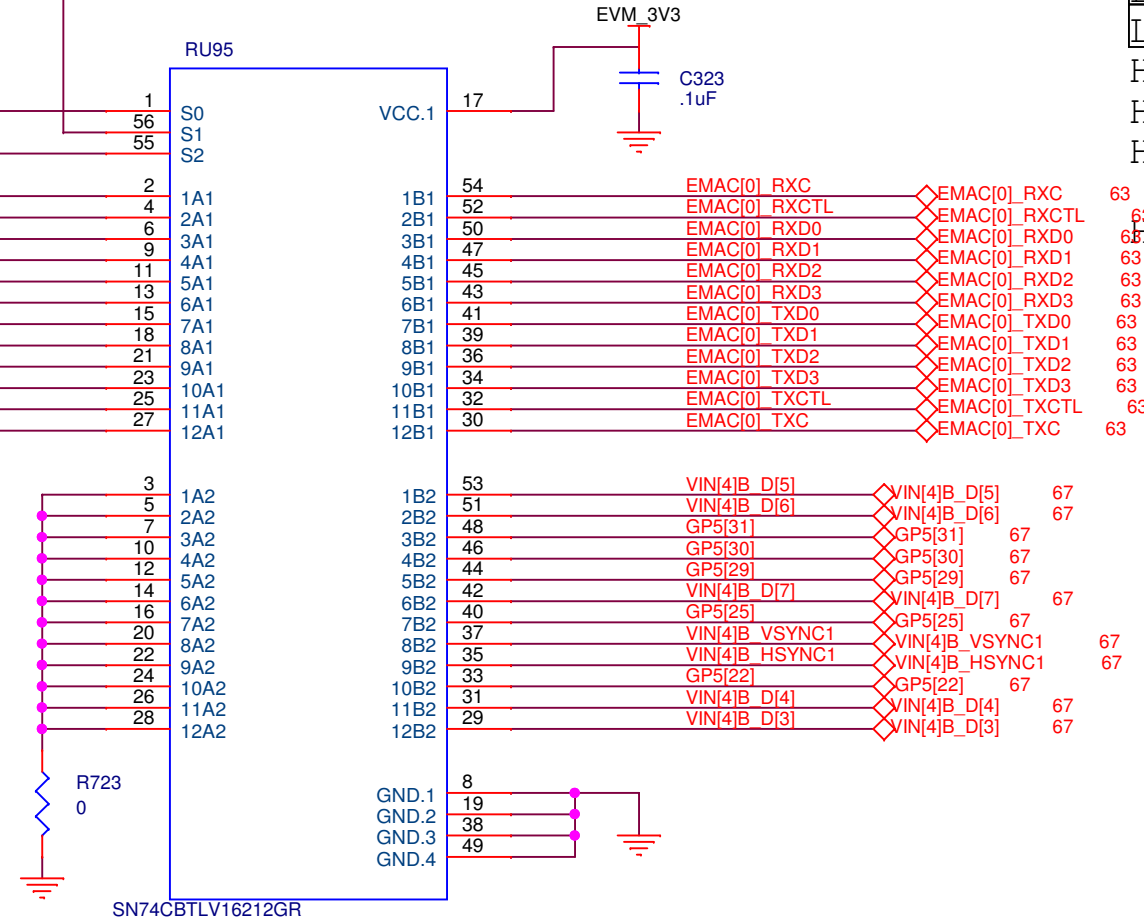
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: ETHERNET 0			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 17 of	89



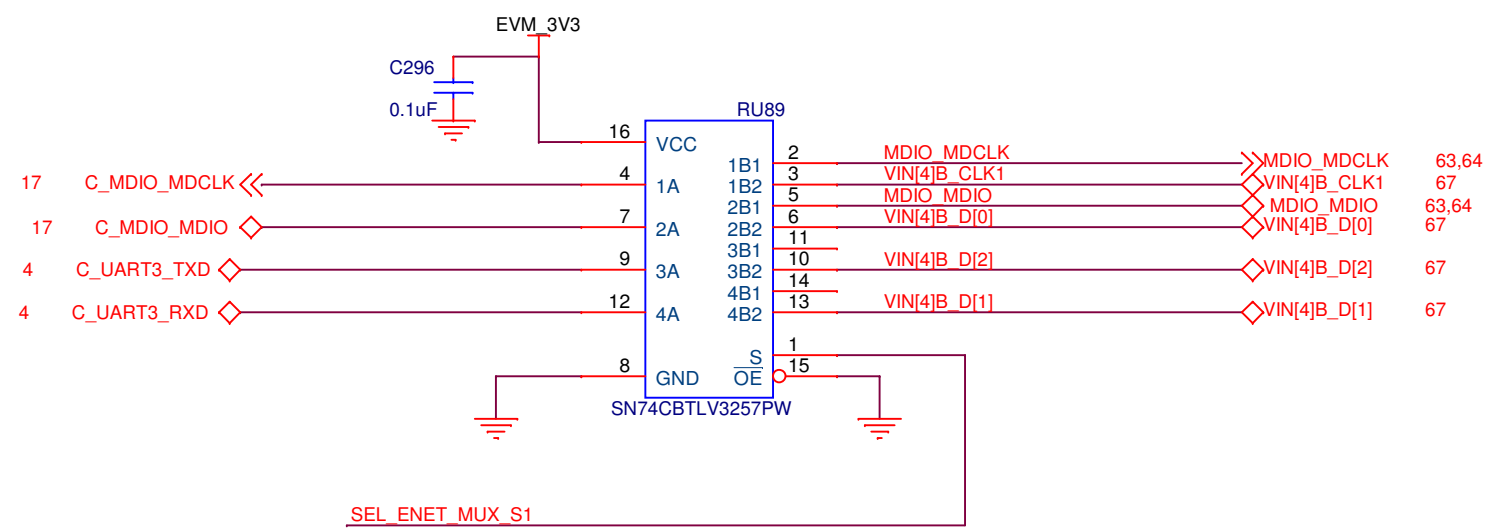
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port
					A2 port = B2 port
	H	H	B2	B1	A1 port = B2 port
					A2 port = B1 port

- 17 C_EMAC[0]_RXC
 - 17 C_EMAC[0]_RXCTL
 - 17 C_EMAC[0]_RXD0
 - 17 C_EMAC[0]_RXD1
 - 17 C_EMAC[0]_RXD2
 - 17 C_EMAC[0]_RXD3
 - 17 C_EMAC[0]_TXD0
 - 17 C_EMAC[0]_TXD1
 - 17 C_EMAC[0]_TXD2
 - 17 C_EMAC[0]_TXD3
 - 17 C_EMAC[0]_TXCTL
 - 17 C_EMAC[0]_TXC
-
- mdio_mclk
 - mdio_d
 - RMTI_MHZ_50_CLK
 - uart3_rxd
 - uart3_txd
 - rgmii0_txc
 - rgmii0_txctl
 - rgmii0_txd[3]
 - rgmii0_txd[2]
 - rgmii0_txd[1]
 - rgmii0_txd[0]
 - rgmii0_rxc
 - rgmii0_rxctl
 - rgmii0_rxd[3]
 - rgmii0_rxd[2]
 - rgmii0_rxd[1]
 - rgmii0_rxd[0]
-
- vin4b_clk1
 - vin4b_d[0]
 - vin4b_d[1]
 - vin4b_d[2]
 - vin4b_d[3]
 - vin4b_d[4]
 - vin4b_del
 - vin4b_hsync1
 - vin4b_vsync1
 - vin4b_d[5]
 - vin4b_d[6]
 - vin4b_d[7]
 - vin4b_fld1
-
- gpio5_15
 - gpio5_16
 - gpio5_17
 - gpio5_18
 - gpio5_19
 - gpio5_20
 - gpio5_21
 - gpio5_22
 - gpio5_23
 - gpio5_24
 - gpio5_25
 - gpio5_26
 - gpio5_27
 - gpio5_28
 - gpio5_29
 - gpio5_30
 - gpio5_31



- EMAC[0]_RXC
- EMAC[0]_RXCTL
- EMAC[0]_RXD0
- EMAC[0]_RXD1
- EMAC[0]_RXD2
- EMAC[0]_RXD3
- EMAC[0]_TXD0
- EMAC[0]_TXD1
- EMAC[0]_TXD2
- EMAC[0]_TXD3
- EMAC[0]_TXCTL
- EMAC[0]_TXC
- VIN[4]B_D[5]
- VIN[4]B_D[6]
- GP5[31]
- GP5[30]
- GP5[29]
- VIN[4]B_D[7]
- GP5[25]
- VIN[4]B_VSYNC1
- VIN[4]B_HSYNC1
- GP5[22]
- VIN[4]B_D[4]
- VIN[4]B_D[3]

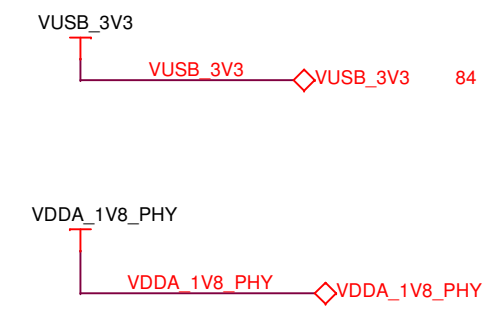
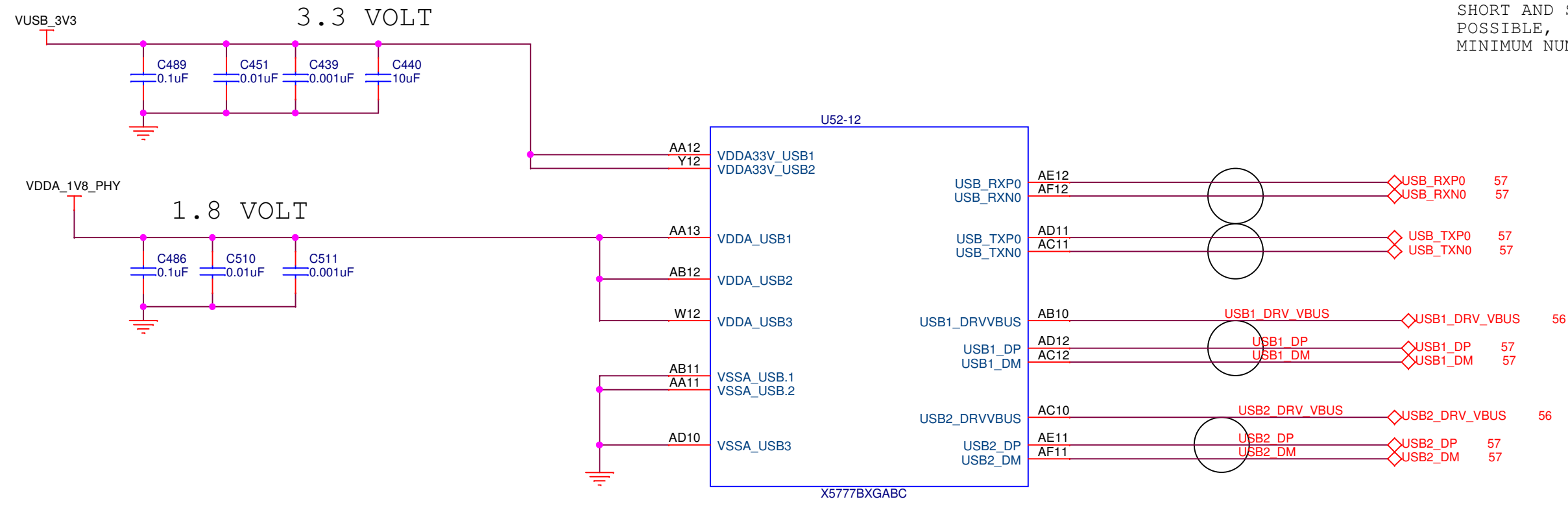


SEL_ENET_MUX_S1

EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85,86

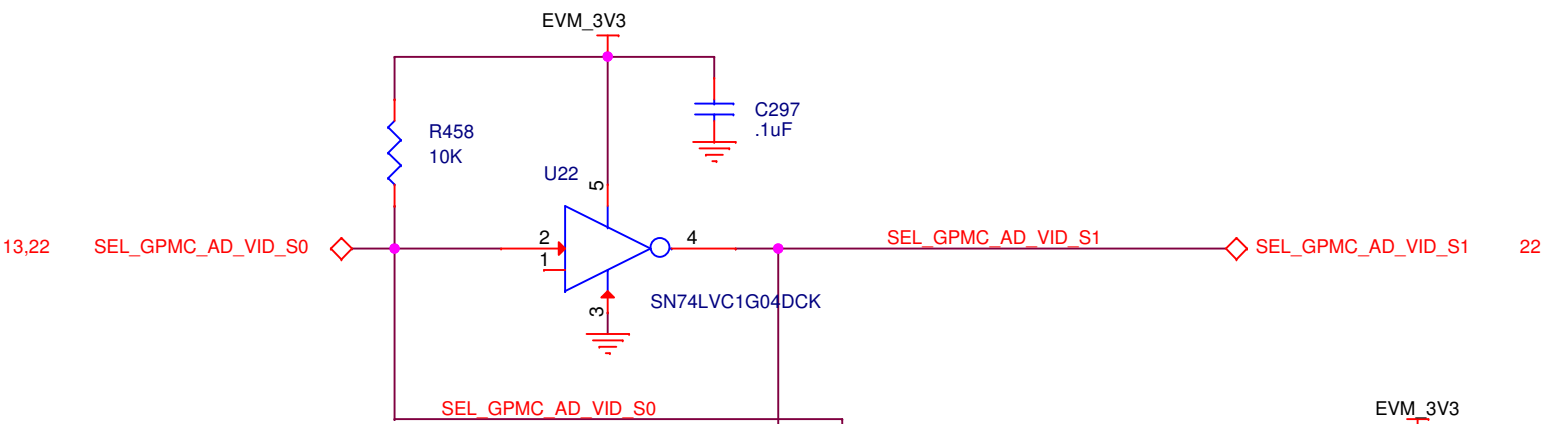
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: ETHERNET 0 / VIN4			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 18 of 89	

DIFFERENTIAL PAIR
 90 OHM DIFFERENTIAL
 IMPEDANCE
 SHORT AND STRAIGHT AS
 POSSIBLE,
 MINIMUM NUMBER OF VIAS



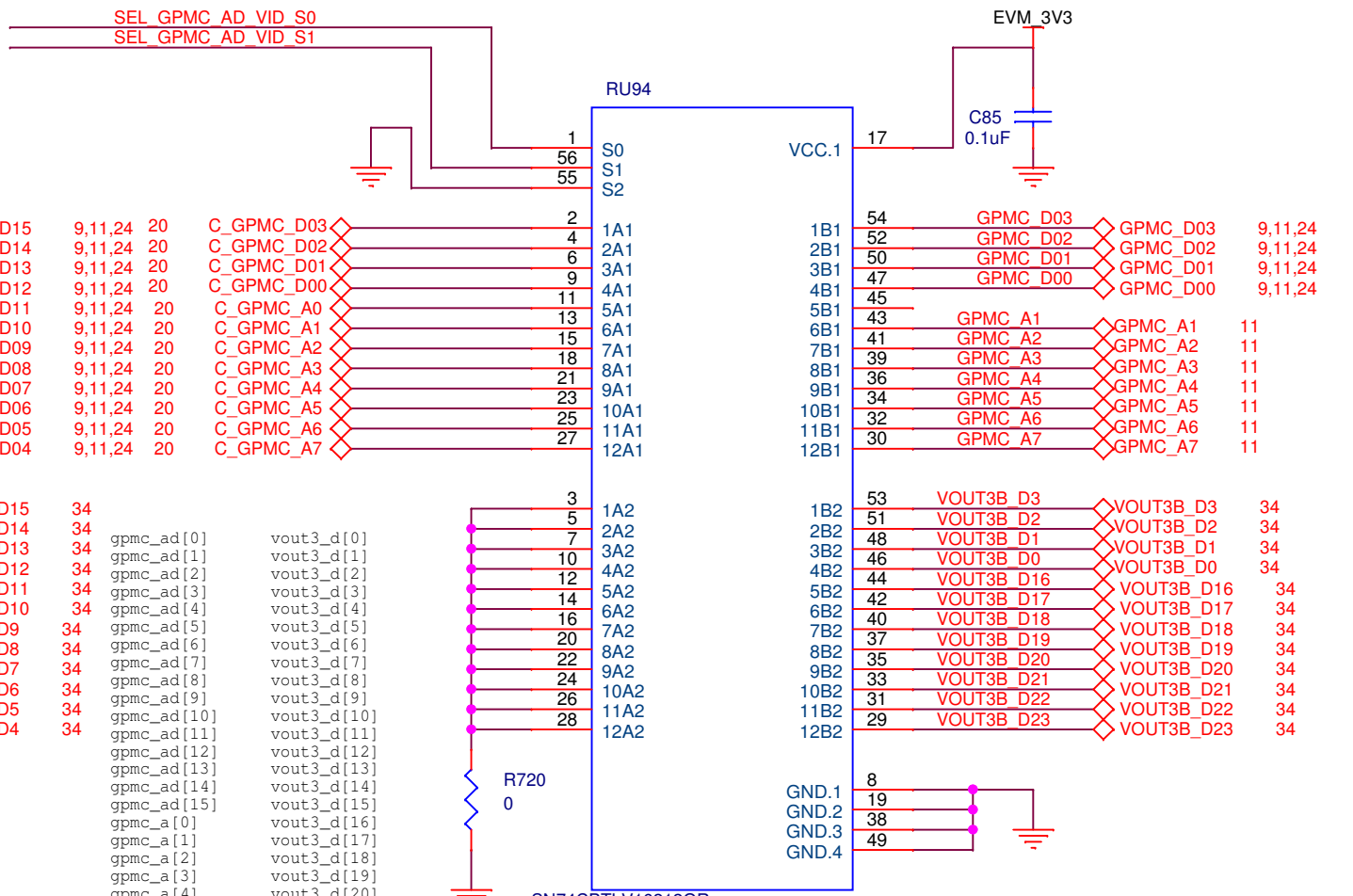
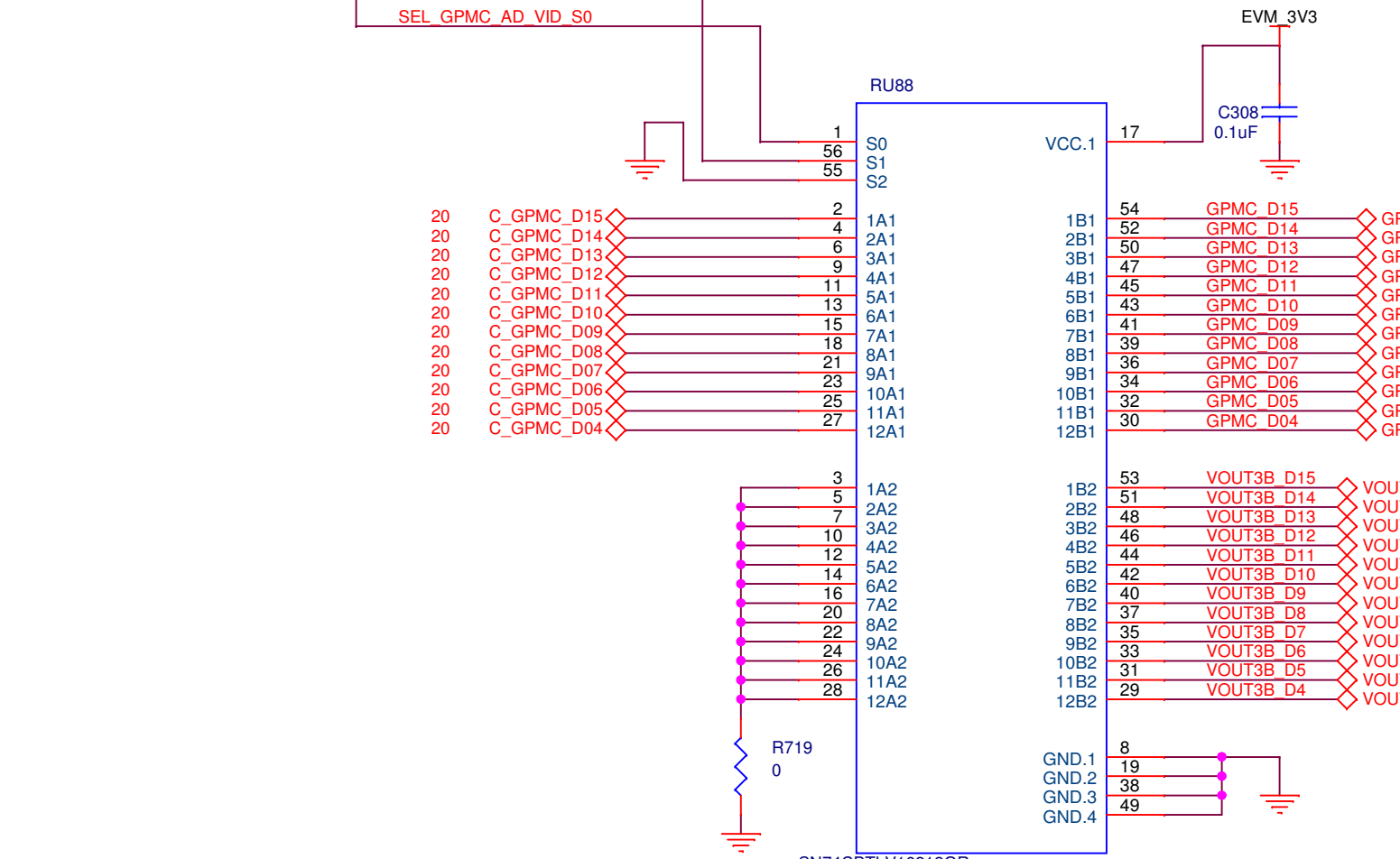
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: USB			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 19 of 89	

DEFAULTS TO GPMC FOR BOOTING



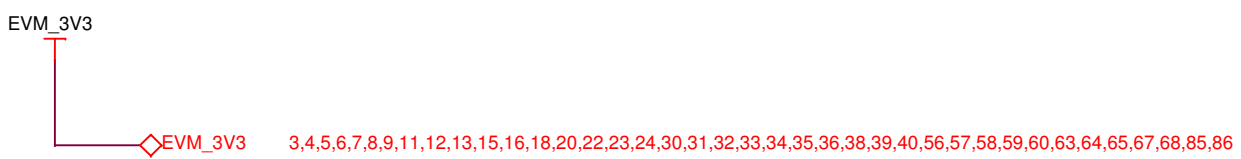
FUNCTION TABLE

INPUTS			INPUTS/OUTPUTS		FUNCTION
S2	S1	S0	A1	A2	
L	L	L	Z	Z	Disconnect
L	L	H	B1	Z	A1 port = B1 port
L	H	L	B2	Z	A1 port = B2 port
L	H	H	Z	B1	A2 port = B1 port
H	L	L	Z	B2	A2 port = B2 port
H	L	H	Z	Z	Disconnect
H	H	L	B1	B2	A1 port = B1 port
					A2 port = B2 port
H	H	H	B2	B1	A1 port = B2 port
					A2 port = B1 port



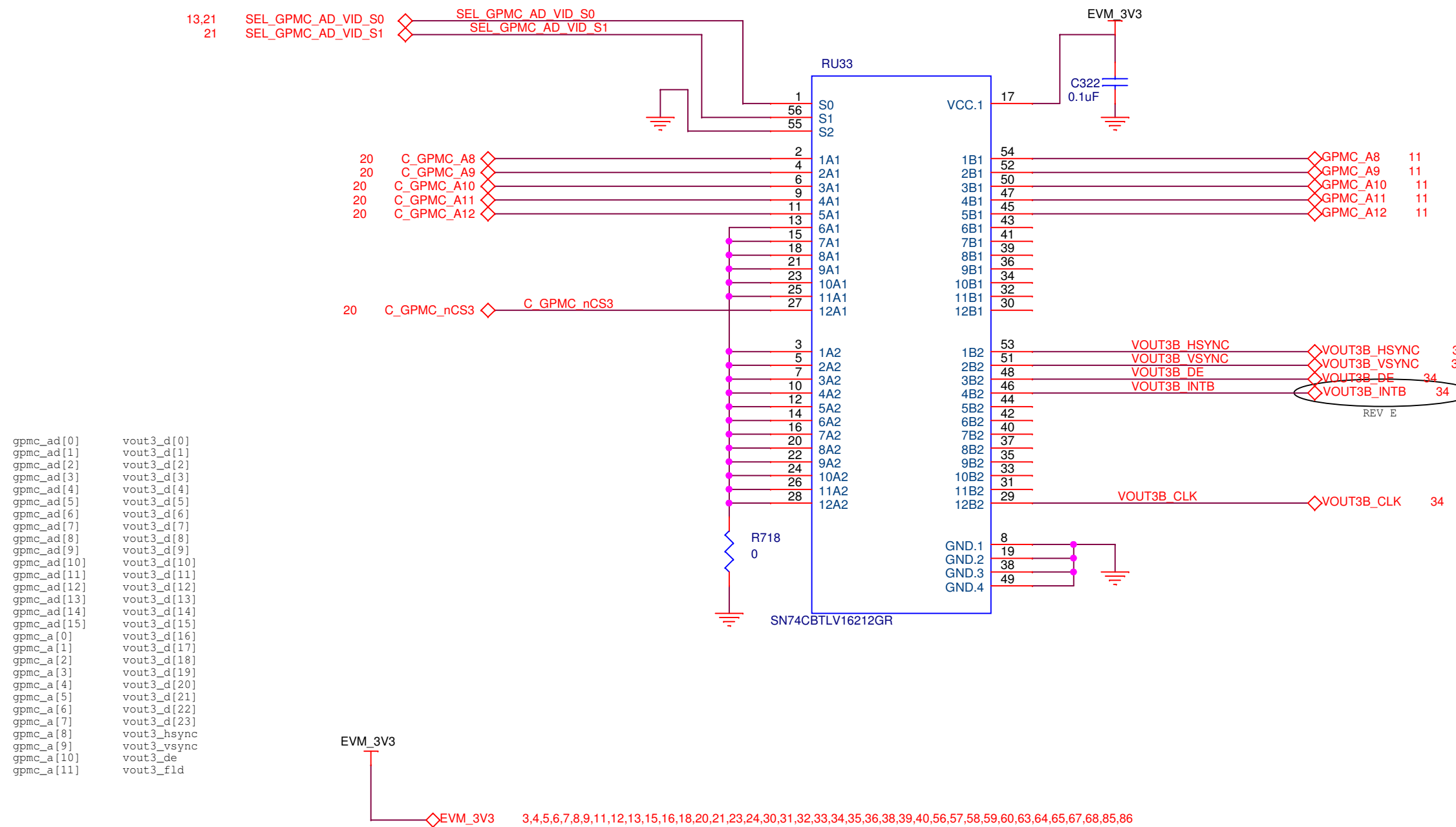
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
20	C_GPMC_D15	2	GPMC D15	54	GPMC D15	9,11,24	20
20	C_GPMC_D14	4	GPMC D14	52	GPMC D14	9,11,24	20
20	C_GPMC_D13	6	GPMC D13	50	GPMC D13	9,11,24	20
20	C_GPMC_D12	9	GPMC D12	47	GPMC D12	9,11,24	20
20	C_GPMC_D11	11	GPMC D11	45	GPMC D11	9,11,24	20
20	C_GPMC_D10	13	GPMC D10	43	GPMC D10	9,11,24	20
20	C_GPMC_D09	15	GPMC D09	41	GPMC D09	9,11,24	20
20	C_GPMC_D08	18	GPMC D08	39	GPMC D08	9,11,24	20
20	C_GPMC_D07	21	GPMC D07	36	GPMC D07	9,11,24	20
20	C_GPMC_D06	23	GPMC D06	34	GPMC D06	9,11,24	20
20	C_GPMC_D05	25	GPMC D05	32	GPMC D05	9,11,24	20
20	C_GPMC_D04	27	GPMC D04	30	GPMC D04	9,11,24	20

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
34	gpmc_ad[0]	3	vout3_d[0]	53	VOUT3B_D3	34	
34	gpmc_ad[1]	5	vout3_d[1]	51	VOUT3B_D2	34	
34	gpmc_ad[2]	7	vout3_d[2]	48	VOUT3B_D1	34	
34	gpmc_ad[3]	10	vout3_d[3]	46	VOUT3B_D0	34	
34	gpmc_ad[4]	12	vout3_d[4]	44	VOUT3B_D16	34	
34	gpmc_ad[5]	14	vout3_d[5]	42	VOUT3B_D17	34	
34	gpmc_ad[6]	16	vout3_d[6]	40	VOUT3B_D18	34	
34	gpmc_ad[7]	20	vout3_d[7]	37	VOUT3B_D19	34	
34	gpmc_ad[8]	22	vout3_d[8]	35	VOUT3B_D20	34	
34	gpmc_ad[9]	24	vout3_d[9]	33	VOUT3B_D21	34	
34	gpmc_ad[10]	26	vout3_d[10]	31	VOUT3B_D22	34	
34	gpmc_ad[11]	28	vout3_d[11]	29	VOUT3B_D23	34	

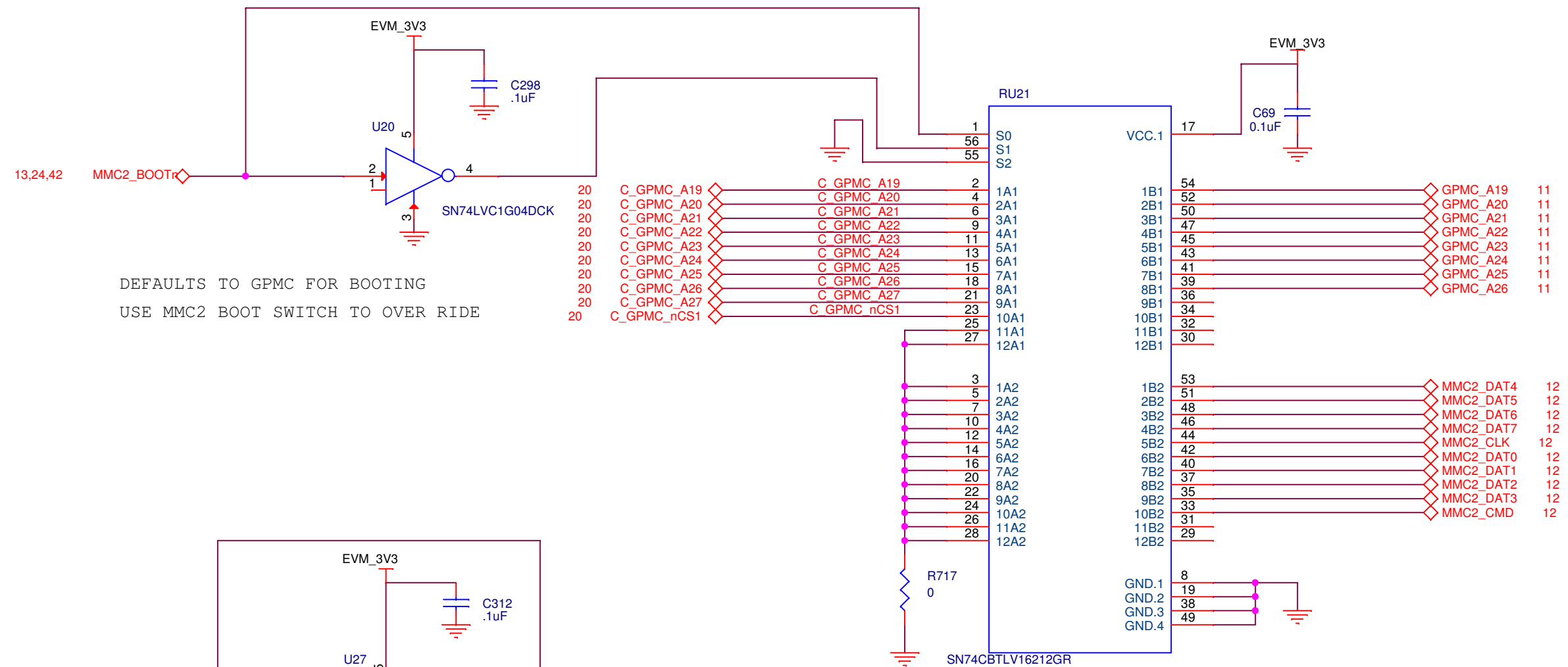


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: GPMC MUXES			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016	Sheet 21 of 89		

DEFAULTS TO GPMC FOR BOOTING



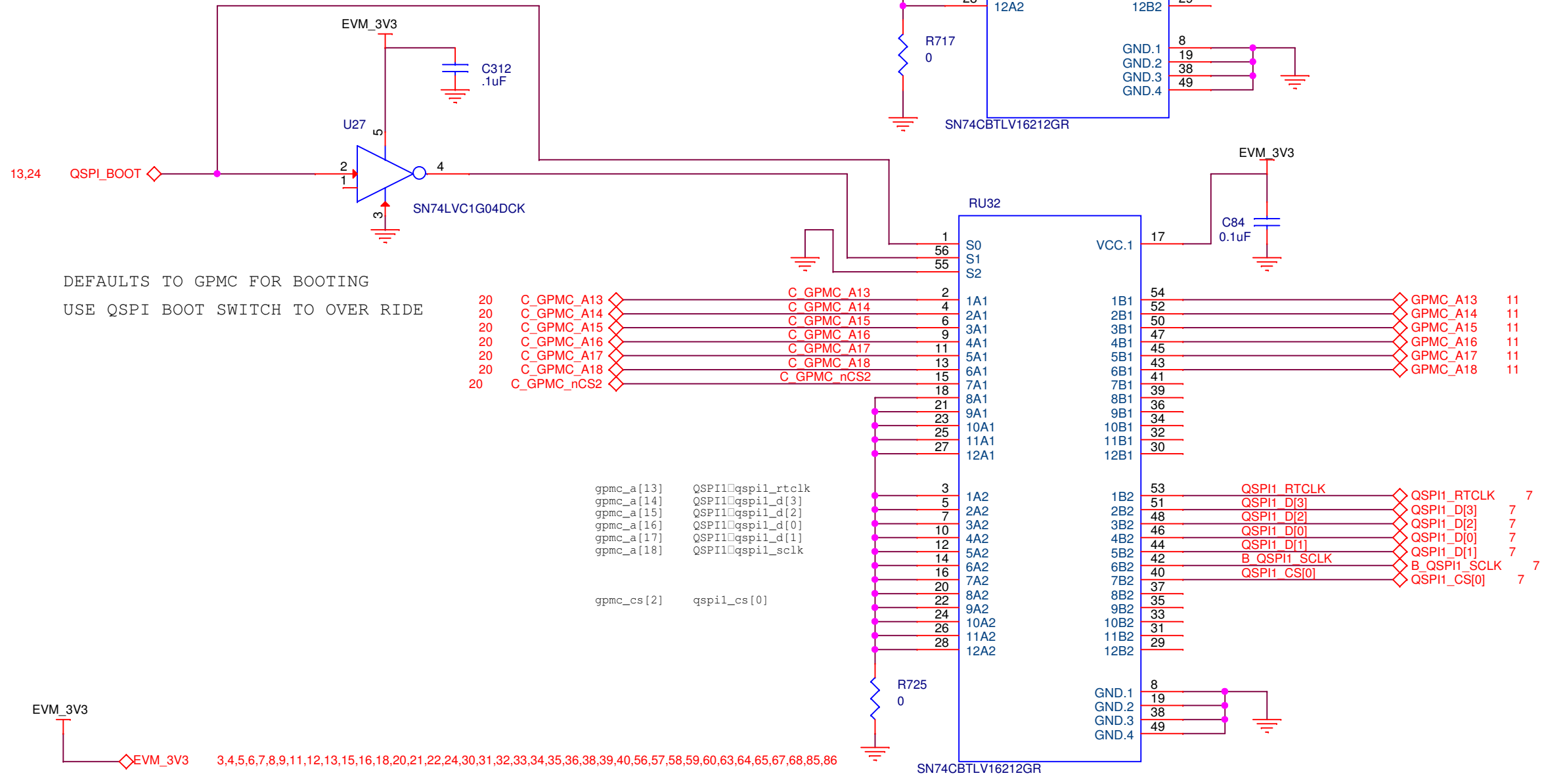
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: GPMC MUXES			
Size: B	DWG NO	516582-0001	Revision: E
Date: Tuesday, January 12, 2016	Sheet	22 of	89



```

gpmc_a[19] mmc2_dat[4]
gpmc_a[20] mmc2_dat[5]
gpmc_a[21] mmc2_dat[6]
gpmc_a[22] mmc2_dat[7]
gpmc_a[23] mmc2_clk
gpmc_a[24] mmc2_dat[0]
gpmc_a[25] mmc2_dat[1]
gpmc_a[26] mmc2_dat[2]
gpmc_a[27] mmc2_dat[3]
gpmc_cs[1] mmc2_cmd

```



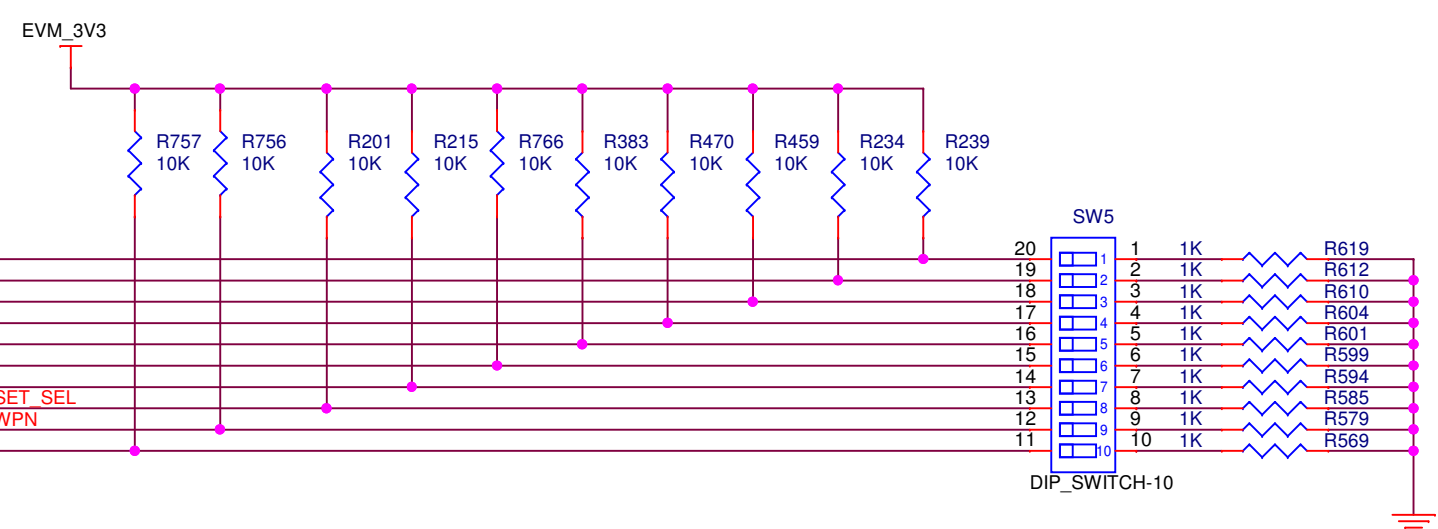
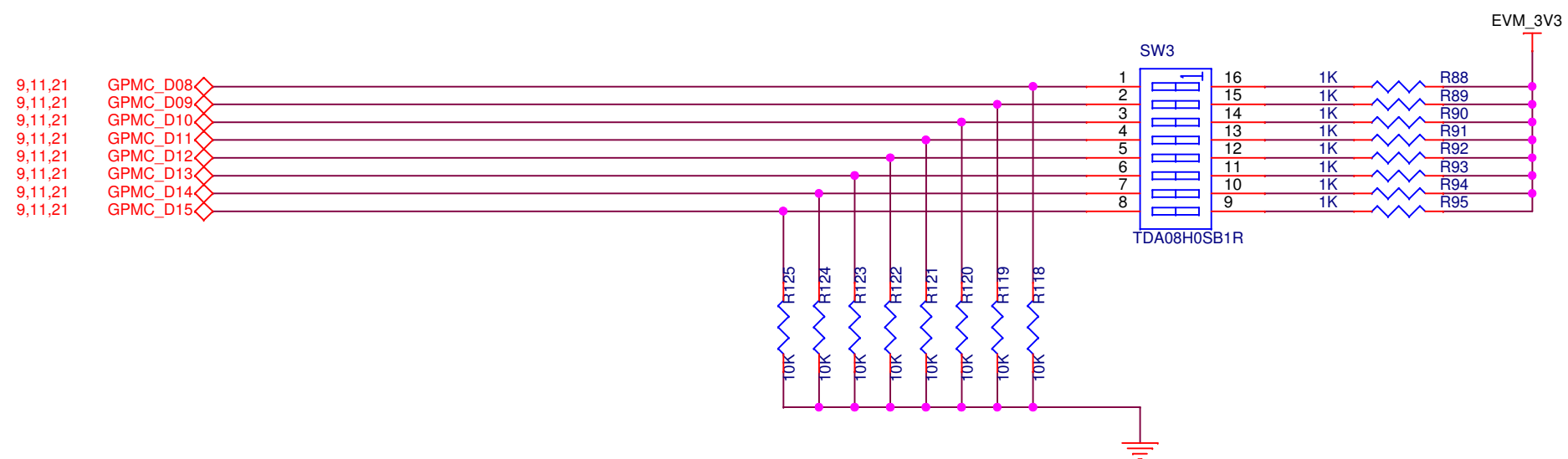
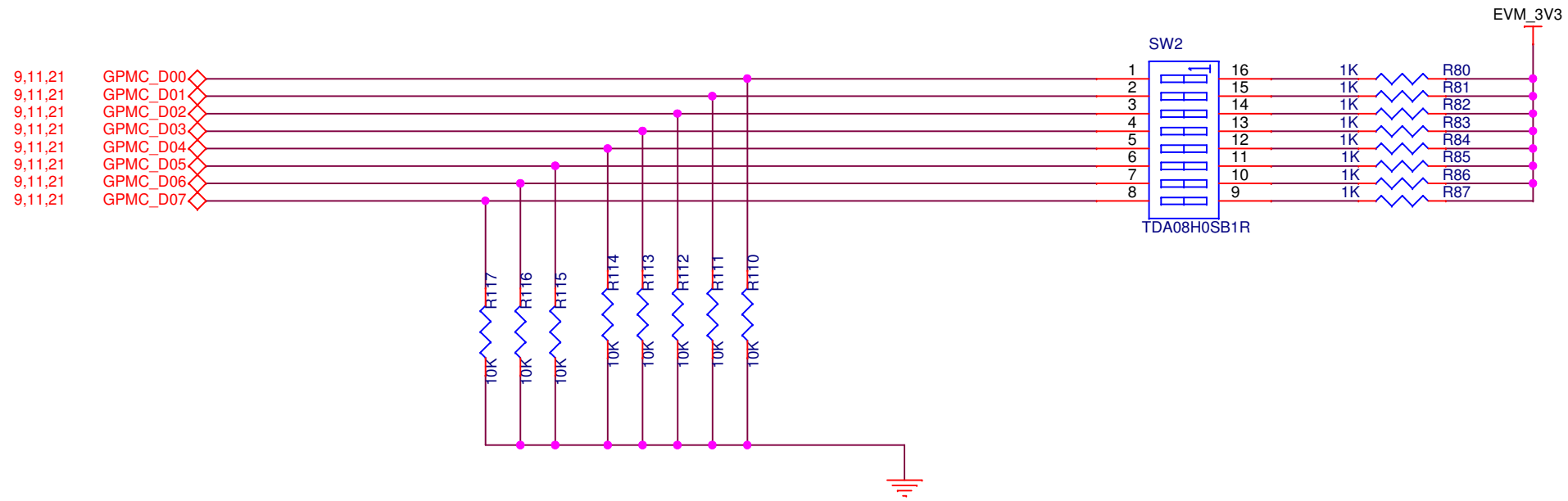
```

gpmc_a[13] QSPI1_qspi1_rtclk
gpmc_a[14] QSPI1_qspi1_d[3]
gpmc_a[15] QSPI1_qspi1_d[2]
gpmc_a[16] QSPI1_qspi1_d[0]
gpmc_a[17] QSPI1_qspi1_d[1]
gpmc_a[18] QSPI1_qspi1_sclk

gpmc_cs[2] qspi1_cs[0]

```

TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		GPMC MUXES	
Size: B	DWG NO	516582-0001	Revision: D2
Date: Tuesday, January 12, 2016	Sheet	23 of	89



MMC2 BOOT PULL UP ON PAGE 23 SET TO LOGIC 0 TO ENABLE MMC2 MUX FOR BOOTING SET TO 1 FOR GPMC BOOTING

QSPI BOOT PULL UP ON PAGE 23 SET TO LOGIC 0 TO ENABLE QSPI MUX FOR BOOTING SET TO 1 FOR GPMC BOOTING

UART SEL1_3 PULL UP ON PAGE 58 SELECTS UART3 MUX INPUT TO BE USART PORT AT MINI_USB A(J1) DURING BOOTING. MCASP1_ENn MUST BE SET TO LOGIC 1 TO DISABLE COM8. ALSO OTHER MUX NEEDS TO BE IN DEFAULT CONFIGURATION

EVM_3V3

3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85,86

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: BOOT SWITCHES			
Size: B	DWG NO	516582-0001	Revision: B
Date: Tuesday, January 12, 2016	Sheet 24 of		89

EACH DATA GROUP IS MATCHED WITHIN THE GROUP

○ differential pairs 100 ohm
6 places

U52-5

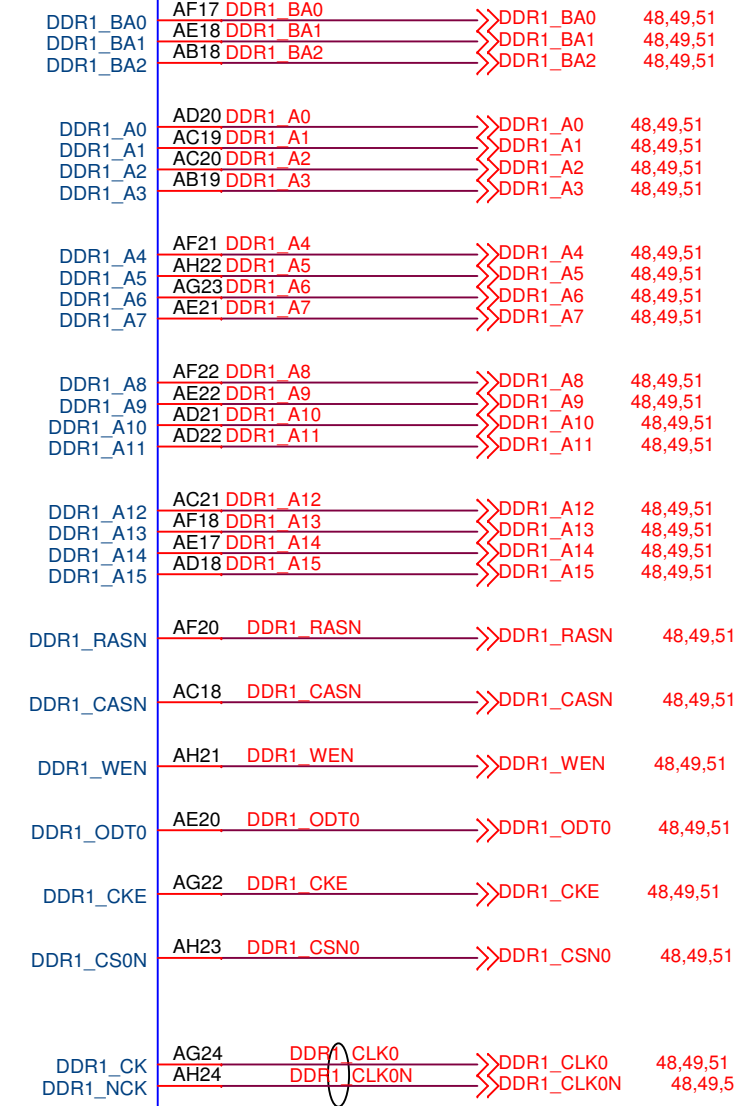
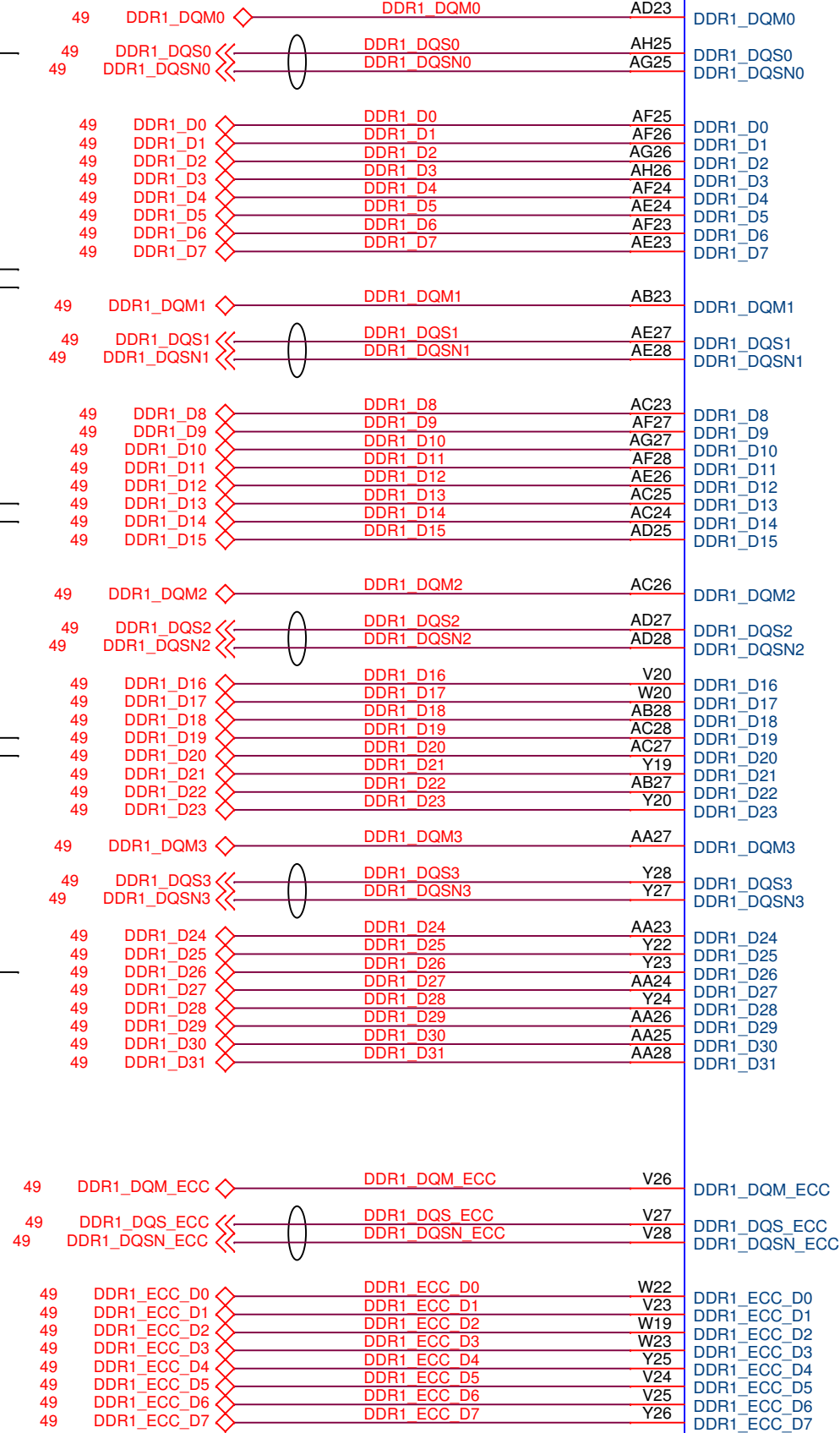
X5777BXXGABC

USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: DDR EMIF1			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet	25 of 89

EACH DATA GROUP IS MATCHED WITHIN THE GROUP

○ differential pairs 100 ohm
5 places

Data Group 2-0
USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

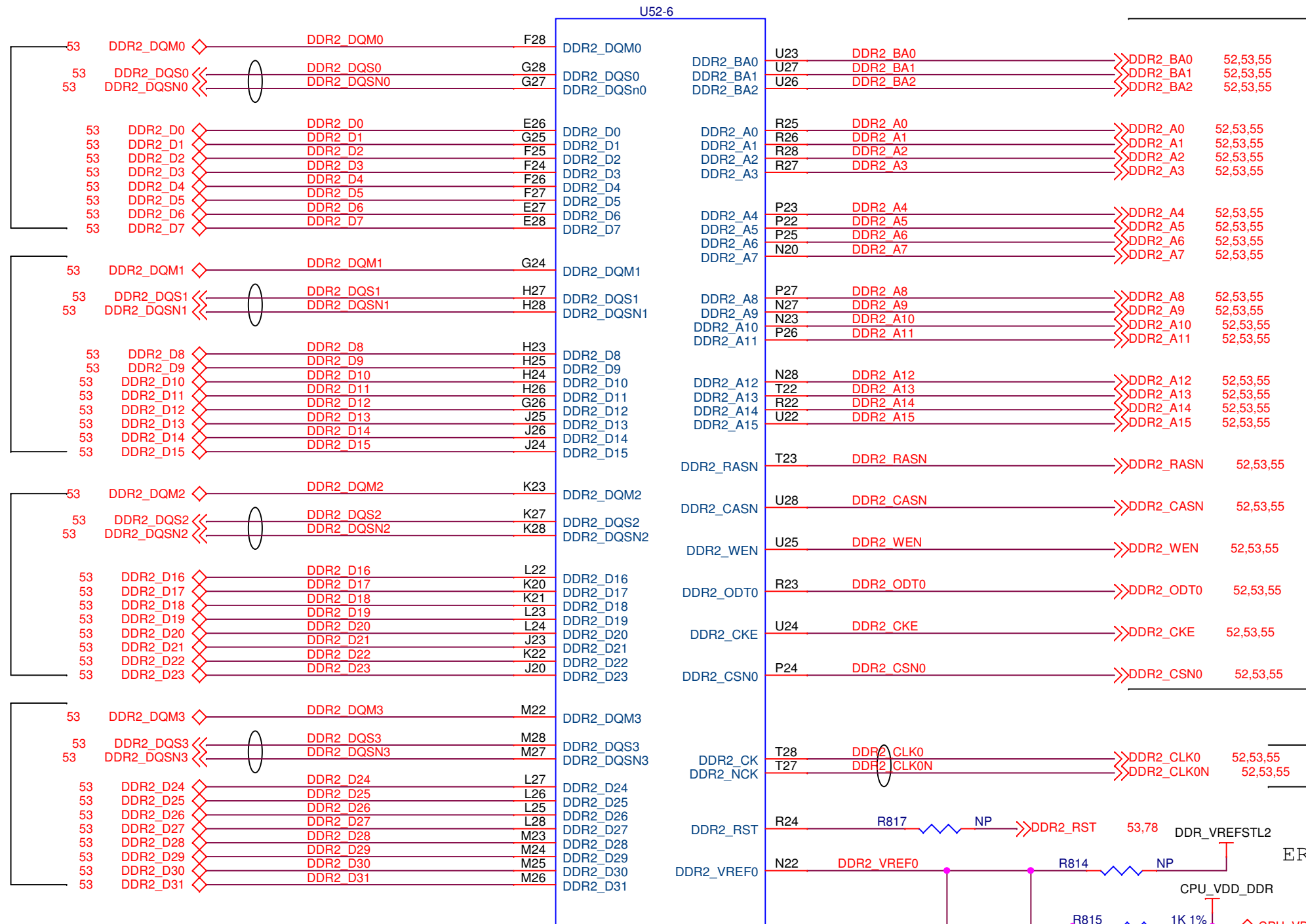
Data Group 2-1
USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

Data Group 2-2
USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

Data Group 2-3
USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

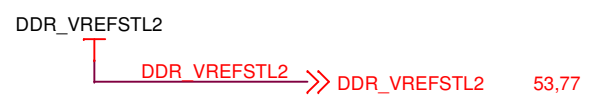
CONTROL GROUP 2
USE 4X SPACING TRACE
TO TRACE EQUAL LENGTH
+/-5 MIL

CLOCK GROUP 2

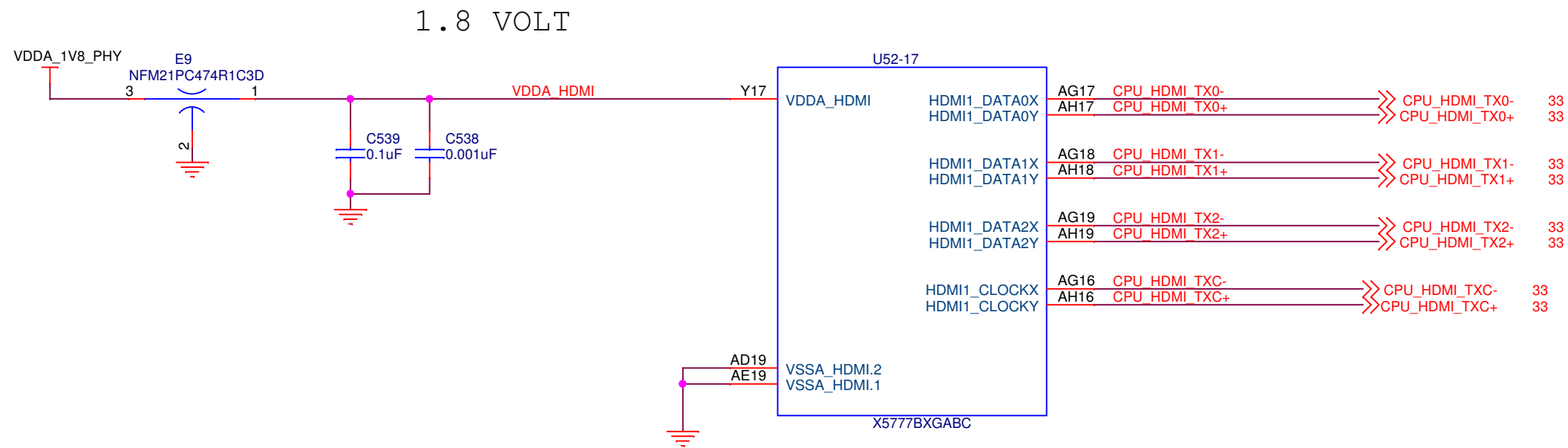


WARNING [DRC0006] Net has fewer than two connections N23667068: VAYU_EVM, SH26 - VAYU DDR EMIF2 INTERFACE (3.20, 4.00)
 WARNING [DRC0006] Net has fewer than two connections N23667055: VAYU_EVM, SH26 - VAYU DDR EMIF2 INTERFACE (3.20, 2.40)
 WARNING [DRC0006] Net has fewer than two connections N25725225: VAYU_EVM, SH25 - VAYU DDR EMIF1 INTERFACE (3.10, 3.50)
 WARNING [DRC0006] Net has fewer than two connections N25725223: VAYU_EVM, SH25 - VAYU DDR EMIF1 INTERFACE (3.10, 2.20)

DDR2_RST is not part of group
DDR2_VREFSSTL is not part of group

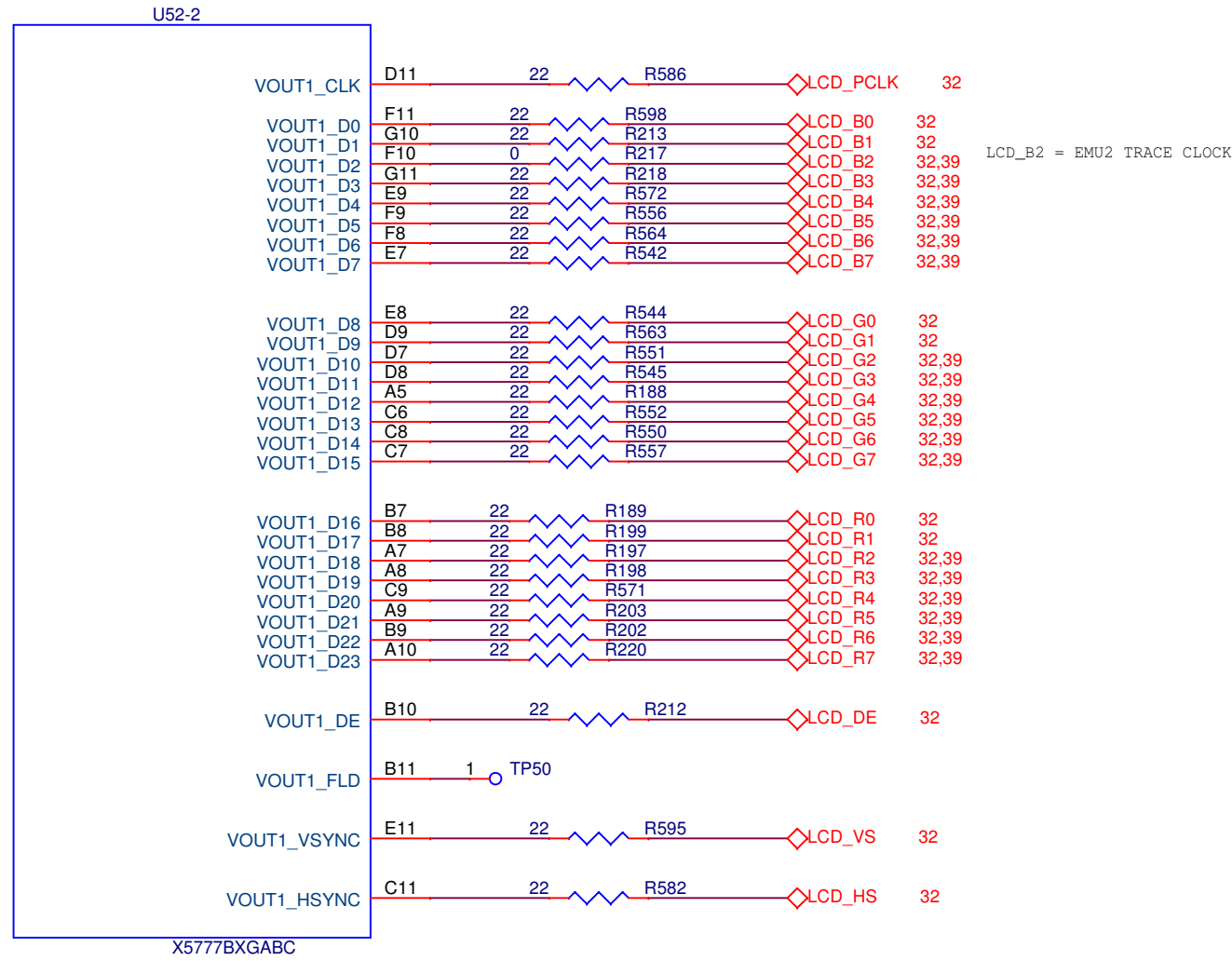


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: DDR EMIF2			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016	Sheet	26 of	89

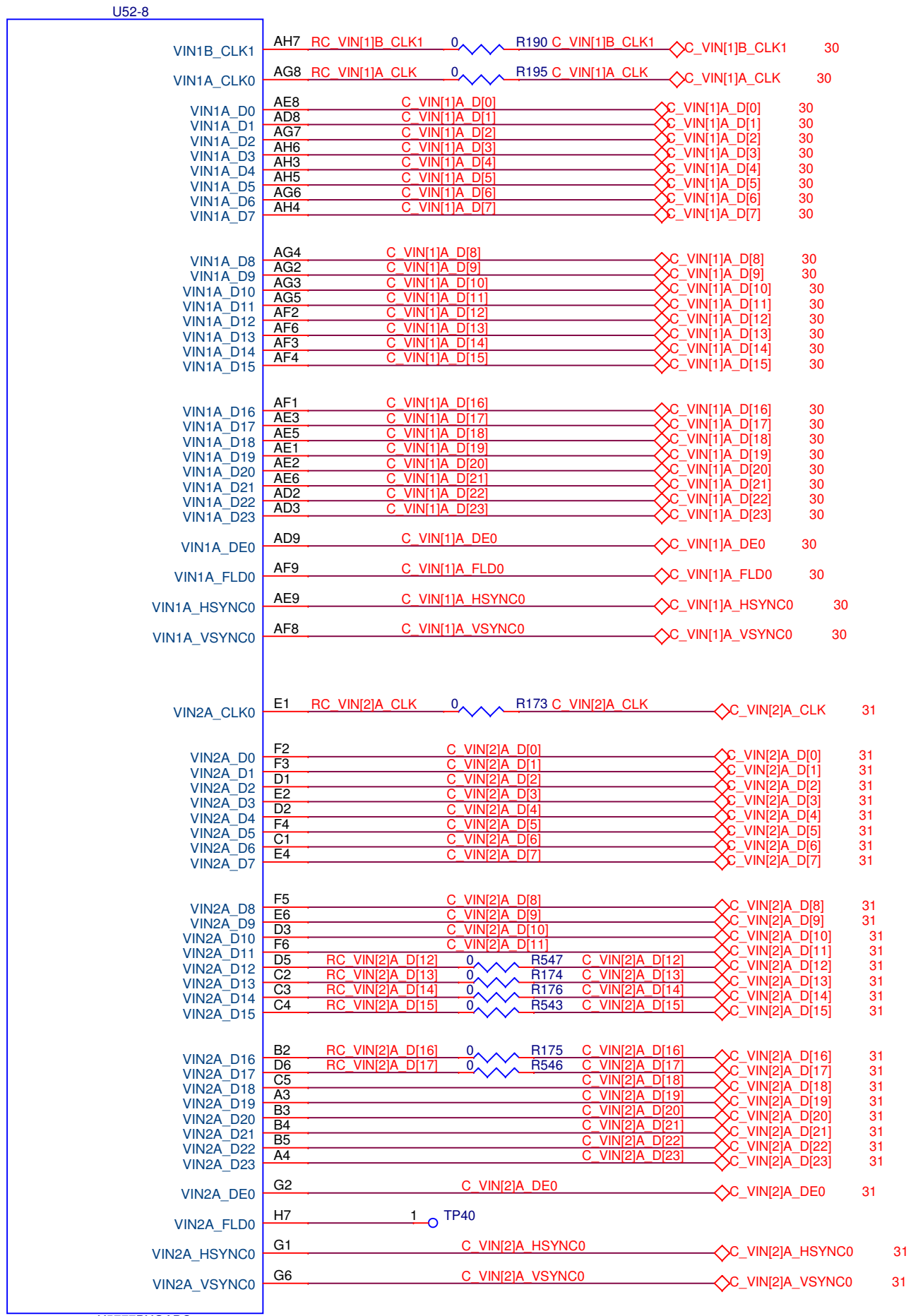


TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		HDMI INTERFACE	
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 27 of	89

22 OHM OK FOR LCD AS IT IS NOT GOING THROUGH MUXES.



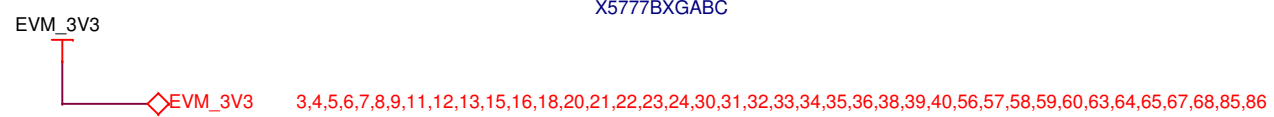
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: VIDEO OUT PORTS			
Size: B	DWG NO	516582-0001	Revision: C
Date: Tuesday, January 12, 2016		Sheet 28 of	89



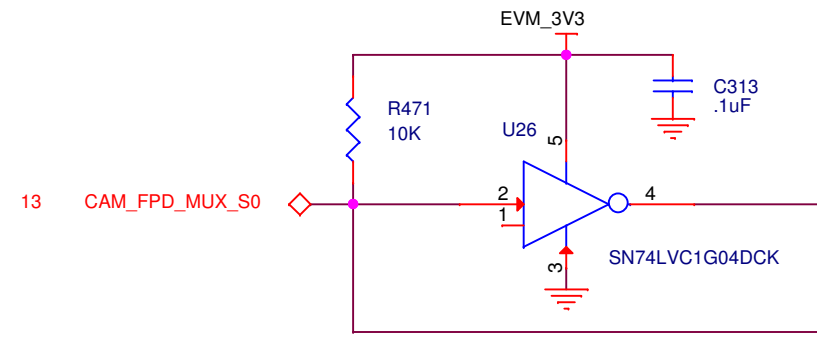
```

vin2a_d[12] rgmii_txc
vin2a_d[13] rgmii_txctl
vin2a_d[14] rgmii_txd[3]
vin2a_d[15] rgmii_txd[2]
vin2a_d[16] rgmii_txd[1]
vin2a_d[17] rgmii_txd[0]
vin2a_d[18] rgmii_rxc
vin2a_d[19] rgmii_rxctl
vin2a_d[20] rgmii_rxd[3]
vin2a_d[21] rgmii_rxd[2]
vin2a_d[22] rgmii_rxd[1]
vin2a_d[23] rgmii_rxd[0]

```

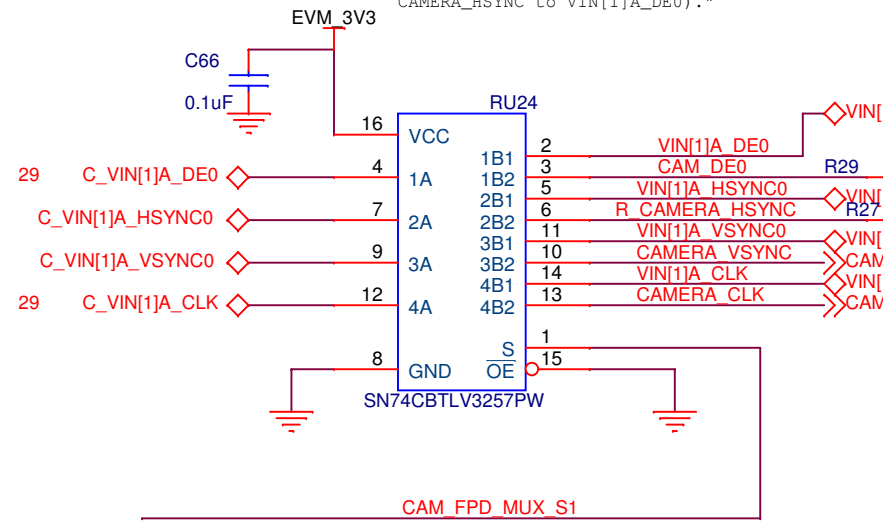


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: VIDEO IN PORTS			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 29 of	89

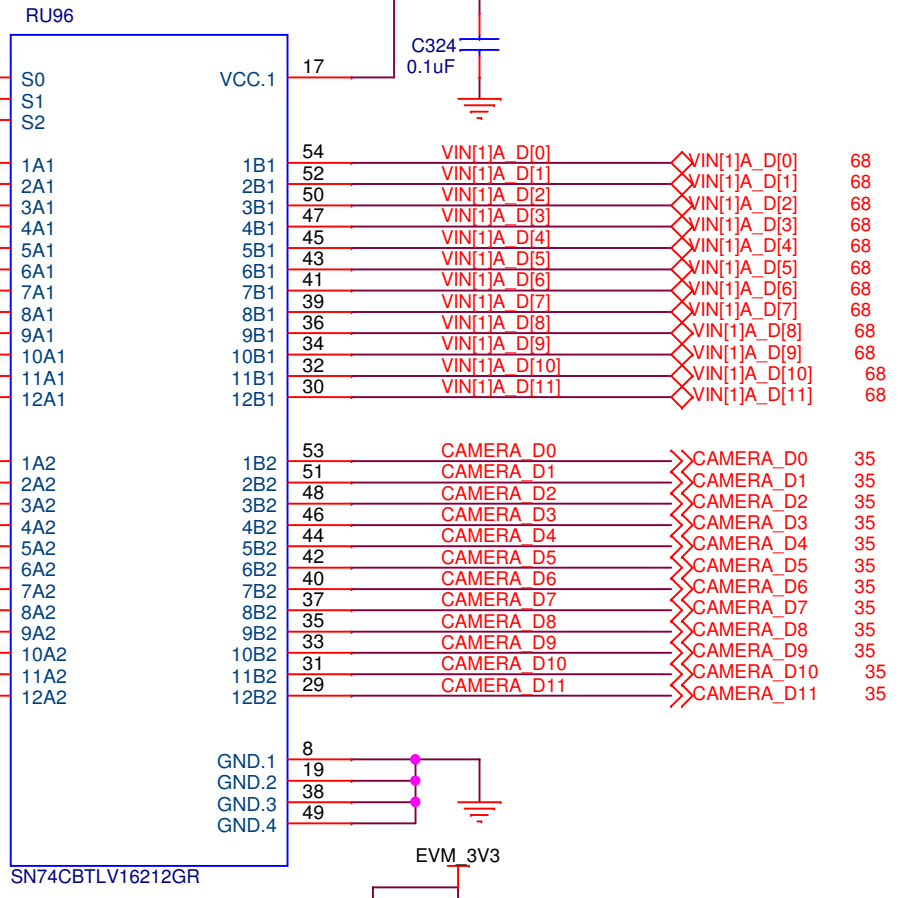


This will allow testing of the ACTVID style of capture with the sensor. Add 0 Ohm series resistor between U24 pin 6 and CAMERA_HSYNC signal.
 Add no-pop resistor between CAMERA_HSYNC signal and U24 pin 3 (enables routing CAMERA_HSYNC to VIN[1]A_DE0)."

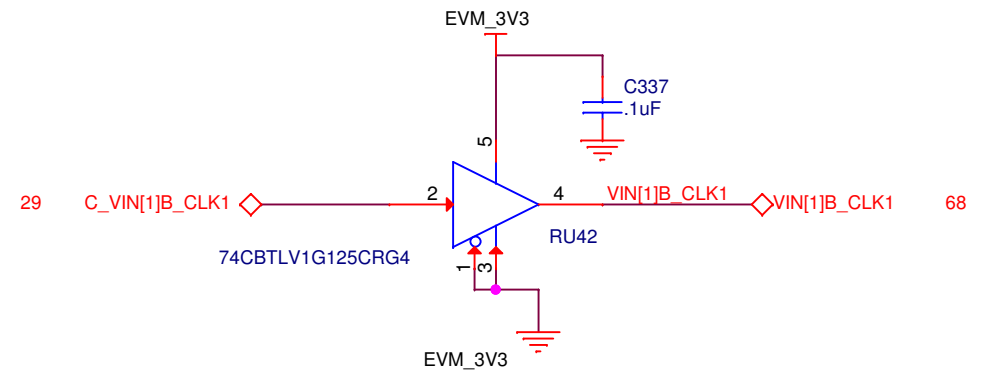
- 29 C_VIN[1]A_D[0]
- 29 C_VIN[1]A_D[1]
- 29 C_VIN[1]A_D[2]
- 29 C_VIN[1]A_D[3]
- 29 C_VIN[1]A_D[4]
- 29 C_VIN[1]A_D[5]
- 29 C_VIN[1]A_D[6]
- 29 C_VIN[1]A_D[7]
- 29 C_VIN[1]A_D[8]
- 29 C_VIN[1]A_D[9]
- 29 C_VIN[1]A_D[10]
- 29 C_VIN[1]A_D[11]



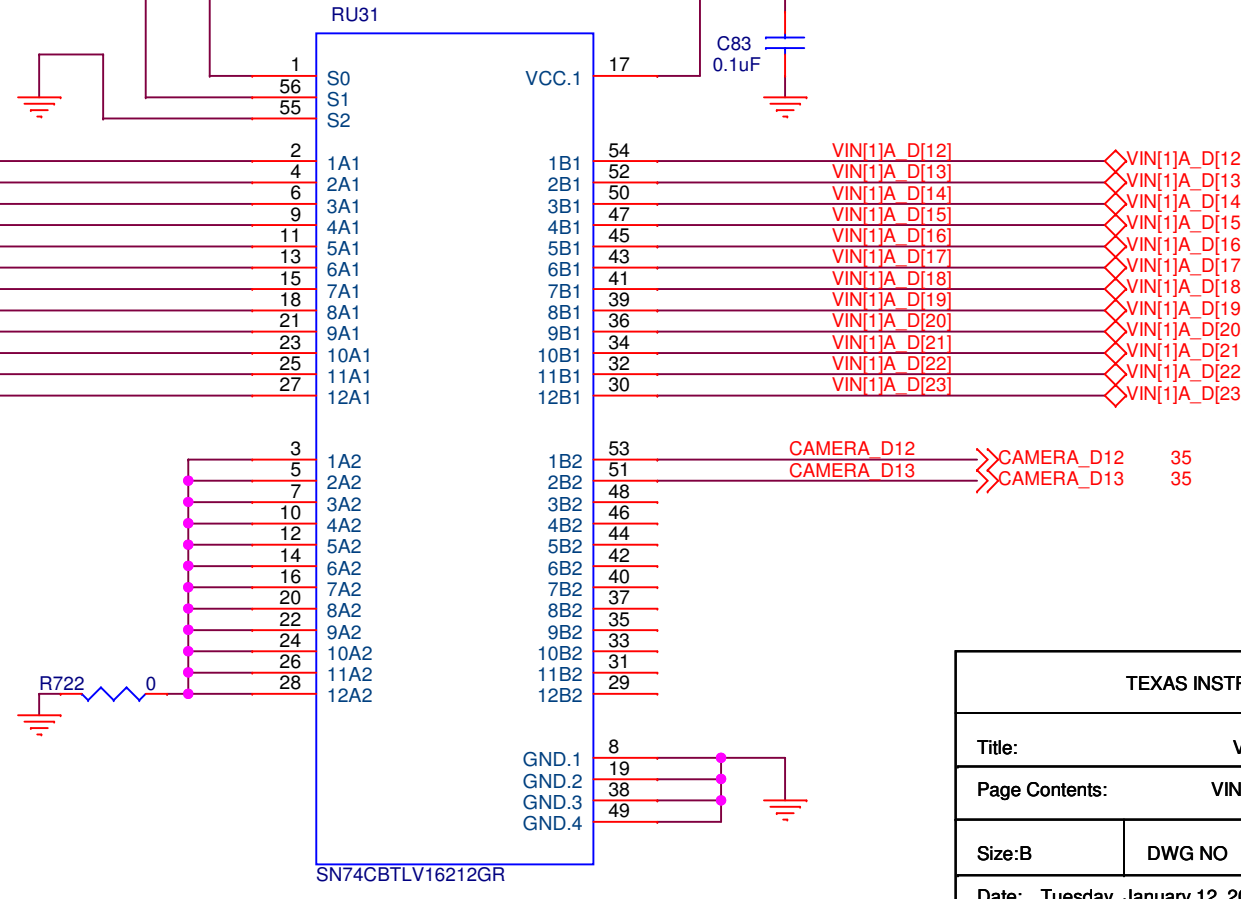
- VIN[1]A_DE0
- CAM DE0
- VIN[1]A_HSYNCO
- R CAMERA_HSYNC
- VIN[1]A_VSYNCO
- CAMERA_VSYNC
- VIN[1]A_CLK
- CAMERA_CLK



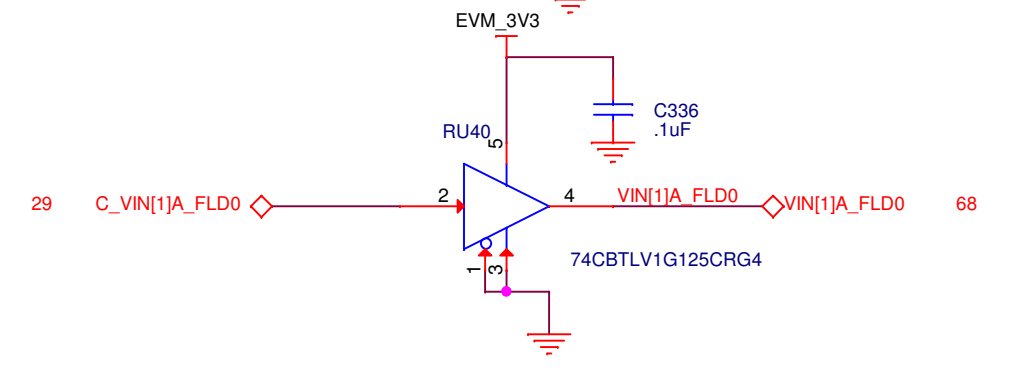
- VIN[1]A_D[0]
- VIN[1]A_D[1]
- VIN[1]A_D[2]
- VIN[1]A_D[3]
- VIN[1]A_D[4]
- VIN[1]A_D[5]
- VIN[1]A_D[6]
- VIN[1]A_D[7]
- VIN[1]A_D[8]
- VIN[1]A_D[9]
- VIN[1]A_D[10]
- VIN[1]A_D[11]
- CAMERA_D0
- CAMERA_D1
- CAMERA_D2
- CAMERA_D3
- CAMERA_D4
- CAMERA_D5
- CAMERA_D6
- CAMERA_D7
- CAMERA_D8
- CAMERA_D9
- CAMERA_D10
- CAMERA_D11



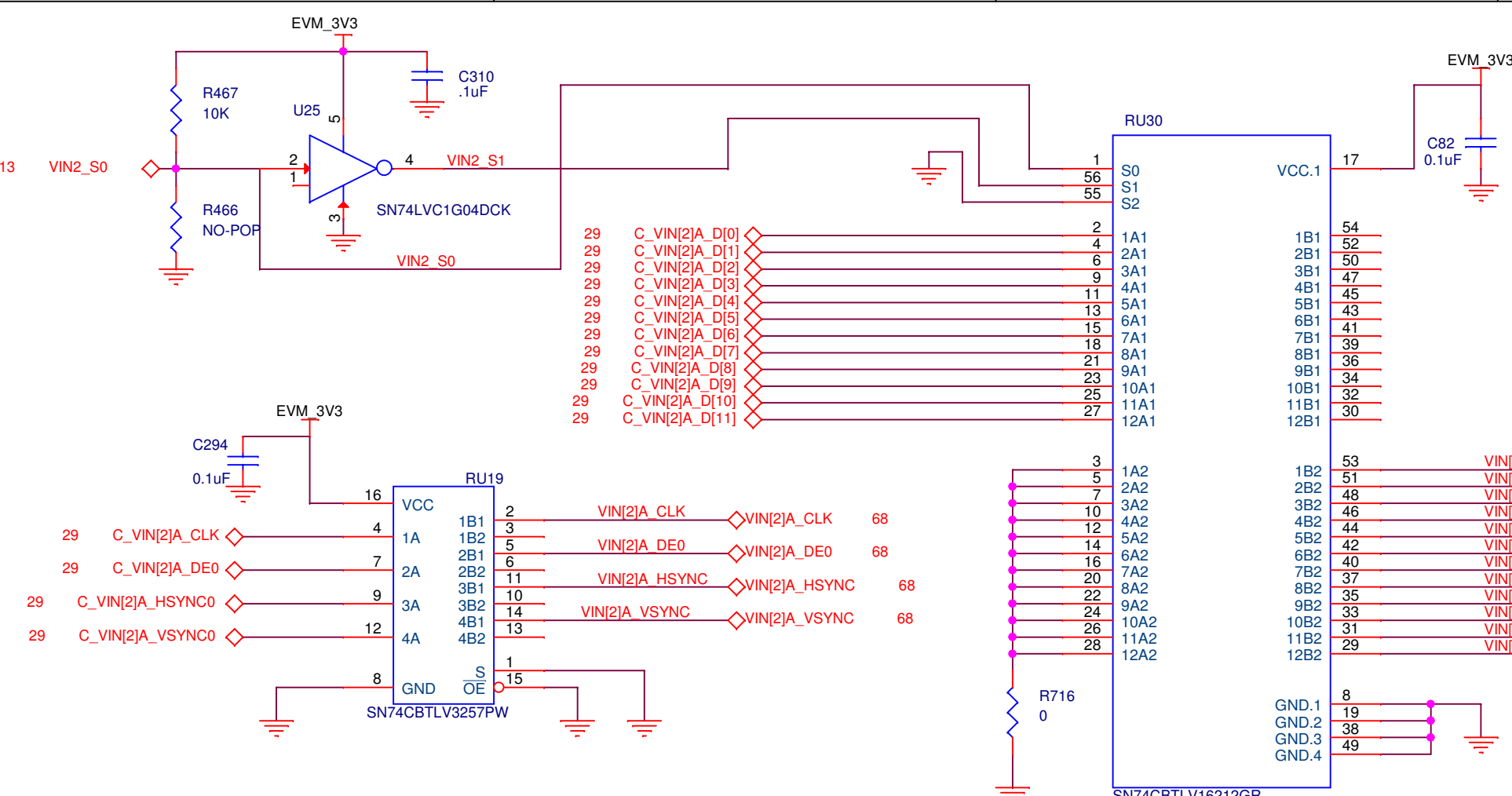
- C_VIN[1]A_D[12]
- C_VIN[1]A_D[13]
- C_VIN[1]A_D[14]
- C_VIN[1]A_D[15]
- C_VIN[1]A_D[16]
- C_VIN[1]A_D[17]
- C_VIN[1]A_D[18]
- C_VIN[1]A_D[19]
- C_VIN[1]A_D[20]
- C_VIN[1]A_D[21]
- C_VIN[1]A_D[22]
- C_VIN[1]A_D[23]



- VIN[1]A_D[12]
- VIN[1]A_D[13]
- VIN[1]A_D[14]
- VIN[1]A_D[15]
- VIN[1]A_D[16]
- VIN[1]A_D[17]
- VIN[1]A_D[18]
- VIN[1]A_D[19]
- VIN[1]A_D[20]
- VIN[1]A_D[21]
- VIN[1]A_D[22]
- VIN[1]A_D[23]
- CAMERA_D12
- CAMERA_D13

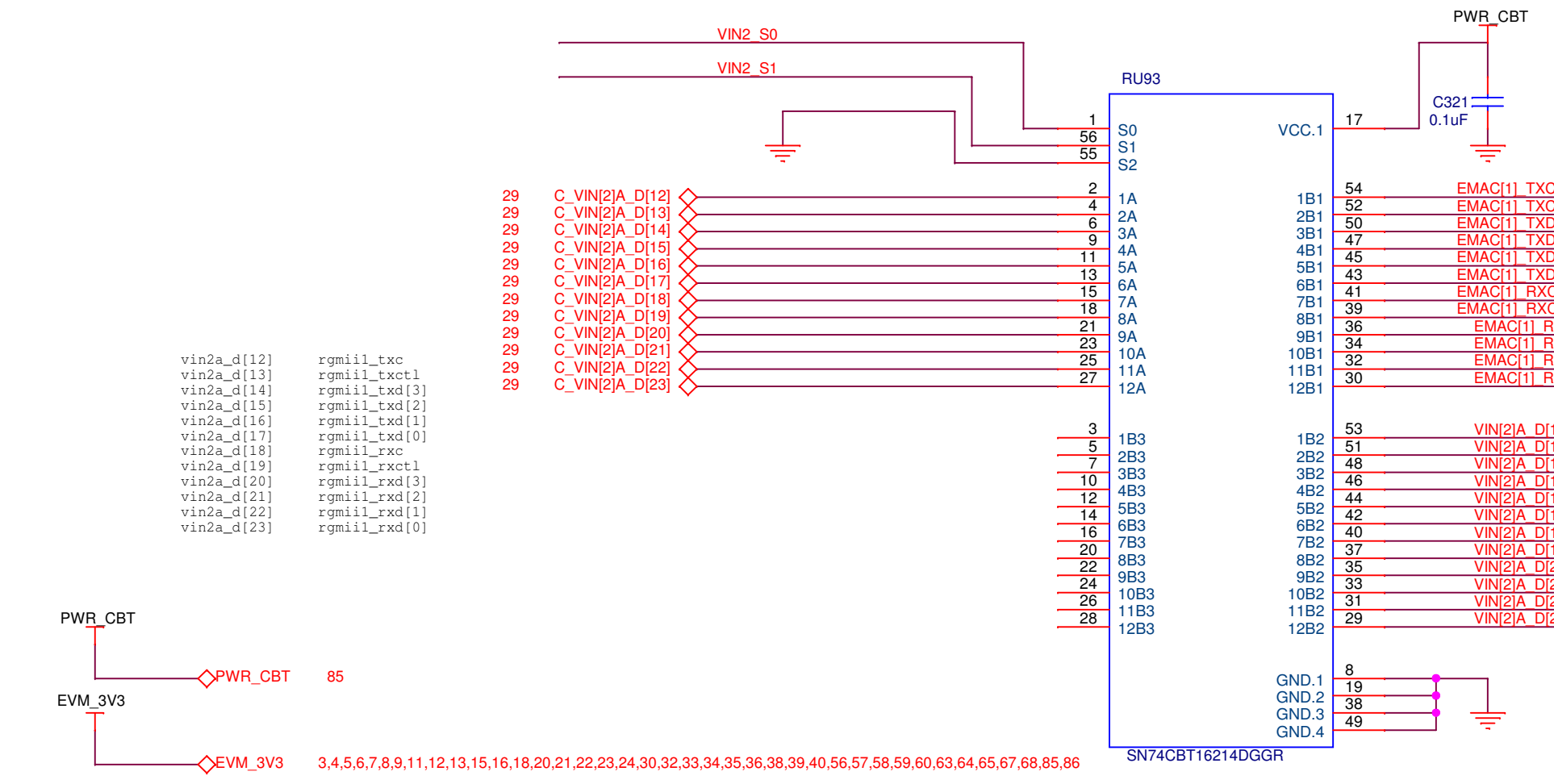


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: VIN1 MUX			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 30 of 89	



FUNCTION TABLE

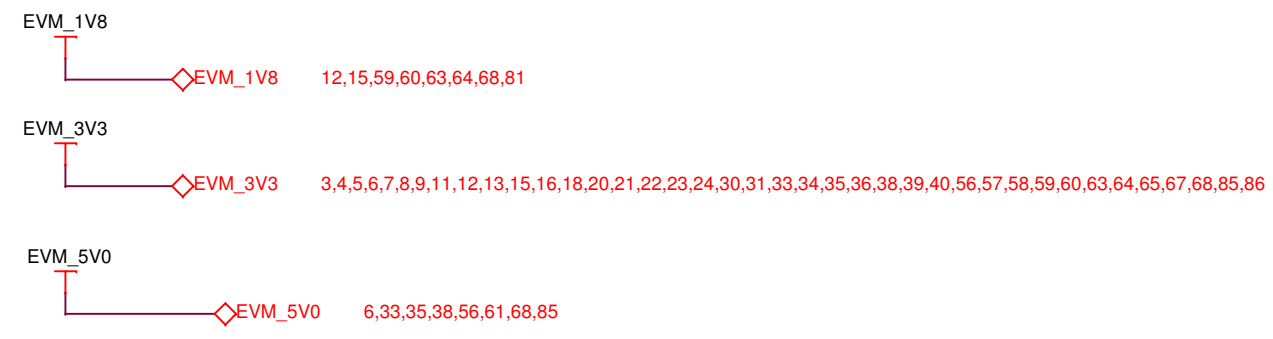
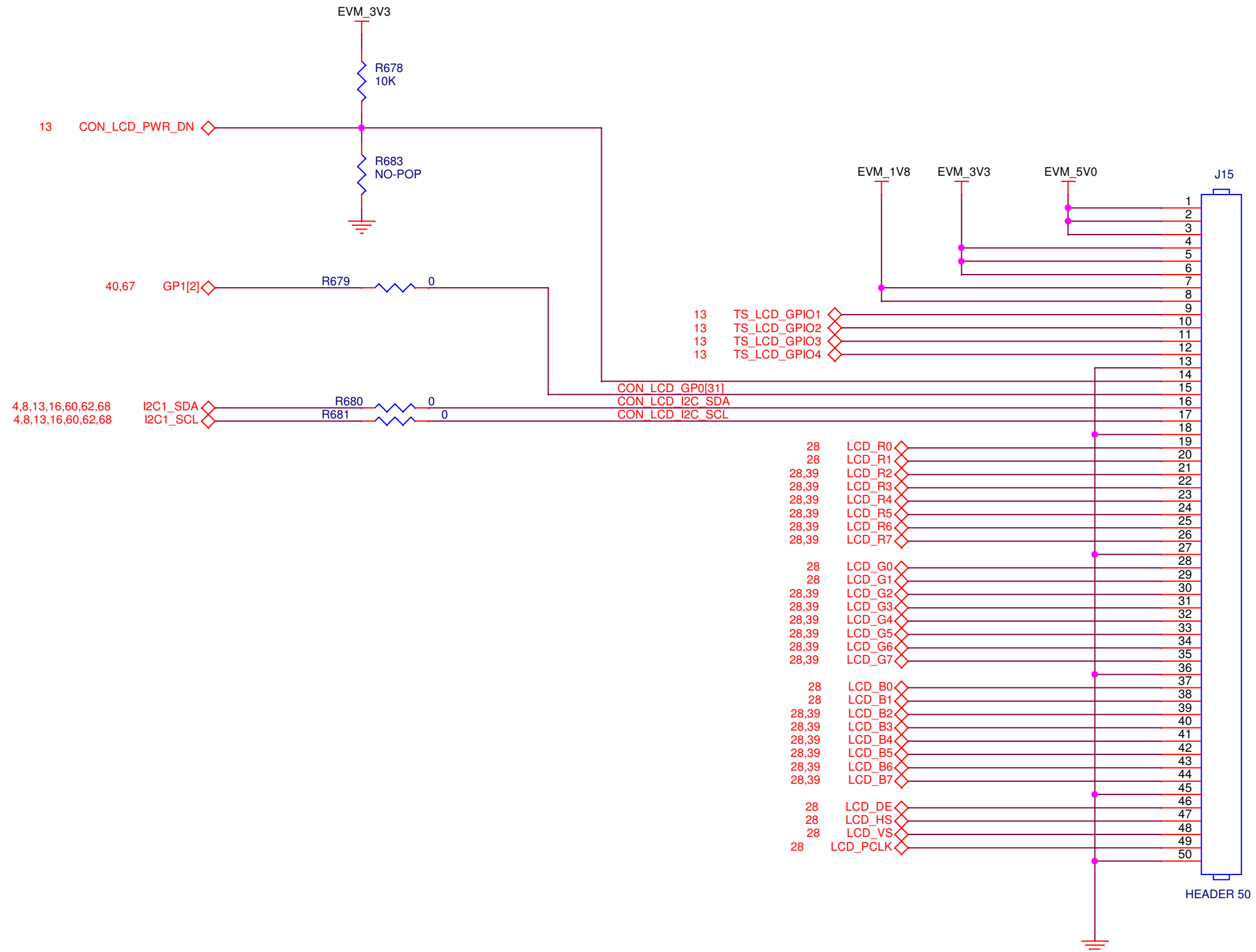
INPUTS	INPUTS/OUTPUTS	FUNCTION
S2 S1 S0	A1 A2	
L L L	Z Z	Disconnect
L L H	B1 Z	A1 port = B1 port
L H L	B2 Z	A1 port = B2 port
L H H	Z B1	A2 port = B1 port
H L L	Z B2	A2 port = B2 port
H L H	Z Z	Disconnect
H H L	B1 B2	A1 port = B1 port
H H H	B2 B1	A2 port = B2 port
H H H	B2 B1	A1 port = B2 port
H H H	B2 B1	A2 port = B1 port



FUNCTION TABLE

INPUTS	INPUTS/OUTPUTS	FUNCTION
S2 S1 S0	A	
L L L	Z	Disconnect
L L H	B1	A port = B1 port
L H L	B2	A port = B2 port
L H H	Z	Disconnect
H L L	Z	Disconnect
H L H	B3	A port = B3 port
H H L	B1	A port = B1 port
H H H	B2	A port = B2 port

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: ETHERNET 1 / VIN2 MUX			
Size: B	DWG NO	516582-0001	Revision: C
Date: Tuesday, January 12, 2016	Sheet 31 of 89		



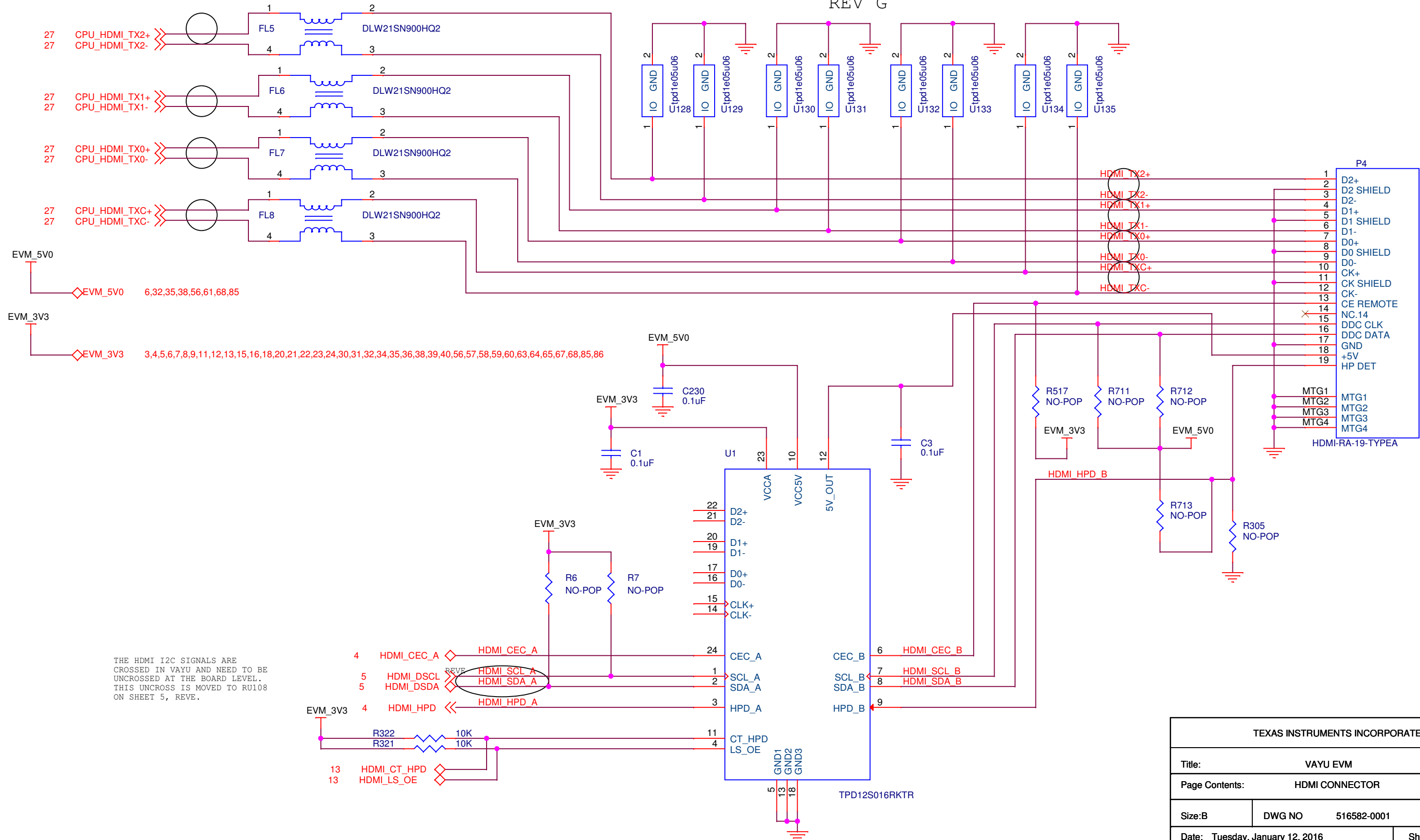
TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		LCD CONNECTOR	
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016	Sheet	32 of	89

DIFFERENTIAL PAIR
 100 OHM DIFFERENTIAL
 IMPEDANCE
 SHORT AND STRAIGHT AS
 POSSIBLE,
 MINIMUM NUMBER OF VIAS

DIFFERENTIAL PAIR
 100 OHM DIFFERENTIAL
 IMPEDANCE
 SHORT AND STRAIGHT AS
 POSSIBLE,
 MINIMUM NUMBER OF VIAS

ER13

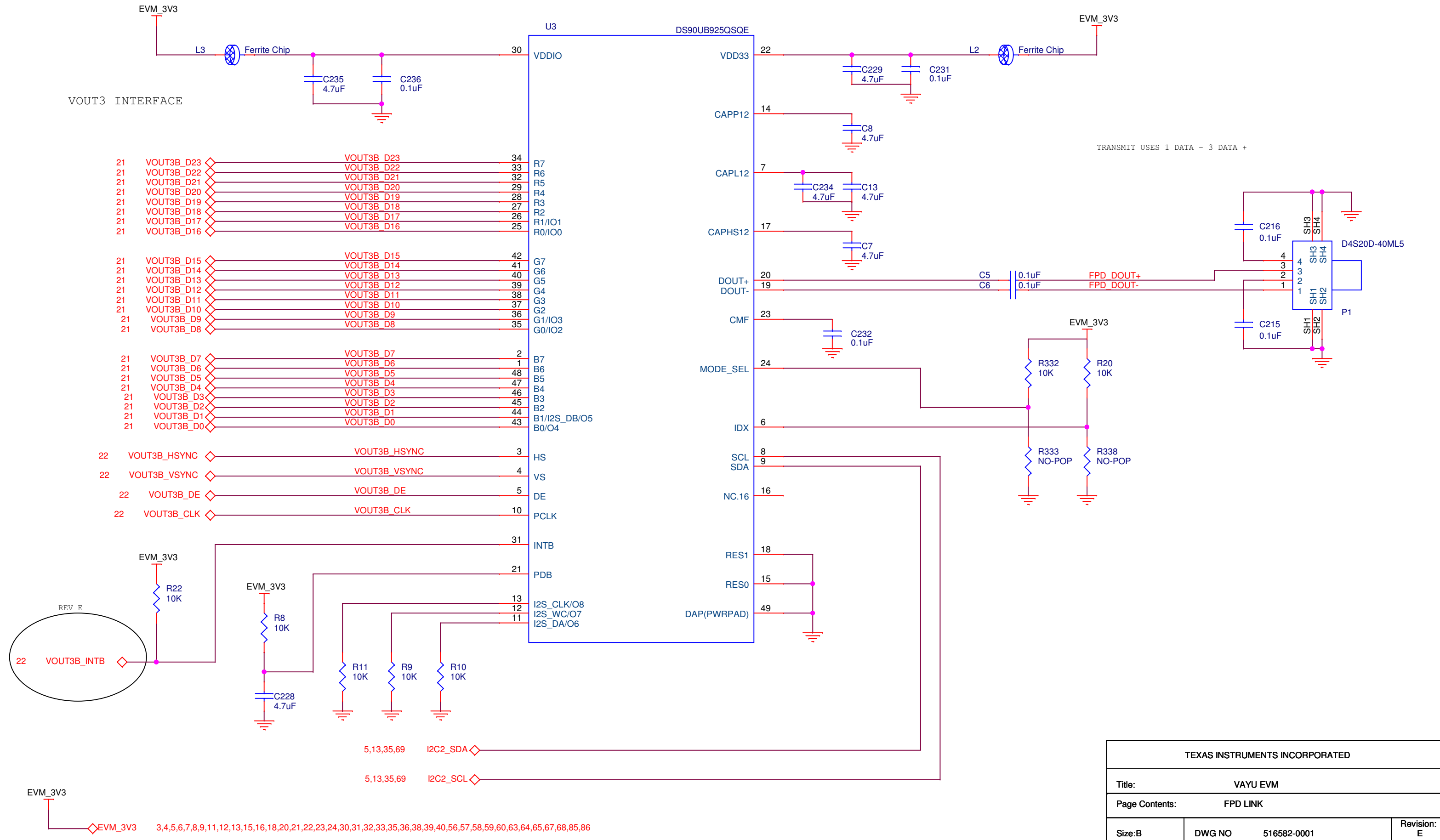
REV G



THE HDMI I2C SIGNALS ARE
 CROSSED IN VAYU AND NEED TO BE
 UNCROSSED AT THE BOARD LEVEL.
 THIS UNCROSS IS MOVED TO RU108
 ON SHEET 5, REVE.

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: HDMI CONNECTOR			
Size: B	DWG NO	516582-0001	Revision: H
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VOUT3 INTERFACE



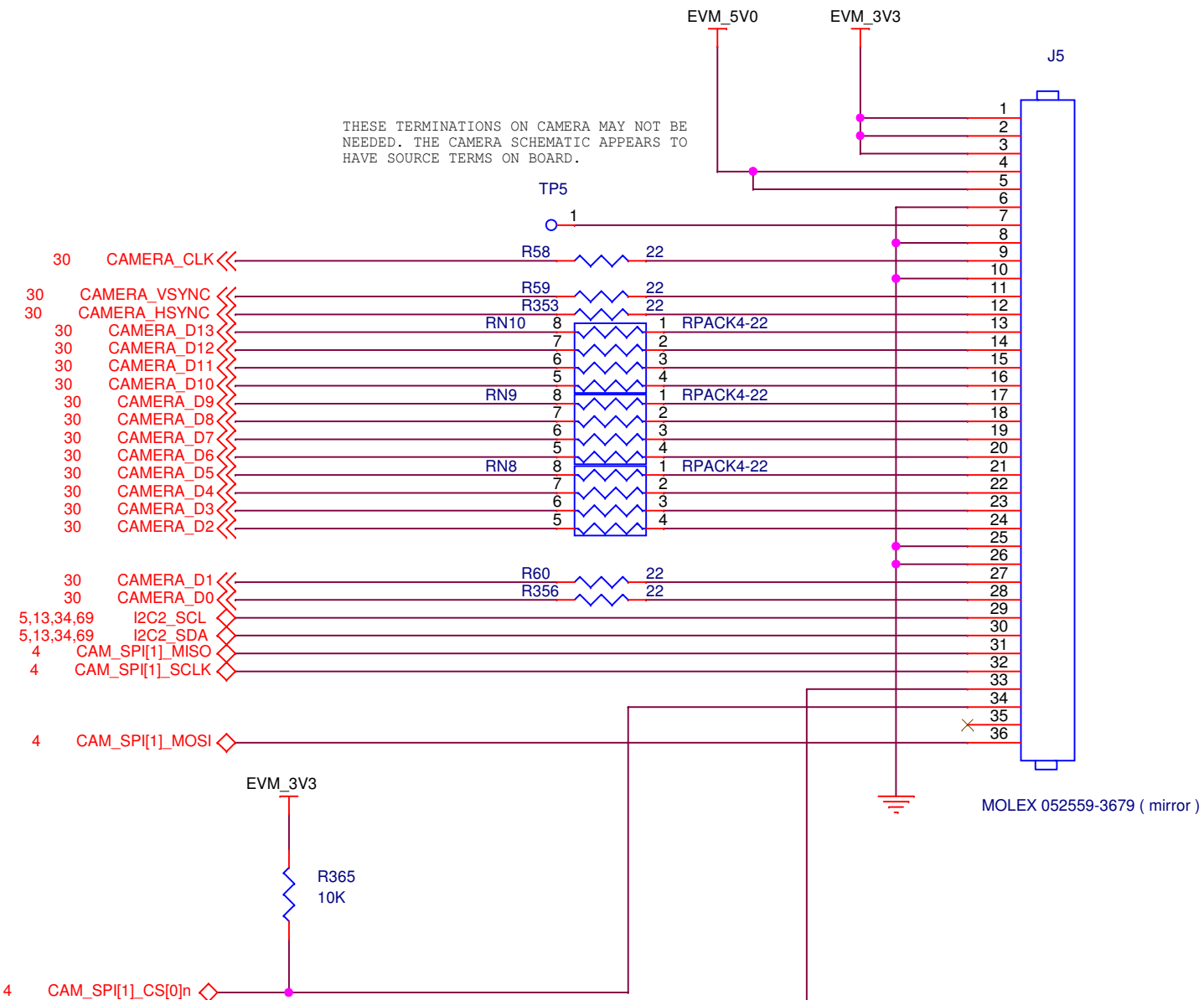
TRANSMIT USES 1 DATA - 3 DATA +

REV E

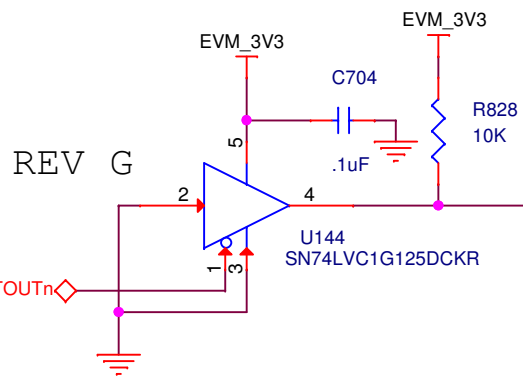
EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85,86

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: FPD LINK			
Size: B	DWG NO	516582-0001	Revision: E
Date: Tuesday, January 12, 2016		Sheet 34 of 89	

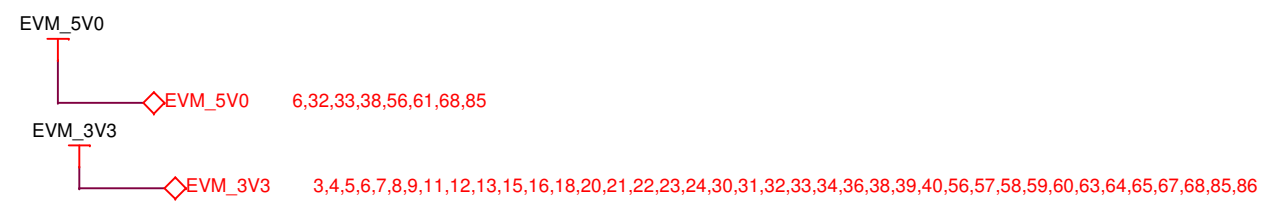
THESE TERMINATIONS ON CAMERA MAY NOT BE NEEDED. THE CAMERA SCHEMATIC APPEARS TO HAVE SOURCE TERMS ON BOARD.



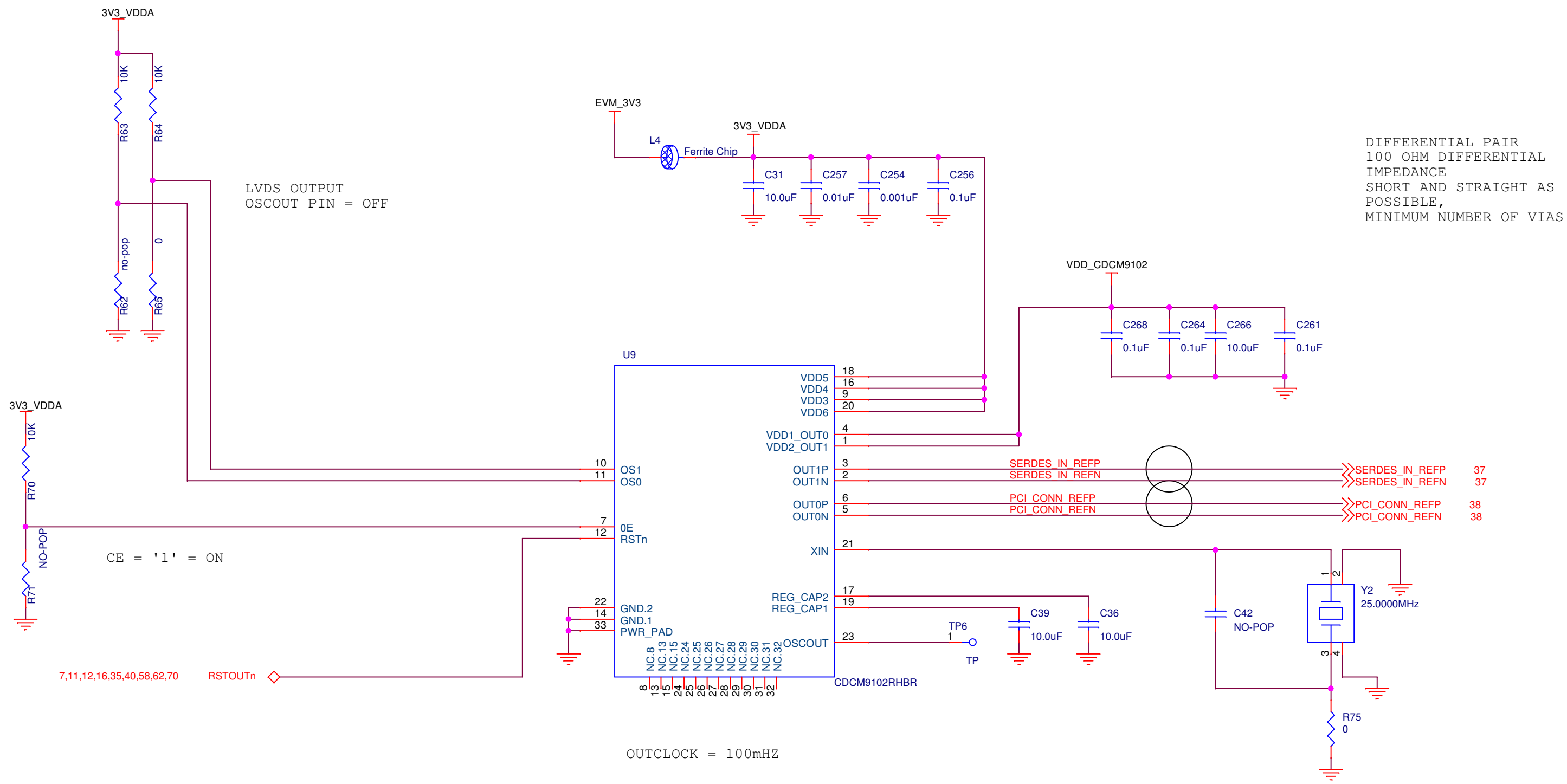
- MHC1
- MHC1
- MHC2
- MHC2



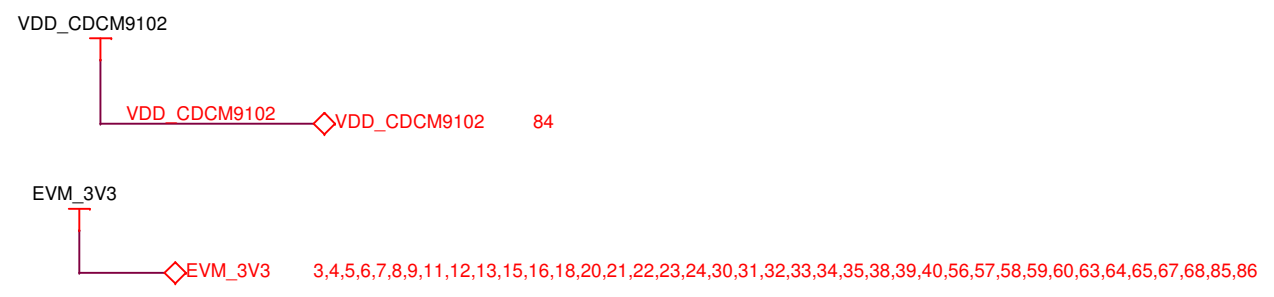
7,11,16,35,36,40,58,62,70 RSTOUTn



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: CAMERA INTERFACE			
Size: B	DWG NO	516582-0001	Revision: G
Date: Tuesday, January 12, 2016		Sheet 35 of	89

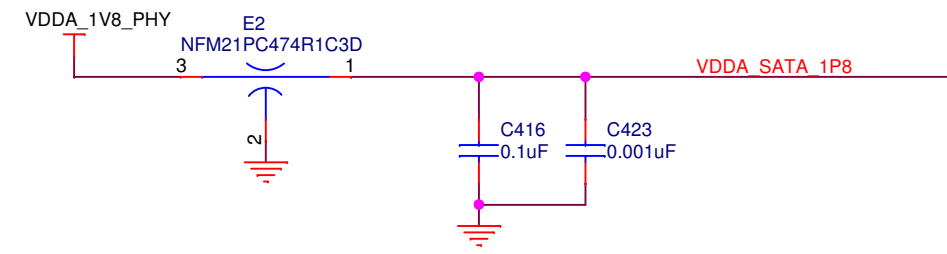


DIFFERENTIAL PAIR
 100 OHM DIFFERENTIAL
 IMPEDANCE
 SHORT AND STRAIGHT AS
 POSSIBLE,
 MINIMUM NUMBER OF VIAS



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: SERDES CLOCKS			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 36 of	89

1.8 VOLT

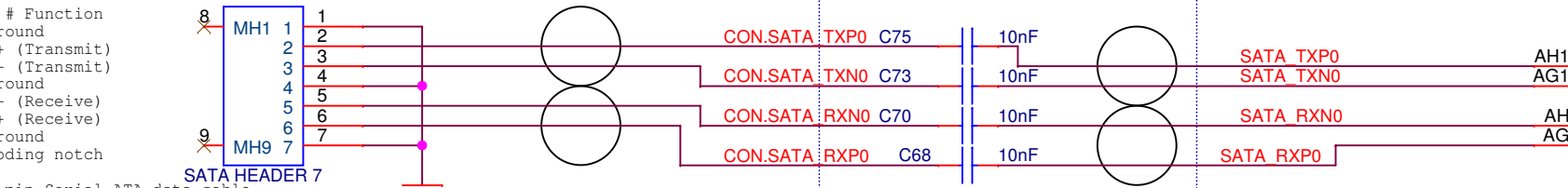


DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS

- Pin # Function
1 Ground
2 A+ (Transmit)
3 A- (Transmit)
4 Ground
5 B- (Receive)
6 B+ (Receive)
7 Ground
- coding notch

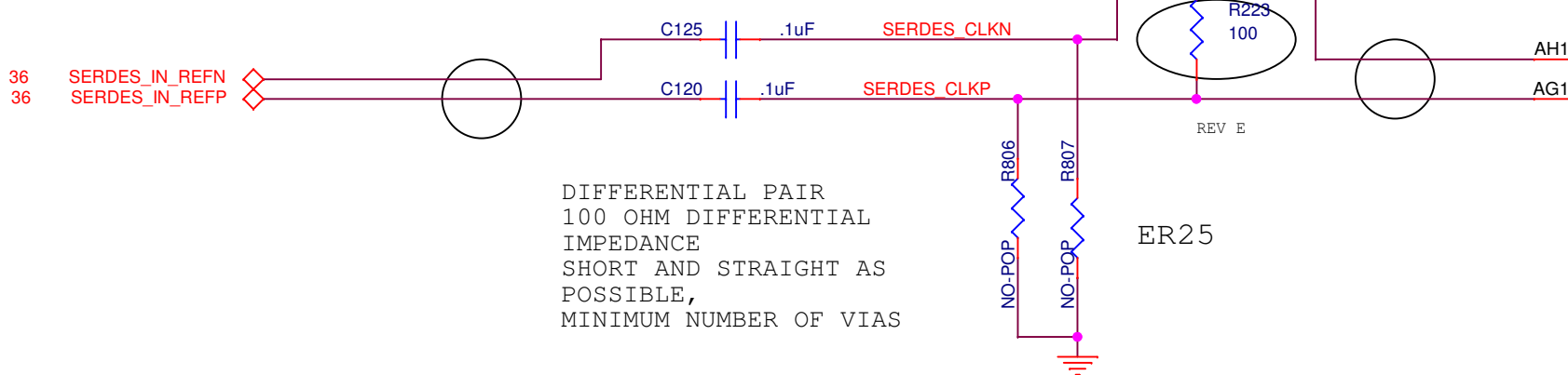
J11
SATA HEADER 7
A 7-pin Serial ATA data cable

AC COUPLING CAP
PLACE BY CONNECTOR

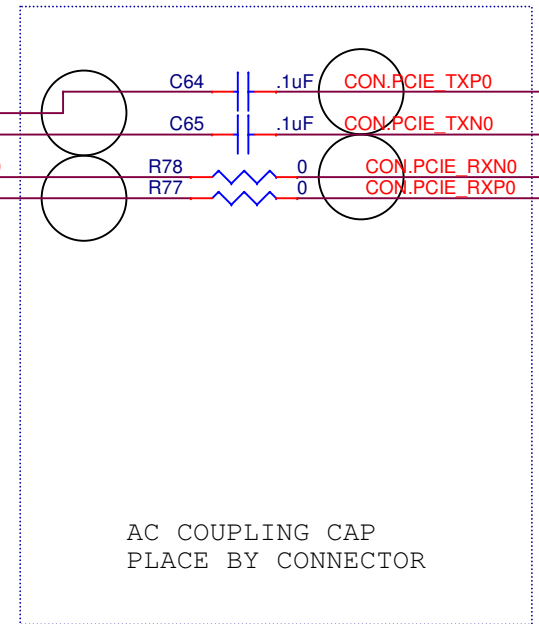
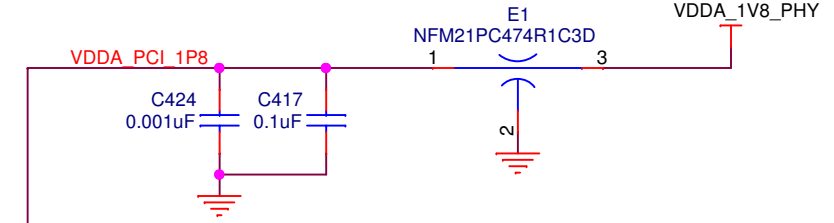


- 36 SERDES_IN_REFN
36 SERDES_IN_REFP

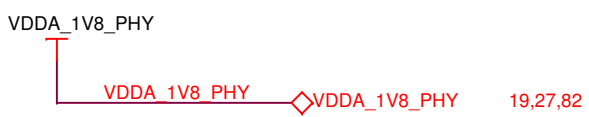
DIFFERENTIAL PAIR
100 OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



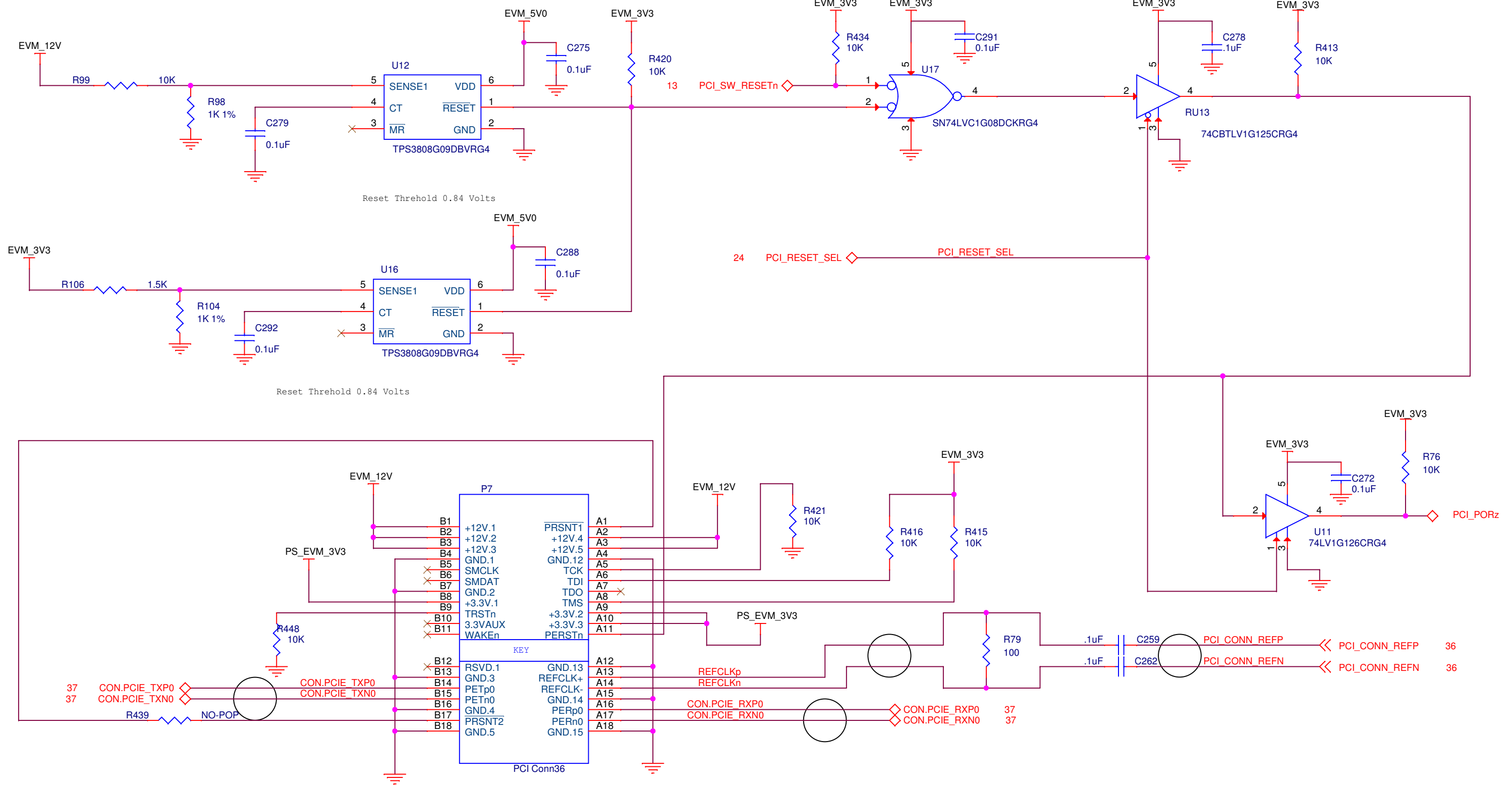
1.8 VOLT



DIFFERENTIAL PAIR
XXXX OHM DIFFERENTIAL
IMPEDANCE
SHORT AND STRAIGHT AS
POSSIBLE,
MINIMUM NUMBER OF VIAS



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: PCIe/SATA INTERFACE			
Size: B	DWG NO	516582-0001	Revision: F
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Connector must be less than 2.25 inches to board edge from key to board edge

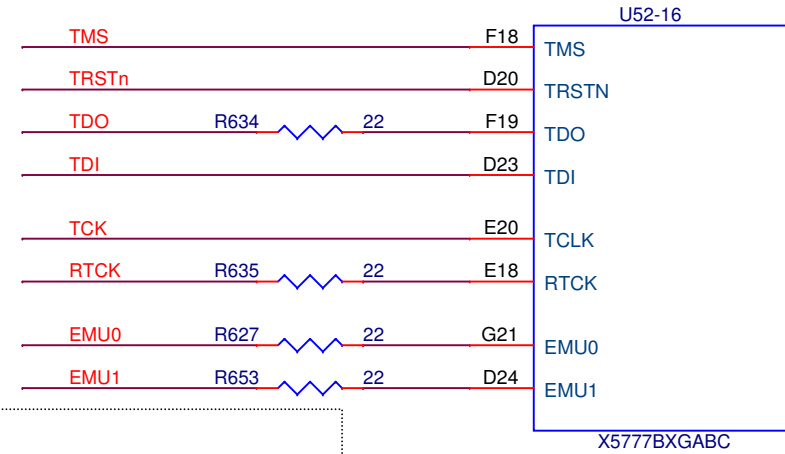
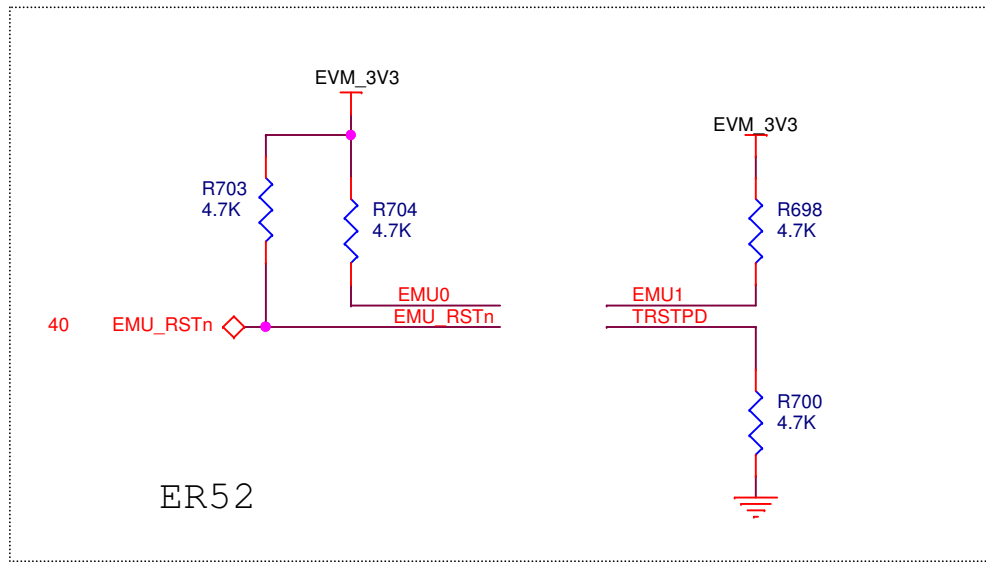
PS_EVM_3V3
PS_EVM_3V3 70,71,72,73,74,75,76,78,79,80,81,82,84,86

EVM_12V
EVM_12V 16,68,74,87

EVM_3V3
EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,39,40,56,57,58,59,60,63,64,65,67,68,85,86

EVM_5V0
EVM_5V0 6,32,33,35,56,61,68,85

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: PCIe CONNECTOR			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 38 of	89

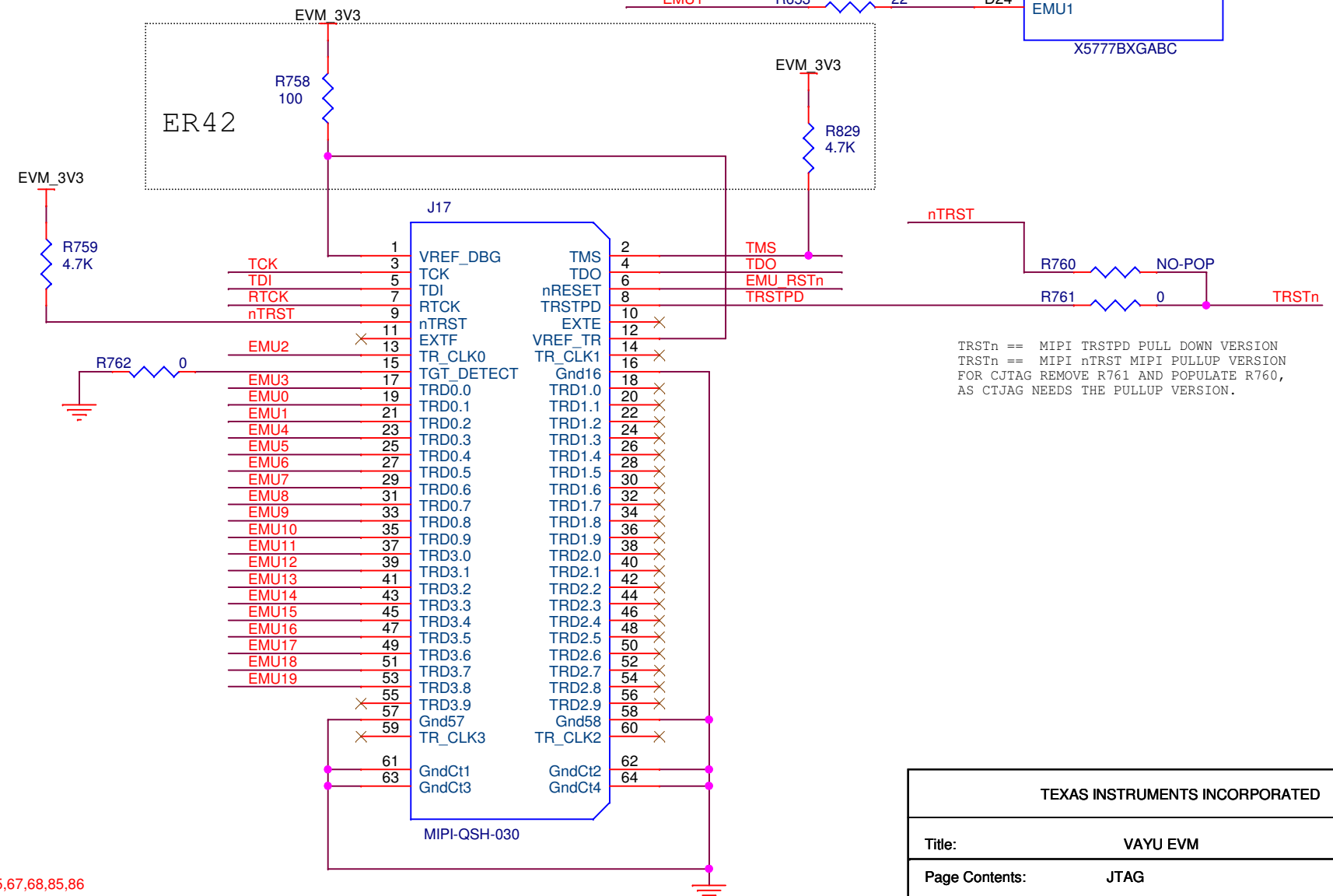


- 28,32 LCD_B2 EMU2
- 28,32 LCD_B3 EMU5
- 28,32 LCD_B4 EMU6
- 28,32 LCD_B5 EMU7
- 28,32 LCD_B6 EMU8
- 28,32 LCD_B7 EMU9

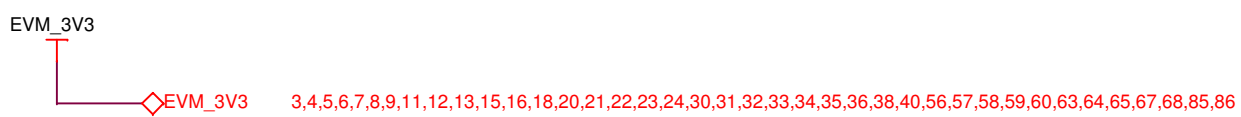
- 28,32 LCD_G2 EMU3
- 28,32 LCD_G3 EMU10
- 28,32 LCD_G4 EMU11
- 28,32 LCD_G5 EMU12
- 28,32 LCD_G6 EMU13
- 28,32 LCD_G7 EMU14

- 28,32 LCD_R2 EMU4
- 28,32 LCD_R3 EMU15
- 28,32 LCD_R4 EMU16
- 28,32 LCD_R5 EMU17
- 28,32 LCD_R6 EMU18
- 28,32 LCD_R7 EMU19

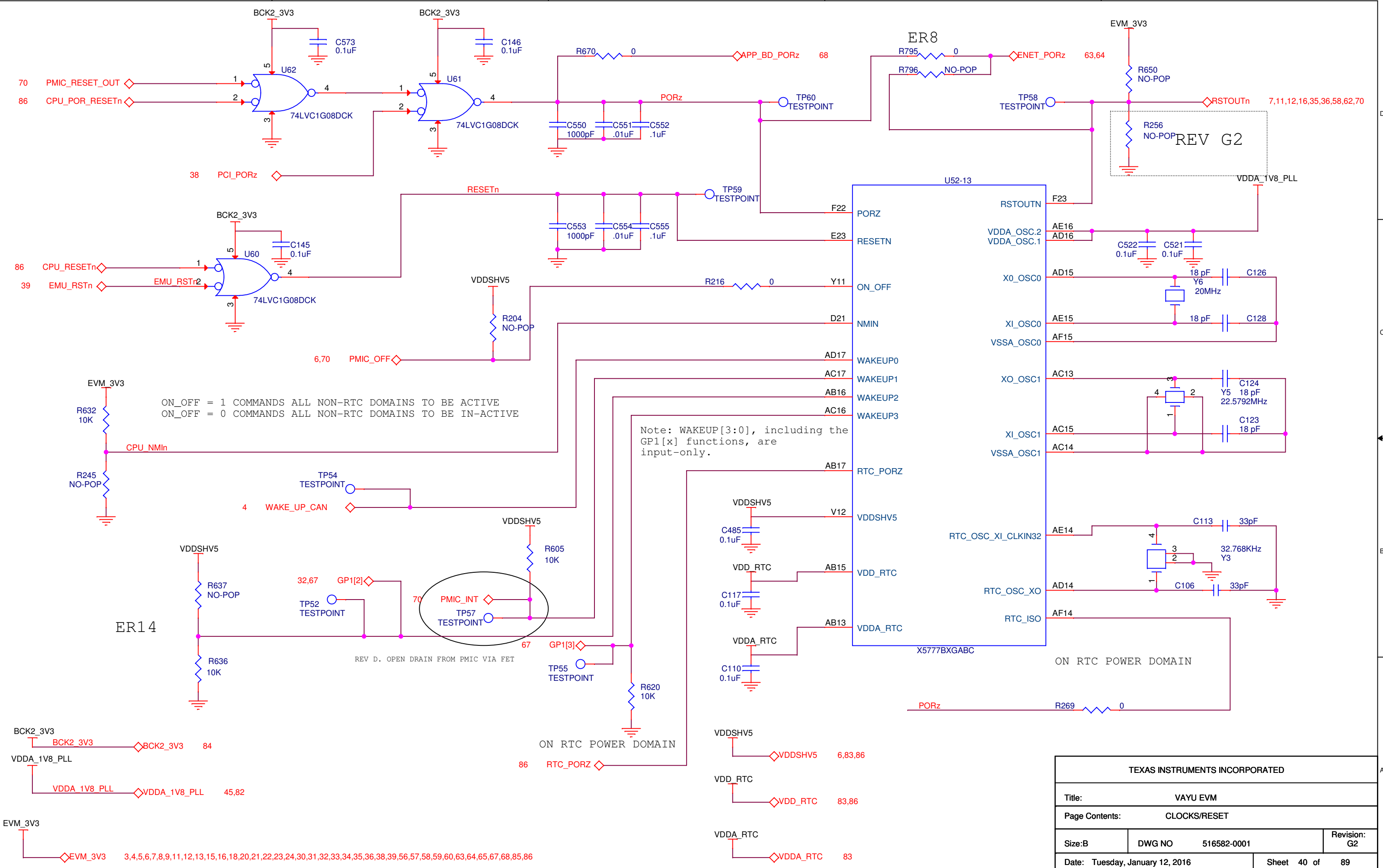
EMUx SIGNALS NEED TO ROUTE FROM U52 THROUGH J17/J14 THEN TO LCD. THE TRACE LENGTH RULES FOR THE LCD SIGNALS NEEDS TO BE MAINTAINED.



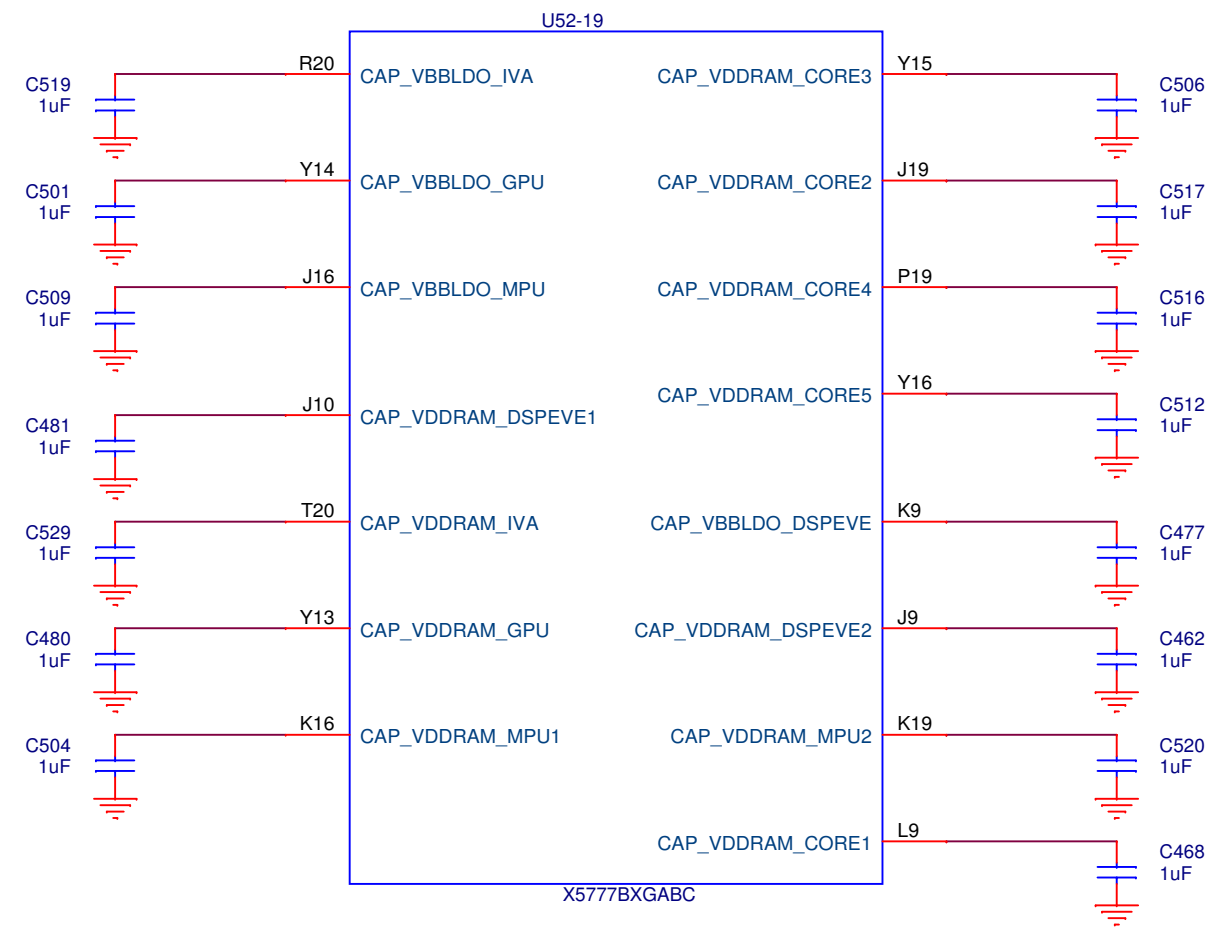
TRSTn == MIPI TRSTPD PULL DOWN VERSION
 TRSTn == MIPI nTRST MIPI PULLUP VERSION
 FOR CJTAG REMOVE R761 AND POPULATE R760,
 AS CJTAG NEEDS THE PULLUP VERSION.



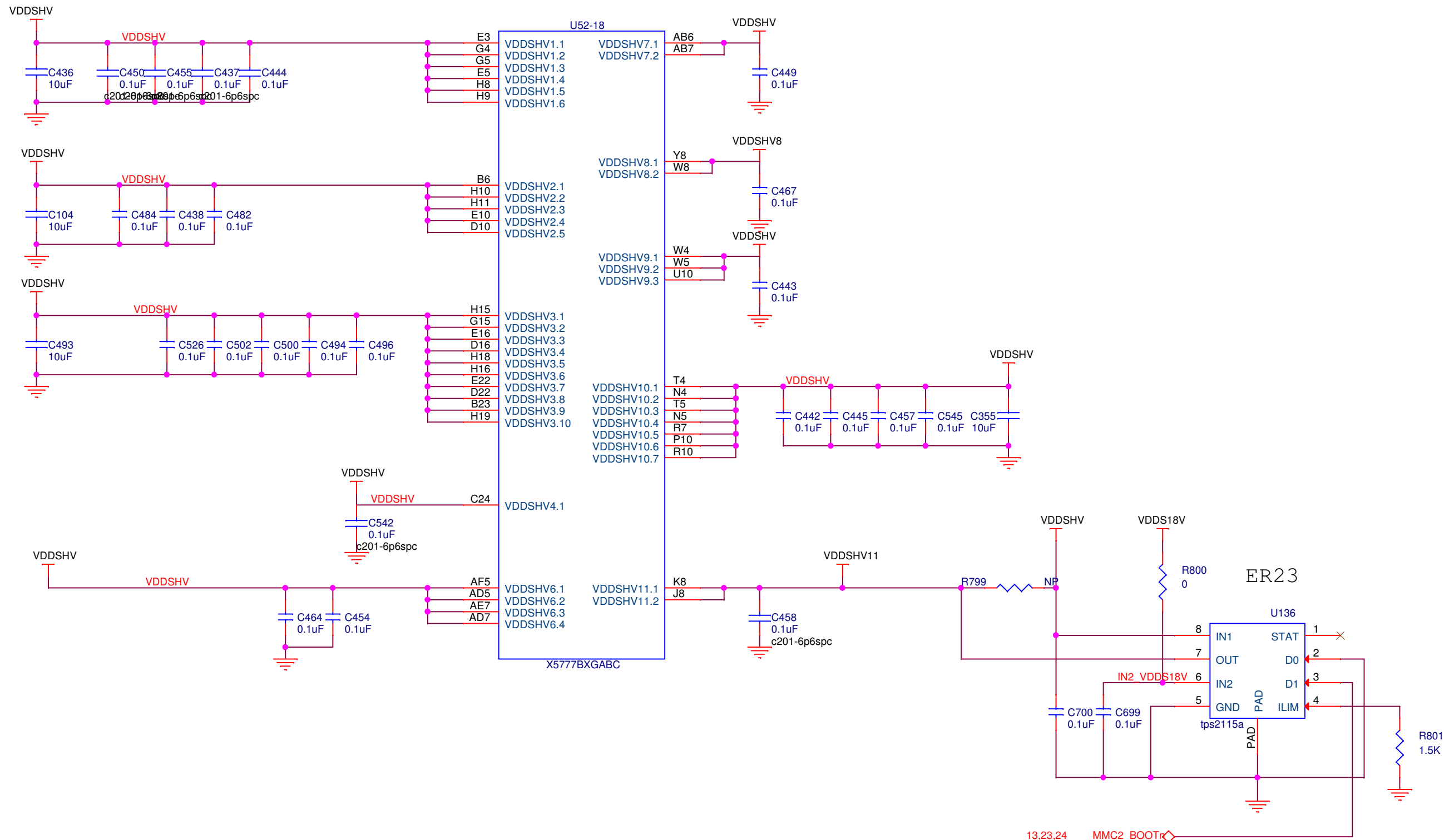
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: JTAG			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 39 of 89	



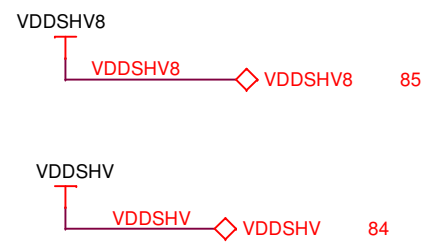
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: CLOCKS/RESET			
Size: B	DWG NO	516582-0001	Revision: G2
Date: Tuesday, January 12, 2016		Sheet 40 of 89	



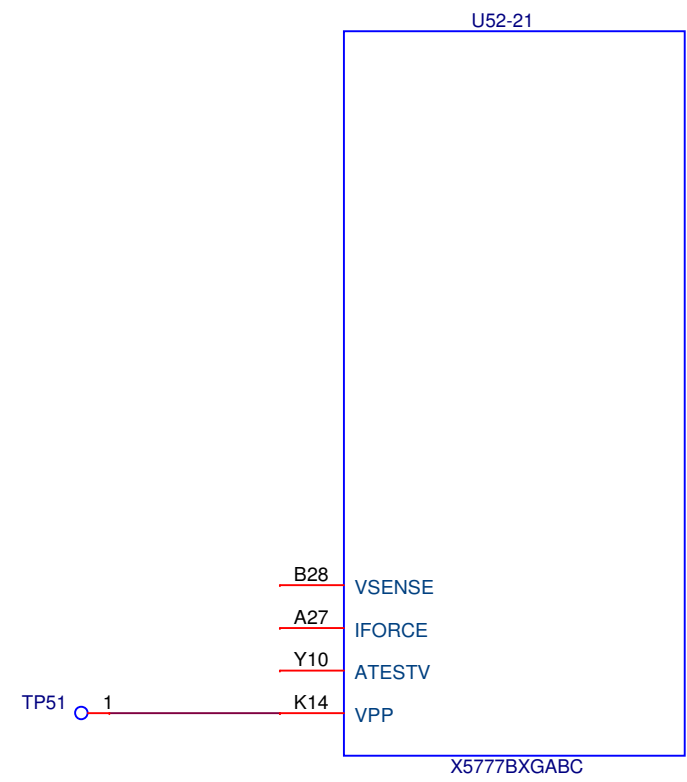
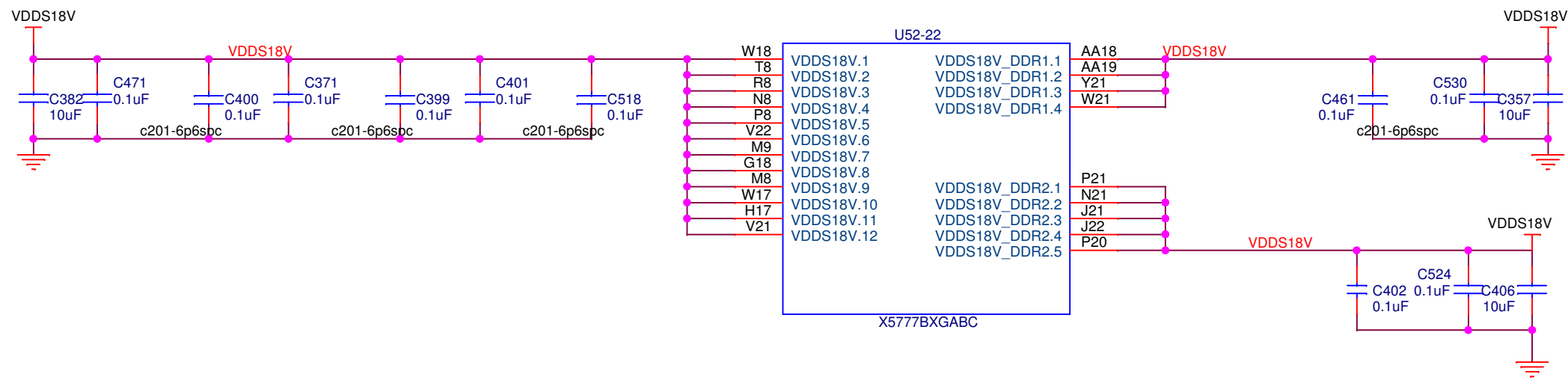
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: INTERNAL LDOS			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 41 of	89



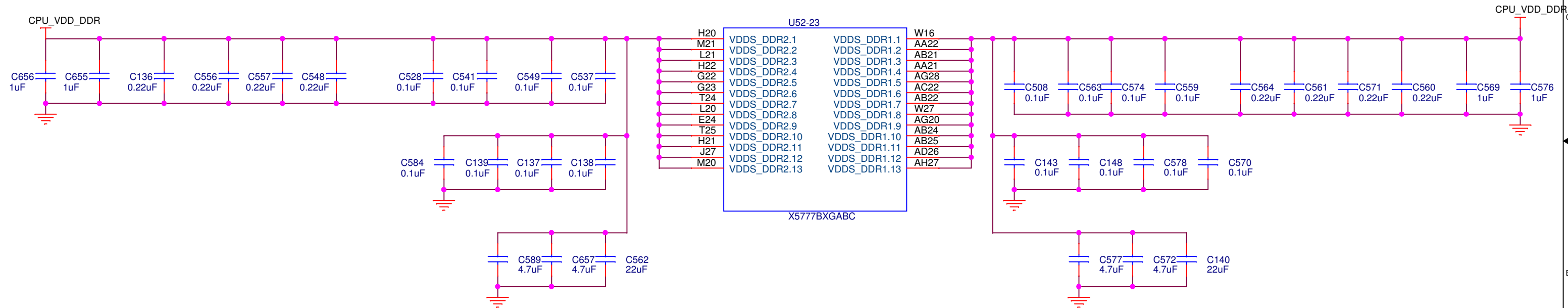
D1=1, IN1 NOR BOOT
D1=0, IN2 eMMC BOOT
BOOT SWITCHES DEFAULT AS PULLUPS. SWITCH
CLOSED IS PULL DOWN TO SELECT FUNCTION.



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: I/O POWER			
Size: B	DWG NO	516582-0001	Revision: F
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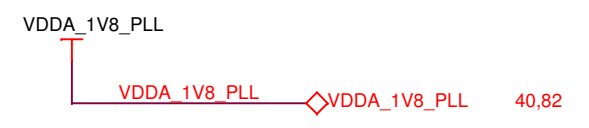
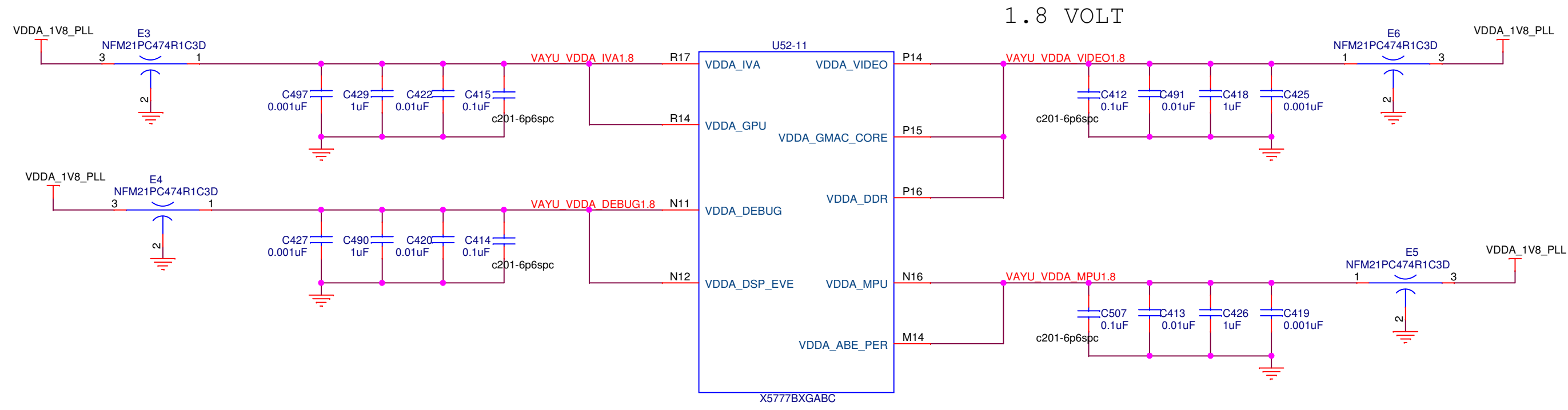


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: 1V8 POWER			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 43 of	89

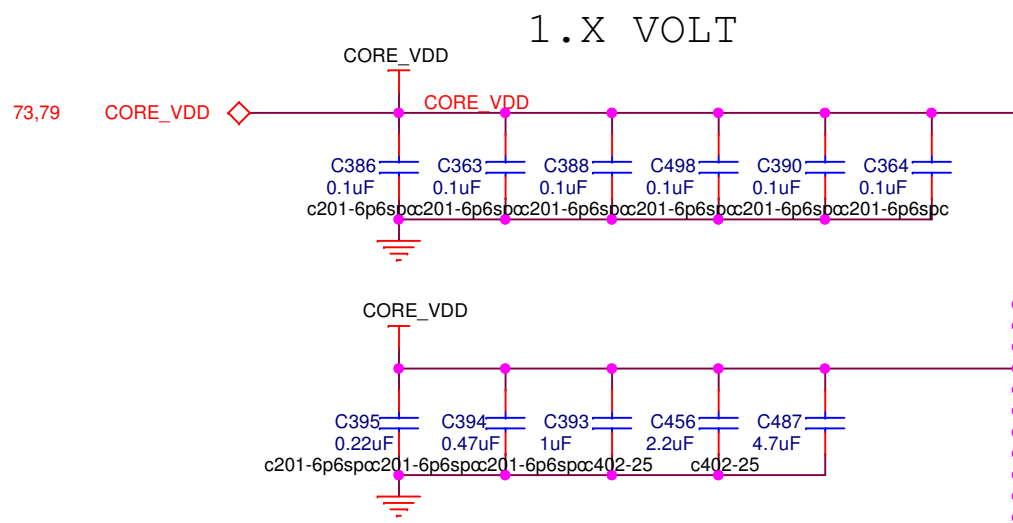


CPU_VDD_DDR
 CPU_VDD_DDR \diamond CPU_VDD_DDR 25,26,80

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: DDR3 POWER PINS			
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 44 of	89



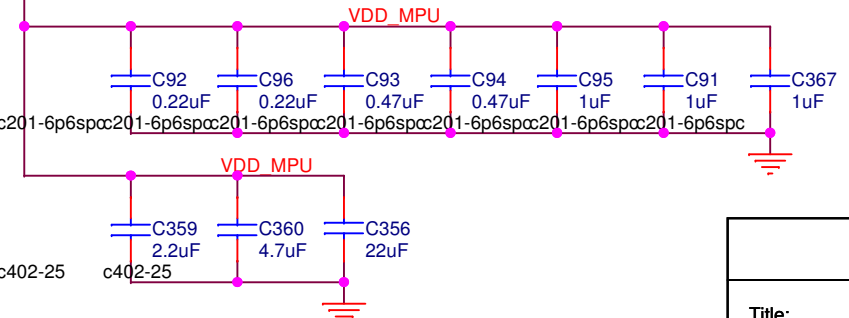
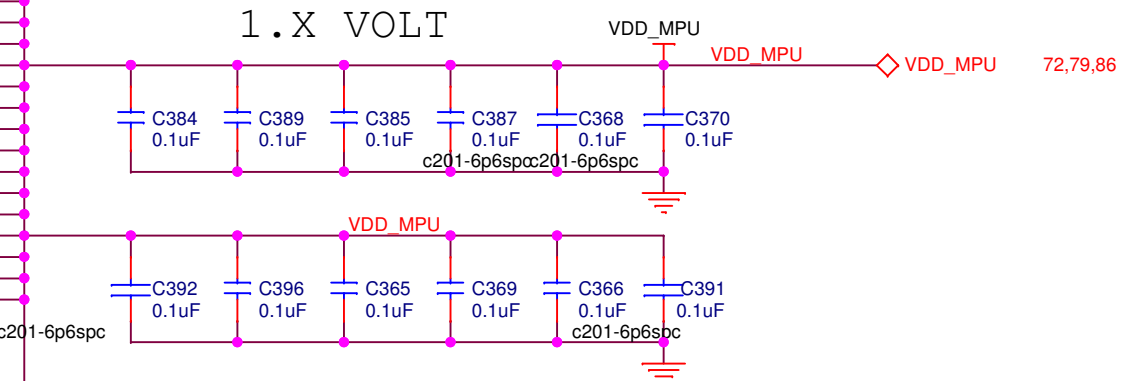
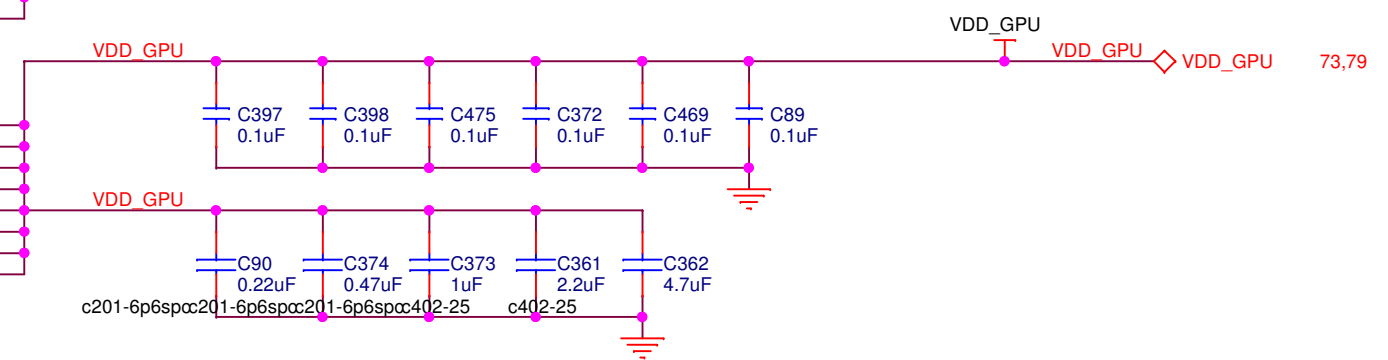
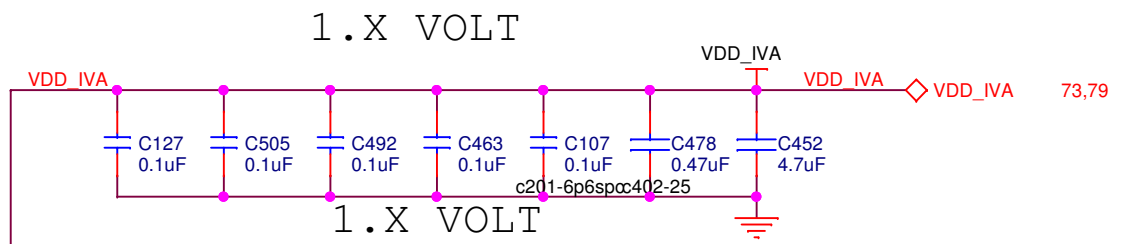
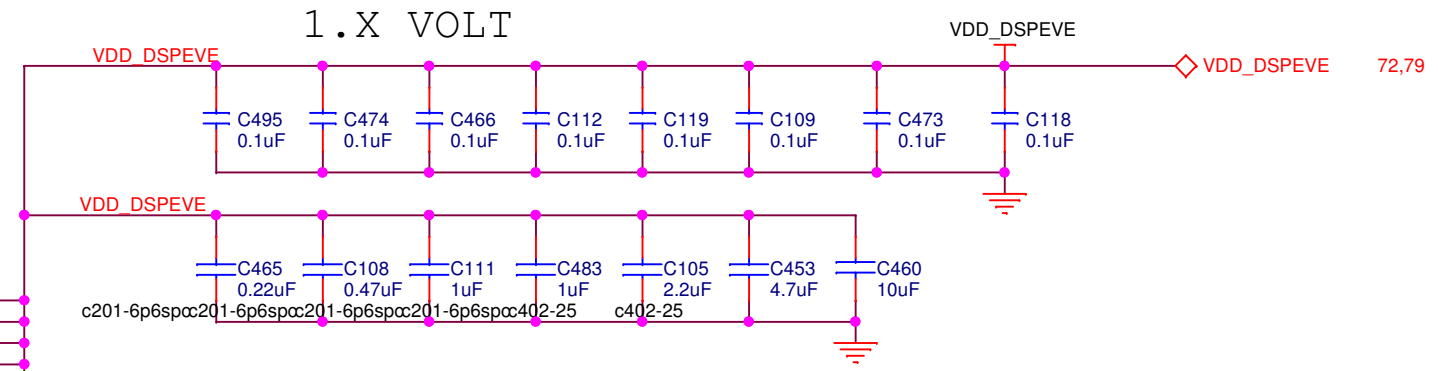
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: 1V8 VDDA			
Size: B	DWG NO	516582-0001	Revision: A
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U52-9

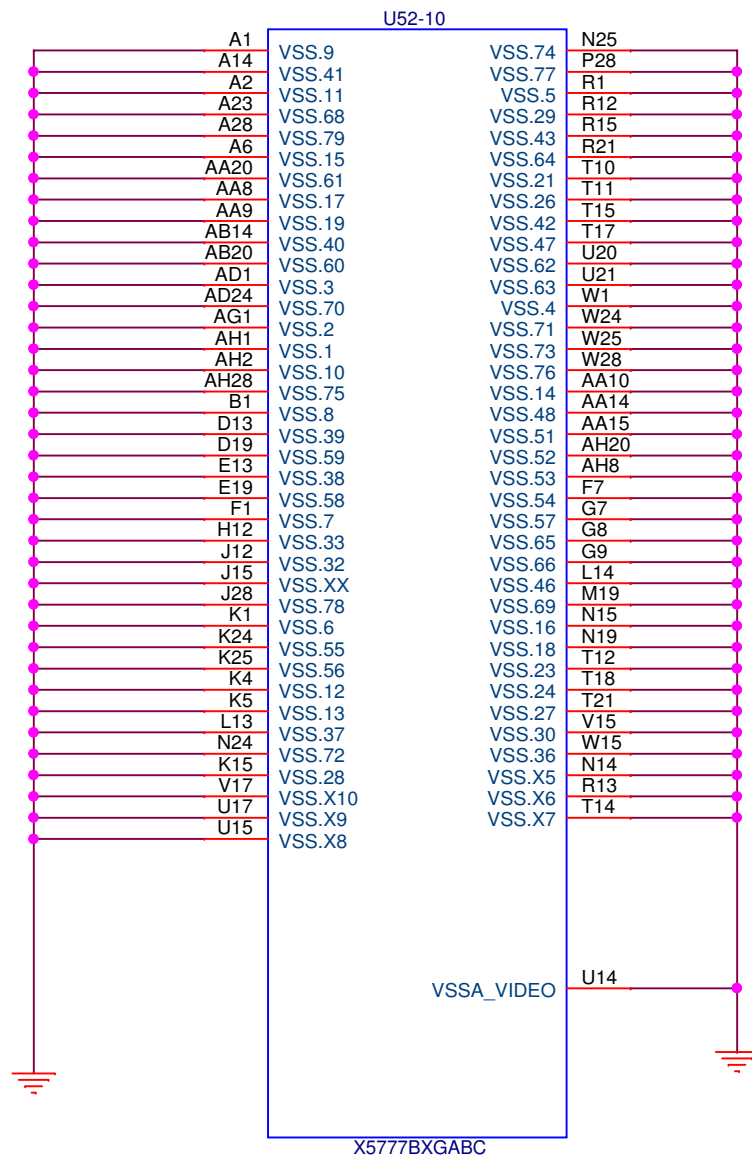
V8	VDD.1
H13	VDD.18
H14	VDD.22
N10	VDD.6
N13	VDD.16
P11	VDD.9
R11	VDD.8
R16	VDD.26
R19	VDD.27
T13	VDD.13
T16	VDD.25
U8	VDD.29
U9	VDD.2
U13	VDD.3
P12	VDD.12
L7	VDD.34
L8	VDD.15
J17	VDD.X1
J18	VDD.X2
P13	VDD.X3
T19	VDD.X7
U16	VDD.X8
V16	VDD.X9

X5777BXCABC

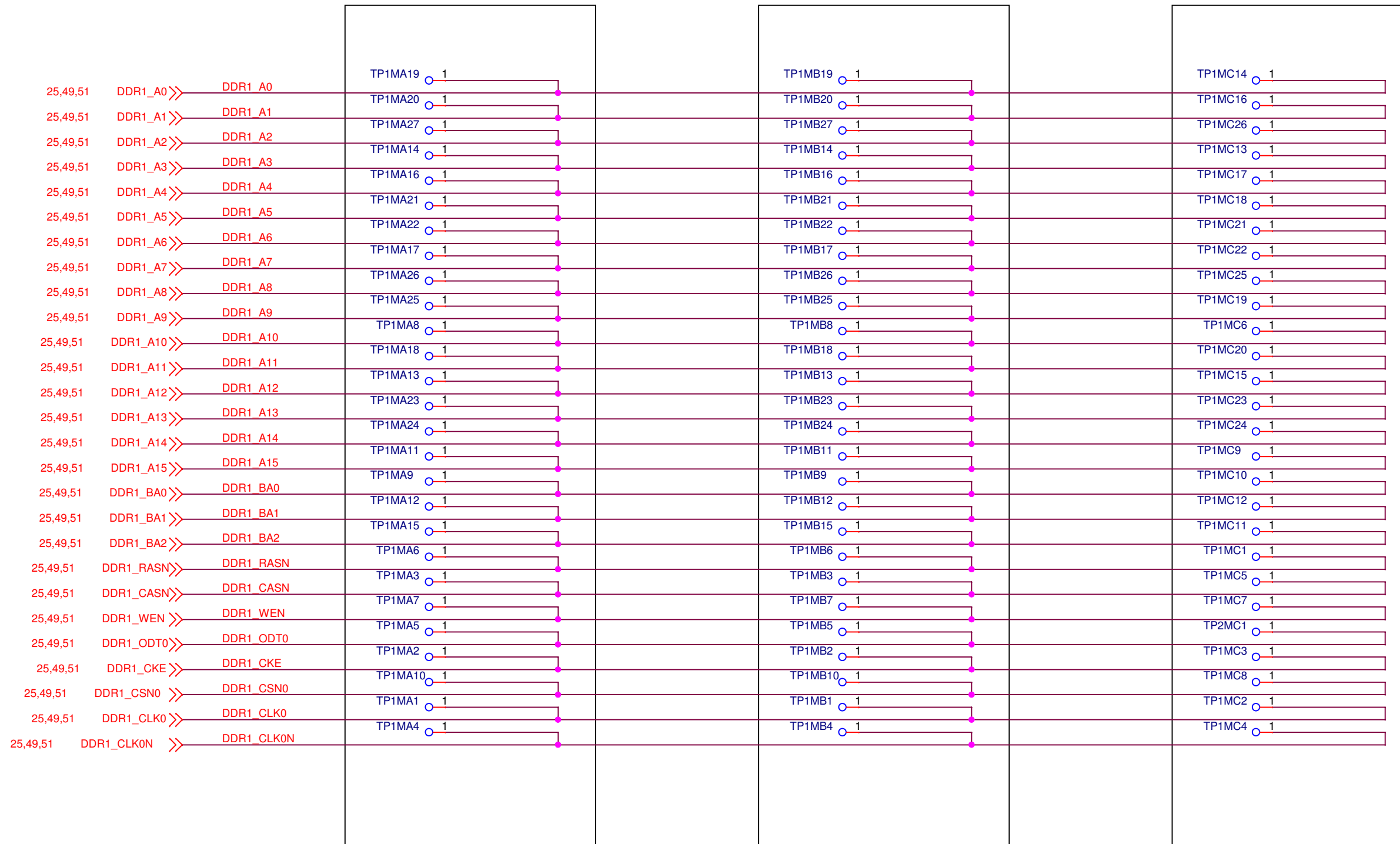


CAPACITANCE	SIZE
.1uF	0201
.22uF	0201
.47uF	0201
1uF	0201
2.2uF	0402
4.7uF	0402
10uF	0402
22uF	0603

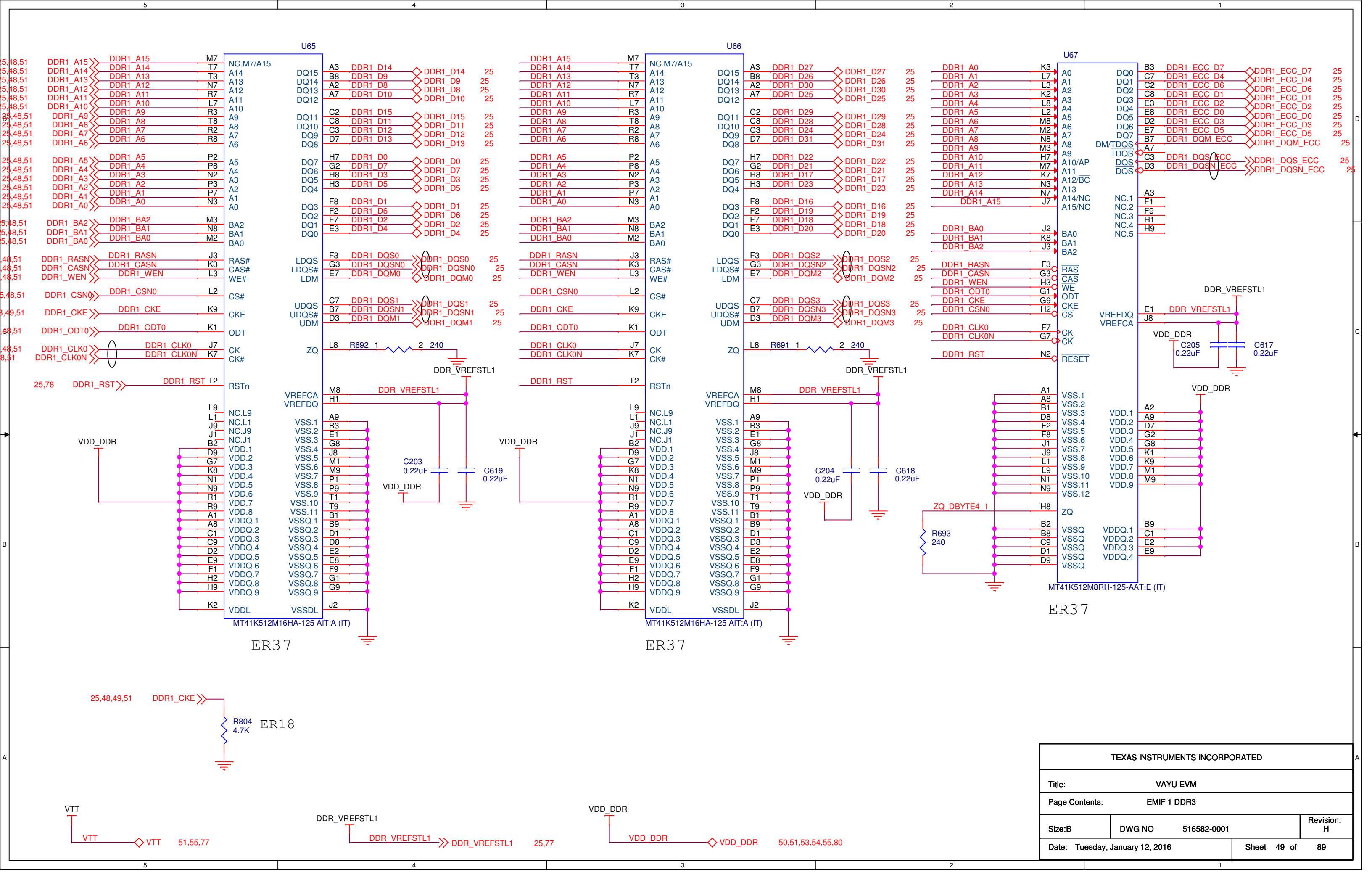
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: CORE POWERS			
Size: B	DWG NO	516582-0001	Revision: A
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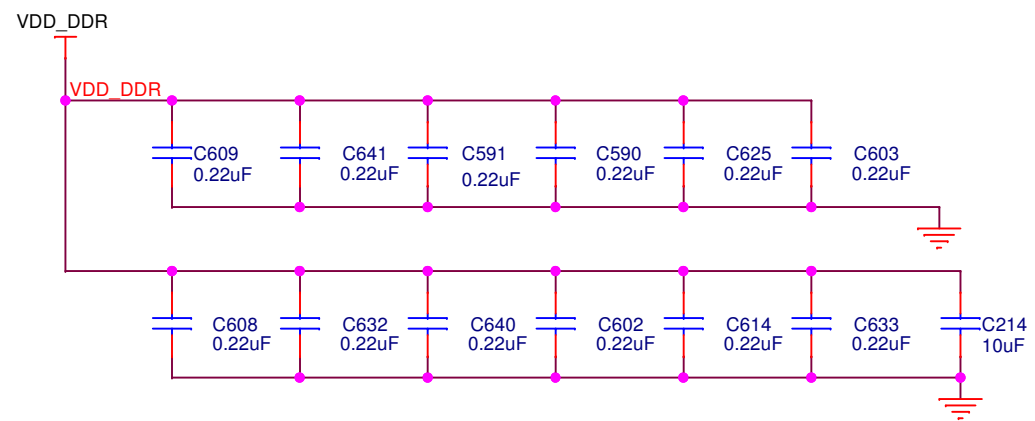
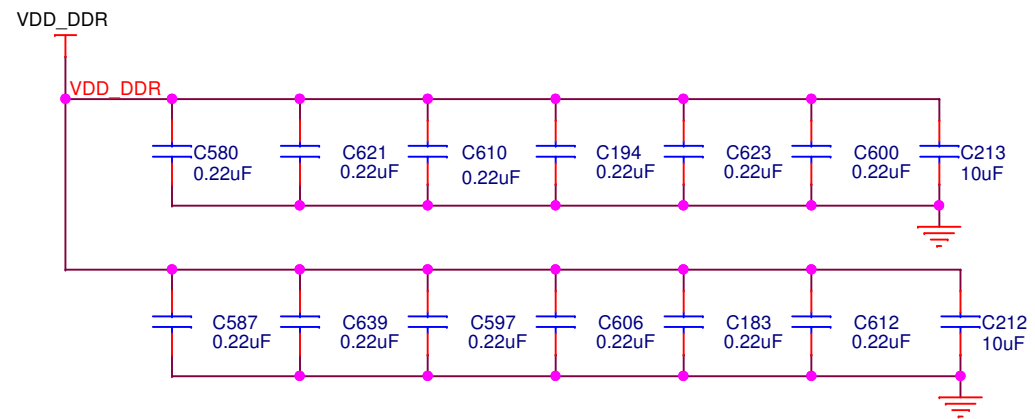
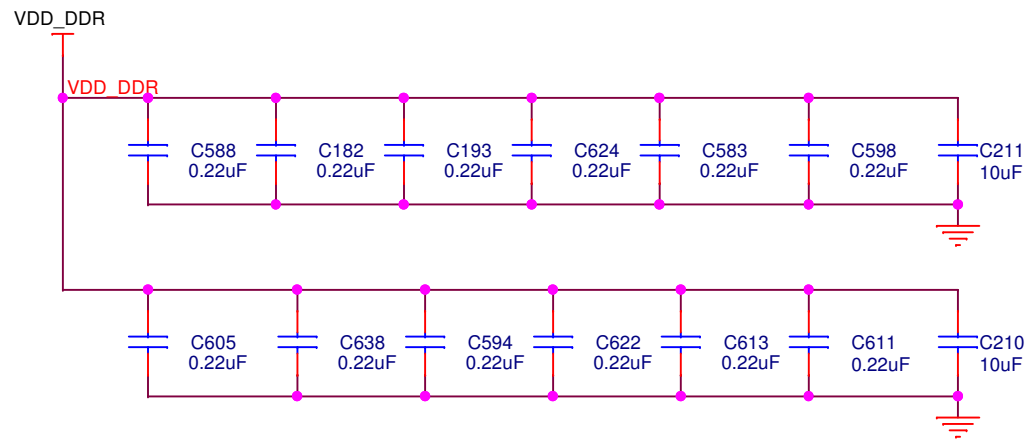
TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		GROUND PINS	
Size: B	DWG NO	516582-0001	Revision: A
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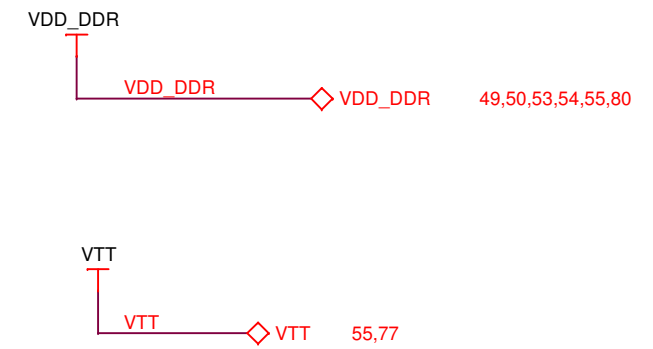
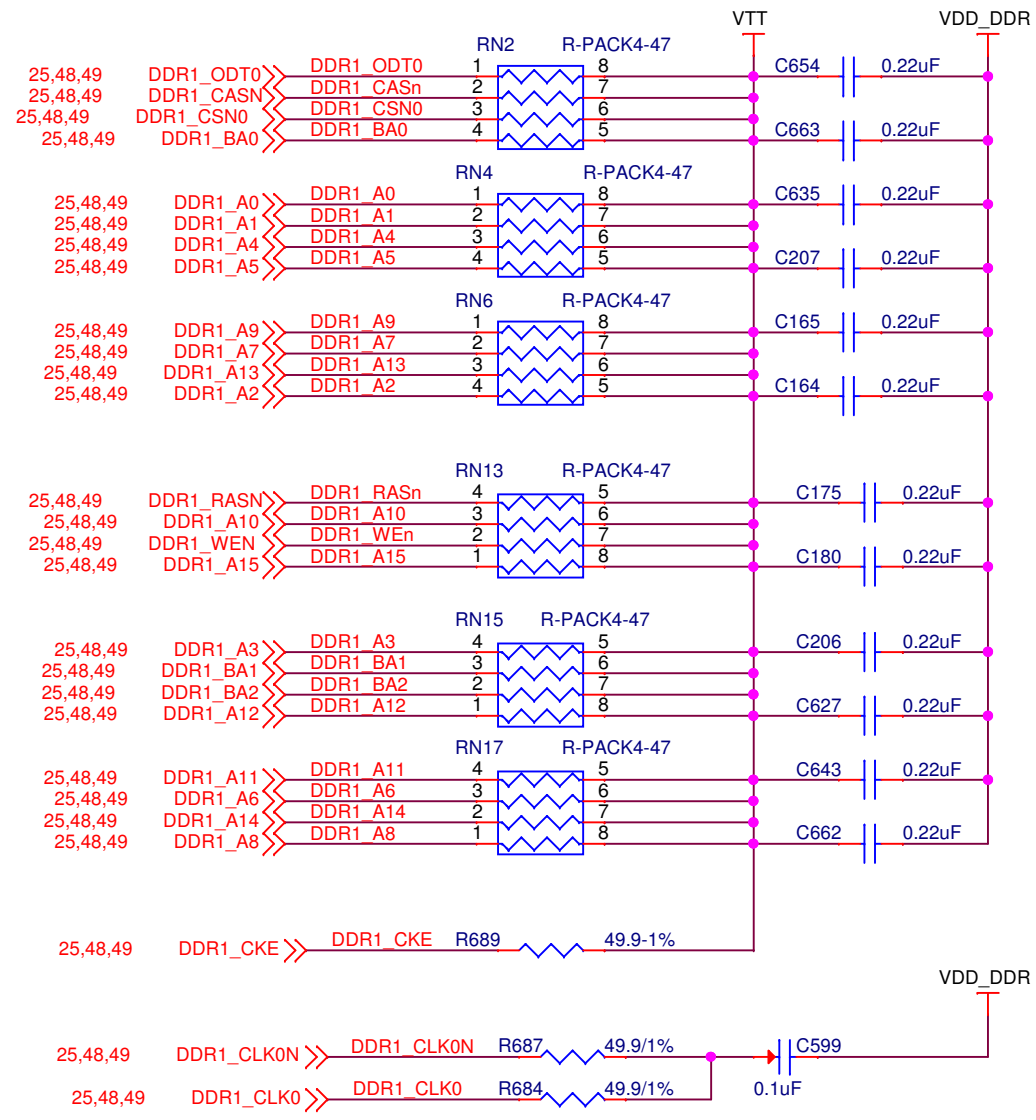
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EMIF 1 DDR3 TESTPOINTS			
Size: B	DWG NO	516582-0001	Revision: A
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TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EMIF 1 DDR3			
Size: B	DWG NO	516582-0001	Revision: H
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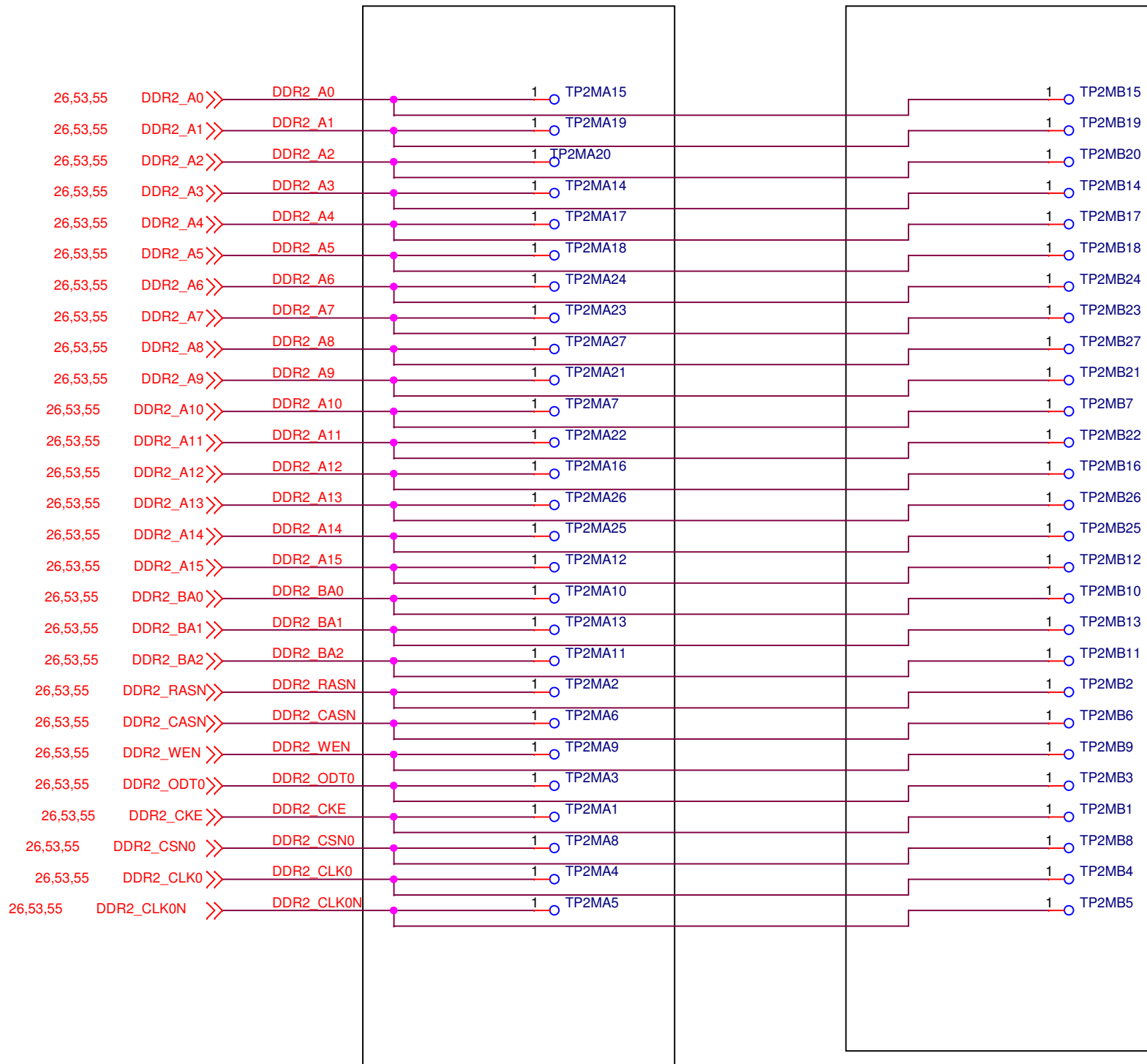
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EMIF 1 DDR3 CAPACITORS			
Size: B	DWG NO	516582-0001	Revision: A
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TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EMIF 1 DDR3 TERMINATION			
Size: B	DWG NO	516582-0001	Revision: A
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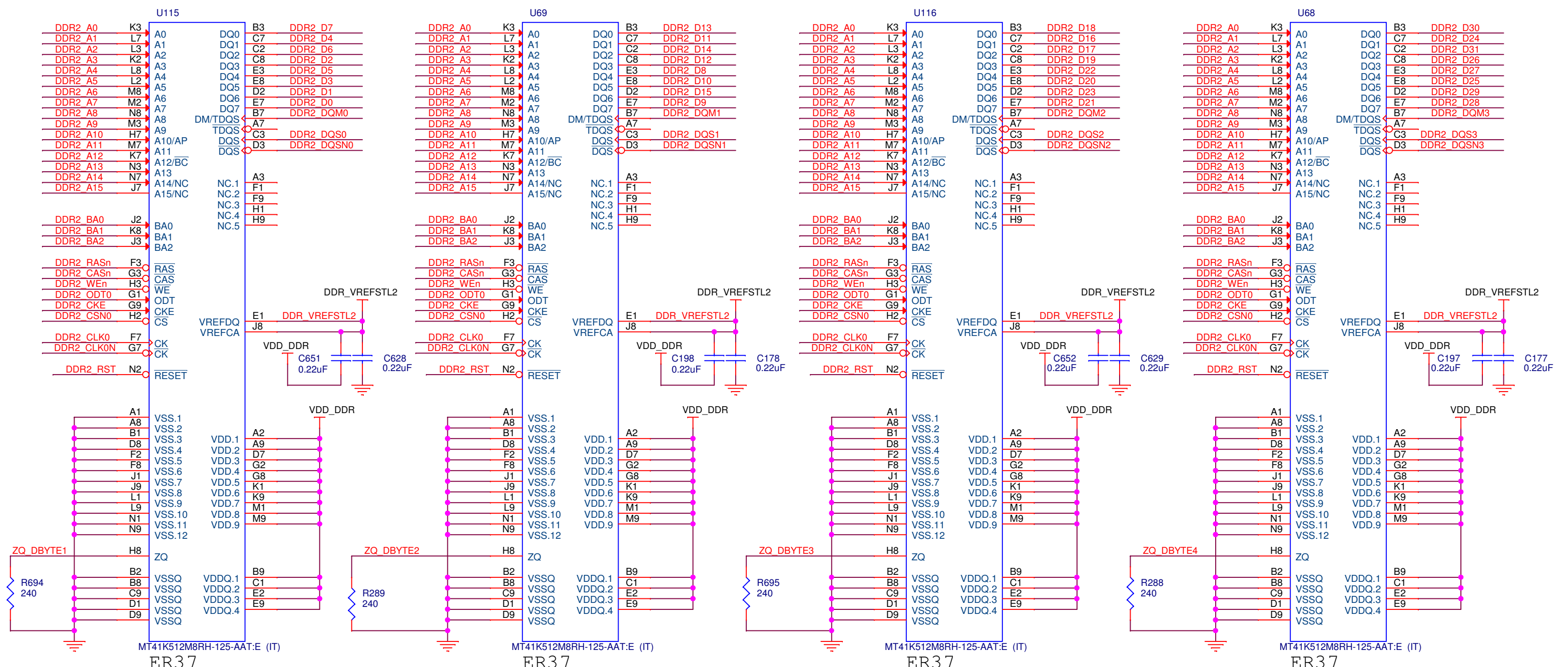
MEMORY 1
MEMORY 2

MEMORY 3
MEMORY 4



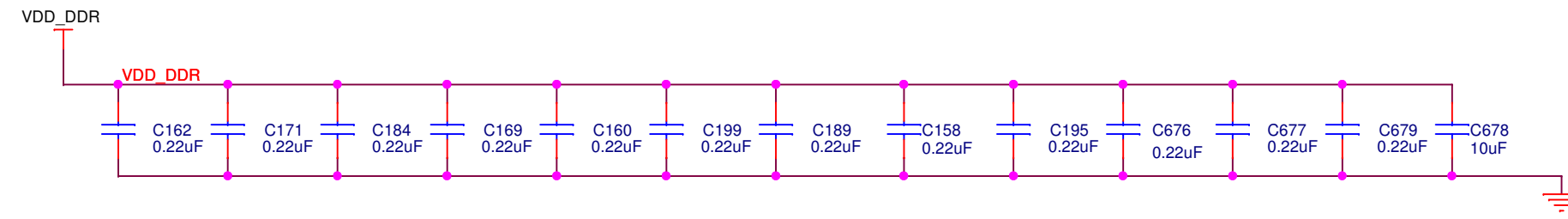
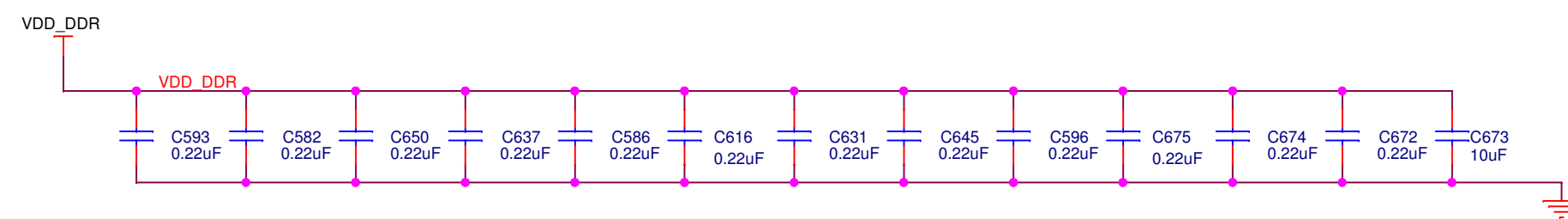
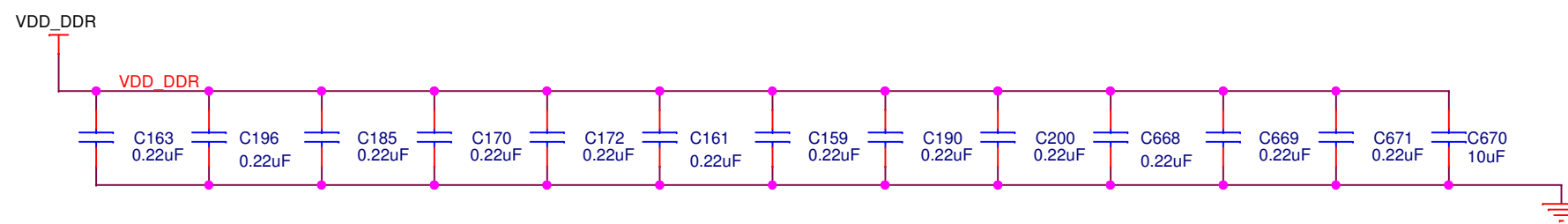
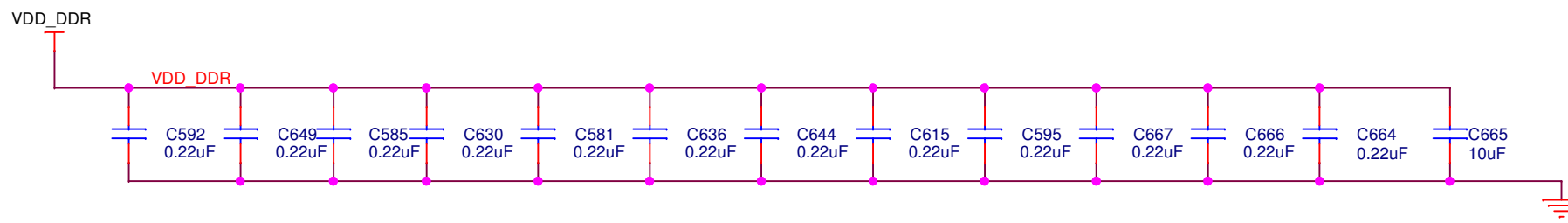
This section is an outline of vias labeled as Testpoints in the schematic. This allows us to determine pwb line lengths for memory to memory and CPU to memory it is purely a visibility tool no actual "component" is used the vias are just replaced with a via that is labeled a test point

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: TEST POINTS EMIF 2			
Size: B	DWG NO	516582-0001	Revision: A
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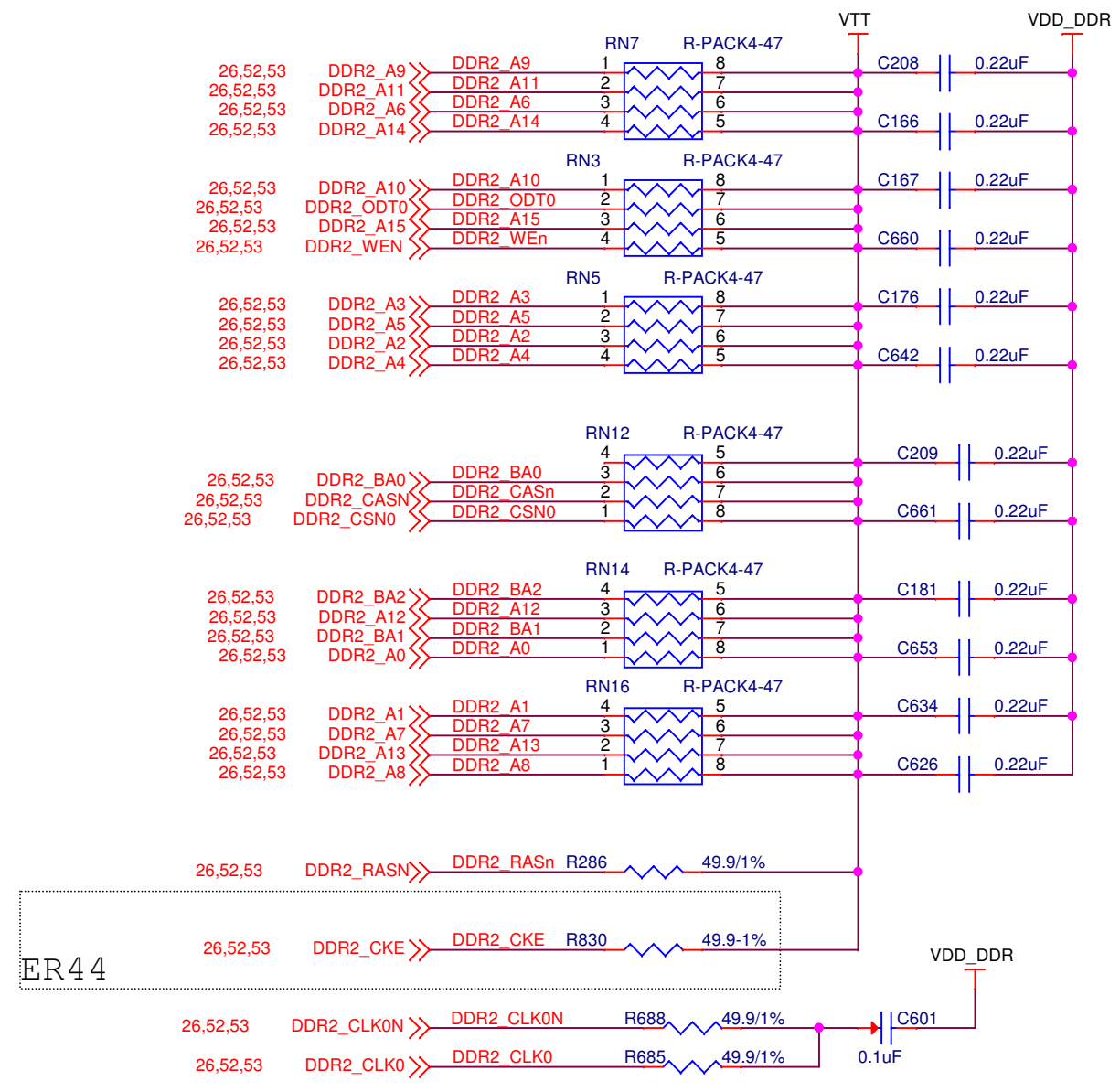
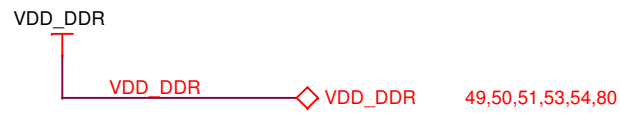


26,52,55	DDR2_A0	DDR2_A0	26,52,55	DDR2_D0	DDR2_D0	26	DDR2_D16	DDR2_D16	26	DDR2_D16	DDR2_D16
26,52,55	DDR2_A1	DDR2_A1	26,52,55	DDR2_D1	DDR2_D1	26	DDR2_D17	DDR2_D17	26	DDR2_D17	DDR2_D17
26,52,55	DDR2_A2	DDR2_A2	26,52,55	DDR2_D2	DDR2_D2	26	DDR2_D18	DDR2_D18	26	DDR2_D18	DDR2_D18
26,52,55	DDR2_A3	DDR2_A3	26,52,55	DDR2_D3	DDR2_D3	26	DDR2_D19	DDR2_D19	26	DDR2_D19	DDR2_D19
26,52,55	DDR2_A4	DDR2_A4	26,52,55	DDR2_D4	DDR2_D4	26	DDR2_D20	DDR2_D20	26	DDR2_D20	DDR2_D20
26,52,55	DDR2_A5	DDR2_A5	26,52,53,55	DDR2_D5	DDR2_D5	26	DDR2_D21	DDR2_D21	26	DDR2_D21	DDR2_D21
26,52,55	DDR2_A6	DDR2_A6	26,52,53,55	DDR2_D6	DDR2_D6	26	DDR2_D22	DDR2_D22	26	DDR2_D22	DDR2_D22
26,52,55	DDR2_A7	DDR2_A7	26,52,55	DDR2_D7	DDR2_D7	26	DDR2_D23	DDR2_D23	26	DDR2_D23	DDR2_D23
26,52,55	DDR2_A8	DDR2_A8	26,52,55	DDR2_D8	DDR2_D8	26	DDR2_D24	DDR2_D24	26	DDR2_D24	DDR2_D24
26,52,55	DDR2_A9	DDR2_A9	26,52,55	DDR2_D9	DDR2_D9	26	DDR2_D25	DDR2_D25	26	DDR2_D25	DDR2_D25
26,52,55	DDR2_A10	DDR2_A10	26,52,55	DDR2_D10	DDR2_D10	26	DDR2_D26	DDR2_D26	26	DDR2_D26	DDR2_D26
26,52,55	DDR2_A11	DDR2_A11	26,52,55	DDR2_D11	DDR2_D11	26	DDR2_D27	DDR2_D27	26	DDR2_D27	DDR2_D27
26,52,55	DDR2_A12	DDR2_A12	26,52,55	DDR2_D12	DDR2_D12	26	DDR2_D28	DDR2_D28	26	DDR2_D28	DDR2_D28
26,52,55	DDR2_A13	DDR2_A13	26,52,55	DDR2_D13	DDR2_D13	26	DDR2_D29	DDR2_D29	26	DDR2_D29	DDR2_D29
26,52,55	DDR2_A14	DDR2_A14	26,52,55	DDR2_D14	DDR2_D14	26	DDR2_D30	DDR2_D30	26	DDR2_D30	DDR2_D30
26,52,55	DDR2_A15	DDR2_A15	26,52,55	DDR2_D15	DDR2_D15	26	DDR2_D31	DDR2_D31	26	DDR2_D31	DDR2_D31
26,52,55	DDR2_BA0	DDR2_BA0	26	DDR2_DQM0	DDR2_DQM0	26	DDR2_DQM2	DDR2_DQM2	26	DDR2_DQM2	DDR2_DQM2
26,52,55	DDR2_BA1	DDR2_BA1	26	DDR2_DQS0	DDR2_DQS0	26	DDR2_DQS2	DDR2_DQS2	26	DDR2_DQS2	DDR2_DQS2
26,52,55	DDR2_BA2	DDR2_BA2	26	DDR2_DQS0	DDR2_DQS0	26	DDR2_DQS2	DDR2_DQS2	26	DDR2_DQS2	DDR2_DQS2
26,78	DDR2_RST	DDR2_RST	26	DDR2_DQM1	DDR2_DQM1	26	DDR2_DQM3	DDR2_DQM3	26	DDR2_DQM3	DDR2_DQM3
			26	DDR2_DQS1	DDR2_DQS1	26	DDR2_DQS3	DDR2_DQS3	26	DDR2_DQS3	DDR2_DQS3
			26	DDR2_DQS1	DDR2_DQS1	26	DDR2_DQS3	DDR2_DQS3	26	DDR2_DQS3	DDR2_DQS3
			26	DDR2_DQS1	DDR2_DQS1	26	DDR2_DQS3	DDR2_DQS3	26	DDR2_DQS3	DDR2_DQS3

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EMIF 2 DDR3 MEMORIES			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016	Sheet 53 of 89		

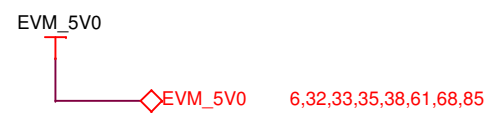
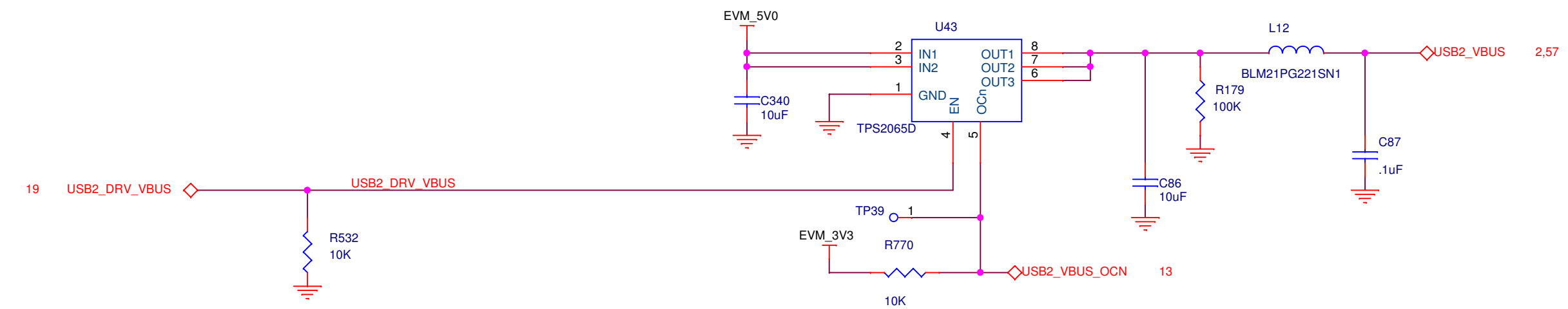
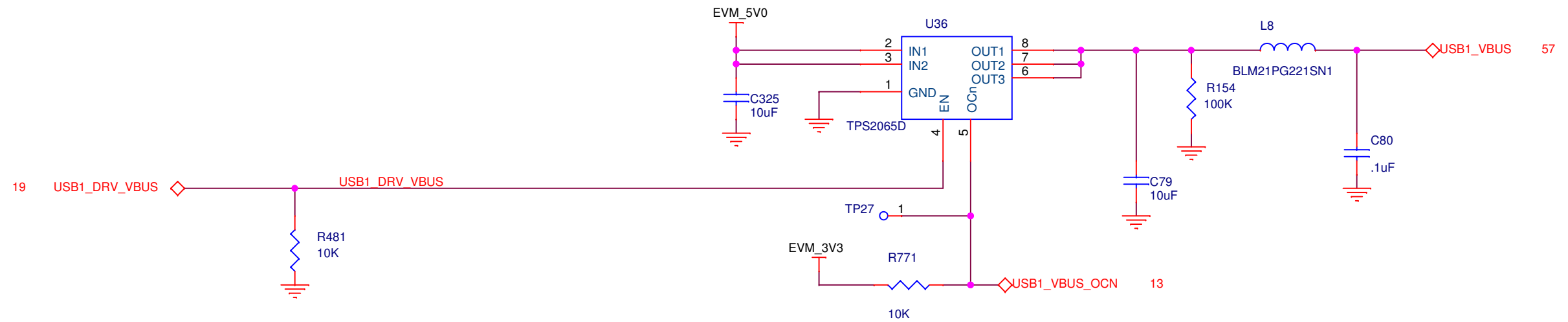


TEXAS INSTRUMENTS INCORPORATED		
Title: VAYU EVM		
Page Contents: EMIF 2 DDR3 CAPACITORS		
Size: B	DWG NO 516582-0001	Revision: A
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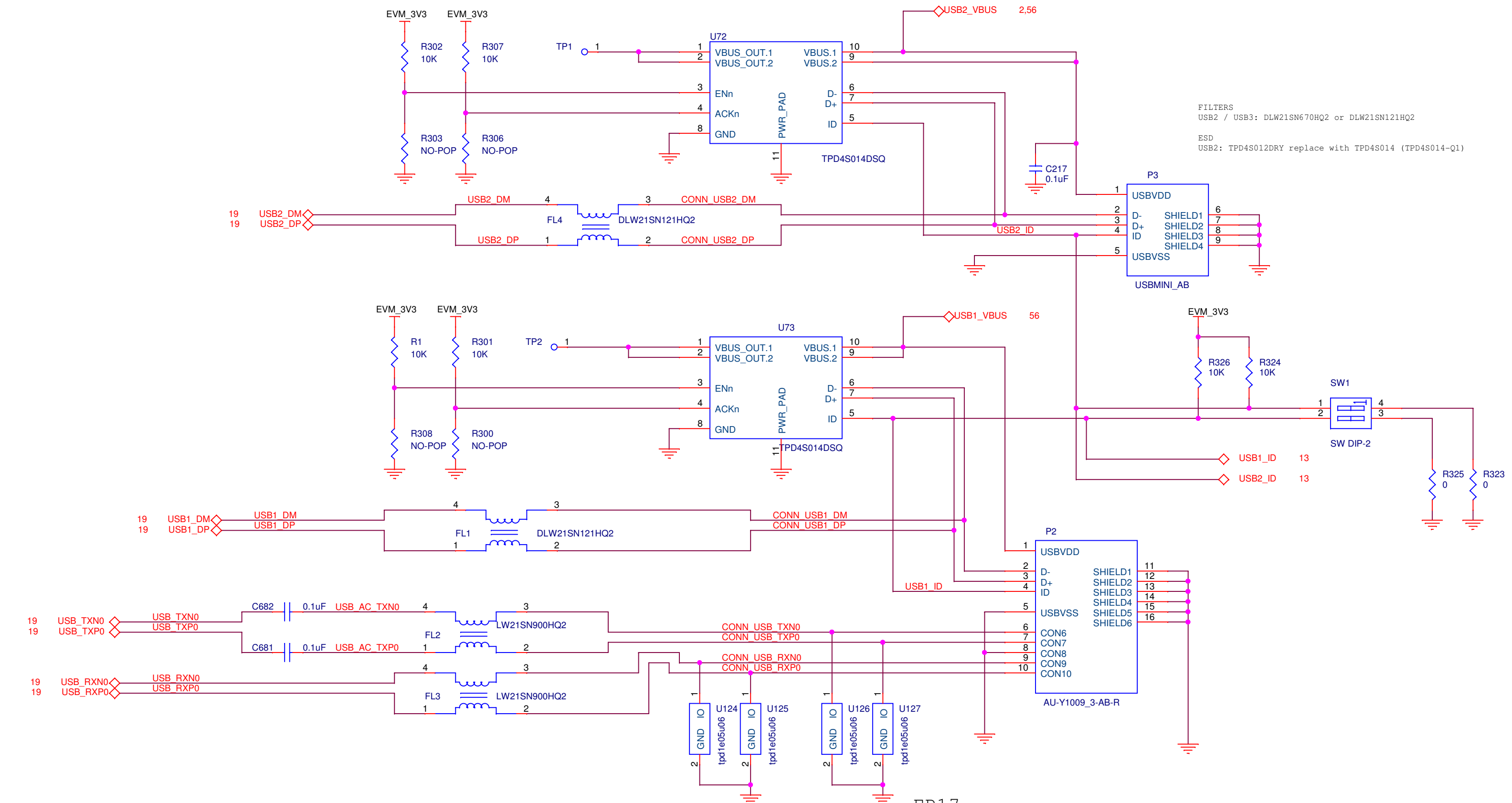


ER44

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: EMIF 2 DDR3 TERMINATION			
Size: B	DWG NO	516582-0001	Revision: H
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TEXAS INSTRUMENTS INCORPORATED		
Title: VAYU EVM		
Page Contents: USB VBUS DRIVERS		
Size: B	DWG NO 516582-0001	Revision: C
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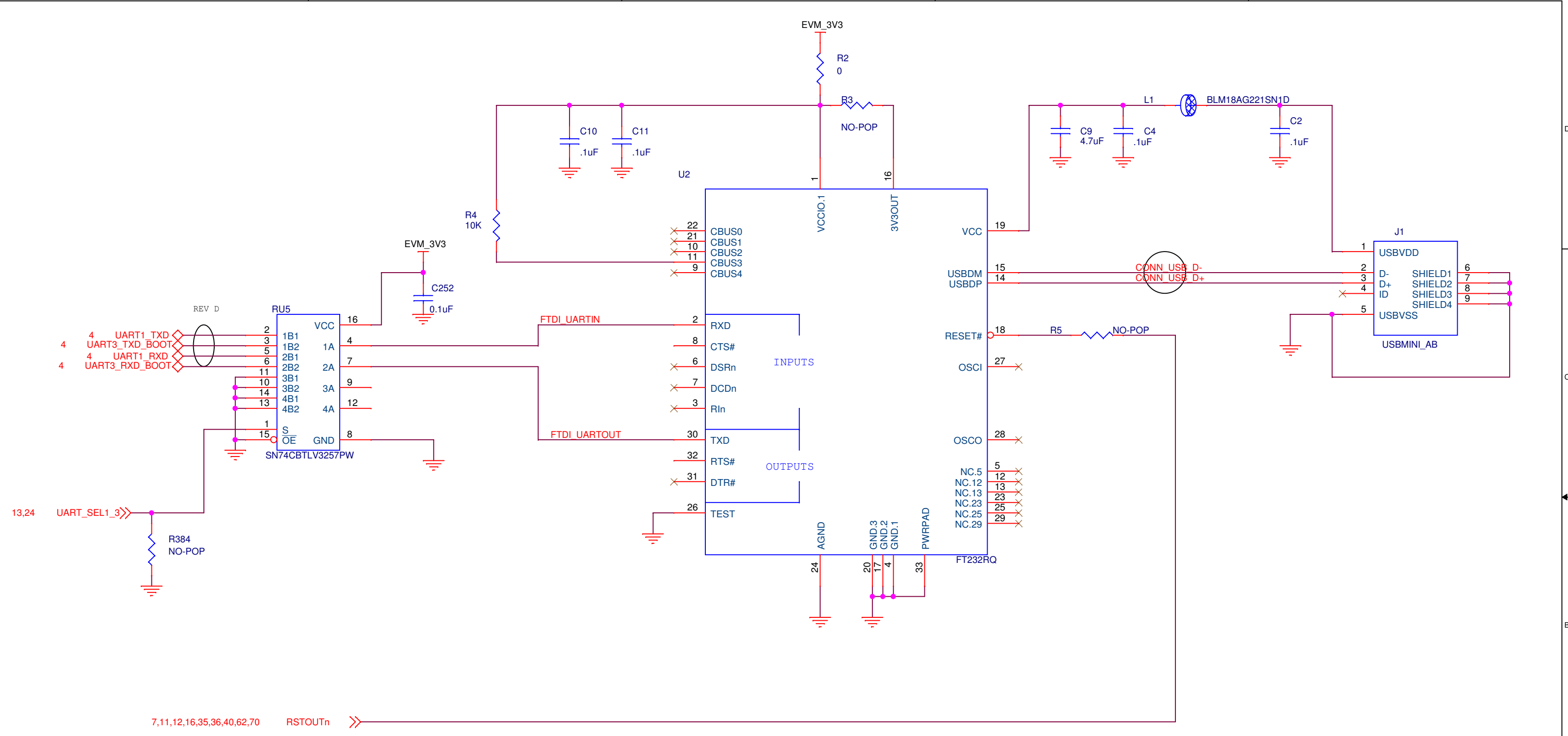
FILTERS
 USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2
 ESD
 USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)

FILTERS
 USB2 / USB3: DLW21SN670HQ2 or DLW21SN121HQ2
 ESD
 USB2: TPD4S012DRY replace with TPD4S014 (TPD4S014-Q1)
 USB3: TPD4EUSB30 replace with two TPD2EUSB30 (TPD2EUSB30-Q1) in drt package

TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		USB CONNECTORS	
Size: B	DWG NO	516582-0001	Revision: F
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EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,58,59,60,63,64,65,67,68,85,86

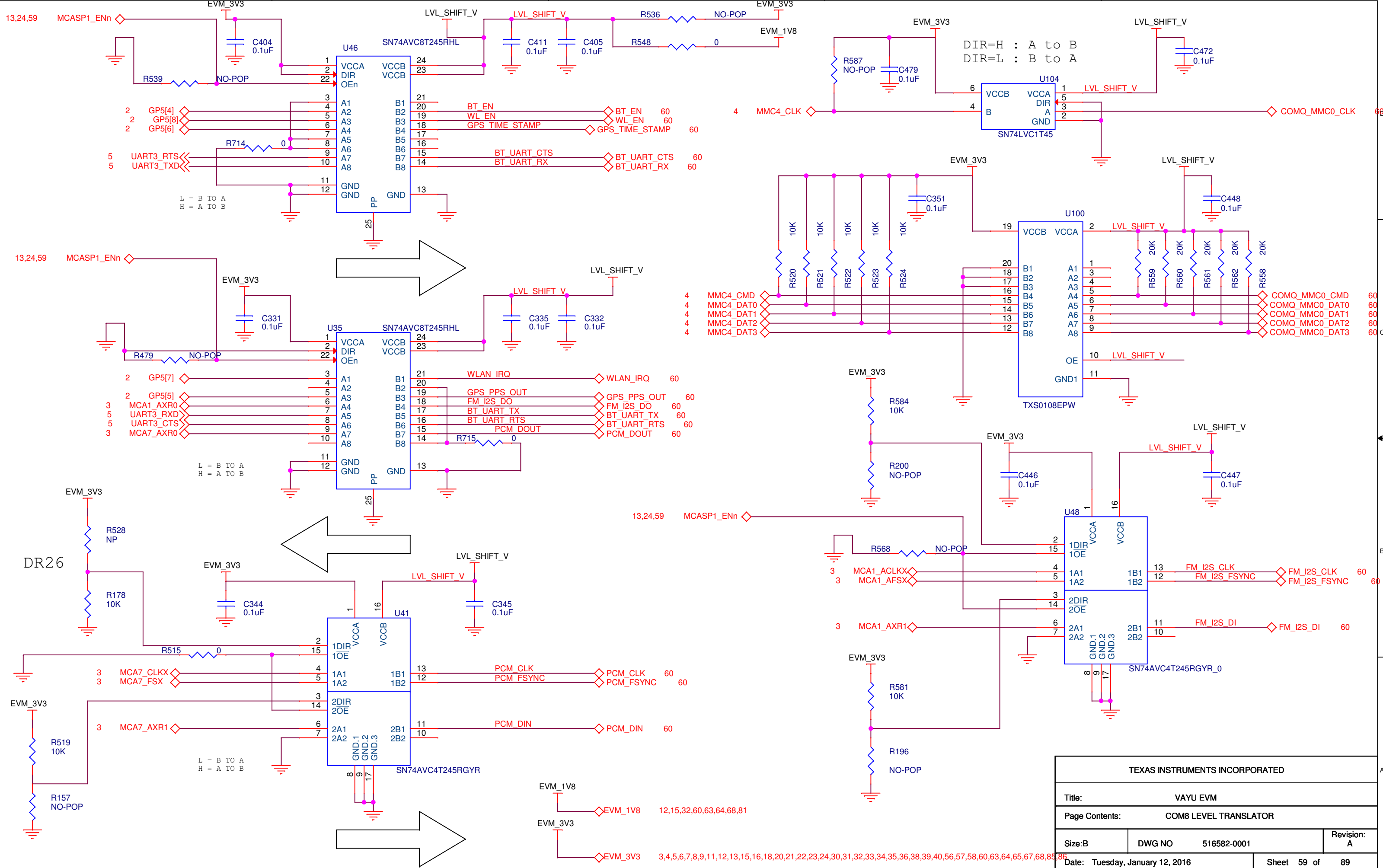
ER17



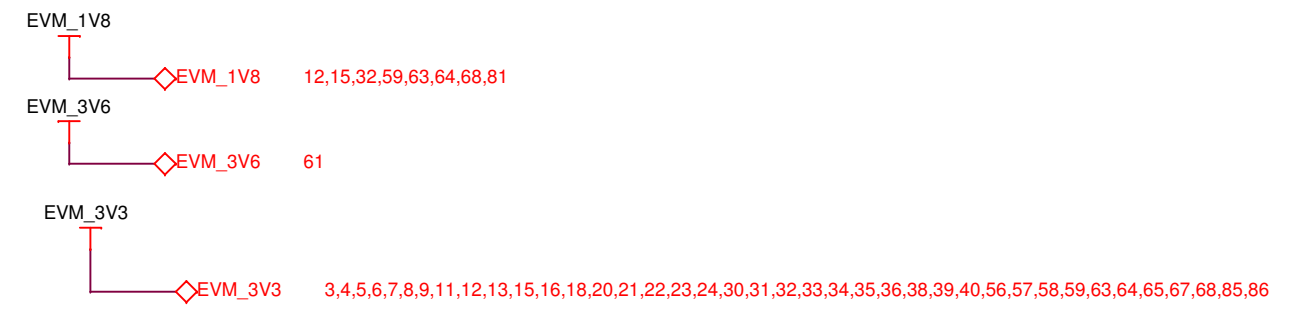
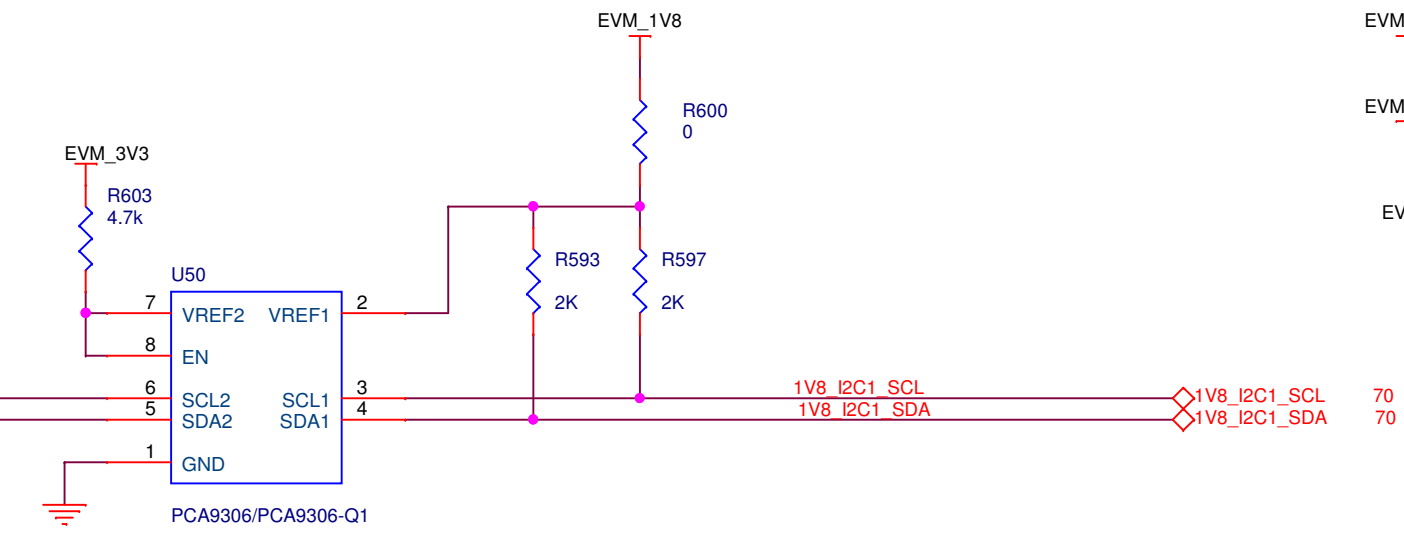
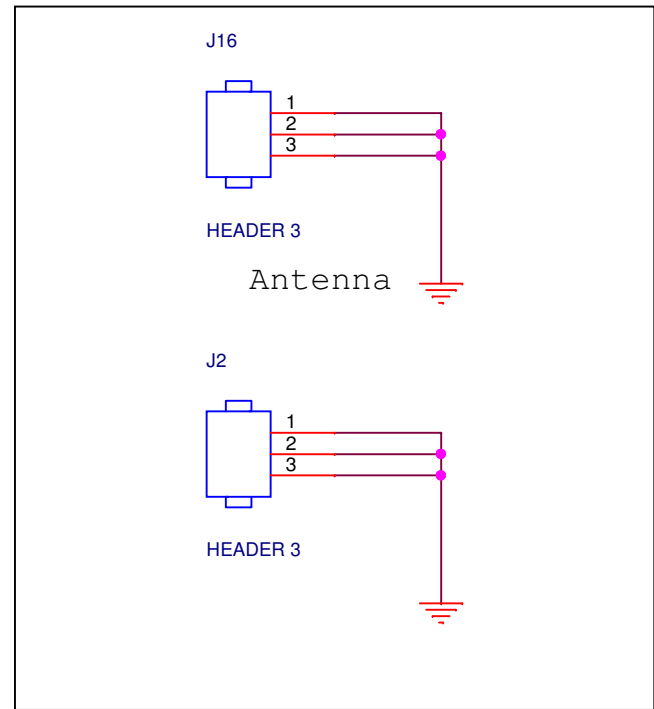
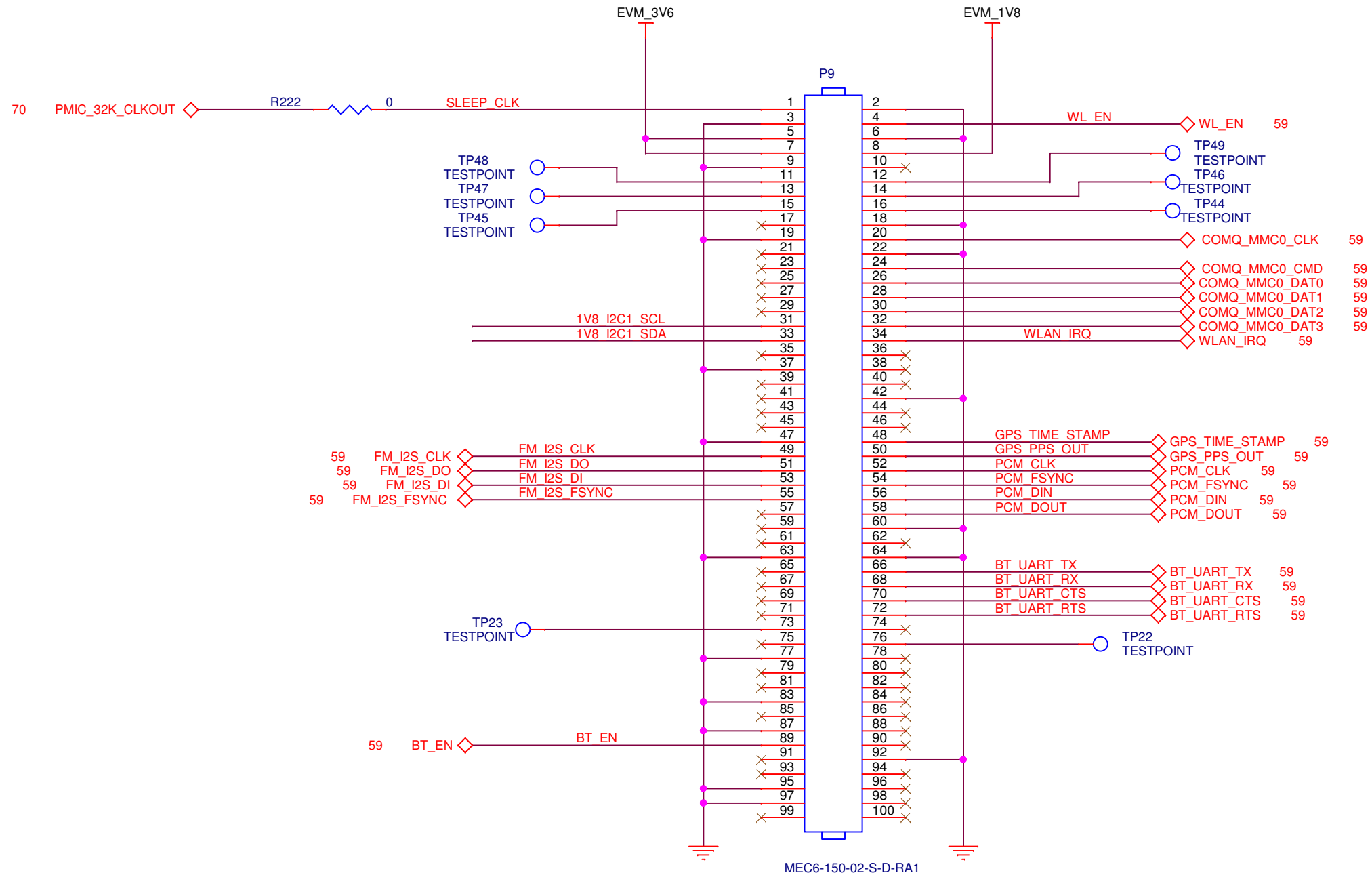
7,11,12,16,35,36,40,62,70 RSTOUTn >>

EVM_3V3
 EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,59,60,63,64,65,67,68,85,86
 EVM_5V0
 EVM_5V0 6,32,33,35,38,56,61,68,85

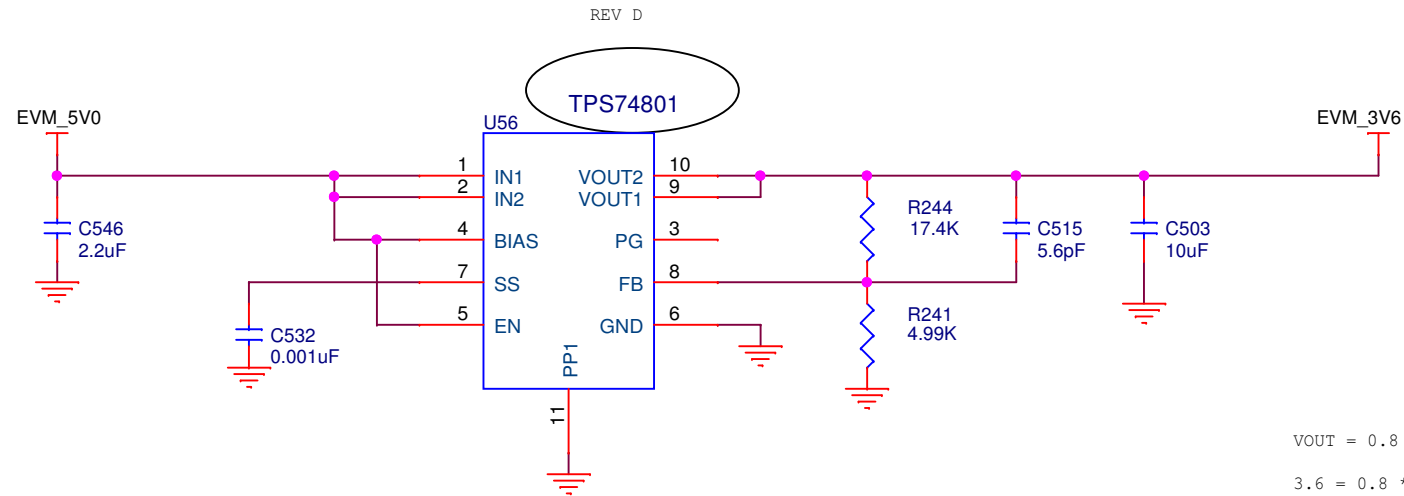
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: FTDI UART			
Size: B	DWG NO	516582-0001	Revision: D
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TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: COM8 LEVEL TRANSLATOR			
Size: B	DWG NO	516582-0001	Revision: A
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TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: COM8 CONNECTOR			
Size: B	DWG NO	516582-0001	Revision: A
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$$V_{OUT} = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

$$3.6 = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

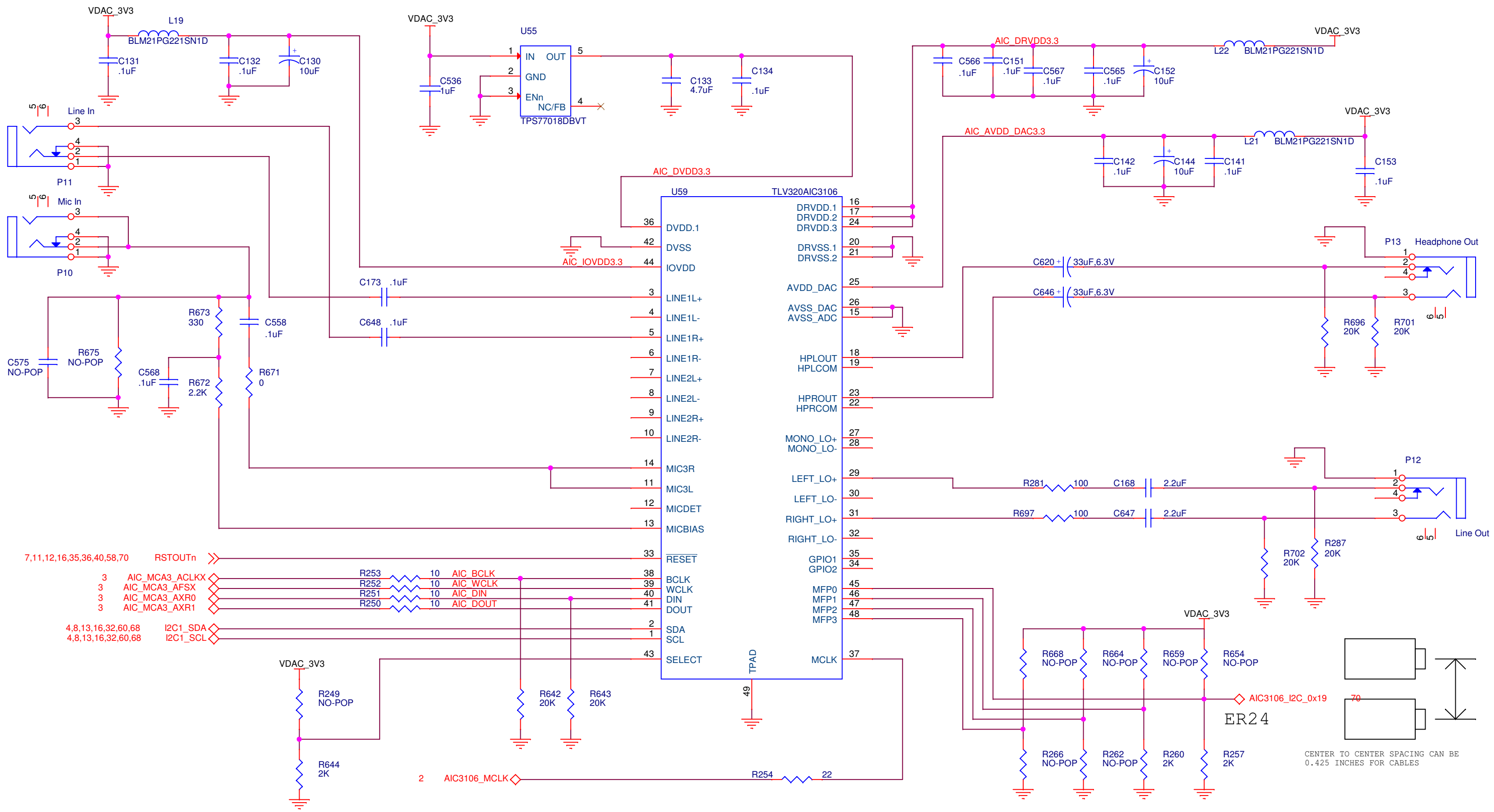
$$4.5 = (1 + (R_{TOP}/R_{BOTTOM}))$$

$$3.5 = ((R_{TOP}/R_{BOTTOM}))$$

$$3.5 R_{BOTTOM} = R_{TOP}$$

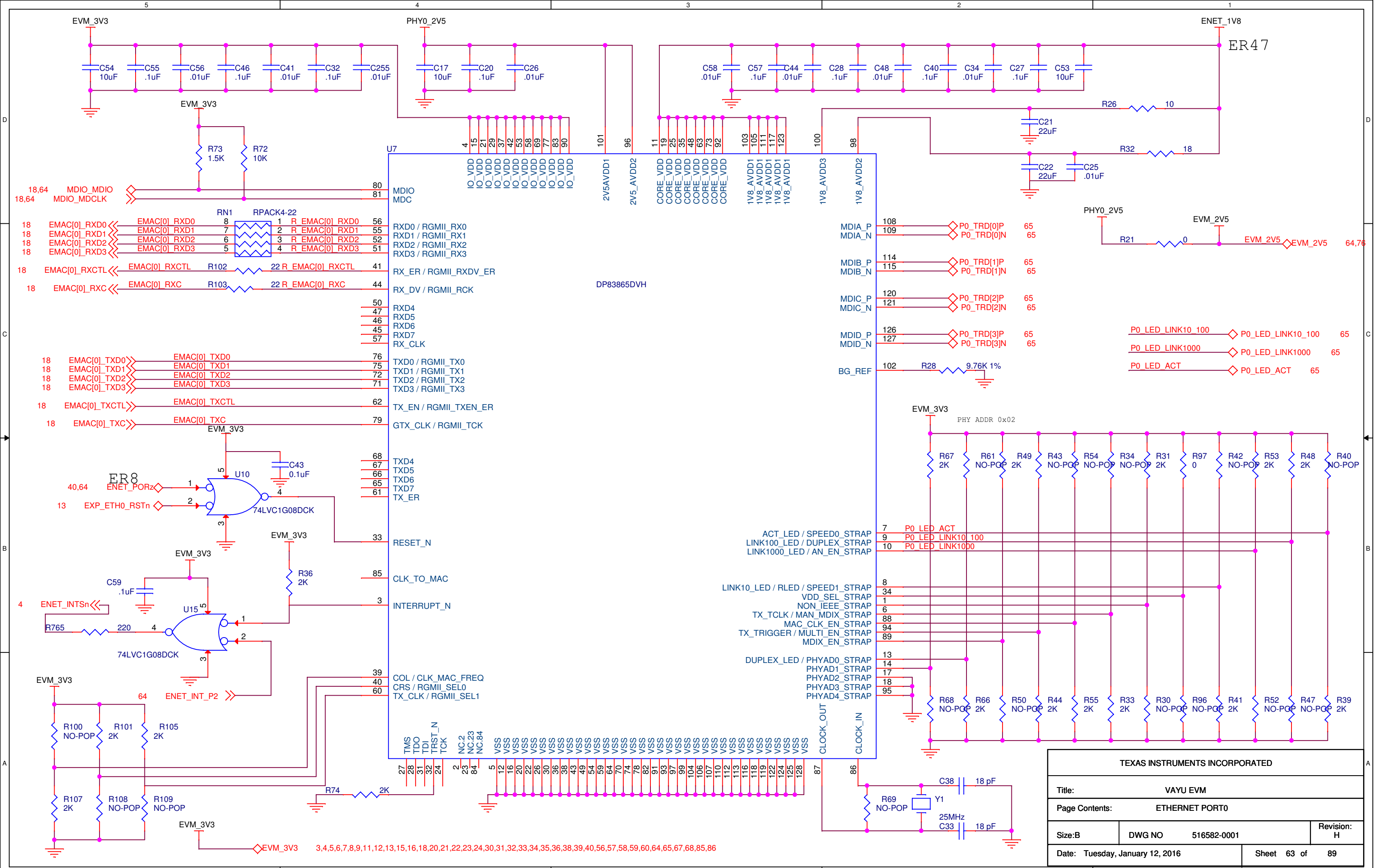


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: COM8 POWER			
Size: B	DWG NO	516582-0001	Revision: D
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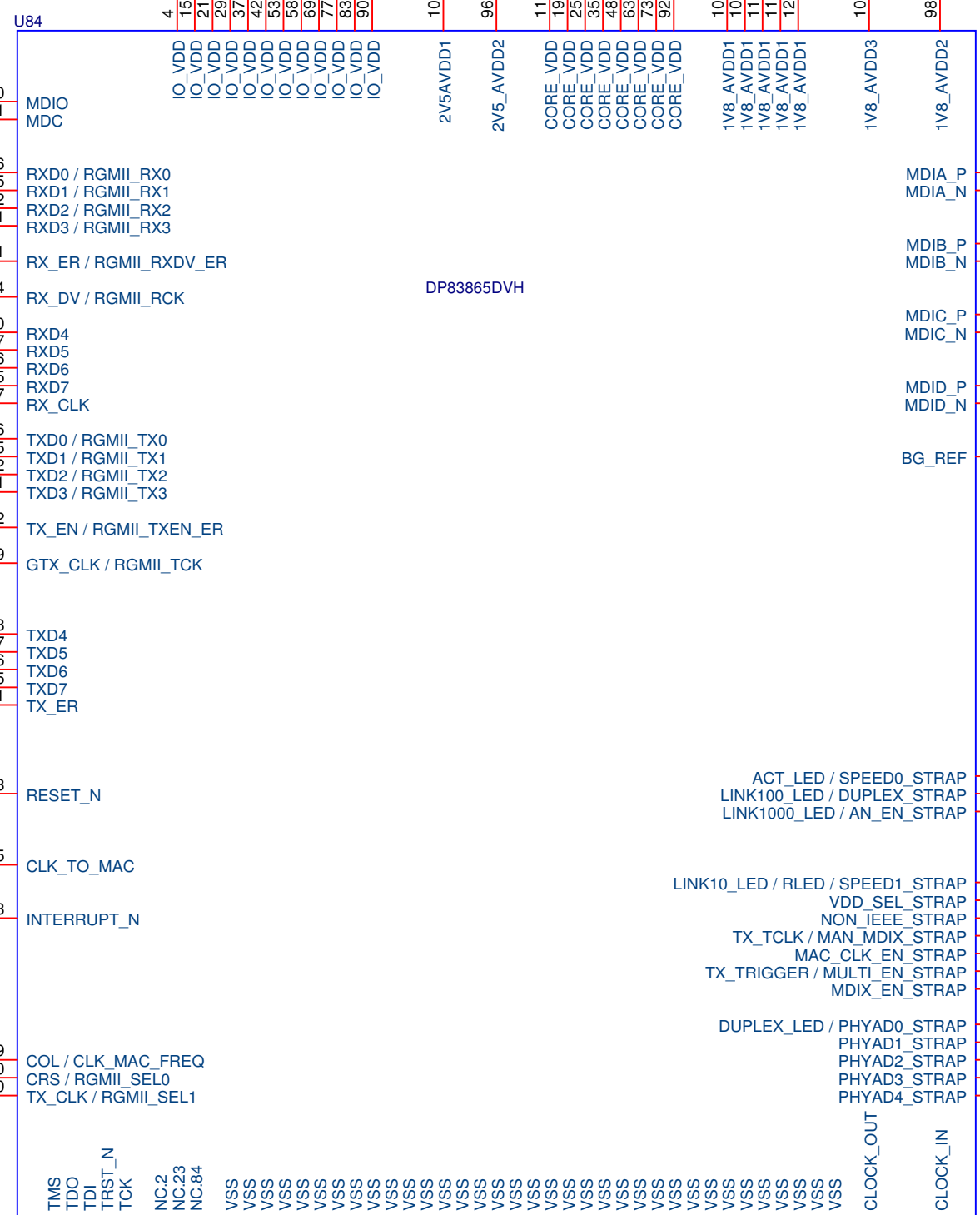
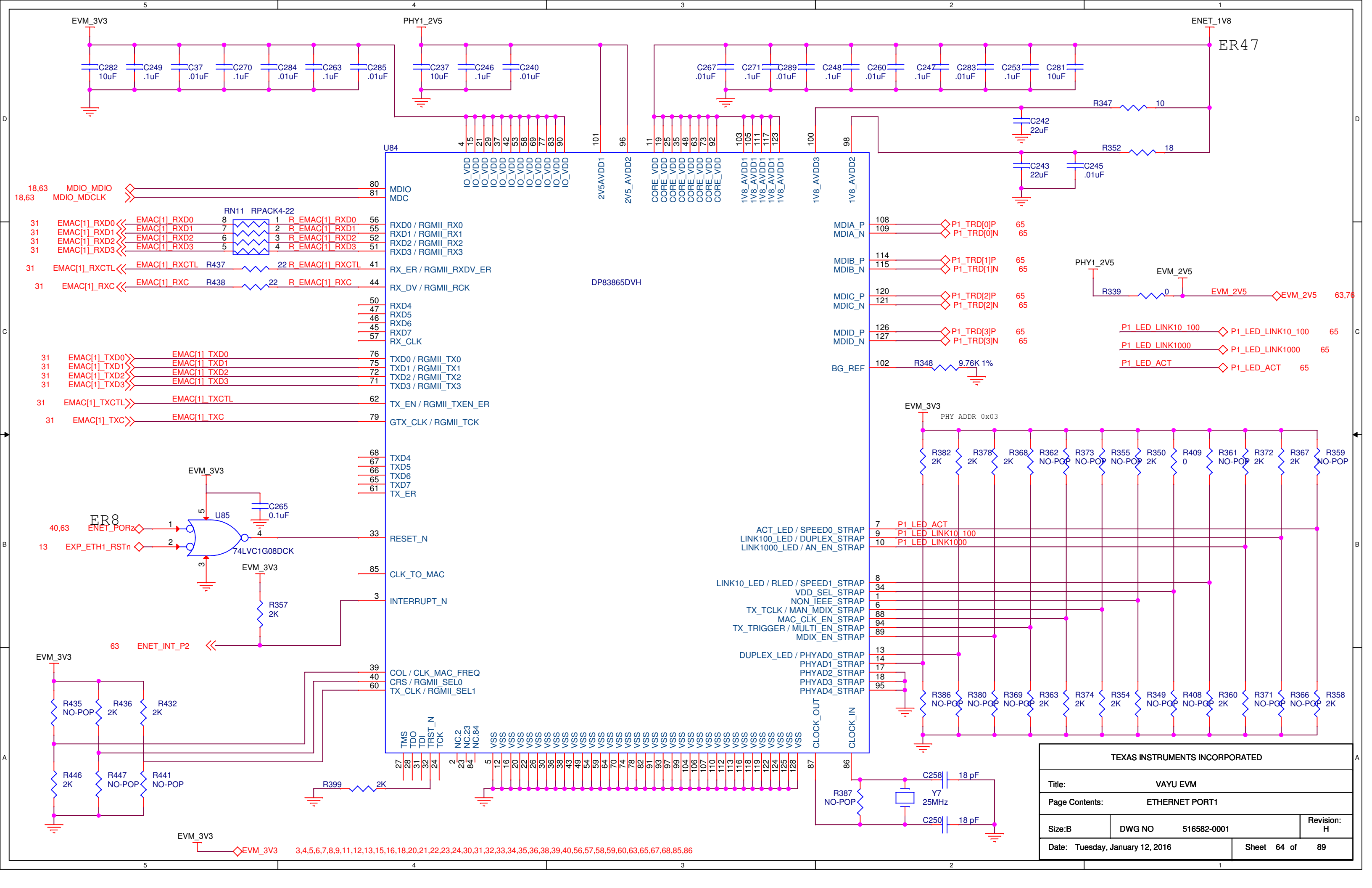
- 7,11,12,16,35,36,40,58,70 RSTOUTn >>
- 3 AIC_MCA3_ACLKX R253 10 AIC_BCLK
- 3 AIC_MCA3_AFSX R252 10 AIC_WCLK
- 3 AIC_MCA3_AXR0 R251 10 AIC_DIN
- 3 AIC_MCA3_AXR1 R250 10 AIC_DOUT
- 4,8,13,16,32,60,68 I2C1_SDA
- 4,8,13,16,32,60,68 I2C1_SCL

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: AIC3106 AUDIO INTERFACE			
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Title: VAYU EVM			
Page Contents: ETHERNET PORT0			
Size: B	DWG NO	516582-0001	Revision: H
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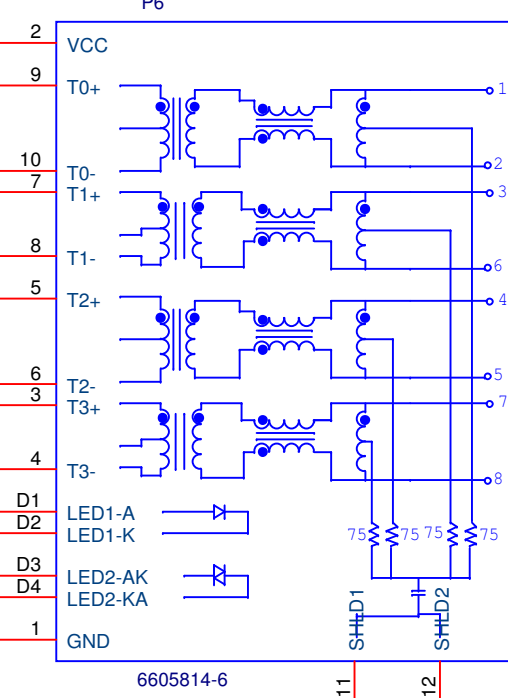
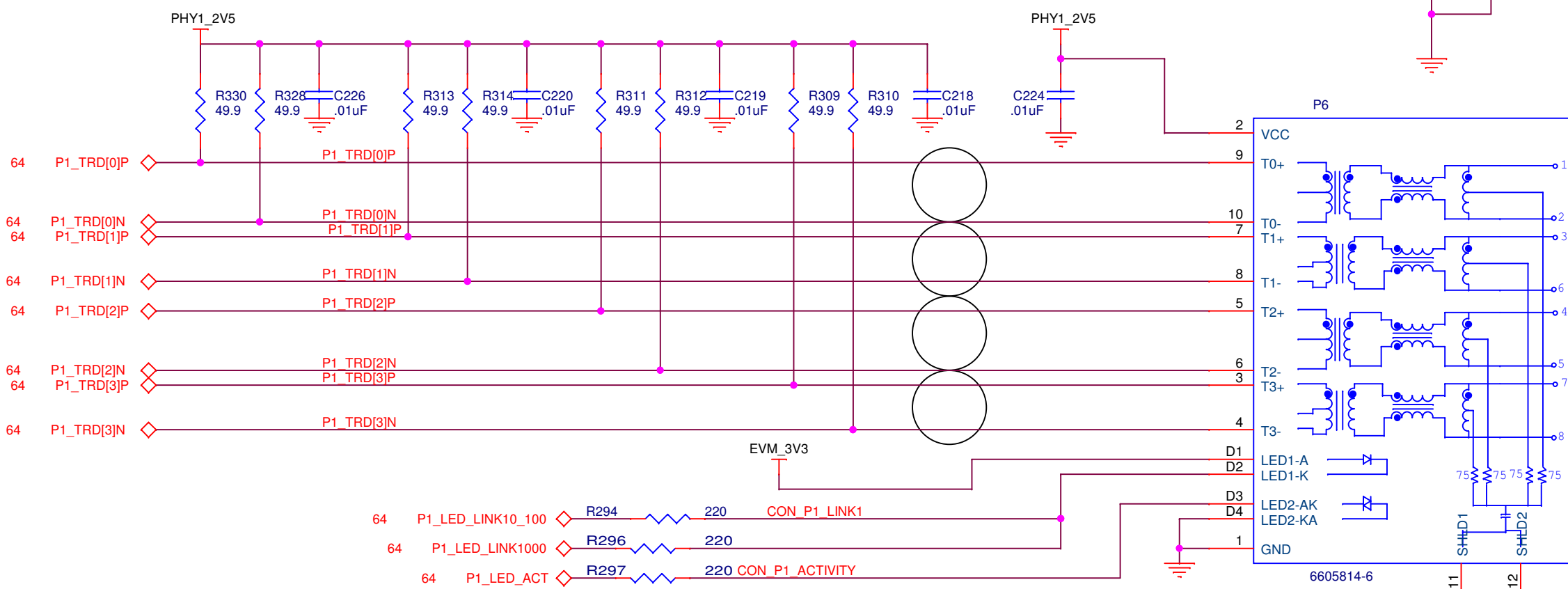
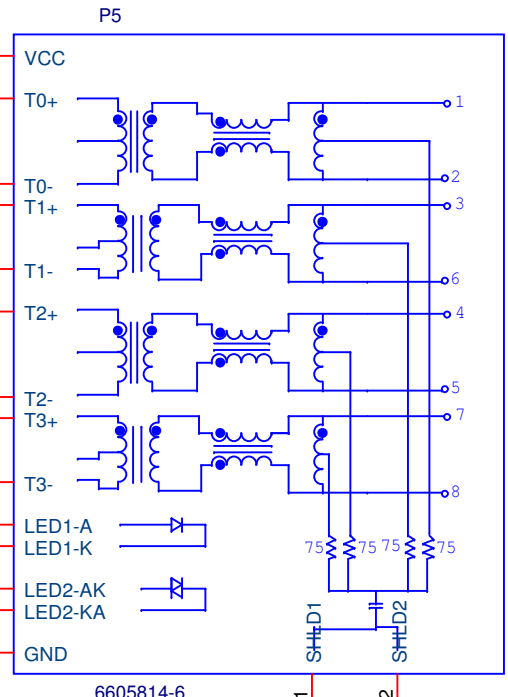
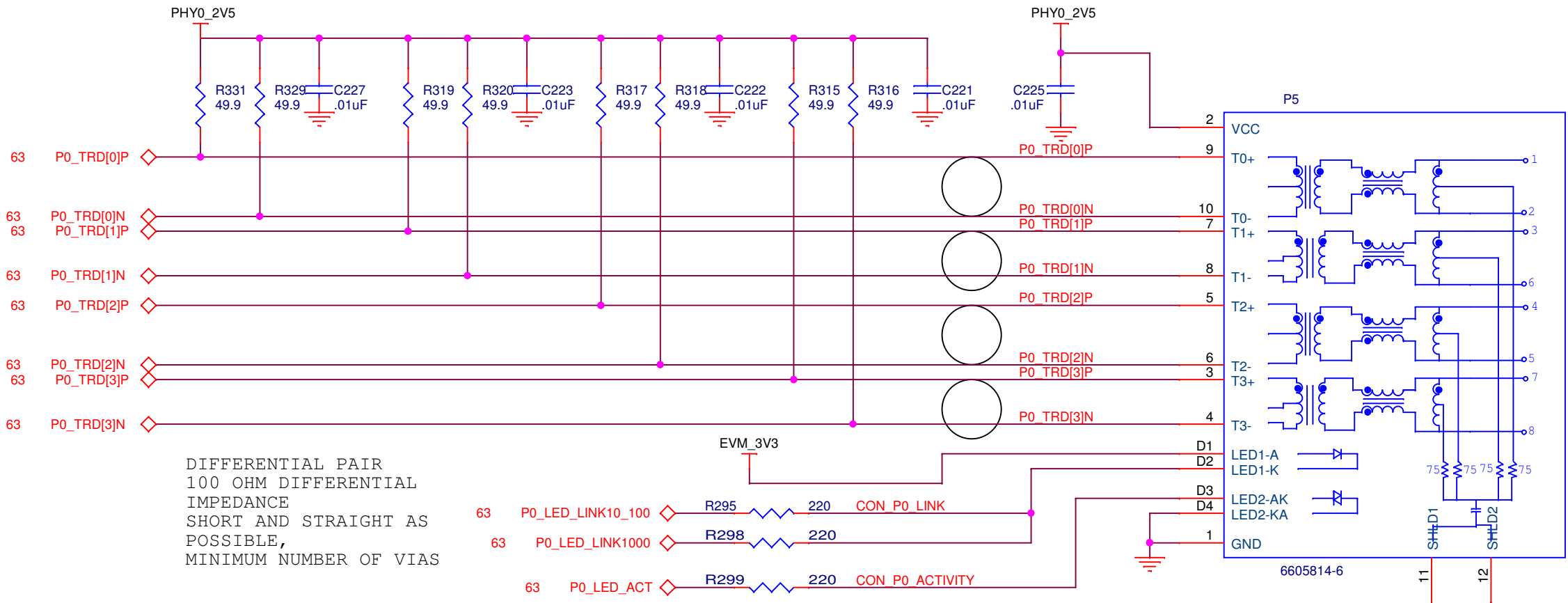
3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,64,65,67,68,85,86



- ACT_LED / SPEED0_STRAP 7
- LINK100_LED / DUPLEX_STRAP 9
- LINK1000_LED / AN_EN_STRAP 10
- LINK10_LED / RLED / SPEED1_STRAP 8
- VDD_SEL_STRAP 34
- NON_IEEE_STRAP 1
- TX_TCLK / MAN_MDIX_STRAP 6
- MAC_CLK_EN_STRAP 88
- TX_TRIGGER / MULTI_EN_STRAP 94
- MDIX_EN_STRAP 89
- DUPLEX_LED / PHYAD0_STRAP 13
- PHYAD1_STRAP 14
- PHYAD2_STRAP 17
- PHYAD3_STRAP 18
- PHYAD4_STRAP 95

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: ETHERNET PORT1			
Size: B	DWG NO	516582-0001	Revision: H
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EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,65,67,68,85,86



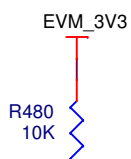
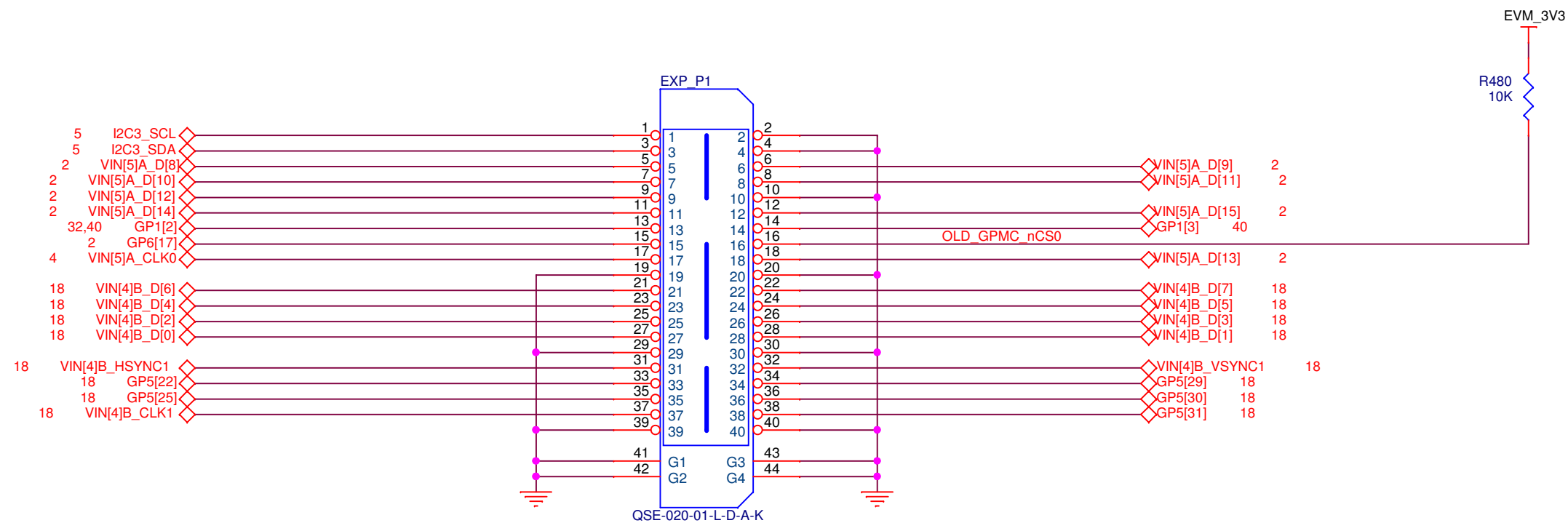
EVM_3V3

EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,67,68,85,86

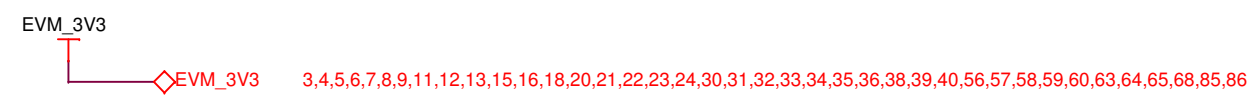
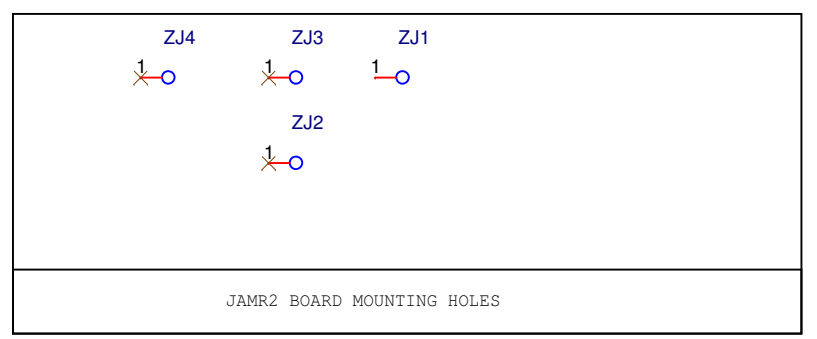
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: ETHERNET - OUTPUT CONNECTOR PORT			
Size: B	DWG NO	516582-0001	Revision: A
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BLANK

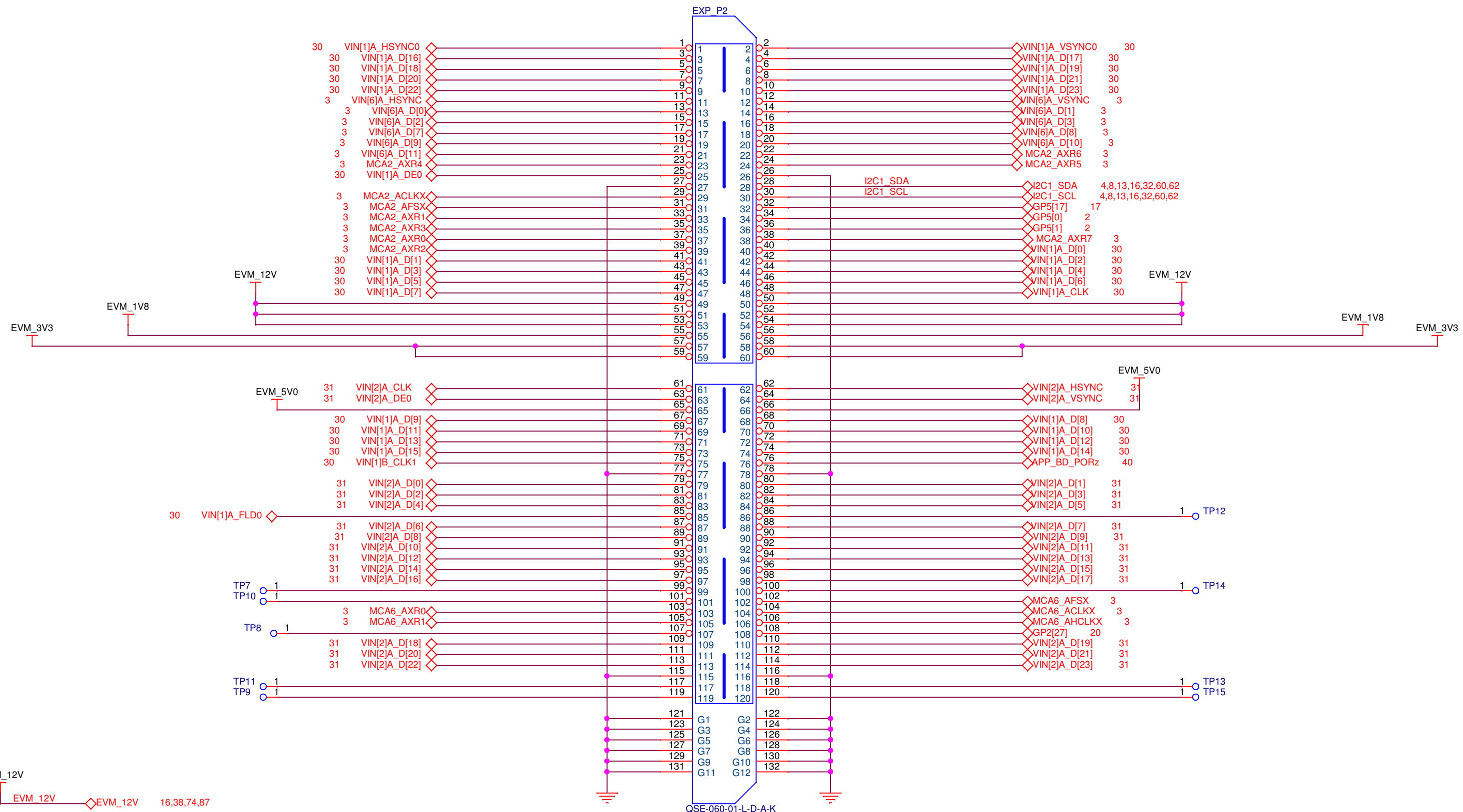
TEXAS INSTRUMENTS INCORPORATED		
Title:	VAYU EVM	
Page Contents:	ETHERNET LEDS	
Size: B	DWG NO 516582-0001	Revision: A
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QSE-020-01-L-D-A-K



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: INTERFACE CONN1			
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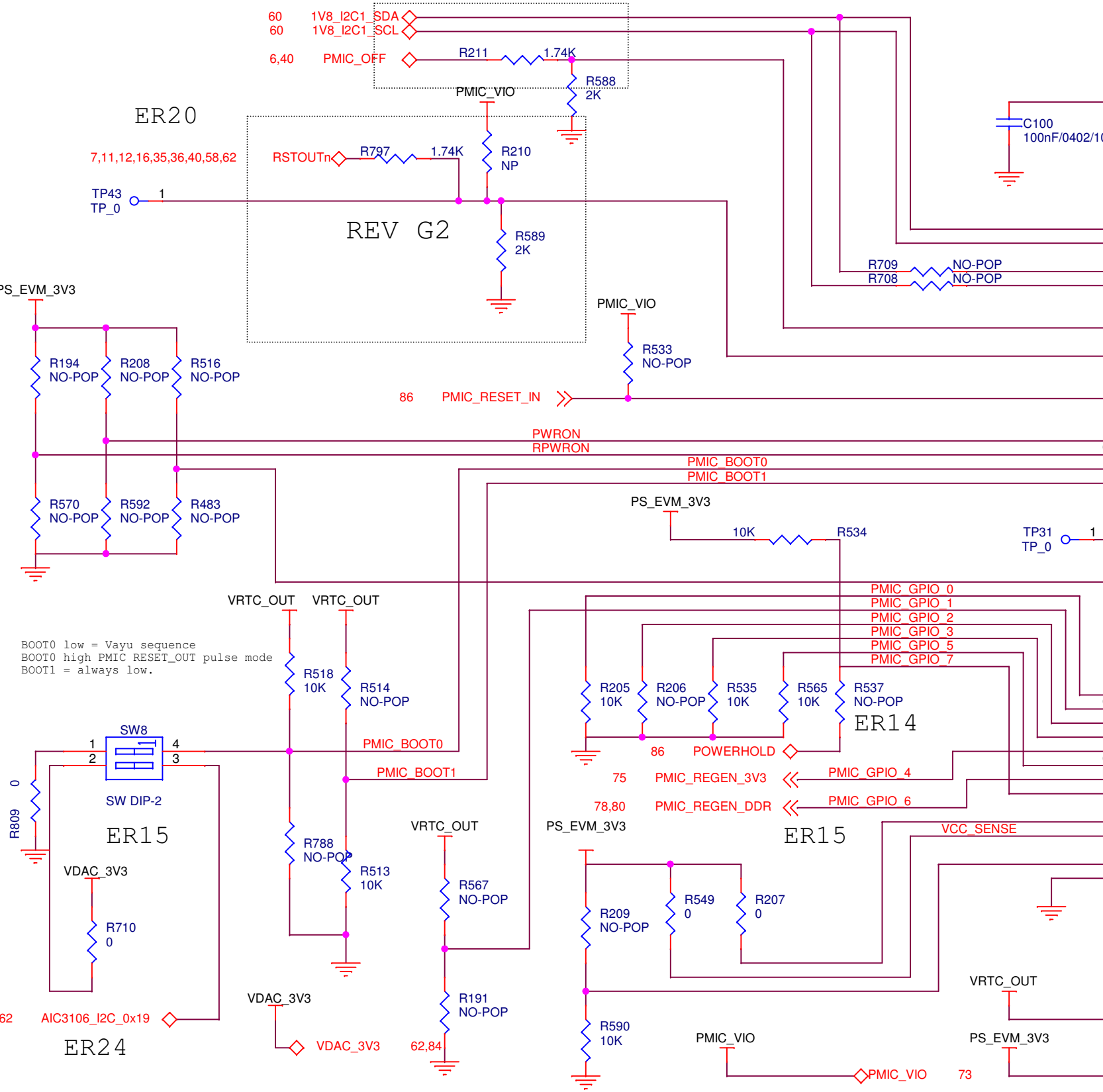
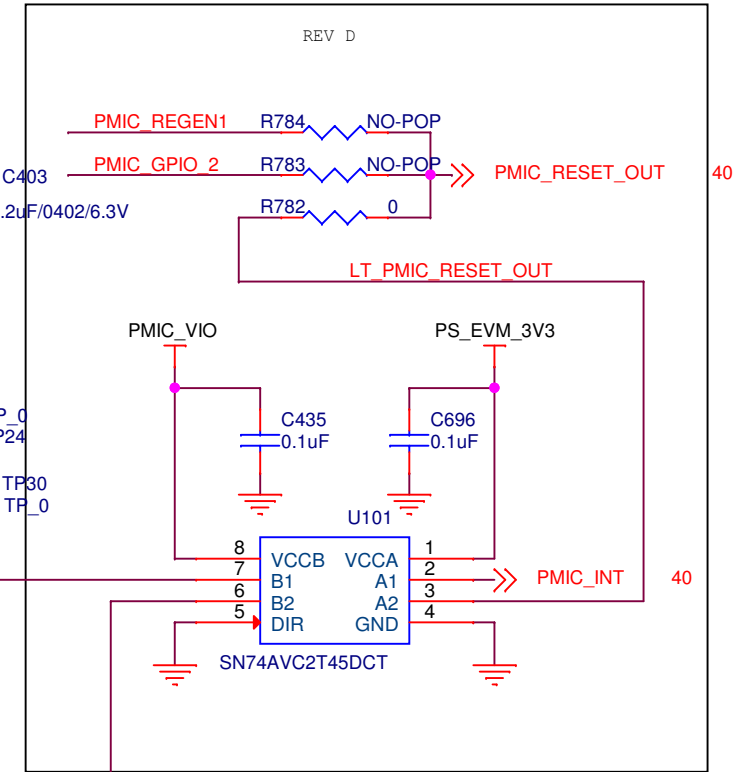
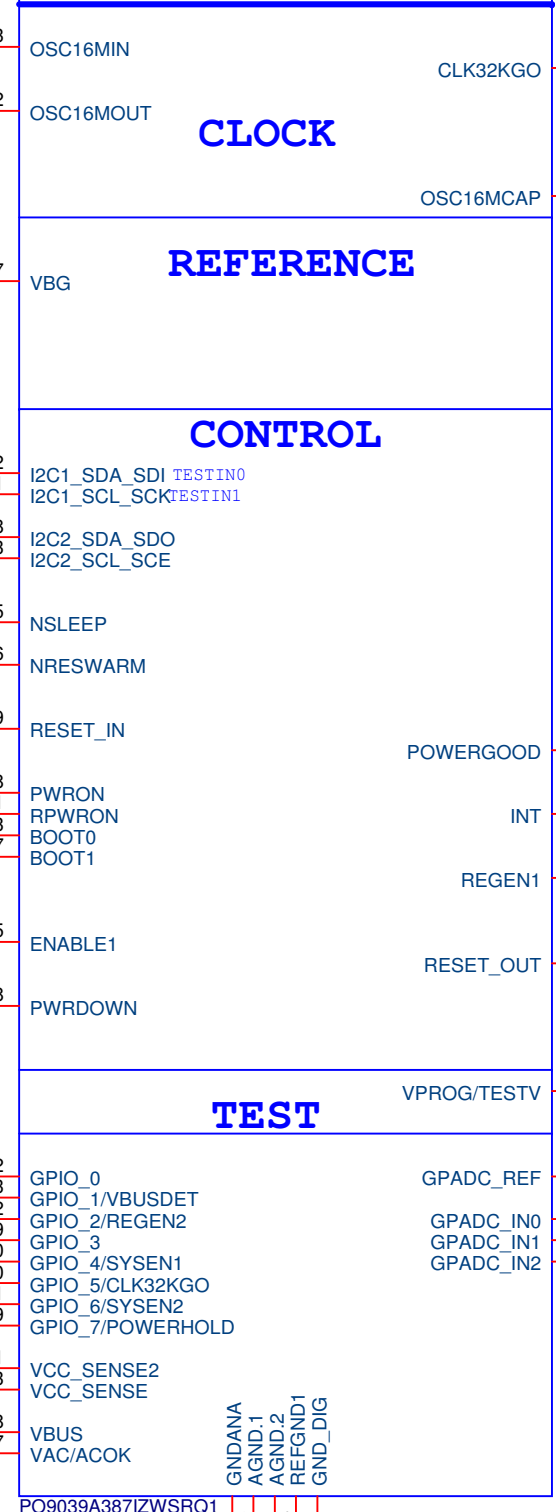
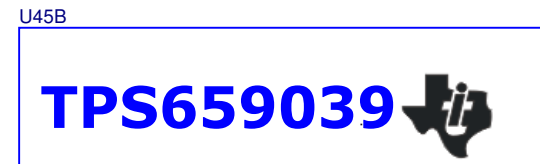


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: INTERFACE CONN2			
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PMIC HAS DUAL FOOTPRINT FOR 32678 HERTZ AND 16.384 MHZ CRYSTAL

PMIC_VIO IS 1.8 VOLTS
NOT THIS MEANS TRANSLATORS FOR I2C AND OTHERS

REV G3



ER20
7,11,12,16,35,36,40,58,62

BOOT0 low = Vayu sequence
BOOT0 high PMIC RESET_OUT pulse mode
BOOT1 = always low.

ER15
VDAC_3V3

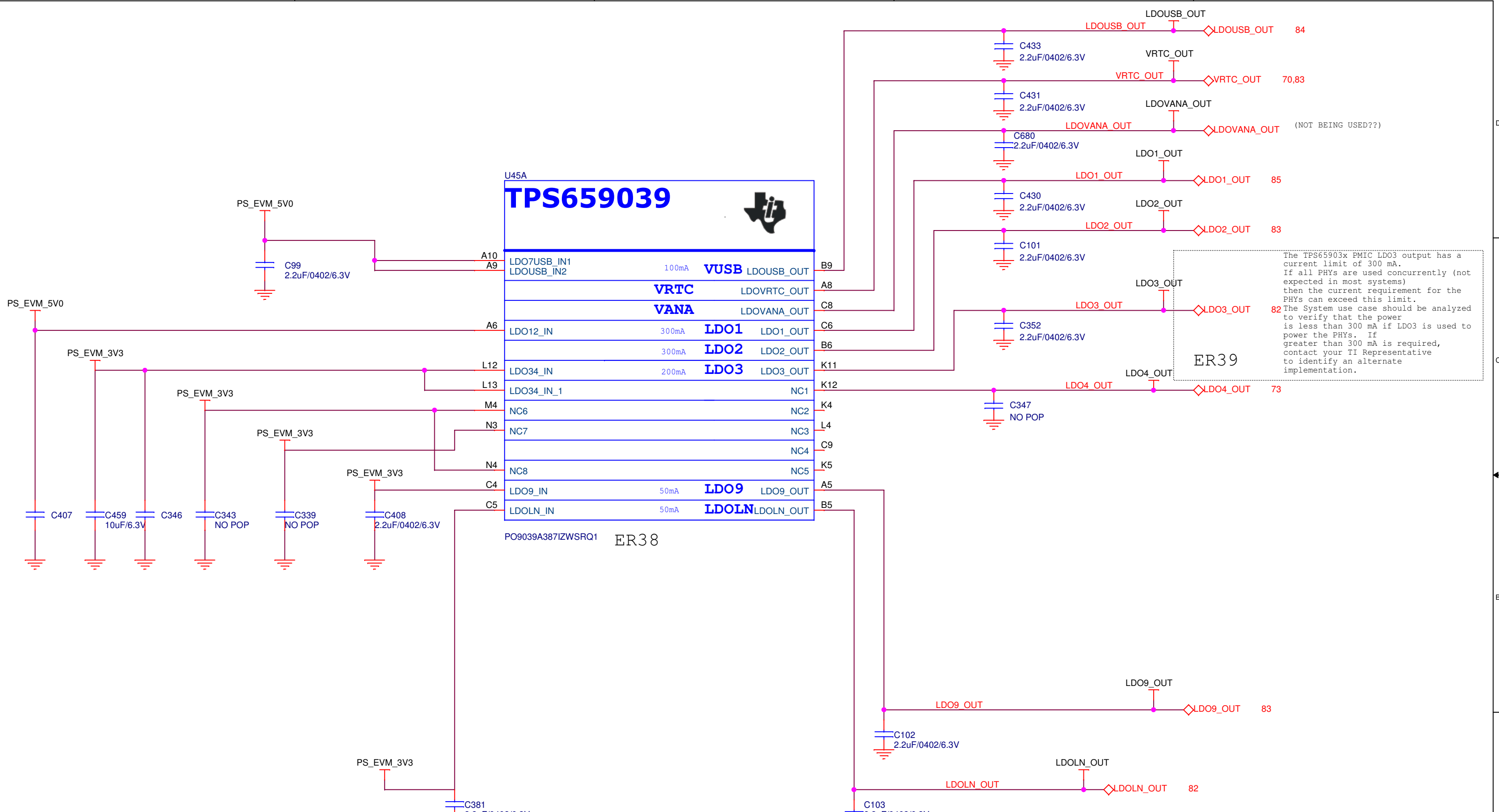
ER24
AIC3106_I2C_0x19

ER14
POWERHOLD, PMIC_REGEN_3V3, PMIC_REGEN_DDR

ER15
VCC SENSE

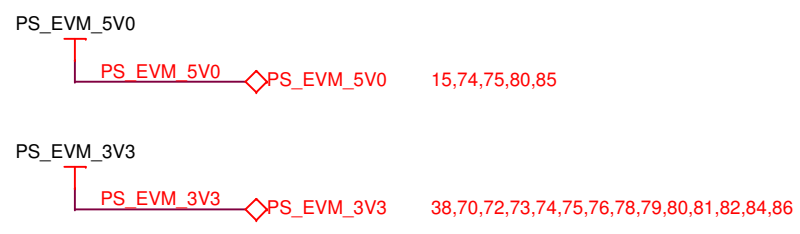
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: PMIC CONTROL			
Size: B	DWG NO	516582-0001	Revision: G3
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62 AIC3106_I2C_0x19 62,84 VDAC_3V3 62,84 VDAC_3V3 73 PS_EVM_3V3 PS_EVM_3V3 38,71,72,73,74,75,76,78,79,80,81,82,84,86

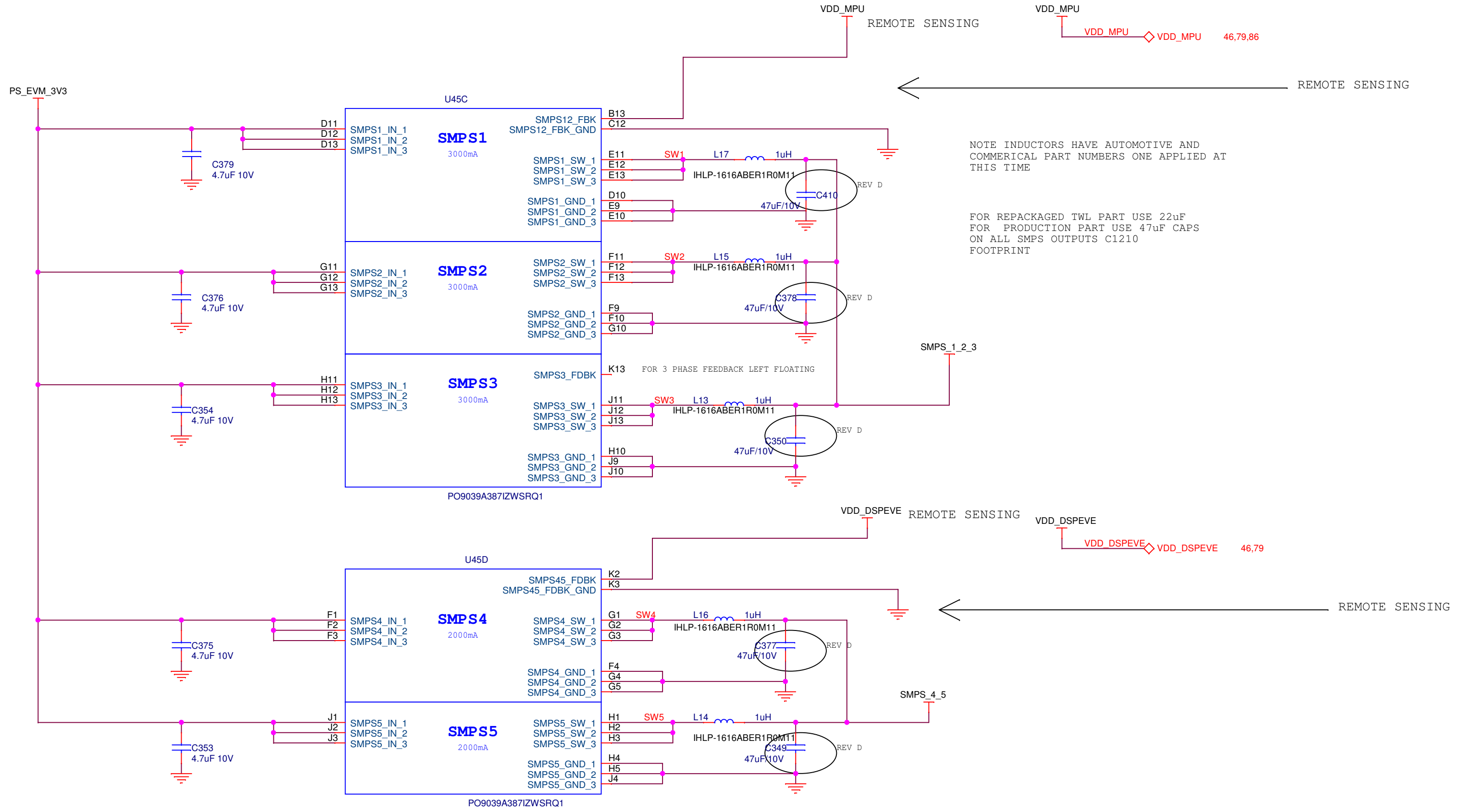


ER39

The TPS65903x PMIC LDO3 output has a current limit of 300 mA. If all PHYs are used concurrently (not expected in most systems) then the current requirement for the PHYs can exceed this limit. The System use case should be analyzed to verify that the power is less than 300 mA if LDO3 is used to power the PHYs. If greater than 300 mA is required, contact your TI Representative to identify an alternate implementation.

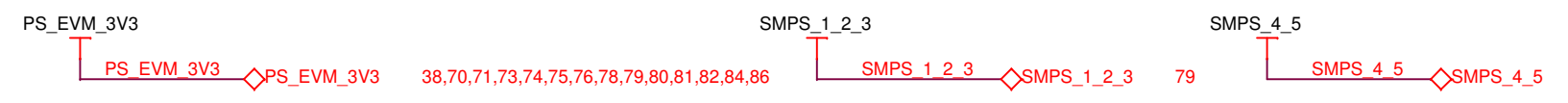


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: PMIC LDO'S			
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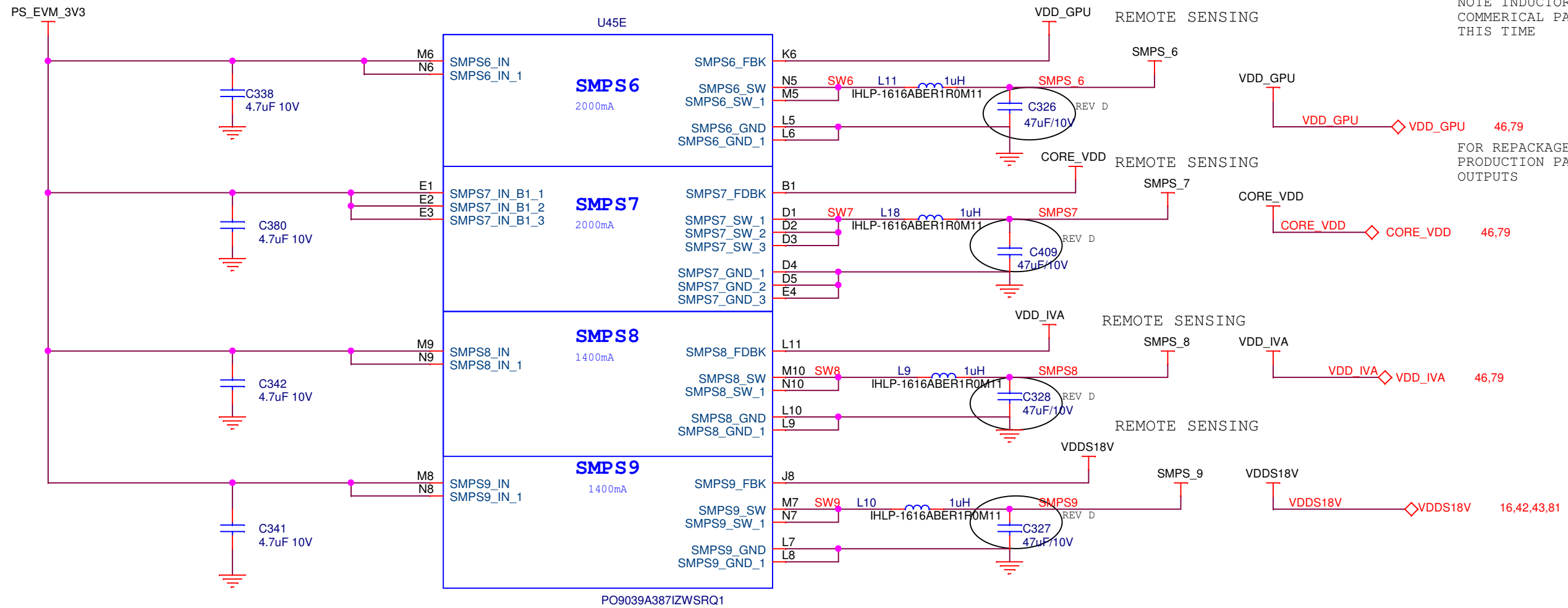


NOTE INDUCTORS HAVE AUTOMOTIVE AND COMMERCIAL PART NUMBERS ONE APPLIED AT THIS TIME

FOR REPACKAGED TWL PART USE 22uF
FOR PRODUCTION PART USE 47uF CAPS
ON ALL SMPS OUTPUTS C1210 FOOTPRINT

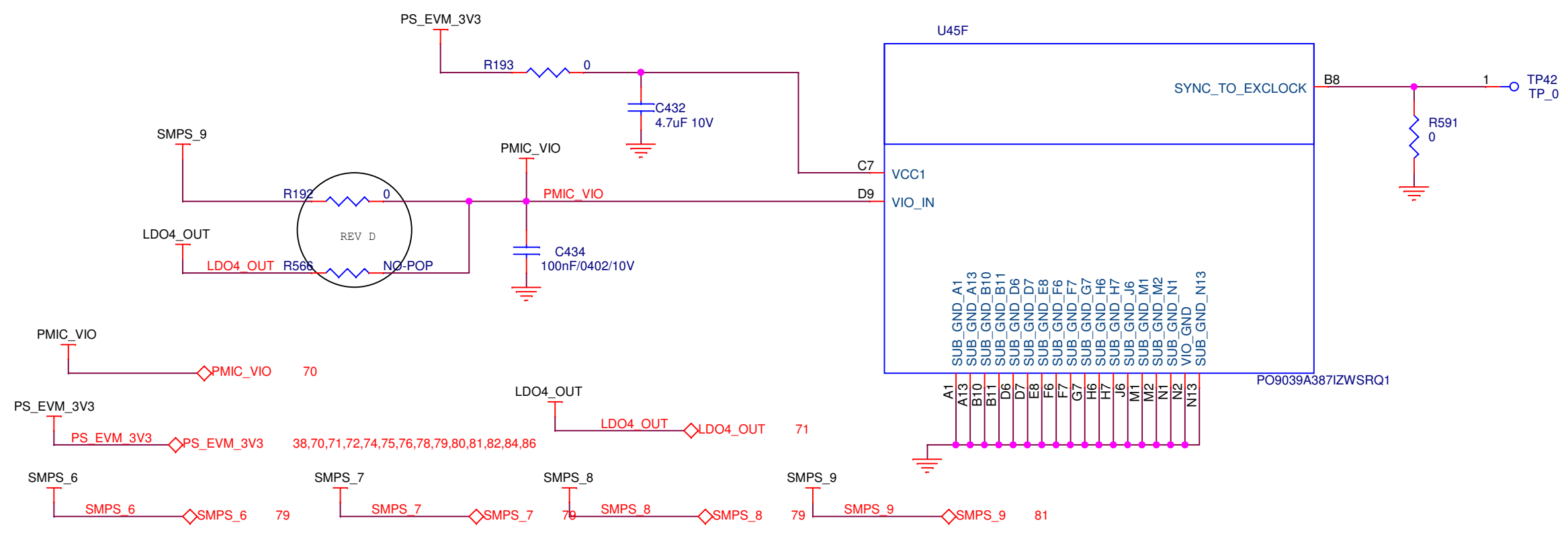


TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: PMIC SWITCHER SECTION 1			
Size: B	DWG NO	516582-0001	Revision: D
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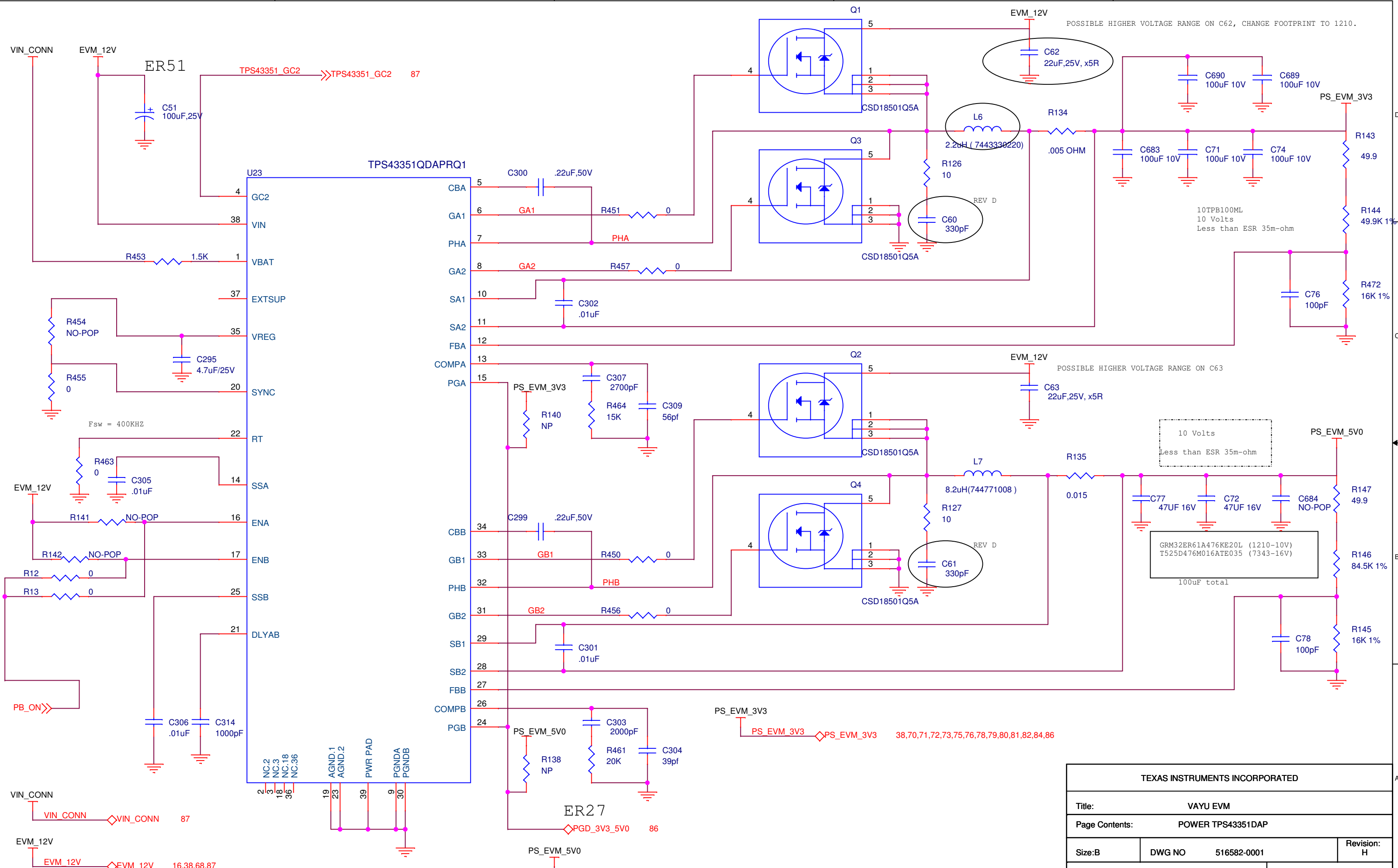


NOTE INDUCTORS HAVE AUTOMOTIVE AND COMMERCIAL PART NUMBERS ONE APPLIED AT THIS TIME

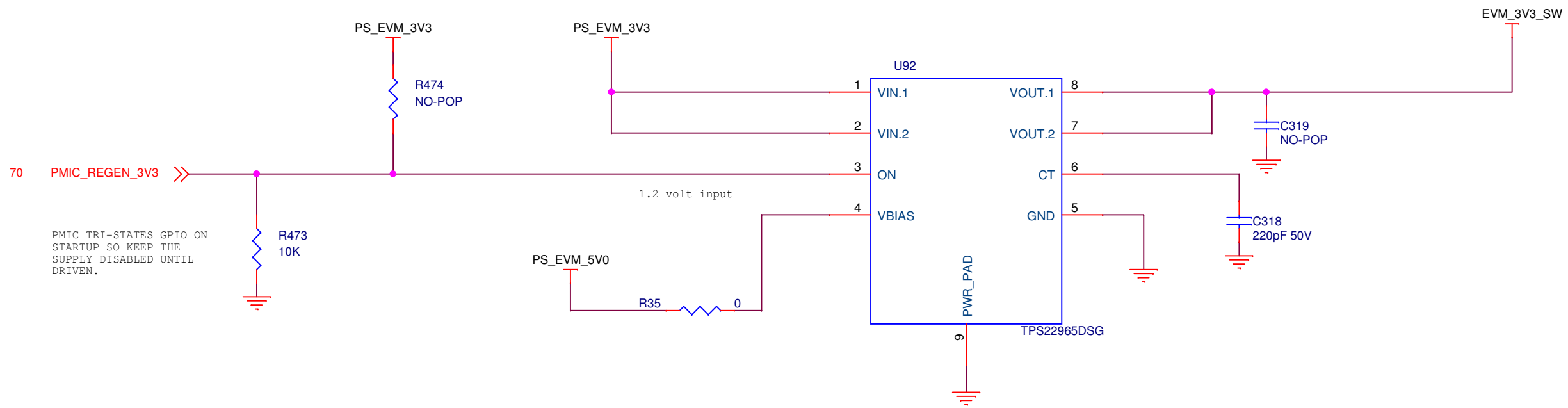
FOR REPACKAGED TWL PART USE 22uF FOR PRODUCTION PART USE 47uF CAPS ON ALL SMPS OUTPUTS



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: PMIC SWITCHER SECTION 2			
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TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER TPS43351DAP			
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PS_EVM_5V0

PS_EVM_5V0 PS_EVM_5V0 15,71,74,80,85

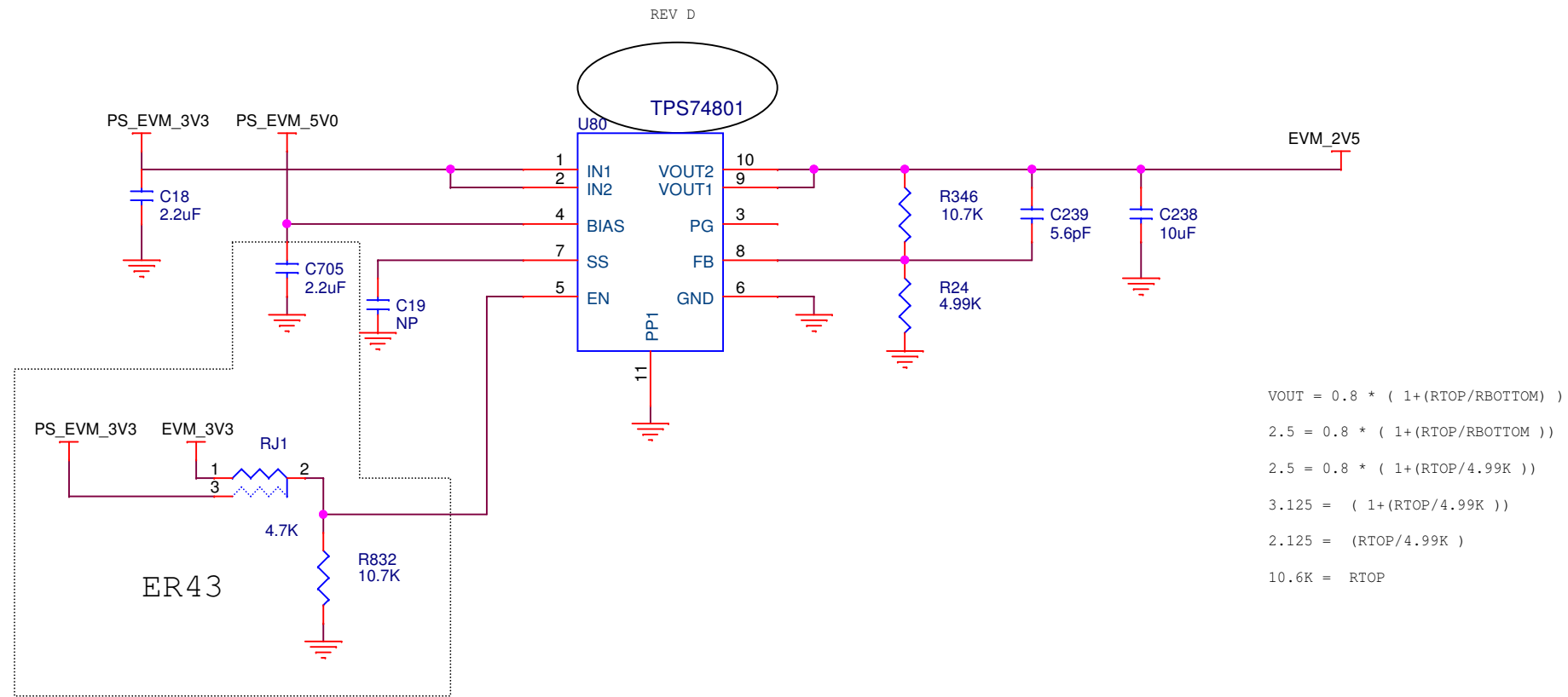
EVM_3V3_SW

EVM_3V3_SW 77,84,85

PS_EVM_3V3

PS_EVM_3V3 PS_EVM_3V3 38,70,71,72,73,74,76,78,79,80,81,82,84,86

TEXAS INSTRUMENTS INCORPORATED		
Title: VAYU EVM		
Page Contents: POWER TPS22965		
Size: B	DWG NO 516582-0001	Revision: A
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$$V_{OUT} = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

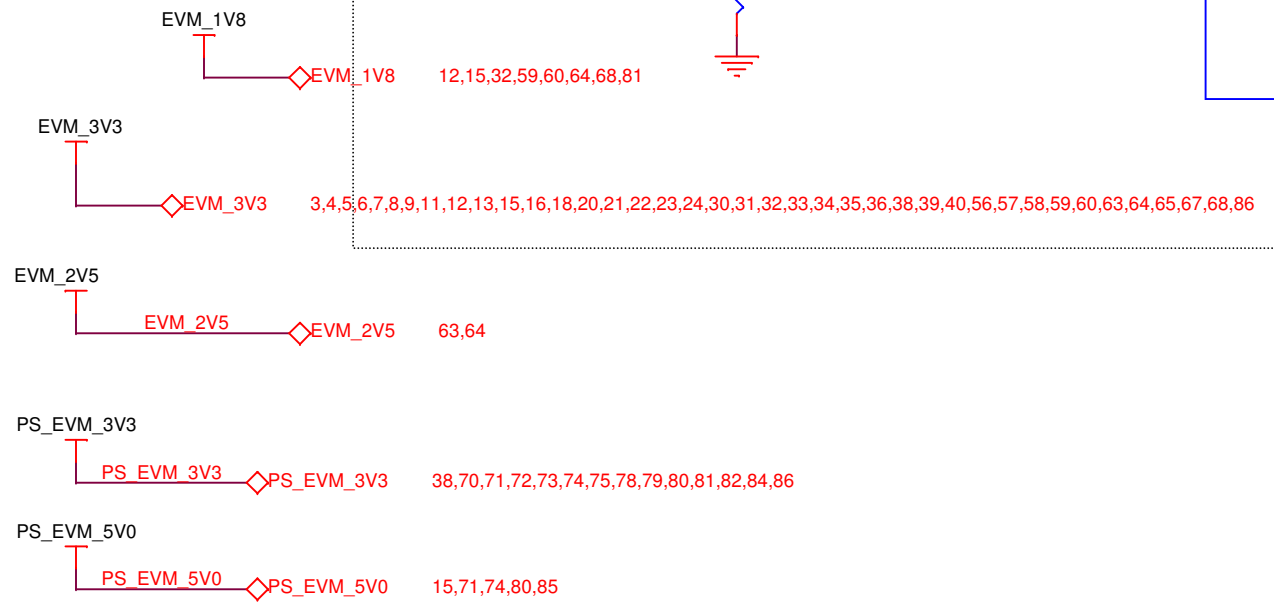
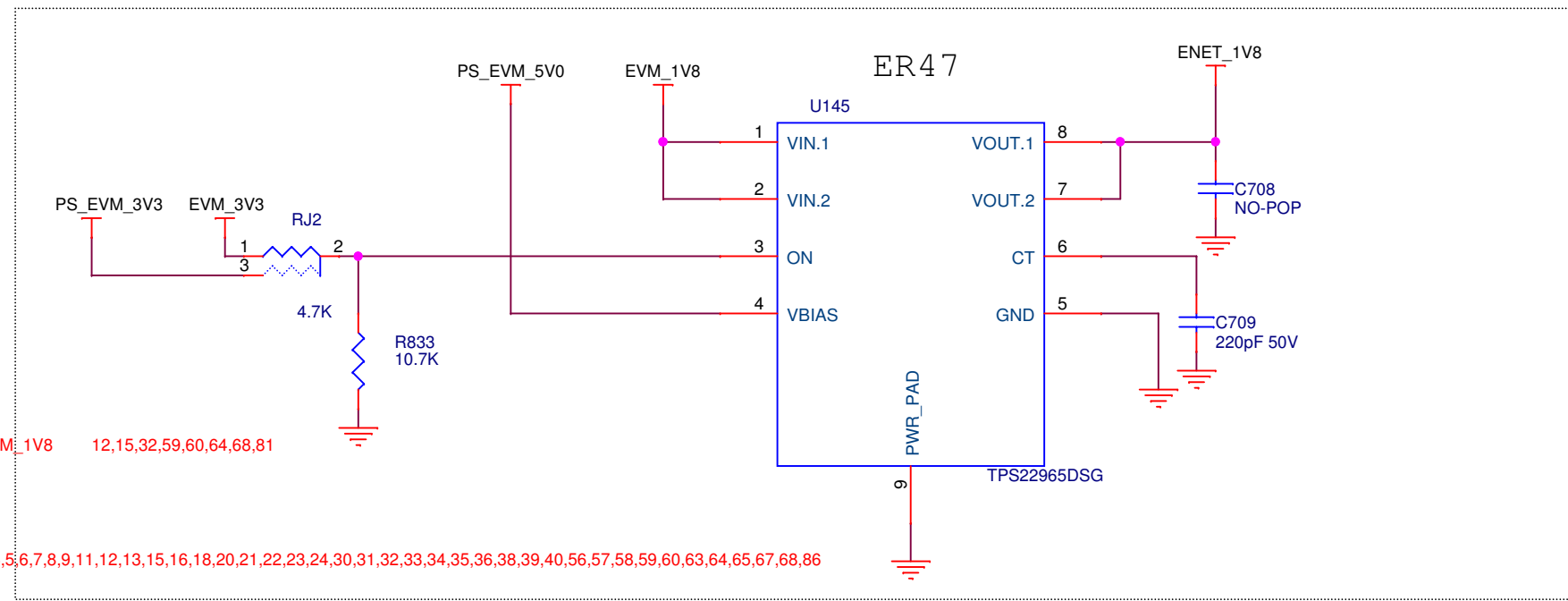
$$2.5 = 0.8 * (1 + (R_{TOP}/R_{BOTTOM}))$$

$$2.5 = 0.8 * (1 + (R_{TOP}/4.99K))$$

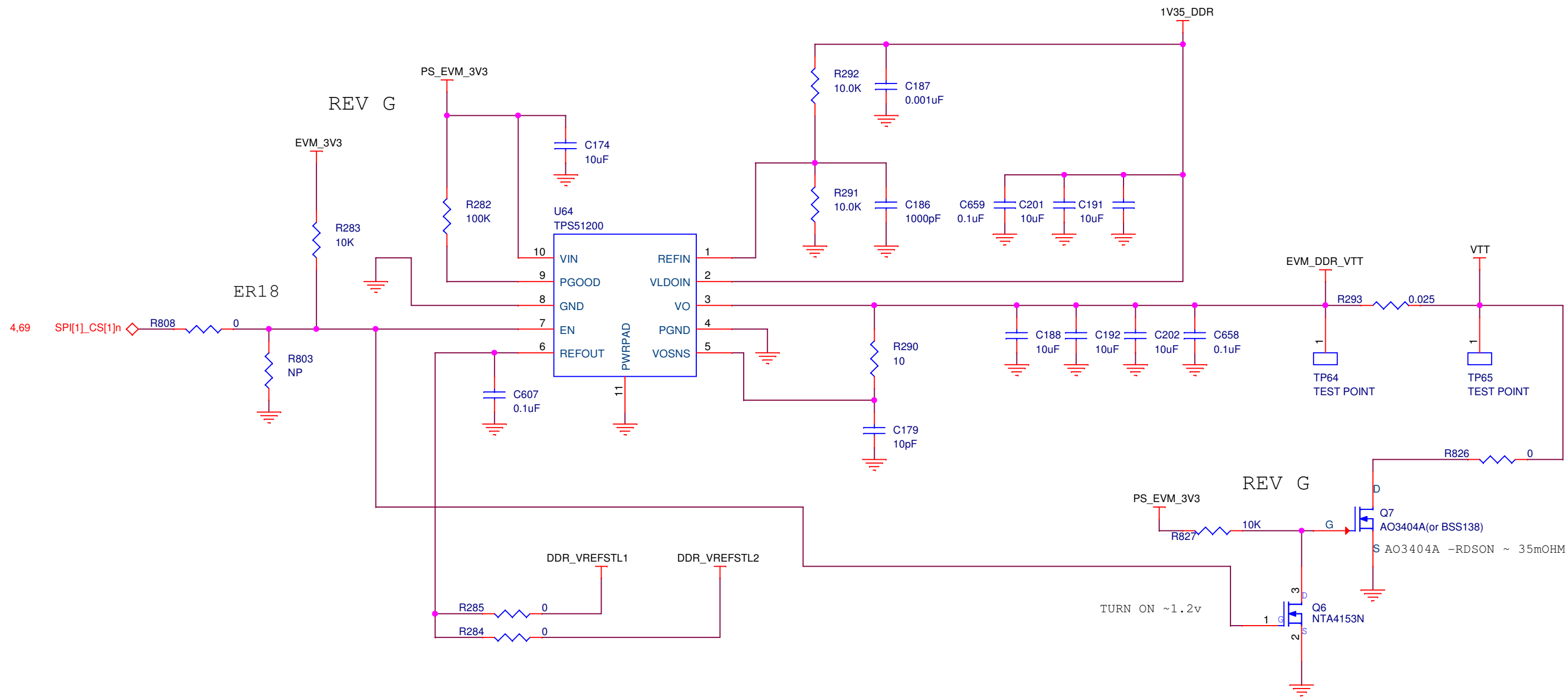
$$3.125 = (1 + (R_{TOP}/4.99K))$$

$$2.125 = (R_{TOP}/4.99K)$$

$$10.6K = R_{TOP}$$



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: 2V5 POWER			
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PS_EVM_3V3
PS_EVM_3V3 \diamond PS_EVM_3V3 38,70,71,72,73,74,75,76,79,80,81,82,84,86

VTT
VTT \diamond VTT 51,55

DDR_VREFSTL2
DDR_VREFSTL2 \ggg DDR_VREFSTL2 26,53

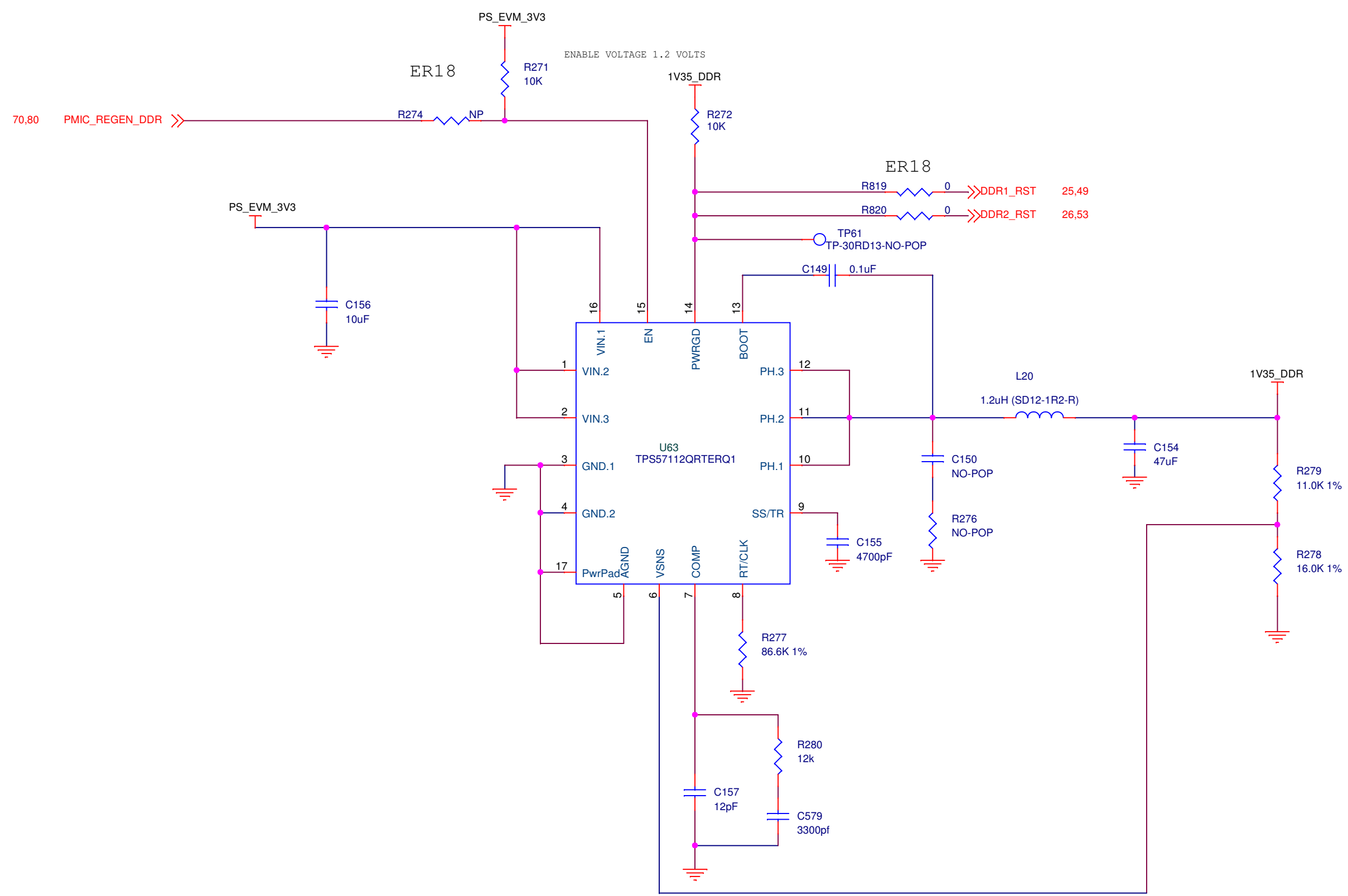
DDR_VREFSTL1
DDR_VREFSTL1 \ggg DDR_VREFSTL1 25,49

1V35_DDR
1V35_DDR \ggg 1V35_DDR 78,80

EVM_3V3
EVM_3V3 \diamond EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,59,60,63,64,65,67,68,85,86

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER TPS51200			
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1.5V at 2 AMP



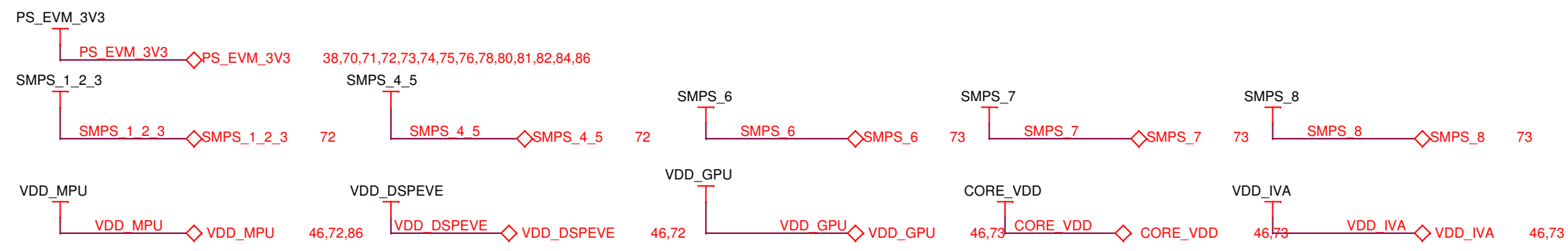
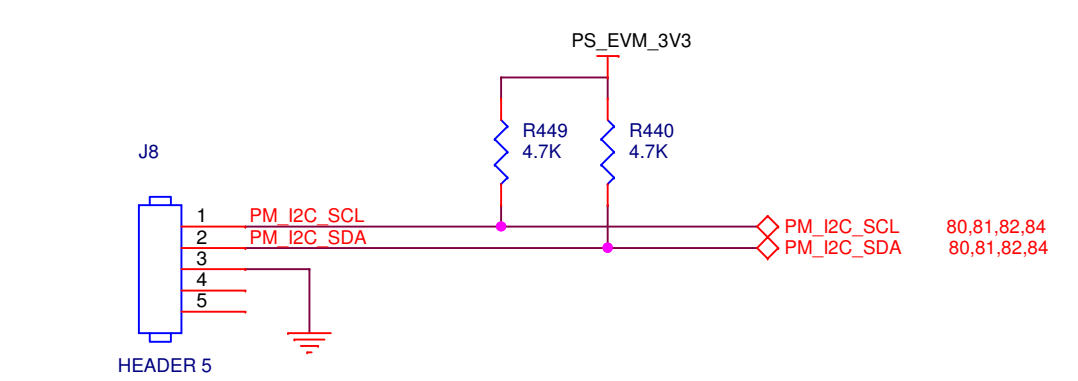
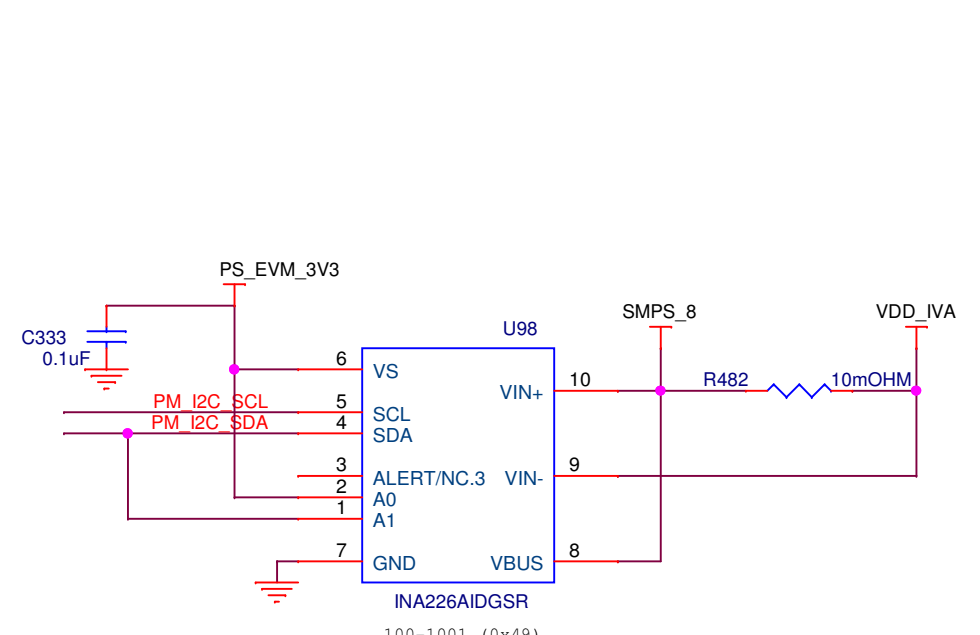
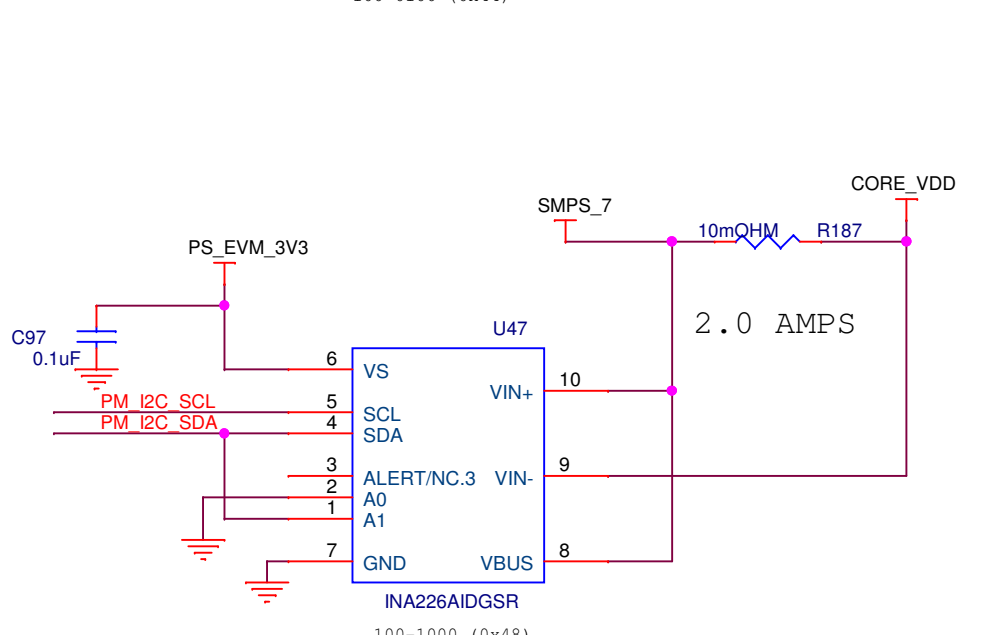
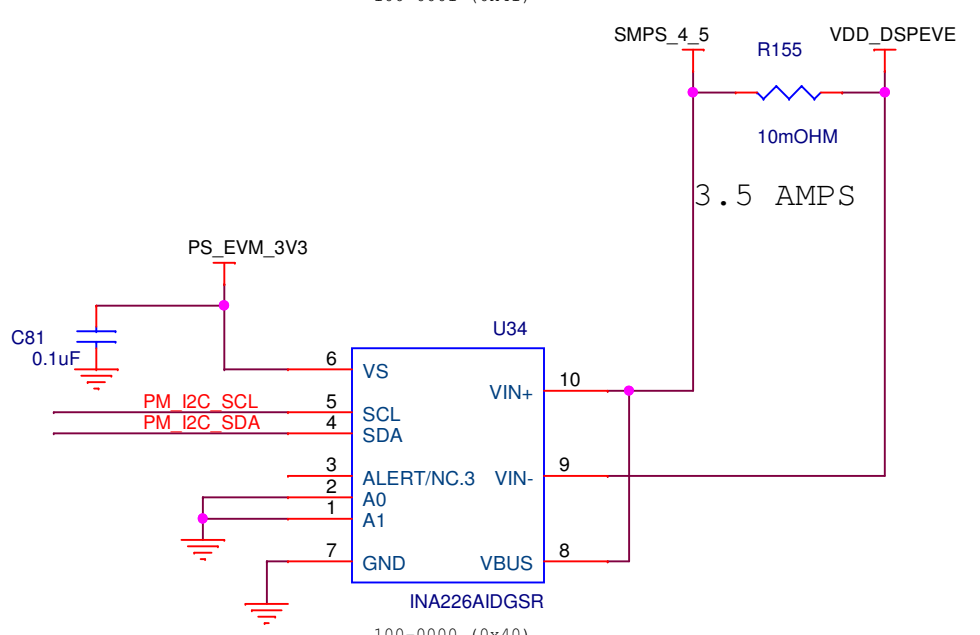
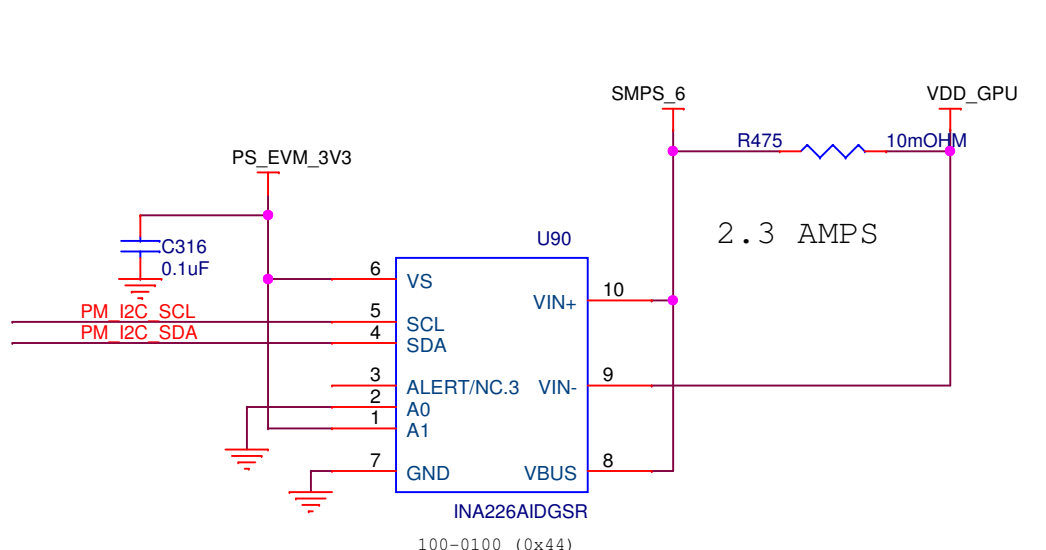
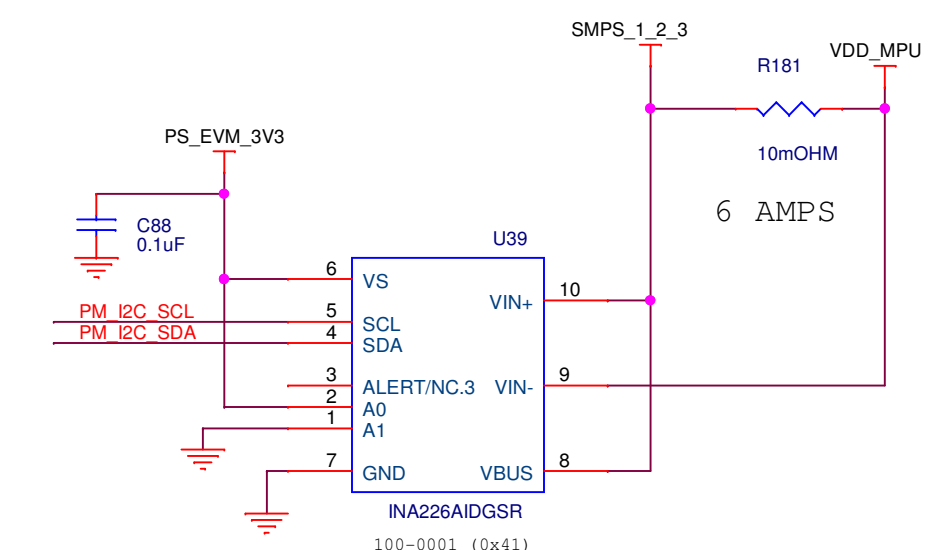
PS_EVM_3V3

PS_EVM_3V3 PS_EVM_3V3 38,70,71,72,73,74,75,76,79,80,81,82,84,86

1V35_DDR

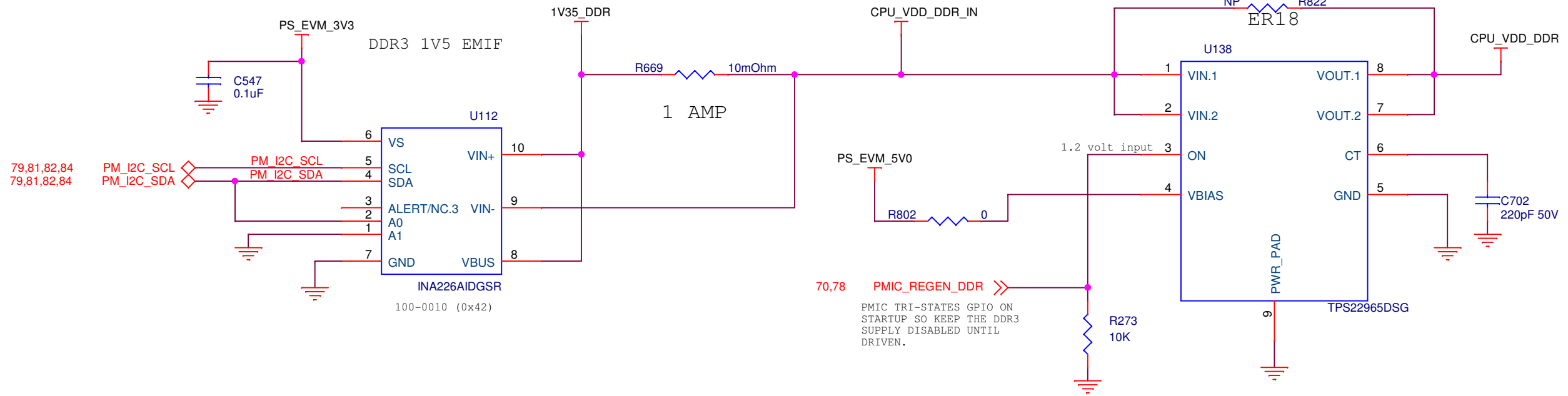
1V35_DDR 1V35_DDR 77,80

Texas Instruments			
Title: VAYU EVM			
Page Contents: VDDR REGULATOR			
Size: B	DWG NO	516172-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 78 of	89

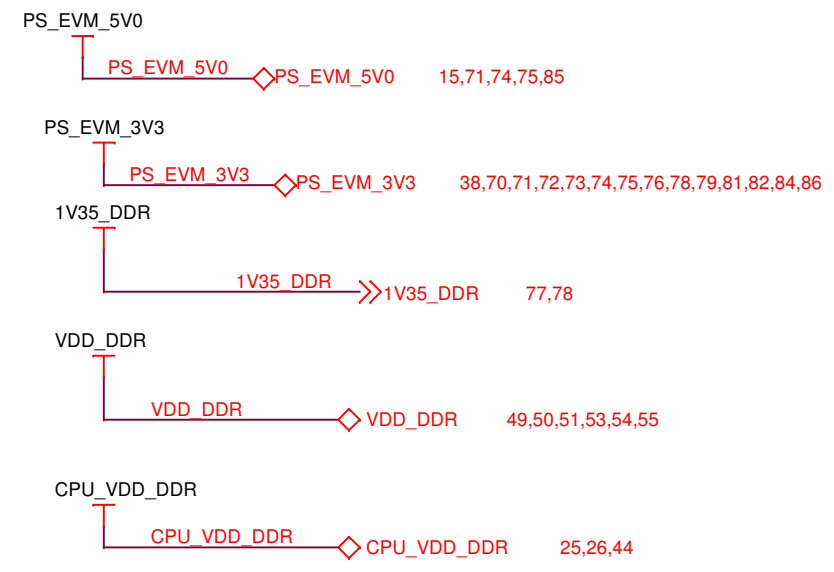
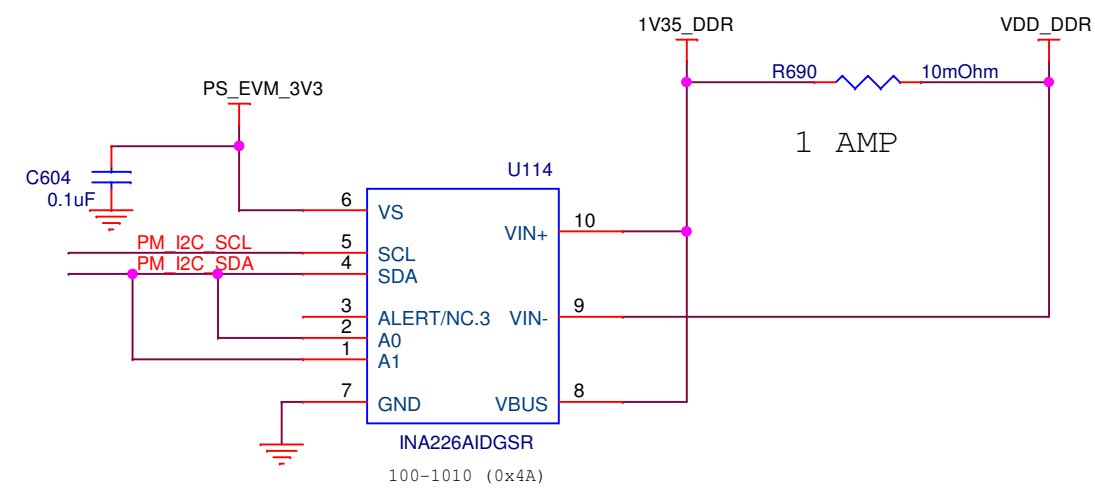


ER48

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: CORE POWER ROUTER			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 79 of 89	

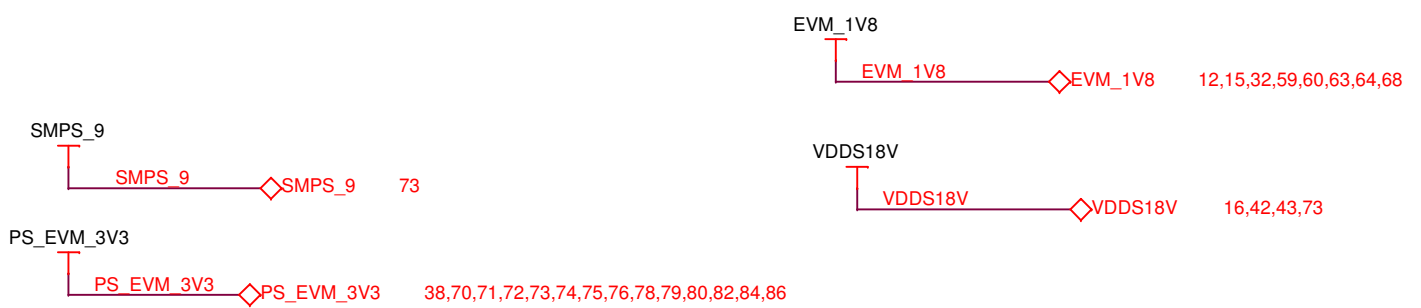
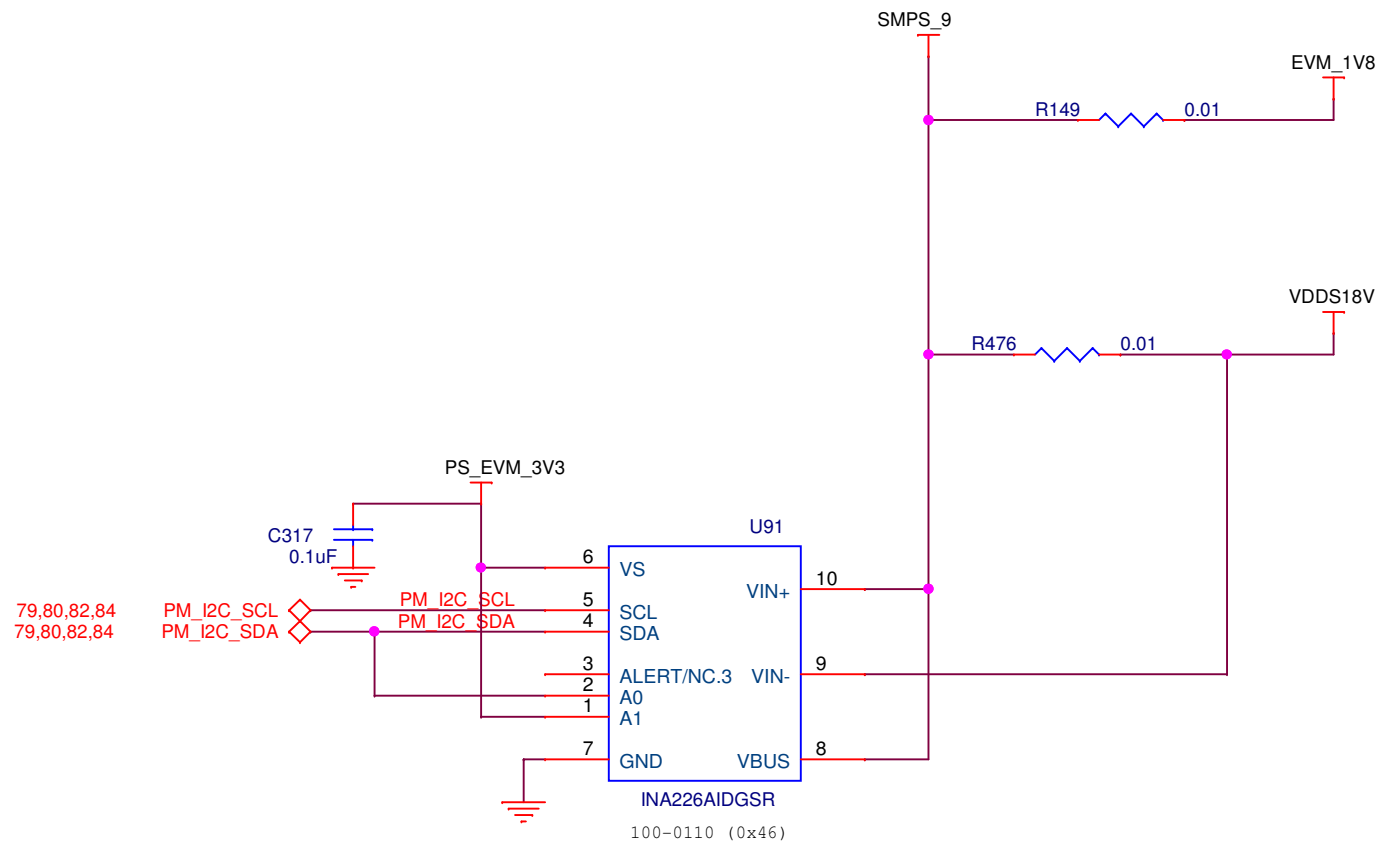


70,78 PMIC_REGEN_DDR >>>
 PMIC TRI-STATES GPIO ON STARTUP SO KEEP THE DDR3 SUPPLY DISABLED UNTIL DRIVEN.

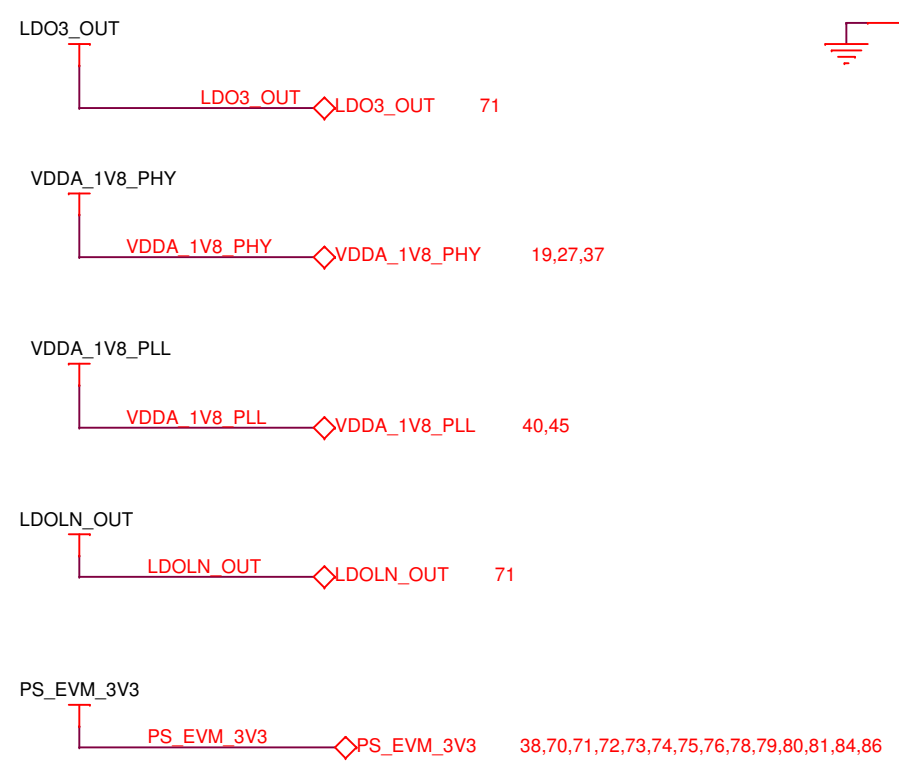
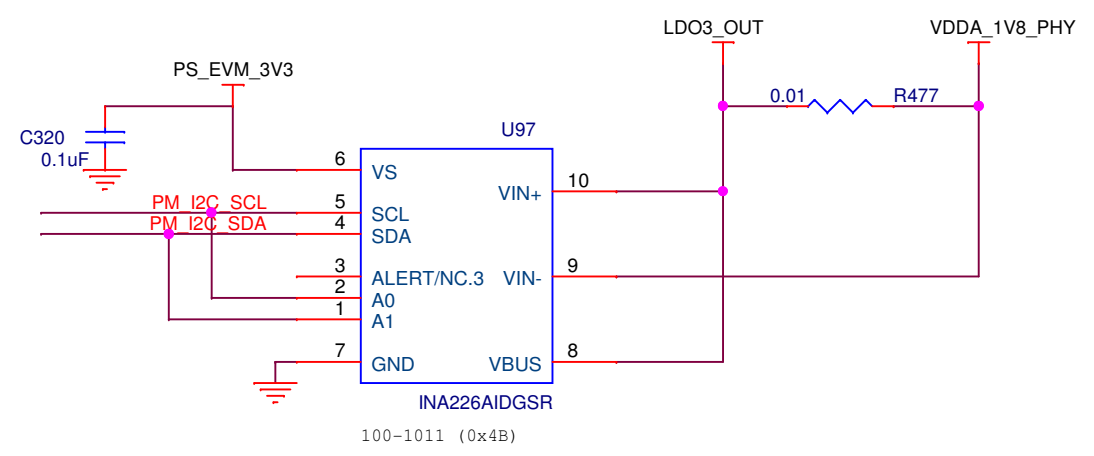
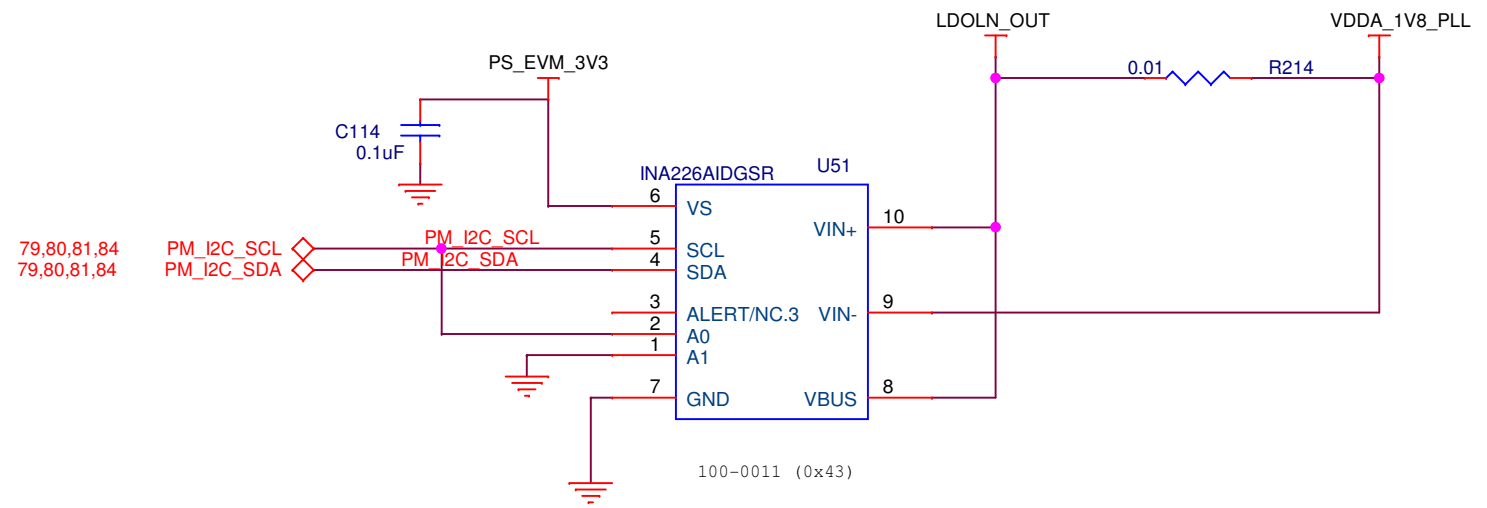


ER48

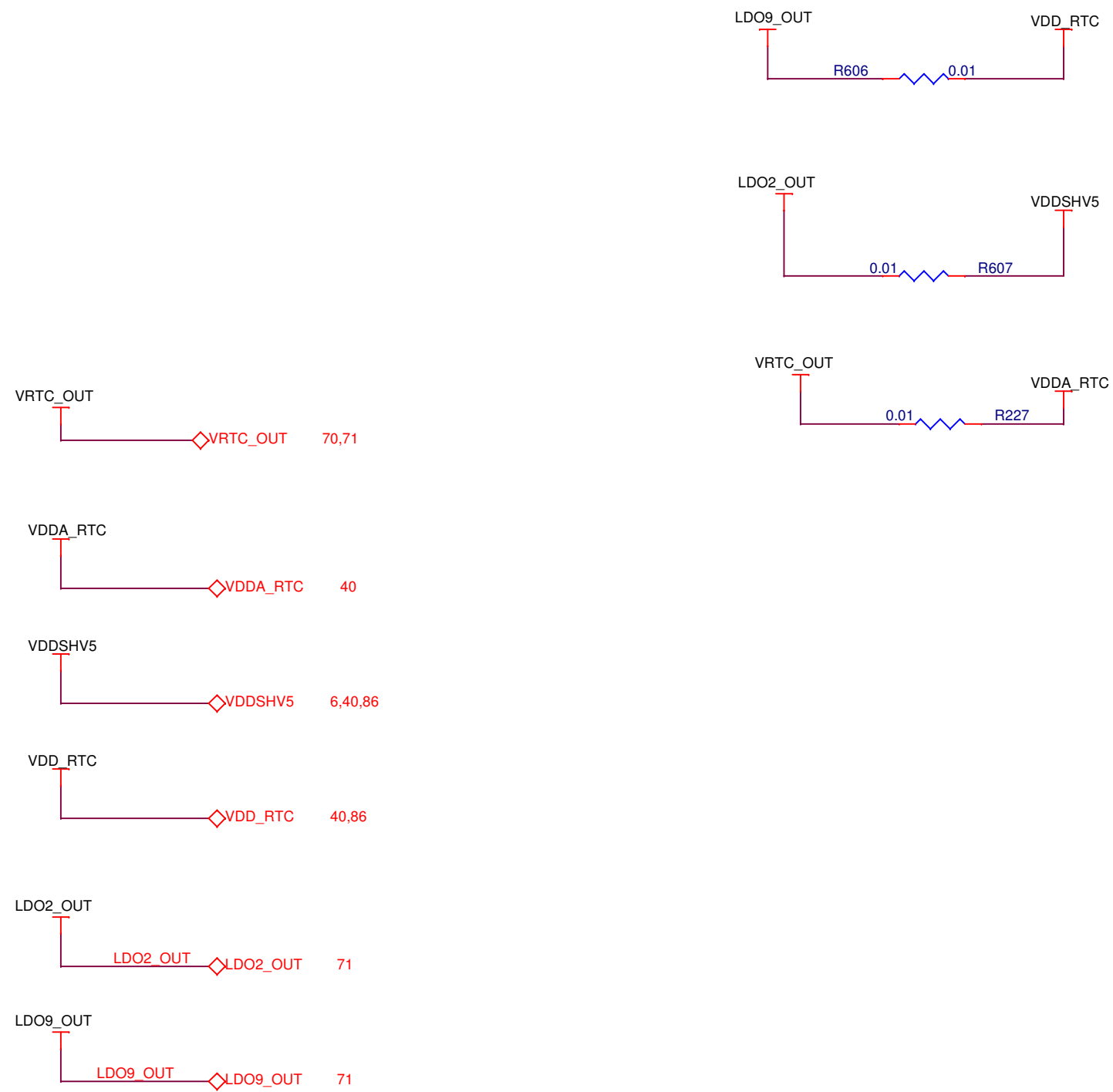
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER ROUTER DDR			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 80 of	89



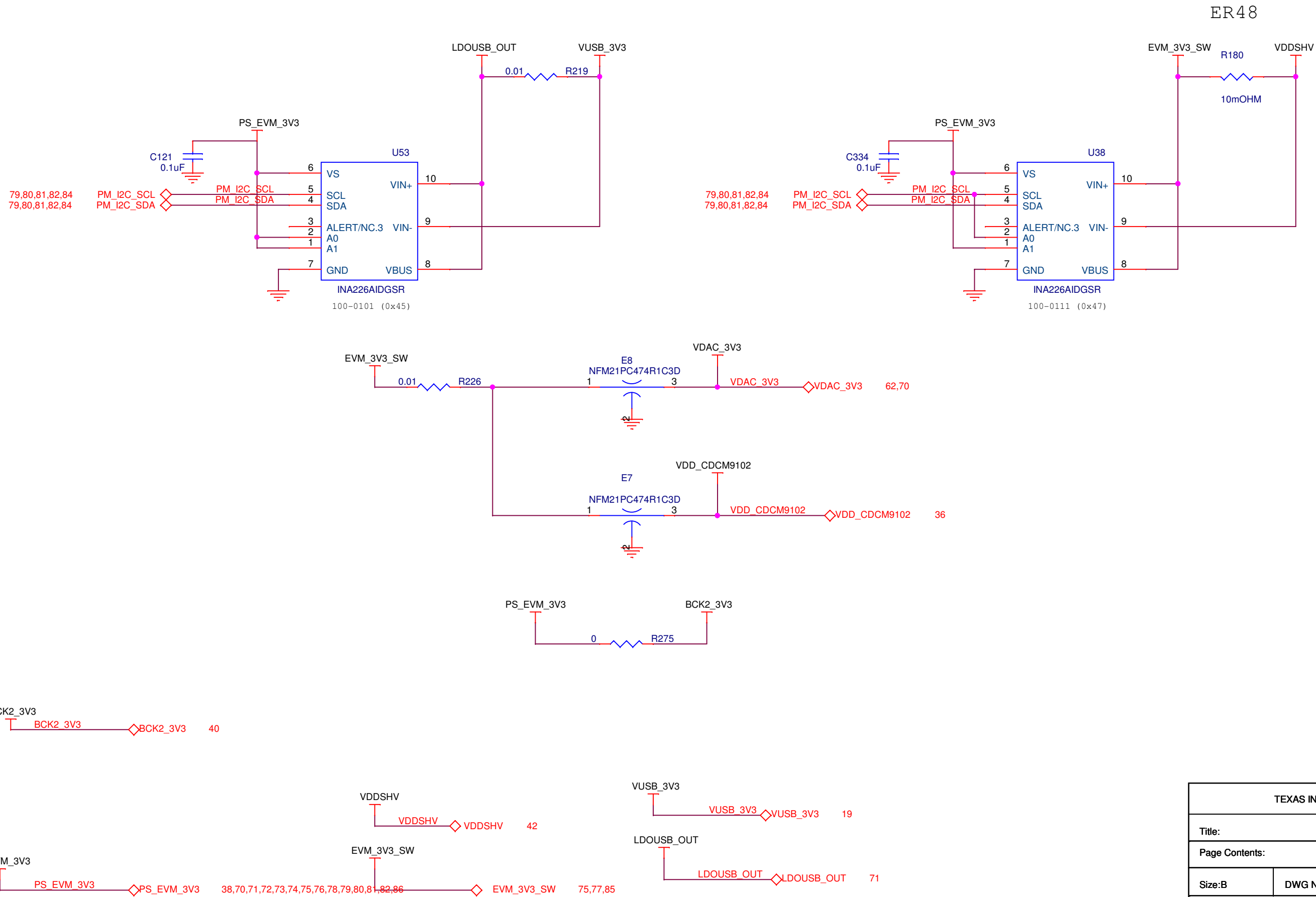
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER ROUTER 1V8			
Size: B	DWG NO	516582-0001	Revision: G4
Date: Tuesday, January 12, 2016		Sheet 81 of	89



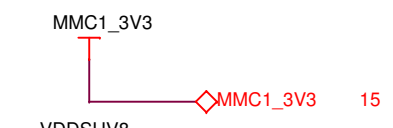
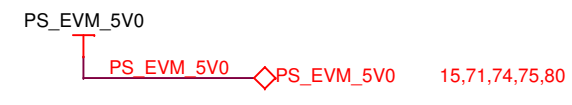
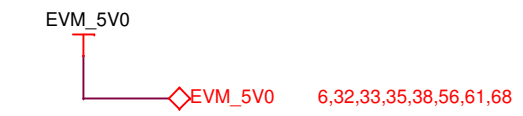
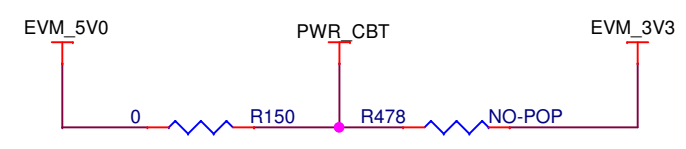
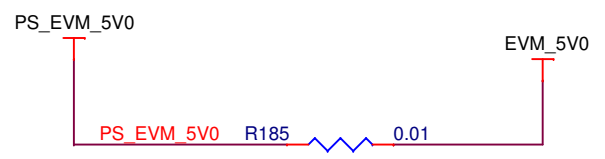
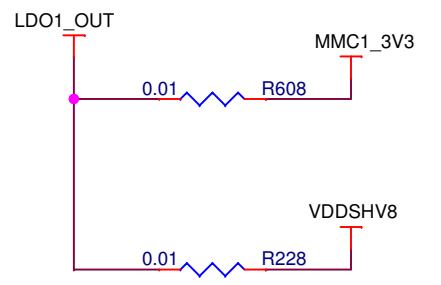
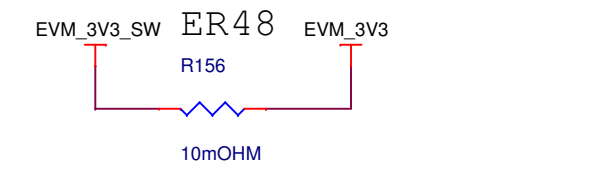
TEXAS INSTRUMENTS INCORPORATED		
Title: VAYU EVM		
Page Contents: POWER ROUTER 1V8A		
Size: B	DWG NO 516582-0001	Revision: G4
Date: Tuesday, January 12, 2016	Sheet 82 of	89



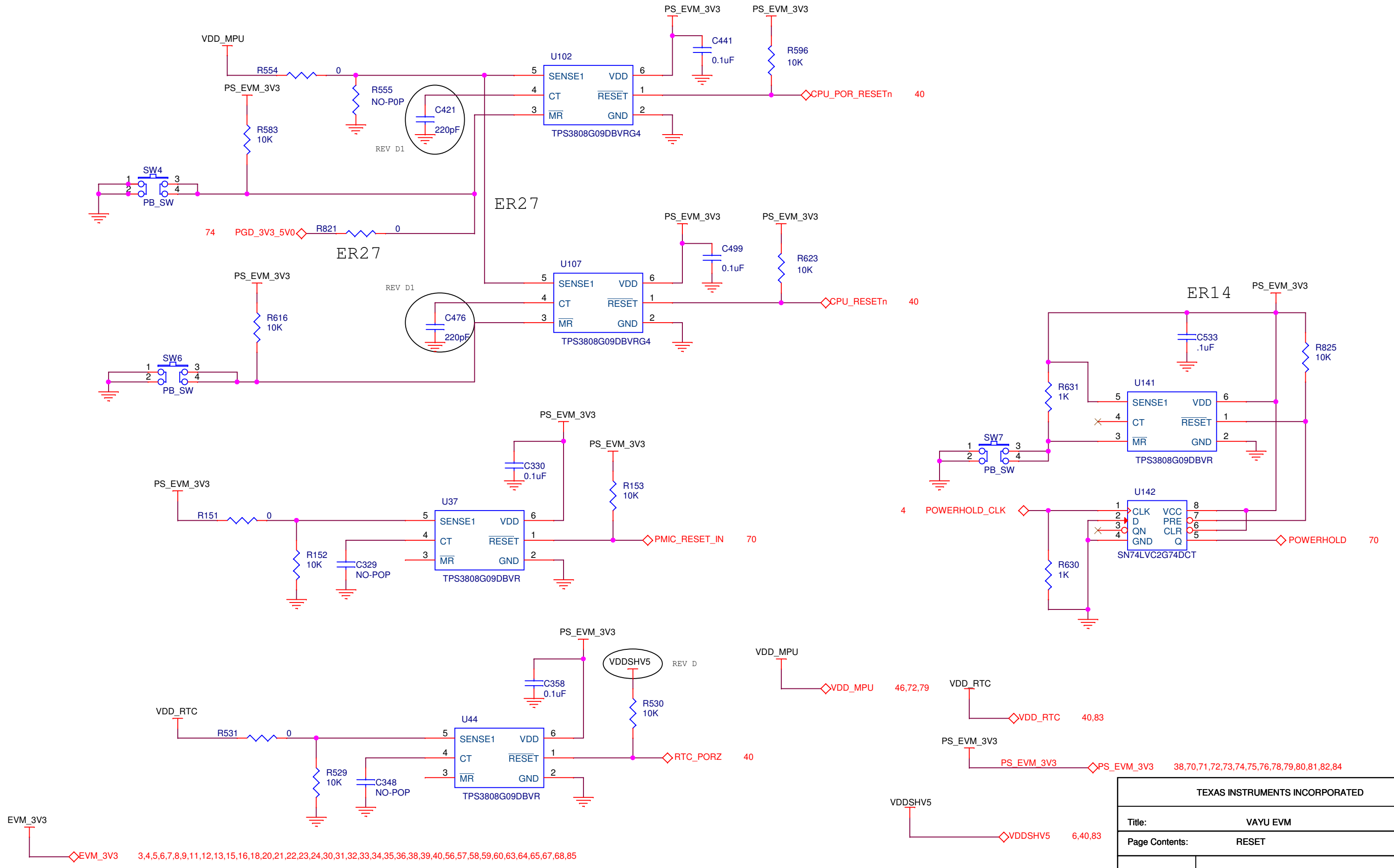
TEXAS INSTRUMENTS INCORPORATED			
Title:		VAYU EVM	
Page Contents:		POWER ROUTER RTC	
Size: B	DWG NO	516582-0001	Revision: A
Date: Tuesday, January 12, 2016		Sheet 83 of	89



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER ROUTER 3V3			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 84 of 89	



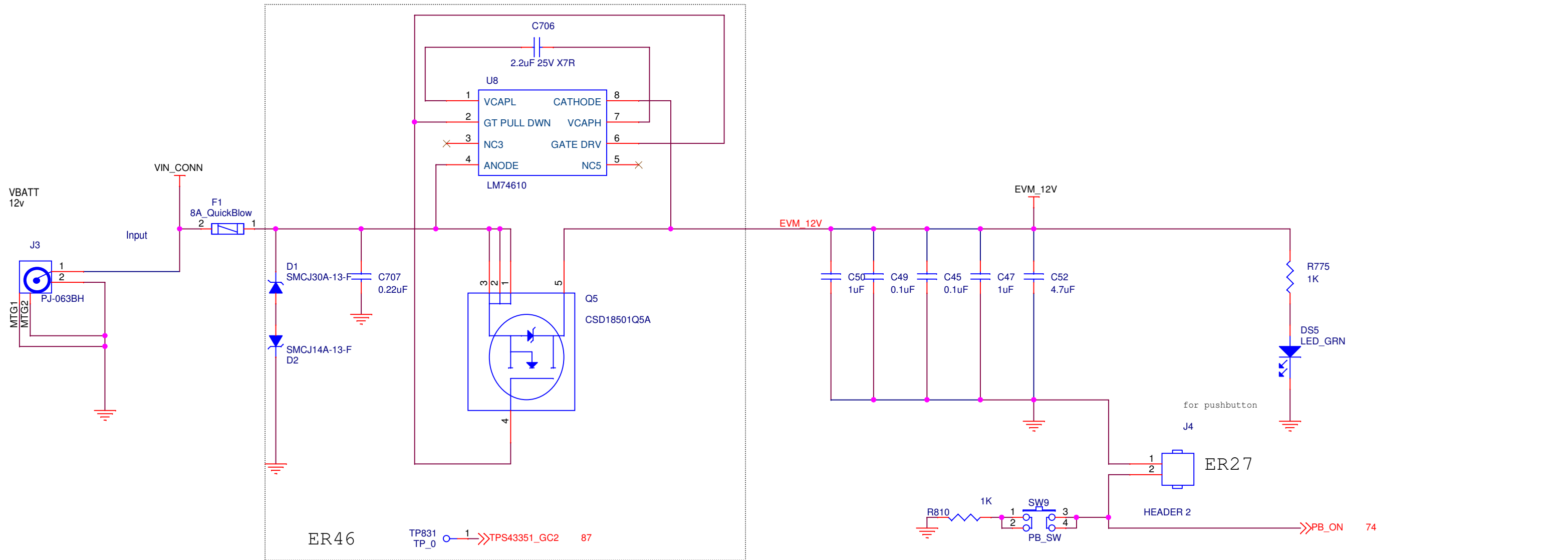
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER ROUTER EVM			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 85 of	89



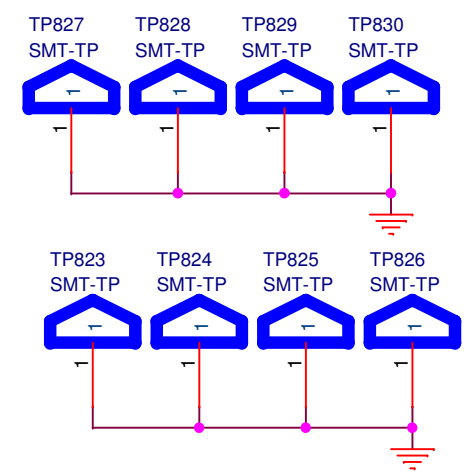
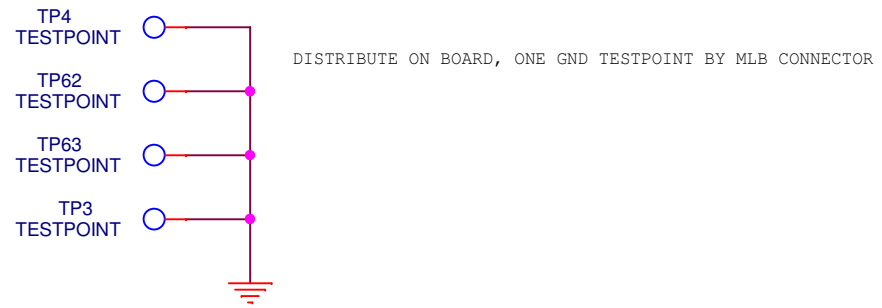
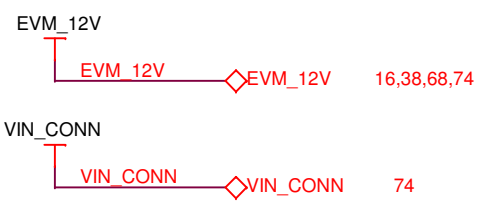
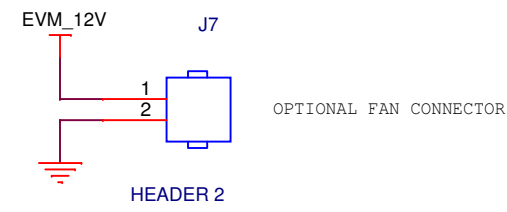
EVM_3V3 3,4,5,6,7,8,9,11,12,13,15,16,18,20,21,22,23,24,30,31,32,33,34,35,36,38,39,40,56,57,58,59,60,63,64,65,67,68,85

VDDSHV5 6,40,83

TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: RESET			
Size: B	DWG NO	516582-0001	Revision: D1
Date: Tuesday, January 12, 2016		Sheet 86 of 89	



ER46 TP831 TP_0 1 >>TPS43351_GC2 87



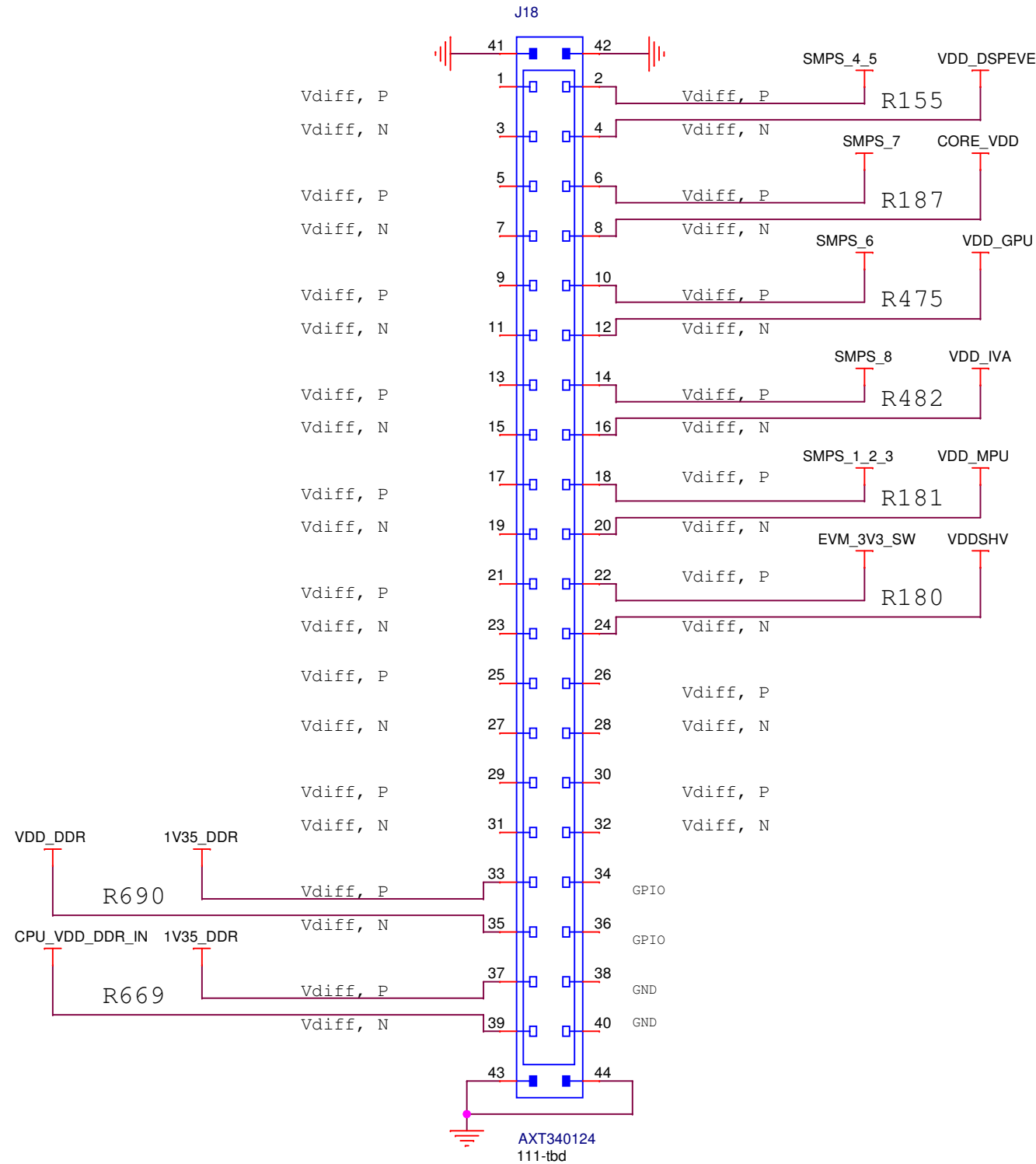
TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER INPUT			
Size: B	DWG NO	516582-0001	Revision: H
Date: Tuesday, January 12, 2016		Sheet 87 of	89

ER52

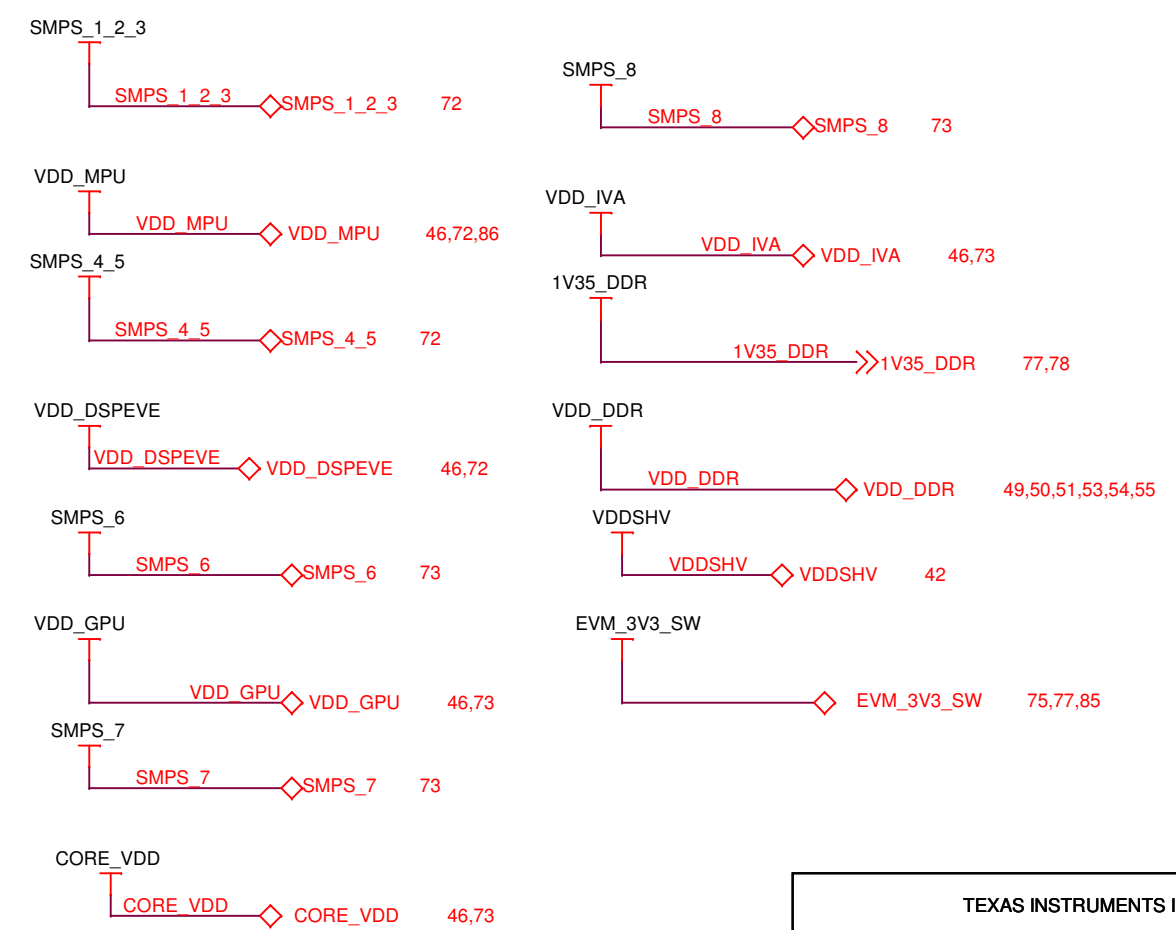
DARA Bd Interface Connector

DARA Bd can be interfaced to conduct more in-depth power measurements.

All Vdiff signal pairs (P & N) shown should be routed as pseudo-Diff Pair segments using min trace widths since these are low voltage sensing nets, not power delivery nets.



ETHERNET STRAPPING		
CLK_MAC_FREQ	Low	(25MHz) <-- CLK_TO_MAC is not used
RGMII_SEL0	High	(RGMII - 3COM)
RGMII_SEL1	High	(RGMII - 3COM)
SPEED0_STRAP	Low	(all speeds ok)
DUPLEX_STRAP	High	(full duplex)
AN_EN_STRAP	High	(auto-negotiation enabled)
SPEED1_STRAP	Low	(all speeds ok)
VDD_SEL_STRAP	High	(3.3V I/O)
NON_IEEE_STRAP	High	(allow IEEE non-compliant operation)
MAN_MDIX_STRAP	Low	(straight through mode)
MAC_CLK_EN_STRAP	Low	(disable CLK_TO_MAC output)
MULTI_EN_STRAP	Low	(single endpoint during auto-negotiation)
MDIX_EN_STRAP	High	(auto MDIX pair swap enable)



TEXAS INSTRUMENTS INCORPORATED			
Title: VAYU EVM			
Page Contents: POWER MONITOR I2C ADDRESS			
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Item#	Init Date	Priority	Status	Description
				ASST FROM G3 TO H PWB FROM G TO H LOGIC FROM G4 TO H
ER35				Upgrade Vayu Processor to ES 2.0 From 104183-0002R to 104183-0003R From X5777AXGABC to X5777BXGABC Create new Vayu part # 104183-0003R IC_BGA_VAYU_PROCESSOR GP_ES2 0, 9/11/2015 X5777BXGABC
ER37				Sheet 49, 53 Update memory to 4GB total U115, U116, U88, U69, U67 From 104177-0125R To 104695-0125R M14141512M1FPA-125-AS2-E (T) M65 and M66 From 104254-0012R To 104694-0125R M1418112M1FPA-125-AS1-A (T)
ER38				Change Boot voltages for MPUCORE to 1.15V U45 FROM 104252-0005B-T1 to 104252-0006B-T1 Create new PMIC flash number 104252-0006B-T1 and 104252-0006R T1 Part # P0691A31712018G1
ER39				Sheet 71 Add note about LDO 3 current The TPS65933 PMIC LDO3 output has a current limit of 300 mA If all PHYs are used concurrently (not expected in most systems) then the current requirement for the PHYs can exceed this limit. The System use case should be analyzed to verify that the power is less than 300 mA. If LDO3 is used to power the PHYs, if greater than 300 mA is required, contact your TI Representative to identify an alternate implementation.
ER40				Sheet 12 Update MMC2_DAT[7:0]CMD Pulges with 47K R404, R405, R406, R414, R422, R423, R426, R428 From R0402-NOPOP to 101370-4703R R410, R417 From 102145-4993R to 101370-4703R
ER41				Sheet 16 Update SD Data[0]CMD to 47K R19, R18, R16, R15, R14 From 101370-1003R to 101370-4703R
ER42				Sheet 39 Add pull-up to TMS (silicon does not include PU or PD, so floating) Add R829, 47K, 101370-4703R Change R759 From 0 to 100 From 101370-0001R To 101370-1001R This limits current into VREF with Lauterbach adapter plugged in backwards.
ER43				Sheet 76 Investigate Power sequence of ENET MAC (core before IO) Change the 2.5V PHY power sequence to track EVM_3V3 as recommended in nat 7.17 of the datasheet Add C705, 101007-0200R, 2.2uF Add R11, 101370-4703R, 47K Add R832, 100642-1073R, 107K 2.5v ramp speed up to match the 3.3v/1.8v ramps. With C19 installed the 2.5V was delayed until after ENET reset. Change C19 From 102098-1102R to 00402-NOPOP
ER44				Sheet 55 Move DDR termination (net DDR2_CKE) to discrete resistor (so can be populated for Suspend to RAM) Add R830 49.9, 102145-4993R
ER45				Update part body of SN74AVC0245RH1 devices. Layout only change to improve mfg.
ER46				Sheet 87 Update reverse battery protection to TI smart diode solution using LMT4610 U8 From 103038-0001R To 104635-0001R Q5 From 102098-0001R To 104283-0001R ADD C708 101415-0220R ADD C707 103895-1220R ADD D1 101808-0013R ADD D2 101808-0014R ADD TP831 TP-18R08-NO-POP
ER47				Sheet 76, 83, 84 Ethernet PHY core 1.8V leakage to 3.3V rail. Use load switch and duplicate power up circuitry used on 3.3V supply so it can be adjusted independently. ADD C708 00603-NOPOP C709 100893-1223R R833 100642-1073R R12 101370-4703R U145 104287-0001R
ER48				Sheet 79, 80, 84, 85 Current measurement R changes to 10mOhm R156 From 104226-0001R To 101396-0001R R475 From 104286-0002R To 101396-0001R R155 From 104226-0001R To 101396-0001R R187 From 104297-0002R To 102698-0001R R482 From 104297-0002R To 102698-0001R R669 From 102698-0006R To 101396-0001R R690 From 102698-0006R To 101396-0001R R180 From 104226-0001R To 101396-0001R R181 From 104226-0001R To 101396-0001R
ER49				PD free marking in silk screen
ER50				FCC marking in silk screen. *For evaluation only, not FCC approved for re
ER51				Sheet 74 C51 change to 25V cap from 16 V on 12 V input FROM 101390-0102R TO 104700-0102R
ER52				Sheet 39, 88 Add DARA power measurement and remove unused CT00 JTAG connector Delete J14 NO-POP R699 101370-0001R R705 101370-2200R R706 101370-0001R R707 101370-2200R R767 R0402-NOPOP R768 R0402-NOPOP R769 R0402-NOPOP Add J18 104610-0040R
ER53				Sheet 33 Remove pulldown on HEM1_HPD_B. The TPD device has internal pulldown of 10K and dual 10K is higher load than some monitors can support. R306 from 103158-1003R to R0201-NOPOP

Preliminary Information - Subject to change

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