OMAP5912 Multimedia Processor Device Overview and Architecture Reference Guide

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Preface

Read This First

About This Manual

This document introduces the setup, components, and features of the OMAP5912 multimedia processor and provides a high-level view of the device architecture.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.

Related Documentation From Texas Instruments

Documentation that describes the OMAP5912 device, related peripherals, and other technical collateral, is available in the OMAP5912 Product Folder on TI's website: www.ti.com/omap5912.

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OMAP5912 Device Overview

This document introduces the setup, components, and features of the OMAP5912 multimedia processor and provides a high-level view of the device architecture.

1 Overview

OMAP5912 is the next generation of OMAP processors and succeeds the Texas Instruments OMAP5910 processor. It is built with TI 130-nm process technology and has dual input/output voltage (1.8V−3.3V) capability. Like its predecessor, it is fully programmable to perform one or more of the following personal communication system tasks:

- Call manager
- Mail/fax reader/composer
- Internet access
- Personal digital assistant (PDA)
- Personal information management (PIM)
- Multimedia engines

This system is optimized for various multimedia codecs, such as:

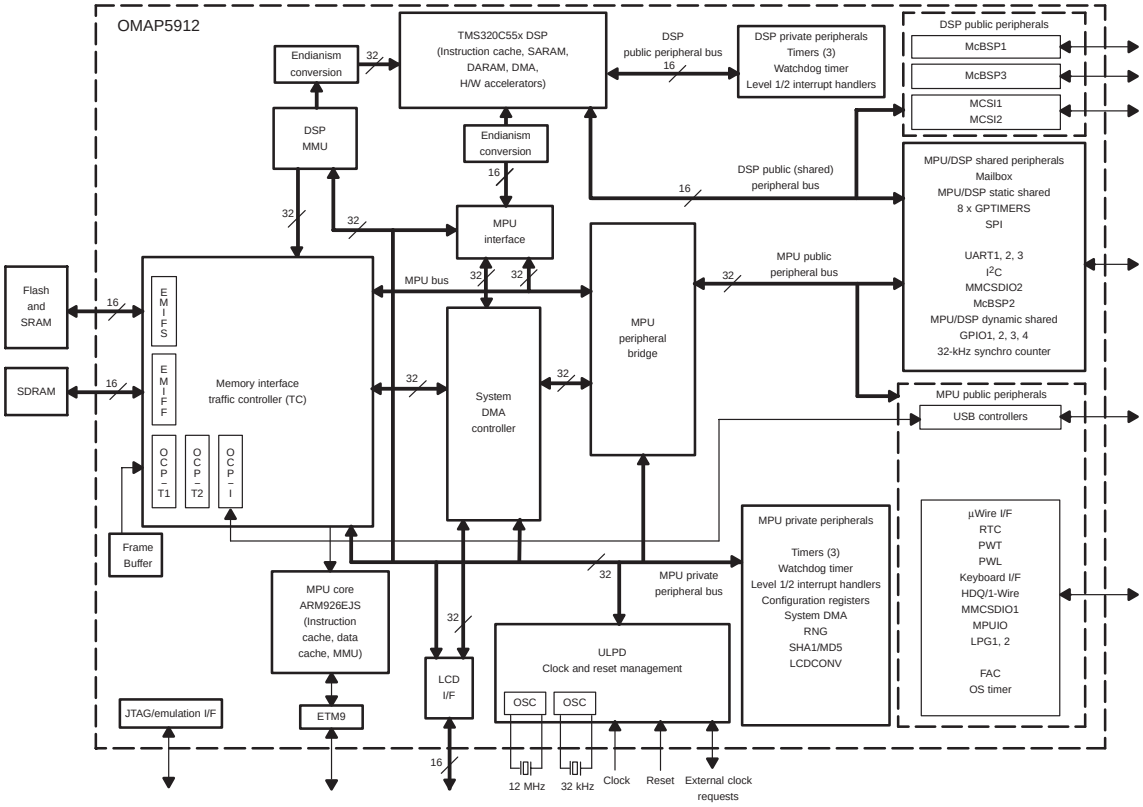
- MPEG4
- MP3
- JPEG
- H.263

Furthermore, it is capable of running advanced speech applications:

- Text to speech
- Speech recognition

Figure 1 shows OMAP5912 at the top level.

Figure 1. Top-Level OMAP5912



The OMAP5912 includes the microprocessor unit (MPU) core subsystem, the digital signal processor (DSP) core subsystem, the system direct memory access (SDMA), and part of the L3 and L4 interconnects. All other components are associated with the OMAP gigacell revision 3.2.

1.1 Subsystems

The chip subsystems have these characteristics:

- The MPU core subsystem is based on the ARM926EJ core, which performs most operations on the chip.
- The DSP core subsystem is based on a TMS320C55x™ DSP core, which performs intensive data computing tasks.
- The internal memory subsystem (frame buffer) is a single-port SRAM.
- The system DMA helps the MPU core perform data memory transfer-specific tasks, leaving a million more instructions available per second (MIPS) for both processors.
- The system components (ULPD, oscillators, etc.) are responsible for managing system interactions, such as interrupt, clock control, and idle.
- The memory interfaces define the system memory access organization of OMAP5912.
- The peripheral subsystem defines all of the components used to interface OMAP5912 with specific external devices, such as keyboard and smart display.
- The device features two types of interconnectivity:
  - The L3 interconnect is the memory interconnection among the MPU core, DSP core, DSP/System DMA, and an external host (through USB interface).
  - The L4 interconnect provides all of the peripheral interconnections among the MPU core, DSP core, and DSP/System DMA.

1.2 SDRAM/DDRAM Memory Interface

The external memory interface fast (EMIFF) is an synchronous dynamic RAM (SDRAM) controller that manages all accesses by the various initiators of an OMAP system. It can support one 16-bit device or two 8-bit devices. The external interface data bus width is always 16 bits.

The following devices are supported:

- Standard single-data-rate SDRAM
- Low-power single-data-rate SDRAM (mobile SDRAM)
- Low-power double-data-rate SDRAM (mobile DDRAM)

In terms of capacity and organization of the memory components that can be attached, the EMIFF can handle:

- 1G-bit, 512M-bit, 256M-bit, 128M-bit, 64M-bit, and 16M-bit devices.
- 2-bank or 4-bank devices for 16M-bit or 64M-bit devices.
- 4-bank devices only for any other capacity.
- x8 (two devices) or x16 (single device) data bus configuration, except for the 1G-bit device. The EMIFF supports only two x8, 512M-bit devices and a single x16, 1G-bit device (128 megabytes, maximum memory configuration).

1.3 Synchronous/Asynchronous Burst Memory Interface

The synchronous/asynchronous external memory interface slow (EMIFS) supports most common memory interface protocols through flexible programming and timing signals control.

The EMIFS controls up to six devices without adding any external logic through six independent chip-selects (CSs) and through dedicated memory interface control signals.

1.4 Other Memory Types

OMAP5912 includes multiple serial interfaces that can be used to connect multiple types of memories, including up to two multimedia cards through the multimedia memory card interfaces (MMC/SDIO).

1.5 Serial Interfaces

OMAP5912 provides several serial interfaces:

- A master/slave serial port interface (SPI), enabling serial data transfer compatible with common SPI protocol.
- Three multichannel buffered serial port (McBSP) peripherals, enabling emulation of the following serial protocols:
  - Serial port interface
  - An I2S-compatible interface
  - A DSP core serial input/output
  - Multichannel time division multiplexer
- An I^2C with multimaster and slave support.
- A universal serial bus (USB) interface client, host, and USB On-The-Go configuration.
- A serial µWire interface.
- Two multichannel serial interfaces (MCSI).
- Three universal asynchronous transceivers (UART1, UART2, UART3).
- HDQ and 1-Wire interfaces.

1.6 Camera and Display Interfaces

There are various video interfaces:

- The camera IF is an 8-bit parallel interface with horizontal/vertical camera input signal.
- The OMAP internal LCD controller that enables simple LCD interfaces and control.

1.7 Emulation and Test Interfaces

OMAP5912 has these emulation and test interface features:

- JTAG emulation capability for non-real-time debug.
- An embedded trace macrocell (ETM) to enable real-time trace of the MPU core subsystem operations.
- Concurrent DSP core and MPU core emulation.

1.8 General-Purpose Interfaces

OMAP5912 includes dedicated modules to support specific modulation and control of general-purpose inputs and outputs:

- General-purpose input/output (GPIO) modules allow the monitoring and control of device input/output pins with event detection for external interrupts support.
- The pulse width tone (PWT) module provides output pins with waveform control for tone generation.
- The pulse width light (PWL) module allows output pins waveform control for brightness light control.
- Two light pulse generator (LPG) modules allow output pins waveform control for LED blinking control.
- Three general-purpose timers enable output pins waveform control for pulse width modulation support.

1.9 Interfaces Multiplexing

Because of the device I/O limitations, the interfaces are not accessible at the same time, and some of them are multiplexed. For more detail on I/O multiplexing and control, see the *OMAP5912 Applications Processor Data Manual (SPRS231)* for complete information.

1.10 Interface Usage Examples

This section contains three examples of usage:

- Audio interface
- Bluetooth™ interface
- Modem connection

1.10.1 Audio Interfaces

OMAP5912 supports a modem audio PCM codec interface, a modem voice interface, and a Bluetooth™ voice interface simultaneously. These interfaces can be provided through various peripherals:

- McBSP, which is compliant with the I^2C standard and can be connected to an audio codec.
- MCSI, which can be used as voice interface (see section 1.10.2 and section 1.10.3).

1.10.2 Bluetooth Interface

The Bluetooth interface has the following data, voice, and power management interfaces:

- The data interface can be provided by UART1.
- The voice interface can be provided by MCSI1.
- The power interface is the clock request pins.

1.10.3 Modem Connection

An example proposes ways to connect a modem to the device:

- Using data, control, voice, and power management interfaces:
  - Data interface can be the McBSP2.
  - Control interface can be the UART2.
  - Power management interface is the clock request pins.
  - Voice interface can be the MCSI2.

2 OMAP5912 Description

Figure 1 shows the OMAP5912 in detail.

Table 1 through Table 8 describe the top-level partitioning. For more details on the core, see *OMAP5912 Multimedia Processor OMAP 3.2 Subsystem Reference Guide (SPRU749)*.

Table 1. MPU Core Private Peripherals

Peripheral Name	General Description
MPU core level 2 interrupt handler	There is one MPU core interrupt handler outside the OMAP 3.2 gigacell. It supports up to 128 interrupt lines. Both IRQ and FIQ are connected to MPU core interrupt handler level 1.
Watchdog Timer	A general-purpose timer with watchdog functionality clocked at 32 kHz.
Timers	Three 32-bit timers for general purpose housekeeping.
ULPD	System clock and reset module. Manages the idle mode, generates main reset to OMAP. Some peripherals clock through its APLL output to generate the OMAP input system clock.
RNG	Random number generator module.
SHA−1/MD5	Module that supports SHA−1 and MD5 hash algorithm.
GDMA handler	64 DMA requests are multiplexed to generate 31 DMA request lines to the system DMA.
OMAP5912 configuration	Controls the various configurations of the functions (I/O functions, debug functions, clock control).
LCD Controller	Supports passive monochrome (STN), passive color (CSTN), and active color (TFT) displays with sizes up to 1024x1024 pixels. Memory bandwidth may reduce performance on large displays.
LCDCONV	Enables conversion of the OMAP LCD 16-bit data bits into 18-bit data bits.

Table 2. DSP Core Private Peripherals

Peripheral Name	General Description
DSP DMA handler	DMA requests are multiplexed to generate 19 DMA request lines to the DSP DMA.
Watchdog Timer	A general-purpose timer with watchdog functionality clocked at 32 kHz.
Timers	Three 32-bit timers for general purpose housekeeping.
DSP core level 2.1 interrupt handler	There is one DSP core interrupt handler outside the OMAP 3.2 gigacell. It supports up to 64 interrupt lines. Only IRQ is connected to the DSP core level 1 interrupt handler. The DSP core interrupt handler module is derived from the MPU core interrupt handler module.

Table 3. MPU Core Public Peripherals

Peripheral Name	General Description
USB On-The-Go	A combination of the USB client and USB host, including an additional module (OTG module).
RTC	An embedded real-time clock module.
µWire	A serial interface that connects external devices such as EEPROM or LCD with µWire standard.
HDQ/1-Wire	Implements the hardware protocol of the master function of the Benchmark HDQ and the Dallas Semiconductor 1-Wire protocol.
MPU core IO	Provides MPU core GPIOs (general-purpose I/Os) and a keypad interface.
FAC	Frame adjustment counter.
PWT	Pulse width time.
PWL	Pulse width length.
2 X LPG	Two instances of a light pulse generation (LPG) module.
OS timer	32-kHz OS timer.
MMC/SDIO1	Multimedia card interface, compatible with digital memory card interface version 1.0.

Table 4. DSP Core Public Peripherals

Peripheral Name	Description
McBSP1	Can be used to interface with the I2S audio codec.
McBSP3	Can be used as an optical audio interface.
2 X MCSI	Two instances of an MCSI module.

All of the DSP core shared peripherals are also accessible by the MPU core through the MPUI internal port.

Table 5. MPU/DSP Core Statically Shared Peripherals

Peripheral Name	Description
MMC/SDIO2	Multimedia card interface, compatible with digital memory card interface version 1.0.
I^2C multimaster/slave	A generic serial link interface that controls several OMAP5912 external I^2C slave devices or slaves them to other OMAP5912 external I^2C master devices.
SPI master/slave	A master/slave serial port interface, running up to 19.2M bits/s in master or slave mode.
8x general purpose timers	All of these general-purpose timers can be configured to count either from the 32-kHz clock or from the system clock. Three of them are also used to provide two PWM signals at the boundary.
McBSP2	Used as communication processor data interface or I2S emulator.
UART1	A UART modem including autobaud. The maximum baud rate is 3.6M bits/s.
UART2	A UART modem with autobaud, as in UART1.
UART3	A UART IrDA enabling slow, medium, and fast configurations.

Each host peripheral access can be configured by software as the DSP core or the MPU core for each peripheral.

Table 6. MPU/DSP Core Dynamically Shared Peripherals

Peripheral Name	Description
4x GPIOs	There are four instances of 16-bit module general-purpose I/Os. Each module can generate its own interrupt. Several general-purpose I/Os are multiplexed with primary I/Os, some of which are connected directly with dedicated I/Os.
32-kHz synchronization counter	This is a simple upward counter clock used by the 32-kHz input clock to enable synchronization between modem and application chips when OMAP5912 is used in conjunction with a modem having the same clock input. As soon as the power-up reset input is released, the counter starts counting.

Each host peripheral access can be either the DSP core or the MPU core; the arbitration is performed in hardware.

Table 7 lists the dedicated modules available in OMAP5912, a general description of each module, and their corresponding functional specifications reference.

Table 7. Dedicated Modules

Module Name	Description
OCP interconnect	A synchronous interface enabling interconnection between the USB and the OCP-I port.
Boot ROM	A 64K-byte ROM accessible only by the MPU core.
Camera interface	Parallel interface that connects an external camera sensor.
Frame Buffer	This 256K−byte SRAM is used to store video frame before emission by the DSP/System DMA LCD channel to the external or internal LCD controller.

Table 8 includes the test modules used in OMAP5912, a general description of each module, and their corresponding functional specifications references.

Table 8. Test Modules

Module Name	Description
JTAG	The 1149.1 TAP controller IEEE compliant used to program the functional test modes.

2.1 OMAP3.2 Gigacell

The OMAP 3.2 gigacell used by OMAP5912 is called OMAP 3.2.

This gigacell features:

- ARM926EJ core, including:
  - ARM926EJS, supporting multiple operating systems (Symbian, Linux, WinCE, and others)
  - MMU with translation lookaside buffer (TLB)
  - L1 16K-byte, four-way set-associative instruction cache
  - L1 8K-byte, four-way set-associative data cache with write buffer
- MPU core level 1 interrupt handler
- Embedded trace macrocell module, ETM version 2.a in 13-bit mode configuration or in 17-bit demultiplexed mode configuration
- TMS320C55x™ (C55x™) DSP core, including:
  - Embedded ICE emulator interface through JTAG port
  - C55x™ DSP rev 2.11
  - L1 cache (24K bytes)
    - 16K-byte, two-way set-associative instruction cache
    - 2x 4K-byte RAM set for instruction
  - DARAM 64K-byte, zero wait state, 32-bit organization
  - SARAM 96K-byte, zero wait state, 32-bit organization
  - PDROM (32K bytes)
  - DSP/System DMA controller: 6 physical channels, 5 ports
  - DSP core trace module
  - Hardware accelerators motion estimation (ME), discrete/inverse discrete cosine transform (DCT/IDCT) and pixel interpolation (PI)
  - DSP core level 1 interrupt handler in the C55x™ DSP core
- DSP core MMU
- DSP core level 2 interrupt handler, which enables the connection to 16 additional interrupt lines outside OMAP. The priority of each interrupt line is controlled by software.

- DSP core interrupt interface, which enables the connection to the interrupt lines coming out of the level 2 interrupt handler and the interrupt lines requiring more priority. The outcome interrupt of this module is then connected to the C55x DSP core to be processed. This module is mainly used to ensure that all interrupts going to the DSP core are level-sensitive.
- DSP core peripherals:
  - 3x 16-bit DSP core private timers
  - 1x 16-bit DSP core private watchdog
- Mailboxes:
  - Four mailboxes are implemented:
    - Two read/write accessible by MPU core, read-only by the DSP core
    - Two read/write accessible by the DSP core, read-only by the MPU core

    Each mailbox is implemented with 2x 16-bit registers. When a write is done into a register by one processor, it generates an interrupt, released by the read access of the other processor.
- MPU core peripherals
  - 3x 32-bit private timers; their clock is either the OMAP3.2 reference input clock or the divided MPU core clock.
  - 1x 16-bit private watchdog; can be configured as a 16-bit general-purpose timer by software. Its clock is the OMAP3.2 reference input clock divided by 14.
- External LCD controller support in addition to the OMAP LCD controller
  - LCD controller with its own tearing effect logic
- Memory traffic controller
  - External memory interface fast (EMIFF) is a memory interface that enables 16-bit data SDRAM memory access.
  - External memory interface slow (EMIFS); it connects external device memories (such as common flash and SRAM memories).

L3 OCP-T1 and L3 OCP-T2 ports are provided to enable memory access from OMAP 3.2 gigacell on a standard basis protocol. Only the L3 OCP T1 is used to access the frame buffer.

- Emulator interface through JTAG port

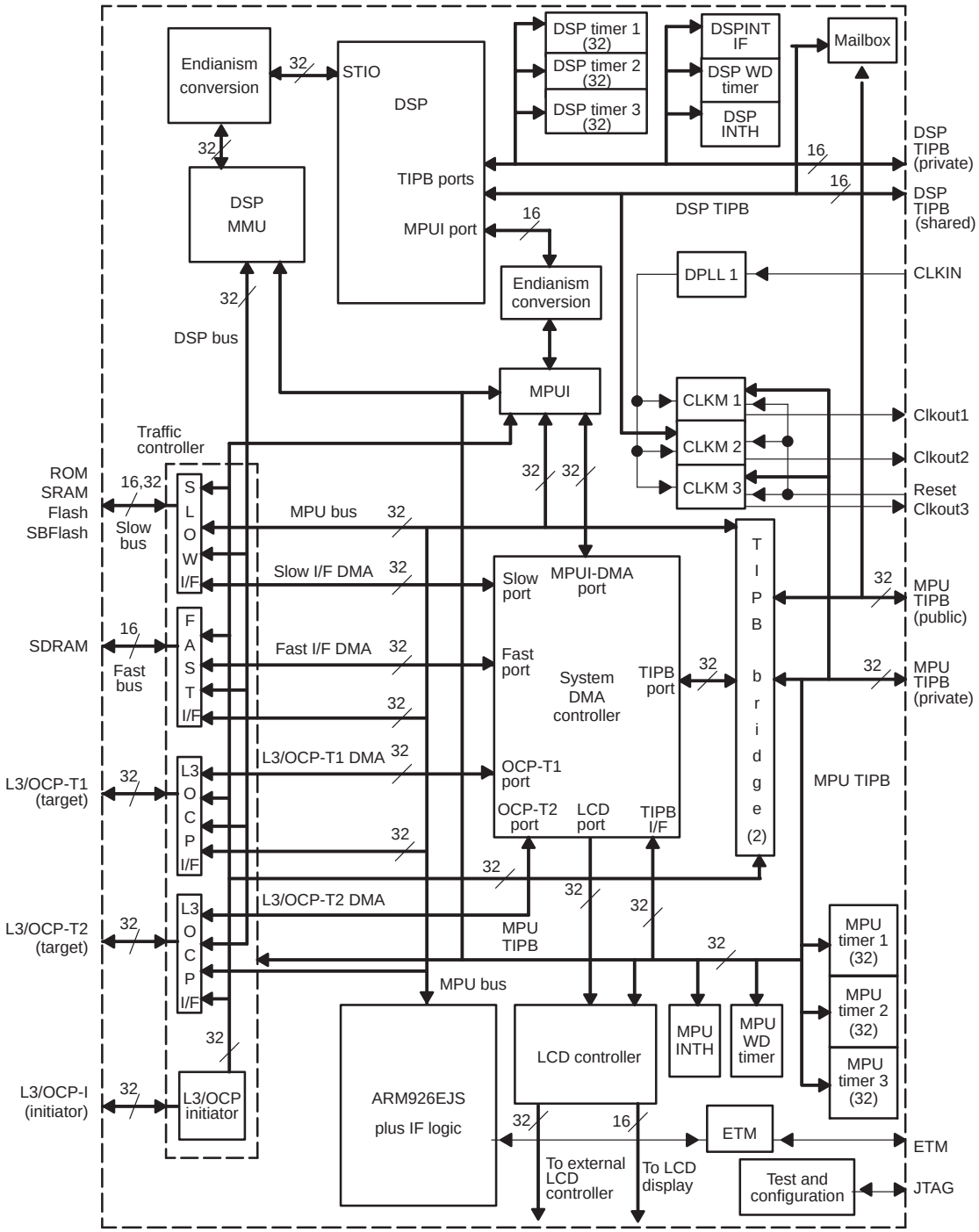
- System DMA, which consists of:
  - Seventeen logical channels
  - Seven physical ports + one for configuration
  - Four physical channels

  The ports are connected to the L3 OCP targets, the external memory, the TIPB bridge, the MPUI, and one dedicated port connected to an LCD controller. The system DMA controller can be controlled via the MPU core private TIPB or by an external host via the OCP-I port.

- One DPLL for the following clock domains:
  - MPU core traffic controller clock domain
  - DSP core clock domain

- Endianism conversion for DSP core
  - The DSP core uses big-endian format, whereas the MPU core uses little-endian format. Also, as a rule, the OMAP5912 chip works in little endian. Thus, the endianism conversion is useful for all memory or peripheral accesses from on-chip peripherals or all shared memories to the C55x DSP core.

Figure 2. OMAP3.2 Gigacell



2.2 Module Descriptions

2.2.1 Clock and Reset Generation

32-kHz Oscillator

The 32-kHz oscillator uses a 32-kHz external quartz. It can be used to generate the 32-kHz clock on the chip. It can be disabled when the 32-kHz is an external source provided by an external clock.

12-MHz Oscillator

This oscillator is to be used with a 12-MHz or 13-MHz external quartz.

The 12- or 13-MHz oscillator allows the generation of the 48 MHz the USB requires. The APLL located in the ULPD provides the x4 factor. The 12- or 13-MHz clock is used as the input clock of the ULPD. The 12- or 13-MHz oscillator is on during awake and big sleep modes. It is off during deep sleep mode. The wake-up sequence is handled from the power management module.

Ultralow-Power Device (ULPD)

The ULPD generates and manages clocks and reset signals to OMAP and to some peripherals. It controls chip-level power-down modes and handles chip-level wake-up events.

The ULPD can handle the high-frequency oscillator on/off sequences, when used, and provides the resets to OMAP. It also allows configuration of the clock sources of the device and management of the APLL interface.

Clock and Reset Architecture

The global clock distribution and the reset distribution scheme are described in the *OMAP5912 Multimedia Processor Initialization Reference Guide (SPRU752)*.

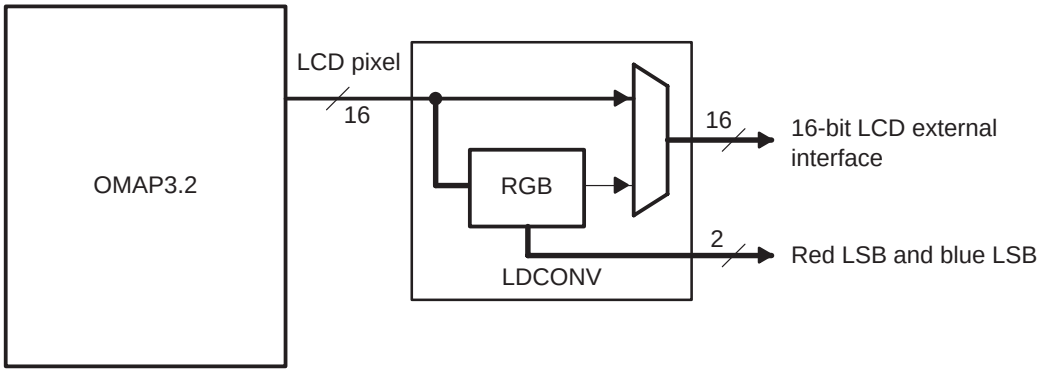
2.2.2 Peripherals Subsystem

LDCONV

This module provides 16-bit to 18-bit LCD data conversion to the OMAP3.2 LCD interface. It supports two operating modes:

- The 16-bit LCD
- The 18-bit LCD

Figure 3. LDCONV Integration



Frame Adjustment Counter (FAC)

The FAC consists of a frame synchronization capture pin (intended to count the number of rising edges of a frame synchronization signal from a synchronous serial port) and a frame start capture pin (intended to count the number of rising edges of a USB frame start signal). The respective count values can then be used by system software to adjust the duration of the two time domains with respect to each other, in order to reduce the overflow and underflow.

The FAC module is used to control the number of McBSP2 and USB frames.

Light Pulse Generator (LPG)

The LPG module is used to control the blinking period of an external LED.

SHA-1/MD5 Accelerator

The SHA-1/MD5 module provides hardware-accelerated hash functions. It can run either the SHA-1 algorithm in compliance with FIPS 180-1 standard, or the MD5 message-digest algorithm developed by Rivest.

Random Number Generator

The random number generator (RNG) module provides a true, nondeterministic noise source to generate keys, initialization vectors (IVs), and other random number requirements. It is designed for FIPS 140-1 compliance, facilitating system certification to this security standard. An ANSI X9.17, annex C postprocessor is available to meet the NIST requirements of FIPS 140-1.

Camera Interface

The camera interface supports 8-bit parallel image data port and horizontal/vertical signal ports separately (stand alone synchronization method).

Real-Time Counter

The real-time counter (RTC) block is an embedded real-time counter module, directly accessible from the MPU core.

Basic functionalities of the RTC block are:

- Time information (seconds/minutes/hours) directly in BCD code.
- Calendar information (day/month/year/day of the week) directly in BCD code, up to year 2099.
- Interrupt generation, periodically (1s/1m/1h/1d period), or at a precise time of the day (alarm function).
- 30-s time correction: oscillator frequency calibration using reference clock input.
- Can be used in standalone when rest of the chip is powered down.

OS Timer

A programmable interval timer is required to generate a periodic interrupt, also called a system clock tick, to the OS. This is used to keep track of the current time and to control the operation of device drivers.

Pulse Width Time (PWT)

This module generates a modulated frequency signal for the external buzzer. Frequency is programmable between 349 Hz and 5276 Hz, with 12 half-tone frequencies per octave. The volume is also programmable.

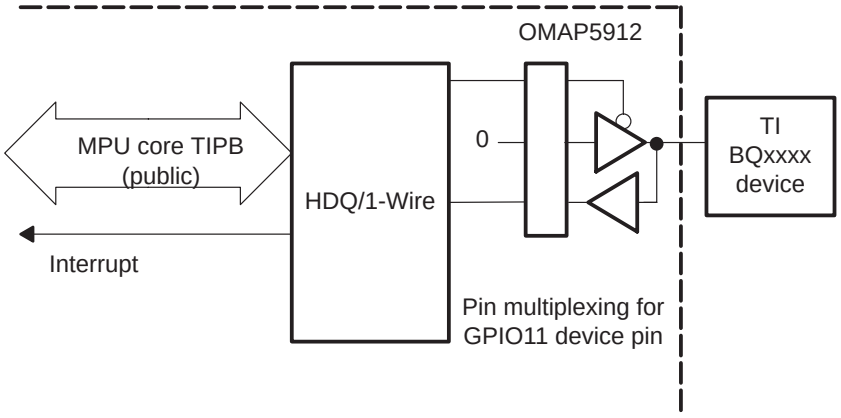
Pulse Width Length (PWL)

This module allows the control of the backlight of the LCD and the keypad by employing a 4096-bit random sequence. This voltage level control technique decreases the spectral power at the modulator harmonic frequencies. The block uses a switchable 32-kHz clock.

HDQ/1-Wire Battery Monitoring Serial Interface

The HDQ/1-Wire battery monitoring serial interface module implements the hardware protocol of the master function of Benchmark's HDQ and Dallas Semiconductor's 1-Wire protocol.

Figure 4. HDQ/1-Wire Overview

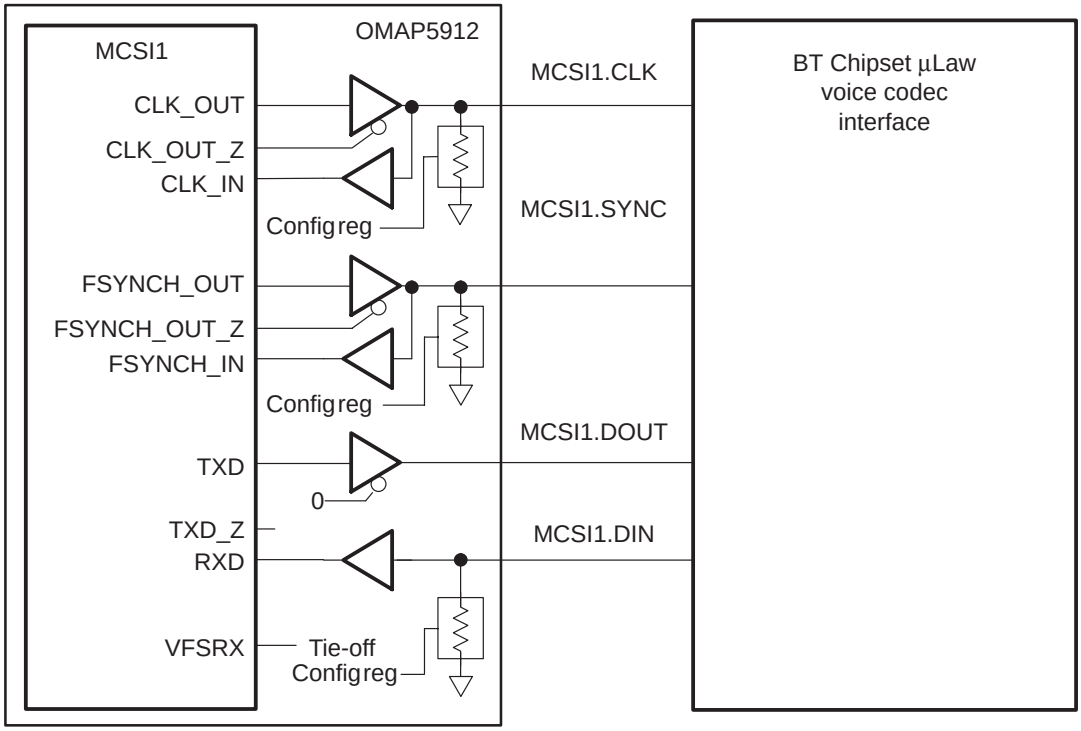


MCSI1

The MCSI1 is a multichannel serial interface, half-duplex, master/slave. MCSI1 can be used to interface the Bluetooth voice module.

In this case, the interface is an 8-kHz frame serial port, 8-bit data transfer. It is a 4-wire interface with a bidirectional serial clock and frame synchronization. If the Bluetooth baseband device is not synchronous with the modem network, the Bluetooth voice interface receives the clock and frame synchronization from MCSI1.

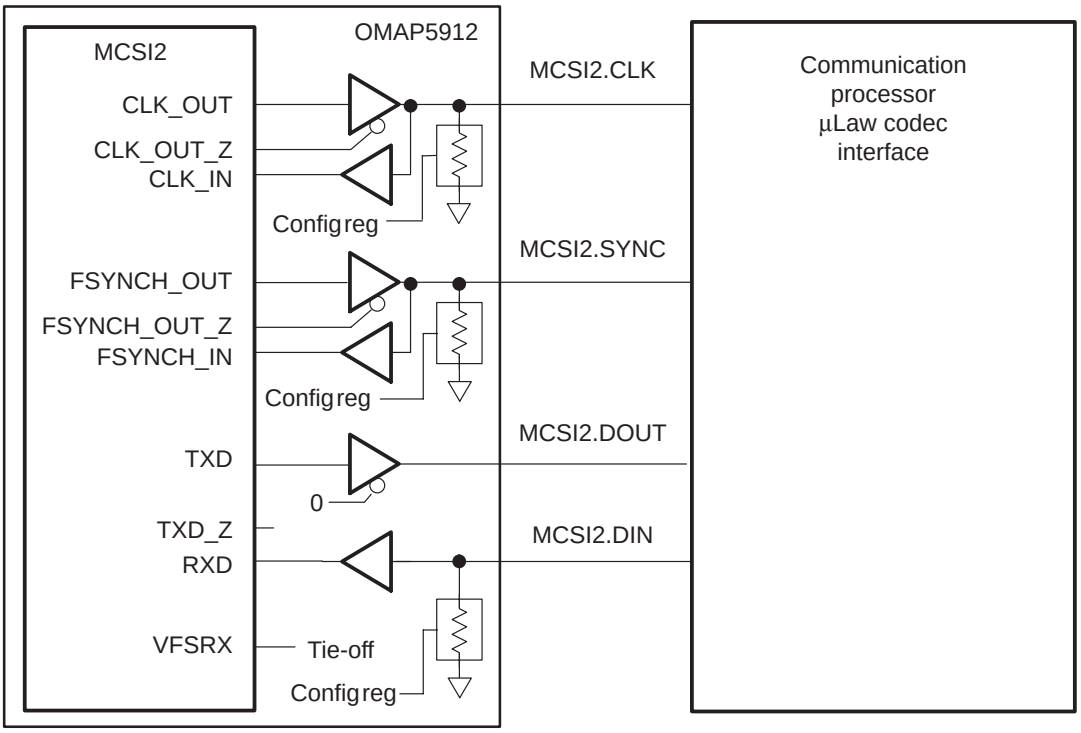
Figure 5. MCSI1 Interface



MCSI2

The MCSI2 is a multichannel serial interface, half-duplex, master/slave. MCSI2 can be used to interface the modem voice module. In this case, it is an 8-kHz frame serial port, 8-bit data transfer. Clock and frame synchronization are bidirectional.

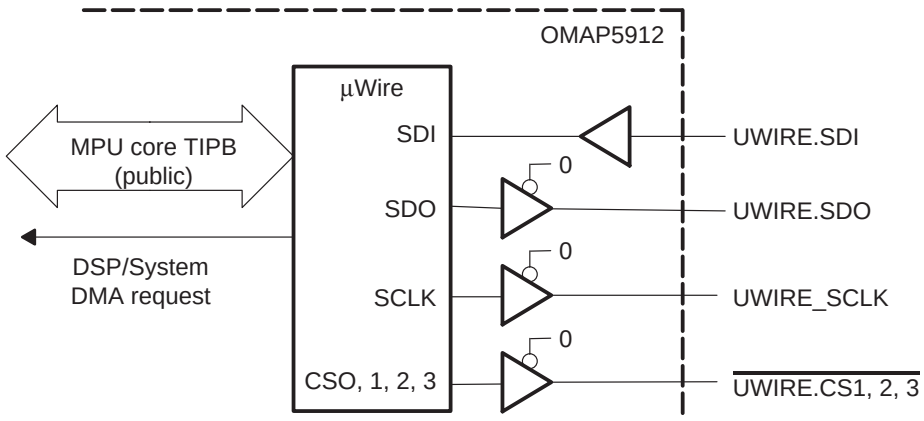
Figure 6. MCSI2 Interface



MicroWire

The MicroWire, or μWire, module is a serial interface that drives external devices like EEPROM or LCD with μWire standard.

Figure 7. μWire Interface



MPU core GPIOs

The MPU core has a 16-bit GPIO (MPUIO) with a programmable debouncing circuit. It can handle maskable interrupt generation on high-to-low or low-to-high transitions on pins configured as input.

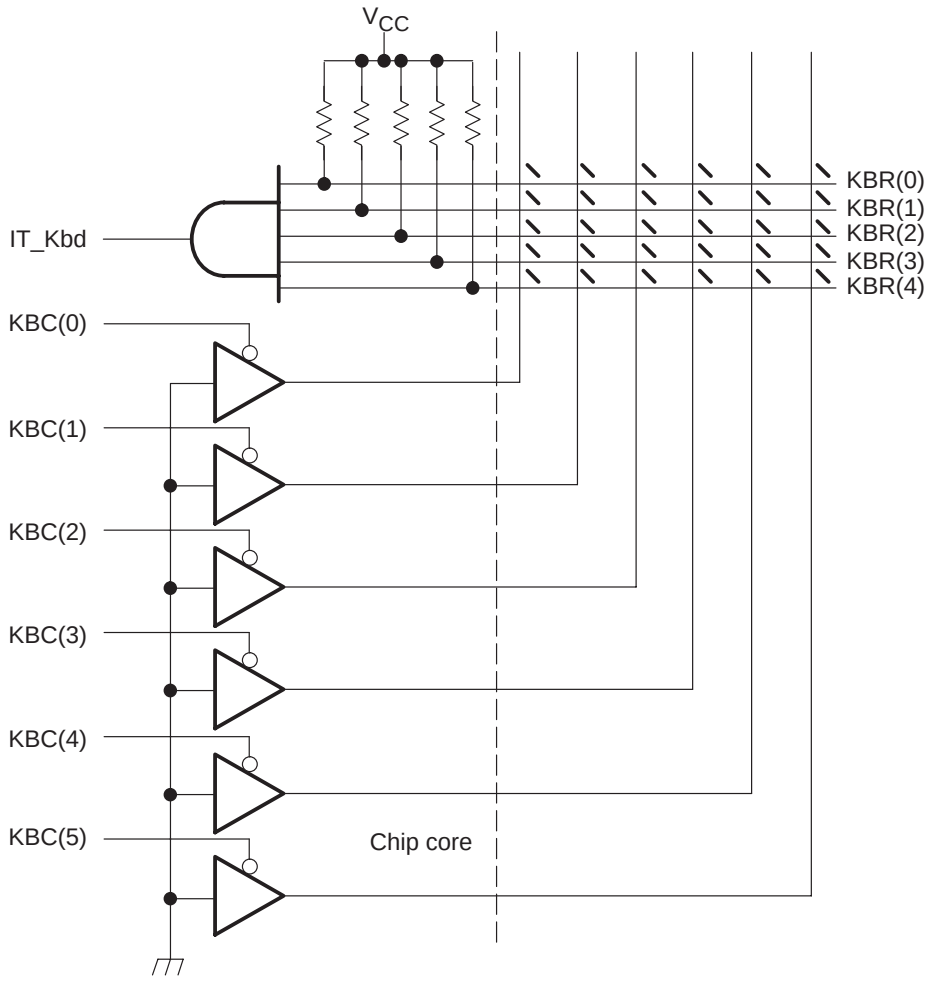
Keyboard

The keyboard interface is a 6 x 5 or 8 x 8 interface. Figure 8 shows the 6 x 5 interface.

The keyboard is connected to the chip using:

- KBR (7:0) input pins for row lines.
- KBC (7:0) output pins for column lines.

Figure 8. 6x5 Keyboard Connection



UARTs

There are three identical UART modules in OMAP5912:

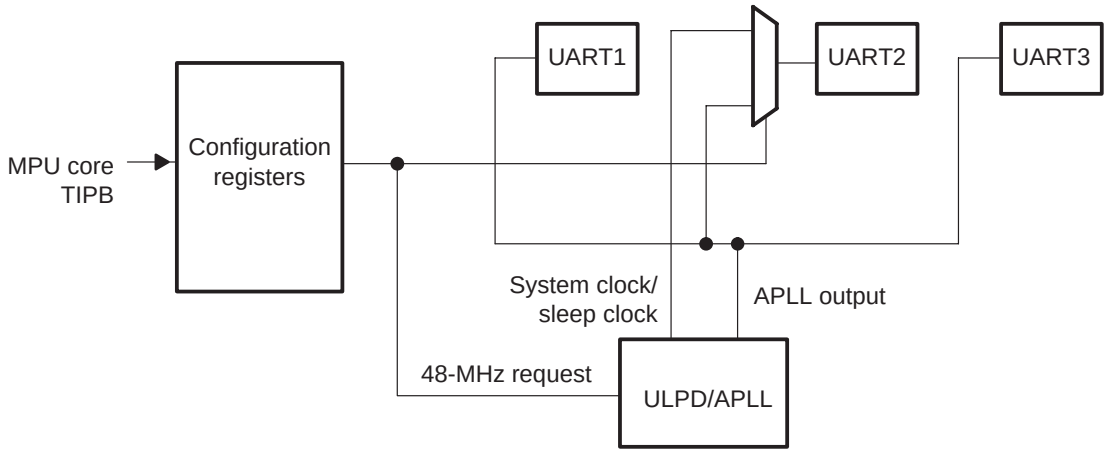
- UART1
- UART2
- UART3

UART1 and UART3 also support the IrDA mode, if the proper set of module inputs/outputs has been configured.

UART Clocking Scheme

Figure 9 describes the clocking scheme used to enable the UARTs to generate their requested baud rate.

Figure 9. UART Clock Scheme



The clock sources for UART1/UART3 can be the APLL output.

The clock source for UART2 can be:

- The system clock or the sleep clock
- The APLL output

Selection of the clock source is done statically from the configuration register, which is accessible by software through a normal MPU core peripheral access.

Available I/Os per UART

Table 9. Available I/Os per UART

Signal	UART1	UART2	UART3
RX	Yes	Yes	Yes
TX	Yes	Yes	Yes
RTS	Yes	Yes	By mux
CTS	Yes	Yes	By mux
DSR	By mux	No	By mux
DTR	By mux	No	By mux
SD_IRDA	No	No	By mux
BD_CLK	No	Yes	No

For more details on I/Os, see the *OMAP5912 Applications Processor Data Manual (SPRS231)*.

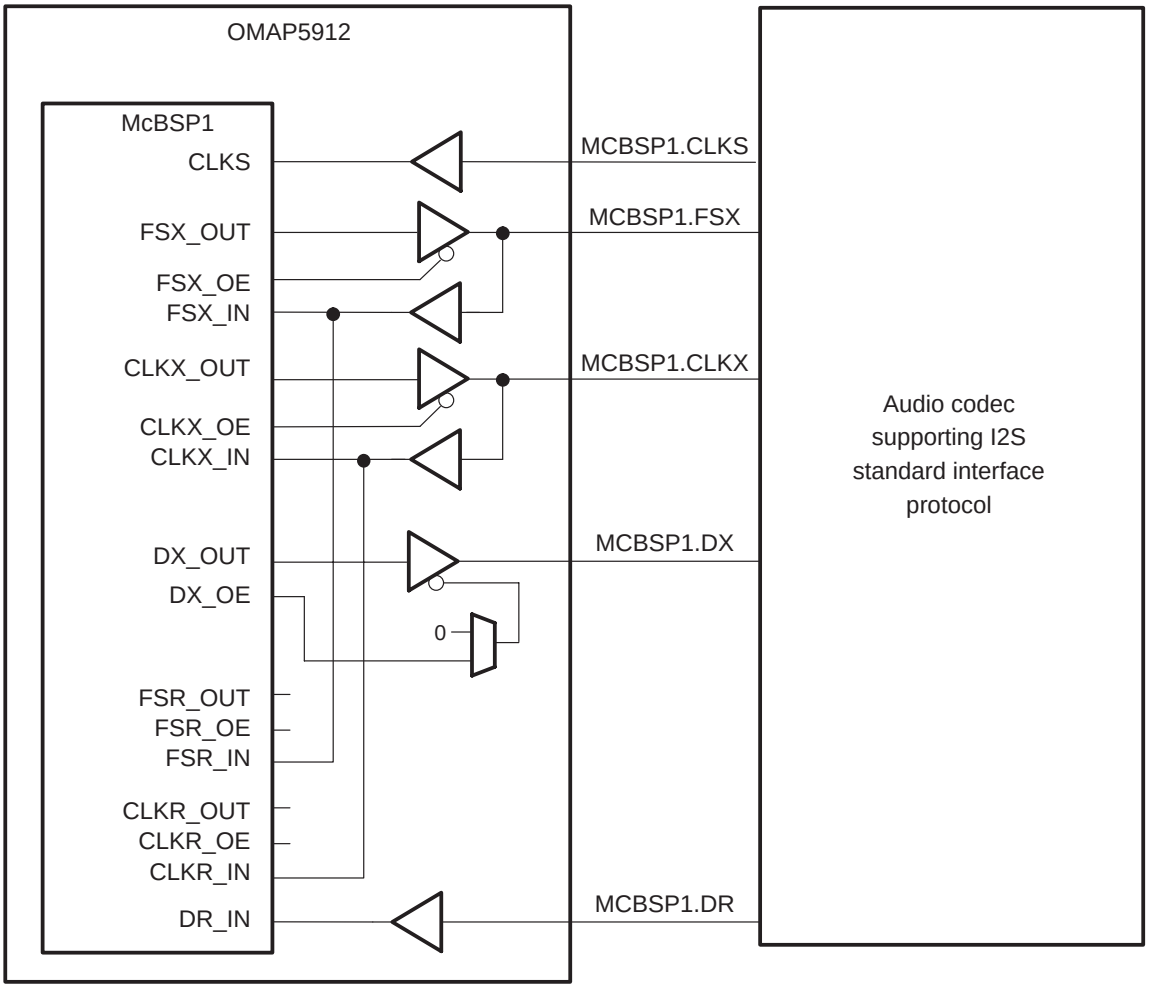
McBSP

The McBSP is a full-duplex serial interface. For example, it can be used to emulate the I2S protocol for interface to an external codec audio device.

McBSP1

McBSP1 is an instance of the McBSP module. The McBSP1 can be used to interface with an audio codec compliant with the I2S protocol (5-pin interface). The codec can provide the reference clock. The serial clock and the frame synchronization can be either inputs or outputs. When outputs, they are derived from the reference clock.

Figure 10. McBSP Interface With I2S-Compliant External Codec

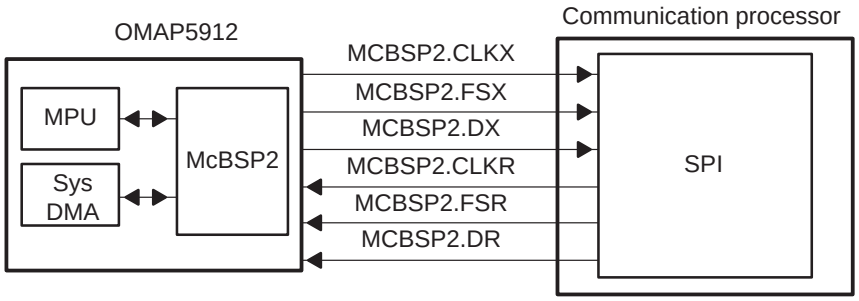


McBSP2

McBSP2 is also an instance of the McBSP module. It can be used either to support SPI mode or to emulate an I2S serial link.

The McBSP2 interface differs from the McBSP1 interface in that there is no capability to connect an OMAP5912 external reference clock to it.

Figure 11. McBSP Interface With Communication Processor



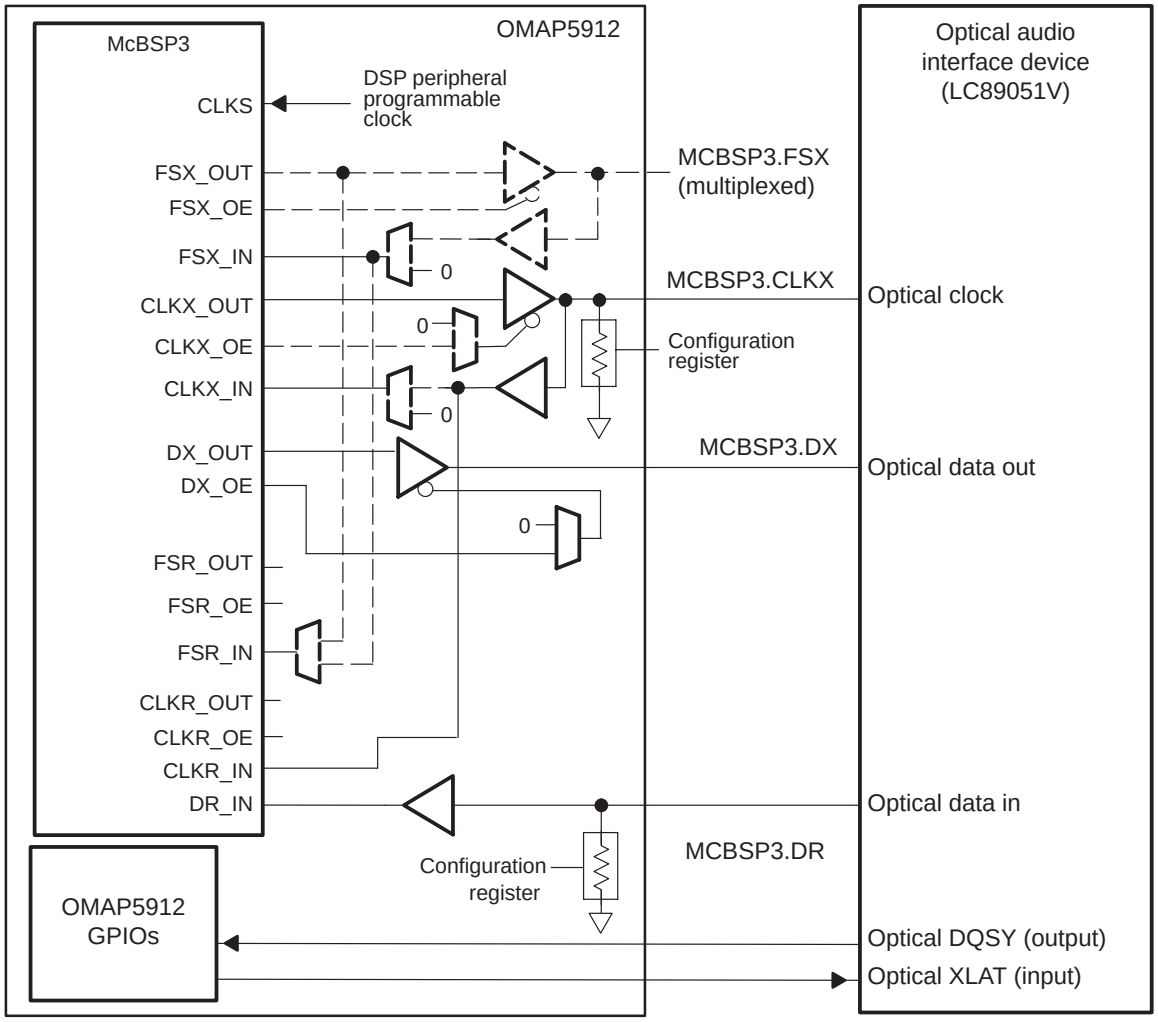
Note: To support I2S master and slave modes, McBSP2_CLKX, McBSP2_XSYNC, McBSP2_RSYNC, and McBSP2_CLKR are inputs/outputs. They are used unidirectionally for the communication processor connection.

McBSP3

McBSP3 is the third instance of the McBSP module. There are two connection modes for this McBSP:

- The first connection mode is a 3-pin interface. The frame synchronization is internally looped back (FSXO to FSRI), as is the clock. This is the default reset configuration. In this case, the McBSP3 is half-duplex, master for transmission, slave for reception. With the assistance of two GPIOs, this McBSP mode (3 pins) can be configured to connect to an external optical audio interface device, such as the Sanyo-LC89051V.
- The second connection mode is a 4-pin interface. The frame synchronization signal is multiplexed to allow a 4-pin McBSP interface. The frame synchronization is bidirectional, as is the clock. In this case, the McBSP3 is half-duplex, master/slave for transmission, slave for reception; enabling an additional I2S emulator.

Figure 12. McBSP3 Interface Connected to Optical Device



Notes: 1) The solid lines show the reset connection configuration, whereas the dashed lines show the second connection configuration.

2) Selection of the interface (3-pin or 4-pin) is done by the software through the CONF_MOD_CTRL_1 register.

Serial Port Interface (SPI)

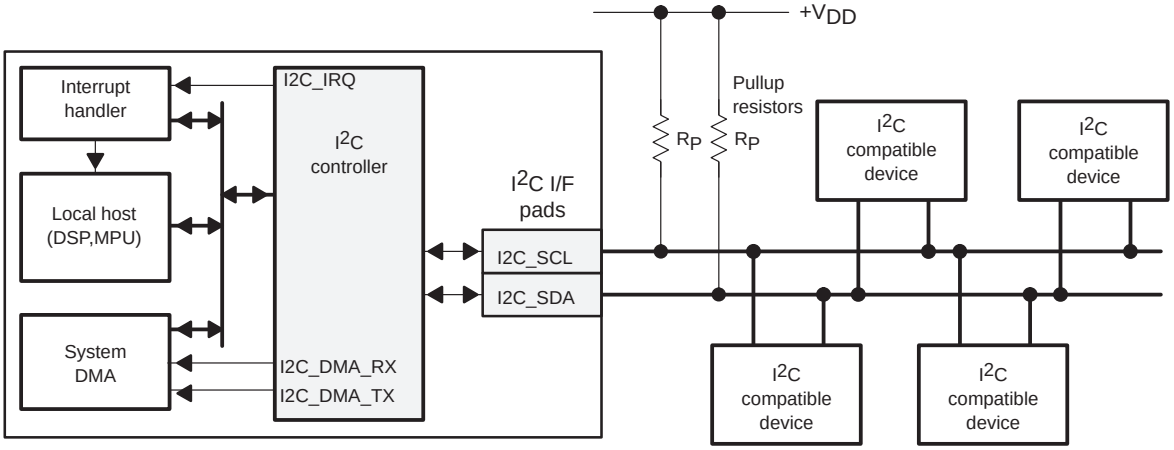
The serial port interface is a bidirectional, four-line interface dedicated to the transfer of data to and from external devices offering a four-line serial interface.

Inter-Integrated Circuit (I^2C)

The multimaster I^2C peripheral provides an interface between a local host (LH), such as an MPU core or DSP core processor, and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit/receive up to 8 bits of data to or from the LH device or a DSP/System DMA through the two-wire I^2C interface.

This I^2C peripheral supports any slave or master I^2C-compatible device. Figure 13 shows an example of a system with multiple I^2C-compatible devices, in which the I^2C serial ports are connected together for a two-way transfer from one device to other devices.

Figure 13. I^2C System Overview



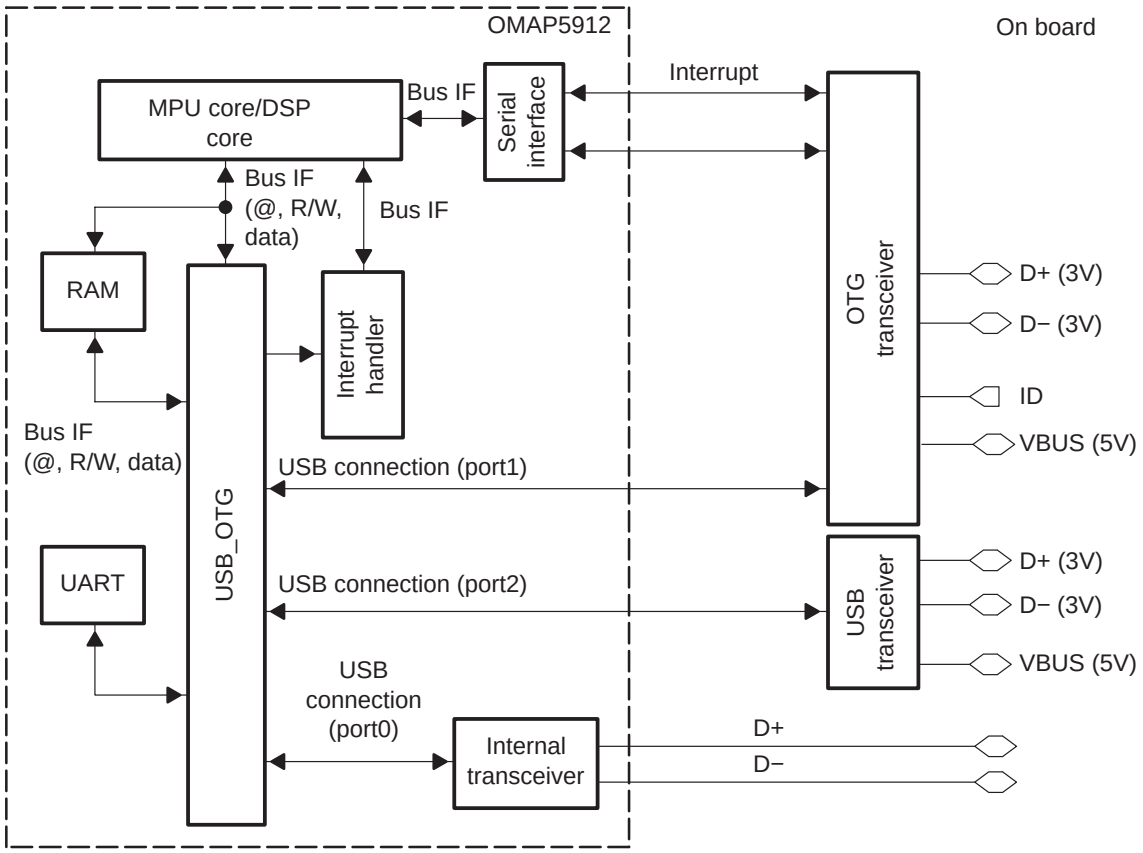
USB On-The-Go (OTG)

The OTG module provides a USB device controller, a three-port USB host controller, and an OTG controller that is capable of providing USB On-The-Go functionality, using the USB device controller and one port of the USB host controller.

The main features of USB On-The-Go are:

- ❏ USB specification version 1.1 compatible with OTG enhanced features
- ❏ USB host is Open HCI Rev 1.0 compatible.

Figure 14. USB OTG Integration at System Level



Note: OTG functionality requires a special transceiver external to OMAP5912. The communication between the transceiver and the controller is done through an I^2C communication channel.

In this case, the USB OTG module port 2 is connected to an external USB OTG transceiver, port 1 is connected to a USB transceiver, and port 0 is connected to the integrated USB transceiver.

GPIO

There are four instances of the GPIO modules (GPIO1, GPIO2, GPIO3, GPIO4) included in OMAP5912.

Each GPIO module supports:

- Data input/output register
- Event detection capability:
  - To generate two synchronous interrupts in active mode
  - To generate a wake-up request while the system is in idle mode

This peripheral allows the connection of 16 dedicated pins configurable either as input or output for general purposes.

Eight data output lines of the GPIO3 are ORed together to generate a global output line at the OMAP5912 boundary.

32-Bit General-Purpose Timer

There are eight instances of this timer. It contains a free-running upward counter with autoreload capability on overflow. The timer counter can be read and written on the fly while counting. The timer module includes compare logic to allow an interrupt event on a programmable counter matching value. A dedicated output signal can be pulsed or toggled on overflow and match event. This offers timing stamp trigger signal or PWM (pulse width modulation) signal sources.

All of the general-purpose timers have the capability to run either from the system clock or from the sleep clock (32-kHz clock).

Note:

Three of the eight dual-mode timer PWM outputs are connected at I/Os. The system clock can come either from OMAP or directly from the input clock. Actual implementation in OMAP is as follows:

- PWM0 PWM output of GPTIMER1
- PWM1 PWM output of GPTIMER2
- PWM2 PWM output of GPTIMER3

32-kHz Synchronization Counter

This is a 32-bit counter, clocked by the falling edge of the 32-kHz clock. It is reset while the power-up reset ($\overline{\text{PWRON\_RESET}}$) primary I/O is active (main OMAP5912 reset). Then, on the rising edge of the power-up reset ($\overline{\text{PWRON\_RESET}}$ release), it starts to count forever. When the highest value is reached, it wraps back to zero and starts running again. The MPU core can read it from a 32-bit peripheral access, whereas the DSP core can access it only through two consecutive 16-bit accesses.

Watchdog

The watchdog module is a 32-bit general-purpose counter (same programming model as the 32-bit general-purpose timer) with watchdog capability (generates a reset). It is clocked by the system clock.

MMC/SDIO

There are two instances of the MMC/SDIO module in OMAP5912. This module is a superset of the MMC/SD module from OMAP5910, including I/O interfacing capability to support an SDIO card.

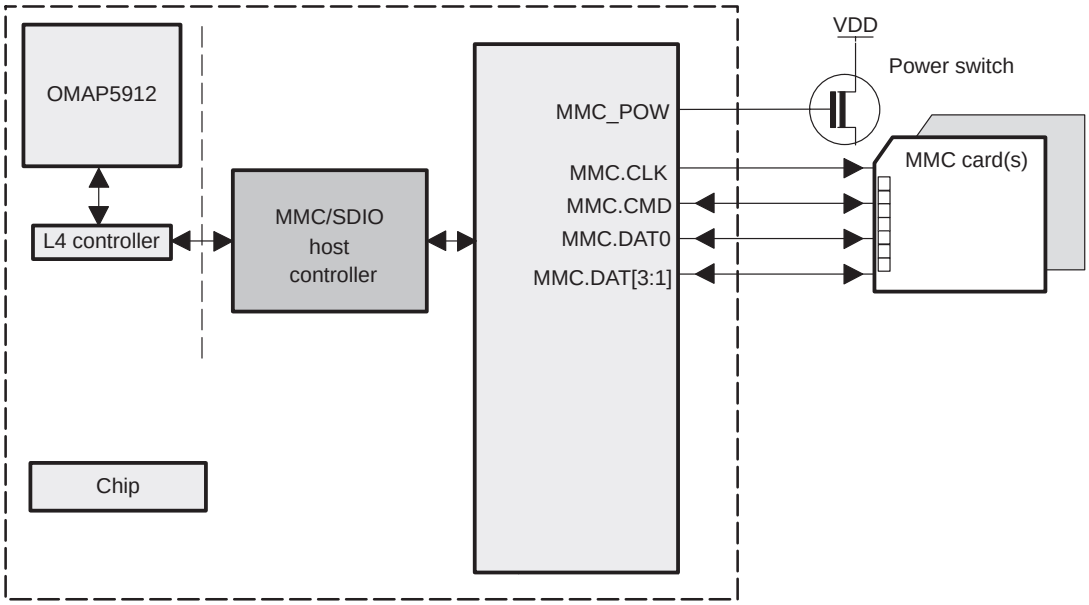
The MMC/SDIO1 replaces the MMC/SD from OMAP5910, whereas the MMC/SDIO2 is an additional peripheral.

The MMC/SDIO host controller provides an interface between a local host, such as the MPU core or DSP core, and MMC/SD/SDIO memory cards, plus up to four serial flash cards.

The following combination of external devices is supported:

- One or more MMC memory cards sharing the same bus.
- One single SD memory card or SDIO card.

Figure 15. MMC/SDIO Block Connection



The main features of the MMC/SDIO module are:

- Full compliance with MMC command/response sets, as defined in the MMC standard specifications v.3.1.
- Full compliance with SD command/response sets, as defined in the SD physical layer specifications v.1.0.
- Full compliance with SDIO command/response sets, as defined in the SDIO card specification v1.0.

OMAP5912 also supports control signals to external level shifters in case the voltage for the OMAP5912 I/O is set to 1.8V. These signals are derived from the direction control of the MMC_DAT0 and MMC_CMD I/O pads (one direction control per data bit line and one direction control for the command line).

Note:

- The MMC/SDIO2 clock is multiplexed between the 48-MHz clock (APLL output) and the system clock (19.2 MHz or 12 MHz).
- At reset, the MMC/SDIO2 clock selection is the system clock.
- Whereas the MMC/SDIO1 interface includes all of the MMC/SDIO pins except the direction controls (data and control), the full MMC/SDIO2 is routed at the OMAP5912 level. The configuration selects only the required part of the interface.

2.2.3 Other Modules

JTAG TAP Controller

JTAG TAP controller handles standard IEEE JTAG interfaces. Boundary scan chain is implemented in OMAP5912.

3 Wake-up Capabilities

Table 10 lists the peripherals able to wake up the system and their event captures. Wake-up can occur either directly or by GPIO.

Table 10. Event Captures for Peripheral Wake-up Capability

Peripheral	Event Capture	Receive Capability in Deep Sleep Mode
UART2	Low transition on RX process by the ULPD module, or using GPIO configuration on the RTS interface.	Provided that the external transmitter uses the UART2 baud clock, the data is received properly and captured.
GPIO1, GPIO2, GPIO3, GPIO4	Asynchronous interrupt detection; all wake-up events per module are merged into one asynchronous interrupt.	NA
GPIO2	Asynchronous interrupt detection.	NA
GPIO3	Asynchronous interrupt detection.	NA
GPIO4	Asynchronous interrupt detection.	NA
SPI	Using GPIO configuration on the all SPI input pins.	Not able to receive the first data in slave mode.
I^2C	Using GPIO configuration on the all I^2C interfaces.	Not able to receive the first data in slave mode
UART3	Using GPIO configuration on the all UART3 input pins.	Not able to receive the data
McBSP1	Using GPIO configuration on the interface.	Not able to receive the data

Notes: 1) When the wake-up is done through the GPIO, the programmer must ensure that the GPIO direction is set up as input.

2) Depending on the configuration before entering into power-down mode, the GPIO can wake either the entire system, or only a specific subsystem.

3) In addition to the wake-up capability mentioned in the above table, several peripherals are also able to generate their own wake-up request. These requests are merged and sent to OMAP3.2 and the MPU core level 2 interrupt handler as a global wake-up request.

Table 10. Event Captures for Peripheral Wake-up Capability (Continued)

Peripheral	Event Capture	Receive Capability in Deep Sleep Mode
McBSP2	Using GPIO configuration on the all McBSP2 input pins.	Not able to receive the data
GPTIMER1…8	Can wake up the system when the clock is configured as 32-kHz through its own interrupt per general-purpose timer.	NA
OS Timer	The timer can generate interrupt.	NA
Emulation wake up	The emulation is also able to wake up the ARM926EJS. This wake up event is also merged with the application wake up event.	NA
USB_OTG	Asynchronous detection on USB device controller to request the USB clock.	NA
MPUIO	Can wake up the system by sampling data at low frequency and sending interrupt to MCU.	NA

Notes: 1) When the wake-up is done through the GPIO, the programmer must ensure that the GPIO direction is set up as input.

2) Depending on the configuration before entering into power-down mode, the GPIO can wake either the entire system, or only a specific subsystem.

3) In addition to the wake-up capability mentioned in the above table, several peripherals are also able to generate their own wake-up request. These requests are merged and sent to OMAP3.2 and the MPU core level 2 interrupt handler as a global wake-up request.

3.1 Pin Description

See the *OMAP5912 Applications Processor Data Manual (SPRS231)* for I/O pin description. It includes the pin description (location on the ballout, reset state, buffer used, signal description, electrical information, and buffer description).

Revision History

The table below lists the changes made since the previous version of this document.

Location	Additions, Modifications, Deletions
10	Removed Camera I/F from Figure 1.
12	Removed the CompactFlash section before section 1.4, *Other Memory Types*.
16	Removed figure as it was a duplicate of Figure 1
16	Modified Table 1 by removing the CompactFlash controller row after the ULPD row
19	Modified Table 8 by removing the ETLM, SCM, and BCM rows.
25−26	Modified section 2.2.2, *Peripherals Subsystem*, by removing the *CompactFlash Controller* section
41	Modified section 2.2.3, Other Modules, by removing the *Boot Device Configuration* and *Boot ROM* sections
42	Modified secttion 3.1, *Pin Description*, by removing the boot configuration pins details

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