TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec

User's Guide

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About This Manual

This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRUFG5 — ***TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide*** This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide*** This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide*** This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus.

SPRUFH5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide*** This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH6 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide*** This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide*** This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide*** This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

SPRUFH9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide*** This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide*** This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide*** This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide*** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide*** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide*** This document describes the operation of the ethernet media access controller interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI7 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Analog to Digital Converter (ADC) User's Guide*** This document describes the operation of the analog to digital conversion in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI8 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Key Scan User's Guide*** This document describes the key scan peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI9 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Voice Codec User's Guide*** This document describes the voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal FIFO (Read FIFO/Write FIFO). The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

SPRUFJ0 — ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Power Management and Real-Time Clock Subsystem (PRTCSS) User's Guide*** This document provides a functional description of the Power Management and Real-Time Clock Subsystem (PRTCSS) in the TMS320DM36x Digital Media System-on-Chip (DMSoC) and PRTC interface (PRTCIF).

SPRUGG8 — *TMS320DM36x Digital Media System-on-Chip (DMSoC) Face Detection User's Guide*This document describes the face detection capabilities for the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Voice Codec

This document describes the 16-bit voice codec peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). This module can access ADC/DAC data with internal read/write FIFO. The CPU communicates to the voice codec module using 32-bit-wide control registers accessible via the internal peripheral bus.

1 Features

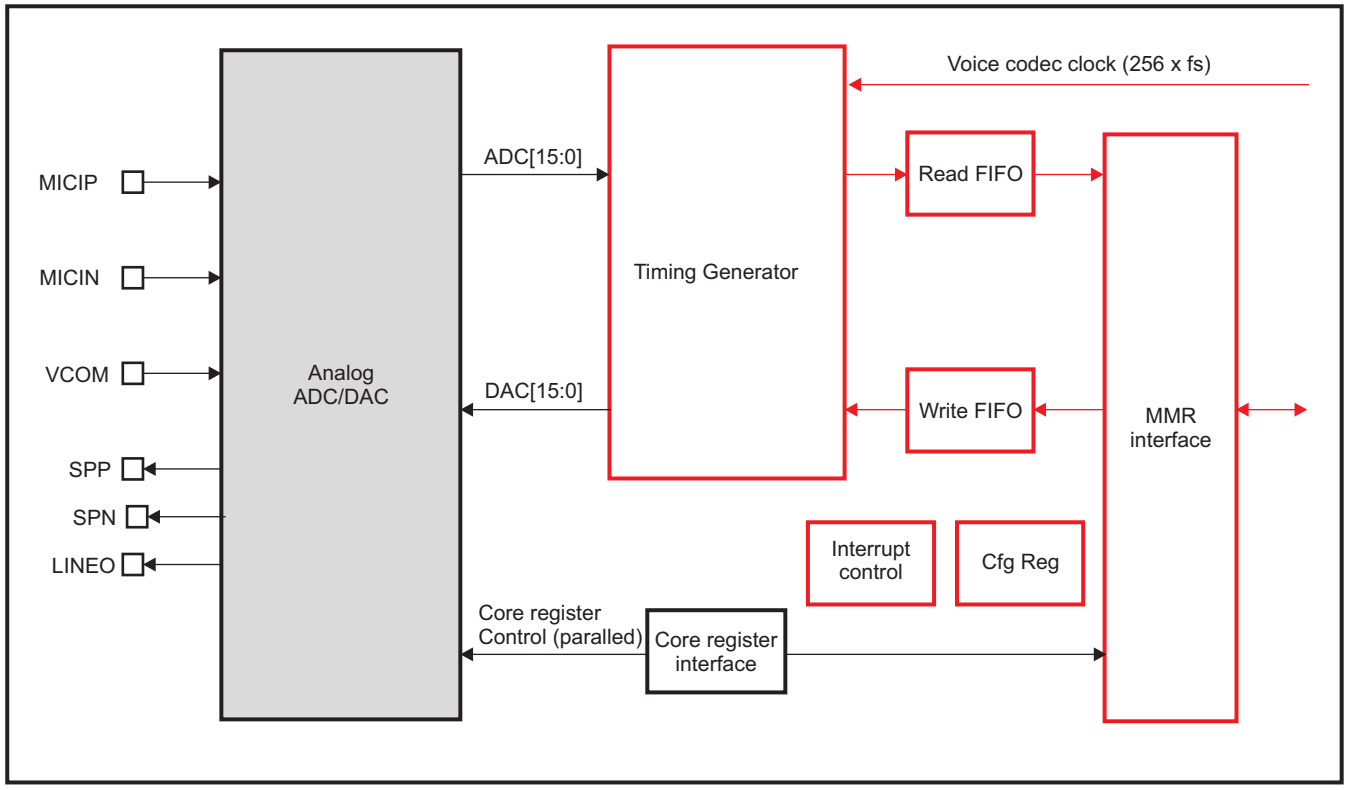
The voice codec module has following features:

- 16 bit x 16 word FIFO for recording/playback data transfer
- Fully differential microphone amplifier
- Monaural single ended line output
- Monaural speaker amplifier (BTL)
- DAC Dynamic range: 70 dB
- ADC Dynamic range: 70 dB
- 200-300mW speaker output at RL = 8Ω
- Sampling frequency (f_s): 8 kHz and 16 kHz
- Automatic level control for recording
- Programmable function by register control
  - Digital attenuator of DAC: 0 dB to -62 dB
  - Digital gain control for recording (0/+6/+12/+18 dB)
  - Power up/down control for each module
  - 20 dB/26 dB boost selectable for microphone input
  - Two-stage notch filter

1.1 Functional Block Diagram

Figure 1 shows the data path and control path of the voice codec module.

Figure 1. Voice Codec Block Diagram



1.2 Voice Codec Module Description

The voice codec module is comprised of the blocks that are described in the following sections.

1.2.1 MIC Input

The microphone input pins (MICIN and MICIP) can be used as a fully differential microphone of line input with selectable 20 dB or 26 dB boost and 0.07V rms input. These analog inputs have high input impedance (10 kΩ), which is not changed by gain setting.

1.2.2 A/D Convertor (ADC)

The ADC includes a single-bit delta sigma modulator (DSM), anti-aliasing filter (AAF), decimation filter, high-pass filter (HPF), notch filter, and automatic level control (ALC). The HPF, notch filter, and ALC can be disabled by register setting.

1.2.3 D/A Convertor (DAC)

The DAC includes a single-bit DSM interpolation filter and switched capacitor reconstruction low-pass filter (SC LPF). These can be used to obtain high PSRR, low jitter sensitivity, and low out-of-band noise.

1.2.4 Common Voltage (VCOM)

The VCOM pin is normally biased to 0.5 VDDA, and it provides the common voltage to internal circuitry. It is recommended that a 10uF capacitor be connected between this pin, and ground to provide clean voltage.

1.2.5 Line Output

The LINEO pin can be used as a monaural single-ended output with 0.9V rms. The line output can drive a 10 kΩ load.

1.2.6 Speaker Output

The SPP and SPN pins are monaural speaker differential outputs (BTL) with a maximum of 240 mW rms into an 8 Ω load.

1.2.7 Automatic Level Control (ALC)

The sound for microphone recording should be expanded to a suitable level without saturation. The digitally-controlled, automatic level control (ALC) provides automatic expansion for small input signal and compression for large input signals during recording. The ALC function supports the sampling frequency (f_s) of 8kHz and 16kHz and can be enabled by setting the ALCEN bit in the automatic level control register (VC_REG06).

1.2.8 High Pass Filter (HPF)

The high-pass filter (HPF) eliminates the DC offset of the ADC analog signal. The high-pass filter can be enabled by setting the HPF bit in the voice codec recording mode control register (VC_REG04).

1.2.9 Notch Filter

The notch filter is provided to remove noise of a particular frequency such as CCD noise, motor noise, or other mechanical noise in a particular application. Its center frequency and frequency bandwidth can be programmed by voice codec registers (VC_REG00-VC_REG03).

Notch filter registers (VC_REG00-VC_REG03) set the notch filter coefficients (NA1 and NA2) in Q2.12 fixed point format. The default value for all these registers is zero. The internal notch filter coefficients are updated with the written values when NTUP (VC_REG04) is set to 1 from 0.

The coefficient of the notch filter (NA1 and NA2) can be derived as below:

$$a1 = -(1 + a2)\cos(\omega c)$$

$$a2 = \frac{1 - \tan(\omega b / 2)}{1 + \tan(\omega b / 2)}$$

Where $\omega c = 2\pi f_c / f_s$, $\omega b = 2\pi f_b / f_s$, f_s= sampling frequency [Hz], f_c= center frequency [Hz], f_b = -3dB bandwidth [Hz]

Example:

f_c = 2 kHz, f_b = 200Hz, f_s = 8kHz

$$\omega c = 2 \times \pi \times \frac{2000}{8000} = 1.571$$

$$\omega b = 2 \times \pi \times \frac{200}{8000} = 0.157$$

$$a2 = \frac{1 - \tan(0.157 / 2)}{1 + \tan(0.157 / 2)} = 0.854$$

$$a1 = -(1 + 0.854) \times \cos(1.571) = 3.7 \times 10^{-4} \cong 0$$

NA2 = a2 x 2^{12} = 0x0DA9; NA1 = a1 x 2^{12} = 0x0001

1.3 Industry Compliance Statement

The voice codec module does not conform to any recognized industry standards.

2 Peripheral Architecture

2.1 Clock Control

The voice codec module supports the sampling frequency (f_s) of 8 kHz and 16 kHz. The voice codec clock is configured by setting the PERI_CLKCTL.PLLDIV2 divider value so that the voice codec clock is the same or close to 256 x f_s. For more information on device clocking, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Users Guide* (SPRUFG5).

2.2 Signal Descriptions

The voice codec module signal descriptions are included in Table 1. Refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) Data Manual* (SPRS457) for more information on these pins.

Table 1. Voice Codec Signal Descriptions

Signal Name	Signal Type	Function
MICIP	Input	MIC positive signal
MICIN	Input	MIC negative signal
LINEO	Output	Line driver signal
SPP	Output	Speaker amplifier positive signal
SPN	Output	Speaker amplifier negative signal
VCOM	Input	Analog block common voltage

2.3 Reset Considerations

2.3.1 Software Reset Considerations

A software reset (such as a reset generated by the emulator) causes the voice codec registers to return to their default state after reset.

2.3.2 Hardware Reset Considerations

A hardware reset of the processor causes the voice codec registers to return to their default values after reset.

2.4 Initialization

The voice codec module can operate in either playback mode or recording mode. The following section provides procedures for initializing the voice codec in recording mode or playback mode.

2.4.1 Recording Mode Initialization

In the recording mode operation, the voice codec receives 16-bit ADC sampled data in a rate of sampling frequency (f_s), which means the ADC[15:0] input is sampled once every 256 voice codec clocks.

1. Make sure the ADC module is in reset by clearing the RSTADC bit in the voice codec control register (VC_CTRL) to 1.
2. Remove the ADC module from reset by setting the RSTADC bit in the VC_CTRL register to 0.
3. Enable the read FIFO (RFIFO) by setting the RFIFOEN bits in the voice codec control register (VC_CTRL).
4. Clear the voice codec internal filter coefficients by setting the NTUP bits in the voice codec recording side mode control register (VC_REG04).
5. Clear the read FIFO (RFIFO) by setting the RFIFOCL bits in the voice codec control register.
6. Configure the desired data format in the voice codec control register (VC_CTRL).
   - Program the read sign bit in the RDUNSIGNED bit
   - Program the read data size in the RDSIZE bit
   - Set the timing control of the read FIFO (RFIFO) data request in RFIFOMD bits
7. Enable the desired interrupts, if any, in the voice codec interrupt register (VC_INTEN).
8. Configure the notch filter 1 coefficient (NA1) in Q2.12 format using the notch filter register (VC_REG00 and VC_REG01). Refer to Section 1.2.9 for deriving the notch filter 1 coefficient (NA1).
9. Configure the notch filter 2 coefficient (NA2) in Q2.12 format using the notch filter register (VC_REG02 and VC_REG03). Refer to Section 1.2.9 for deriving the notch filter 2 coefficient (NA2).
10. Update the notch filter coefficient in the voice codec internal filter coefficient by setting the NTUP bit in the recording mode control register (VC_REG04)
11. Set the microphone gain to a suitable level by configuring the programmable gain amplifier (PGA) and microphone gain control register (VC_REG05)

2.4.2 Playback Mode Initialization

In the playback mode operation, the voice codec outputs 16-bit DAC sampled data in a rate of sampling frequency (f_s), which means the DAC[15:0] output changes once every 256 voice codec clocks.

1. Make sure the DAC module is in reset by clearing the RSTDAC bit in the voice codec control register (VC_CTRL) to 1.
2. Remove the DAC module from reset by setting the RSTDAC bit in the VC_CTRL register to 0.
3. Enable the write FIFO (WFIFO) by setting the WFIFOEN bits in the voice codec control register (VC_CTRL).
4. Clear the write FIFO (WFIFO) by setting the WFIFOCL bits in the voice codec control register.
5. Configure the desired data format in the voice codec control register (VC_CTRL).
   - Program the write sign bit in the WDUNSIGNED bit
   - Program the write data size in the WDSIZE bit

- Set the timing control of the write FIFO (WFIFO) data request in the WFIFOMD bits

6. Enable the desired interrupts, if any, in the voice codec interrupt register (VC_INTEN).
7. Set the attenuation for DAC to a suitable level by configuring the digital soft mute/attenuation control register (VC_REG09).

2.5 Interrupt Support

The voice codec module can send both receive and transmit interrupts to the controller. For more details on the Interrupt Controller, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

2.5.1 Interrupt Events and Requests

The RDRDY and WDREQ bits in the Interrupt status register (VC_INTSTATUS) indicate the ready state of the voice codec receiver and transmitter, respectively. Writes and reads can be synchronized by any of the following methods:

- Polling RDRDY and WDREQ bits in VC_INTSTATUS
- Using the events sent to the EDMA controller (VCREVT and VCXEVT)
- Using the interrupts to the CPU (VCINT) that the events generate

Voice codec generates following interrupt events:

- RDRDY: Read FIFO Data Ready
- WDREQ: Write FIFO Data Request
- WERROVF: Write FIFO Overflow
- WERRUDR: Write FIFO Underrun
- RERROVF: Read FIFO Overflow
- RERRUDR: Read FIFO Underrun

2.5.1.1 Read FIFO Data Ready (RDRDY)

RDRDY = 1 in the interrupt status register (VC_INTSTATUS) indicates that data has been received from ADC to Read FIFO (RFIFO) and the data can now be read by the EDMA controller. Once that data has been read by the EDMA controller, RRDY is cleared to 0. Also, at device reset, the RDRDY bit is cleared to 0 to indicate that no ADC data is ready. When the RFIFOMD bit in control register (VC_CTRL) is set to 1, the RDRDY interrupt will be generated for every cycle of sampling frequency (f_s). When the RFIFOMD bit in control register (VC_CTRL) is set to 0, the RDRDY interrupt will be generated for every 8 cycles of sampling frequency (f_s). In this case, eight words of data can be read from the RFIFO access register. RDRDY directly drives the voice codec interrupt (VCINT) to the ARM CPU if RDRDY = 01b in VC_INTEN register.

2.5.1.2 Write FIFO Data Request (WDREQ)

WDREQ = 1 in the interrupt status register (VC_INTSTATUS) indicates that data has been received from DAC to Write FIFO (WFIFO) and the data can now be written to by the EDMA controller. Once that data has been written by the EDMA controller, WDREQ is cleared to 0. Also, at device reset, the WDREQ bit is cleared to 0 to indicate that there is no request for DAC data. When the WFIFOMD bit in control register (VC_CTRL) is set to 1, the WDREQ interrupt will be generated for every cycle of sampling frequency (f_s). When the WFIFOMD bit in control register (VC_CTRL) is set to 0, the WDREQ interrupt will be generated for every eight cycles of sampling frequency (f_s). In this case, eight words of data can be read from the WFIFO access register. The WDREQ interrupt directly drives the voice codec interrupt (VCINT) to the ARM CPU if WDREQ = 01b in the VC_INTEN register.

2.5.1.3 Write FIFO Overflow

WERROVF = 1 in the interrupt status register (VC_INTSTATUS) indicates a Write FIFO (WFIFO) overflow error when the data is loaded from the WFIFO access register with WFIFO full. The WERROVF interrupt directly drives the voice codec interrupt (VCINT) to the ARM CPU if WERROVF = 01b in the VC_INTEN register.

2.5.1.4 Write FIFO Under run

WERRUDR = 1 in the interrupt status register (VC_INTSTATUS) indicates a Write FIFO (WFIFO) underrun error due to no transmit data in the WFIFO. In this condition, the last transmit data will be sent to DAC. The WERRUDR interrupt directly drives the voice codec interrupt (VCINT) to the ARM CPU if WERRUDR = 01b in VC_INTEN register.

2.5.1.5 Read FIFO Overflow

RERROVF = 1 in the interrupt status register (VC_INTSTATUS) indicates a RFIFO overflow error when the next data from ADC is received with data in RFIFO full. The RERROVF interrupt directly drives the voice codec interrupt (VCINT) to the ARM CPU if RERROVF = 01b in VC_INTEN register.

2.5.1.6 Read FIFO Under run

RERRUDR = 1 in the interrupt status register (VC_INTSTATUS) indicates a RFIFO underrun error when the RFIFO register is accessed in read with no receive data in RFIFO. In this case, the last data will be read from the RFIFO access register. The RERRUDR interrupt directly drives the voice codec interrupt (VCINT) to the ARM CPU if RERRUDR = 01b in VC_INTEN.

2.5.2 Interrupt Multiplexing

The VCINT interrupt generated by the voice codec peripheral to the ARM CPU is multiplexed with other interrupt sources. Refer to the *TMS320DM365 DMSoC ARM Subsystem Reference Guide* (SPRUFG5) for more information on the system control module and ARM interrupt controller.

2.6 EDMA Event Support

2.6.1 DMA Request for Read FIFO: VCREVT

RDRDY = 1 in the interrupt status register (VC_INTSTATUS) indicates that data from ADC to Read FIFO (RFIFO) has been received and that the data can now be read by the EDMA controller. Once that data has been read by the EDMA controller, RRDY is cleared to 0. Also, at device reset, the RDRDY bit is cleared to 0 to indicate that no ADC Data is Ready. RDRDY directly drives the voice codec receive event to the EDMA controller (via VCREVT). When the RFIFOMD bit in control register (VC_CTRL) is set to 1, VCREVT will be generated for every cycle of sampling frequency (f_s). When the RFIFOMD bit in control register (VC_CTRL) is set to 0, VCREVT will be generated with every 8 cycles of sampling frequency (f_s). In this case, eight words of data can be read from RFIFO access register.

For detailed information on using the EDMA to read or write to the voice codec, see the *TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide* (SPRUFI0).

2.6.2 DMA Request for Write FIFO: VCXEVT

WDREQ = 1 in the interrupt status register (VC_INTSTATUS) indicates that data from DAC to Write FIFO (WFIFO) has been received and that the data can now be written to by the EDMA controller. Once that data has been written to by the EDMA controller, WDREQ is cleared to 0. Also, at device reset, the WDREQ bit is cleared to 0 to indicate that there is no request for DAC Data. WDREQ directly drives the voice codec transmit event to the EDMA controller (via VCXEVT). When WFIFOMD in control register (VC_CTRL) is set to “1”, VCXEVT will be generated each every cycle of sampling frequency (f_s). When WFIFOMD in control register (VC_CTRL) is set to “0”, VCXEVT will be generated with every 8 cycles of sampling frequency (f_s). In this case, eight words of data can be read from WFIFO access register.

For detailed information on using the EDMA to read or write to the voice codec, see the *TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Reference Guide* (SPRUF10).

2.7 Power Management

The voice codec module can be placed in reduced-power modes to conserve power during periods of low activity. The power management of the voice codec module is controlled by the processor power and sleep controller (PSC). The PSC acts as a master controller for power management for all of the modules on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5)

2.8 Emulation Considerations

The response of the voice codec events to emulation suspend events (such as halts and breakpoints) is controlled by the FREE bit in the voice codec emulation control register (VC_EMUL_CTRL). The voice codec module either stops exchanging data (FREE = 0) or continues to run (FREE = 1) when an emulation suspend event occurs. When the emulation suspend state is entered, then:

1. Voice codec stops receiving ADC data into Read FIFO (RFIFO)
2. Voice codec stops transmitting data to DAC from Write FIFO (WFIFO)
3. Read FIFO data and Write FIFO data can be accessed from RFIFO/WFIFO register

Section 3.6 shows how the SOFT and FREE bits affect the operation of the emulation suspend.

3 Registers

Table 2 lists the memory-mapped registers for the voice codec peripheral. See the device-specific data manual for the memory address of these registers.

Table 2. Voice Codec Memory Map Registers

Offset	Register	Description	Location
0x00	VC_PID	Voice Codec PID Register	Section 3.1
0x04	VC_CTRL	Voice Codec Control Register	Section 3.2
0x08	VC_INTEN	Voice Codec Interrupt enable Register	Section 3.3
0x0C	VC_INTSTATUS	Voice Codec Interrupt status Register	Section 3.4
0x10	VC_INTCLR	Voice Codec Interrupt status clear Register	Section 3.5
0x14	VC_EMUL_CTRL	Voice Codec Emulator Control Register	Section 3.6
0x20	RFIFO	Voice Codec Read FIFO access Register	Section 3.7
0x24	WFIFO	Voice Codec Write FIFO access Register	Section 3.8
0x28	FIFOSTAT	Voice Codec FIFO Status Register	Section 3.9
0x80	VC_REG00	Notch filter 1 parameter Register	Section 3.10
0x84	VC_REG01	Notch filter 1 parameter Register	Section 3.11
0x88	VC_REG02	Notch filter 2 parameter Register	Section 3.12
0x8C	VC_REG03	Notch filter 2 parameter Register	Section 3.13
0x90	VC_REG04	Voice Codec Recording mode control Register	Section 3.14
0x94	VC_REG05	Programmable Gain Amplifier (PGA) and Microphone gain control Register	Section 3.15
0x98	VC_REG06	Automatic Level control Register	Section 3.16
0xA4	VC_REG09	Digital soft mute/attenuation control Register	Section 3.17
0xA8	VC_REG10	Zero cross detection control Register	Section 3.18
0xB0	VC_REG12	Voice Codec Power up/down control Register	Section 3.19

3.1 Voice Codec PID (VC_PID) Register

The voice codec PID (VC_PID) register is shown in Figure 2 and described in Table 3.

Figure 2. Voice Codec PID (VC_PID) Register

31	8	7	0
Reserved		PID	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. Voice Codec PD (VC_PID) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved		Any writes to these bit(s) must always have a value of 0.
7-0	PID		PID

3.2 Voice Codec Control (VC_CTRL) Register

The voice codec control (VC_CTRL) register is shown in Figure 3 and described in Table 4.

Figure 3. Voice Codec Control (VC_CTRL) Register

31							16
Reserved							
R-0							
15	14	13	12	11	10	9	8
Reserved	WFIFOMD	WFIFOCL	WFIFOEN	Reserved	RFIFOMD	RFIFOCL	RFIFOEN
R-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
WDUNSIGNED	WDSIZE	RDUNSIGNED	RDSIZE	Reserved		RSTDAC	RSTADC
R/W-0	R/W-0	R/W-0	R/W-0	R-0		R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4. Voice Codec Control (VC_CTRL) Field Descriptions

Bit	Field	Value	Description
31-15	Reserved	1 0	Any writes to these bit(s) must always have a value of 0.
14	WFIFOMD		Write FIFO data request timing control
		0	8 word
		1	1 word
13	WFIFOCL		Write FIFO clear
12	WFIFOEN		Write FIFO enable
		0	Disable
		1	Enable
11	Reserved		Any writes to these bit(s) must always have a value of 0.
10	RFIFOMD		Read FIFO data request timing control
		0	8 word
		1	1 word
9	RFIFOCL		Read FIFO clear
8	RFIFOEN		Read FIFO enable
		0	Disable
		1	Enable
7	WDUNSIGNED		Write Data sign bit control
		0	signed
		1	unsigned
6	WDSIZE		Write Data size
		0	16-bit
		1	8-bit
5	RDUNSIGNED		Read Data sign bit control
		0	signed
		1	unsigned
4	RDSIZE		Read Data size
		0	16-bit
		1	8-bit
3-2	Reserved		Any writes to these bit(s) must always have a value of 0.
1	RSTDAC		Analog DAC Reset. DAC reset will be asserted during RSTDAC = 1
0	RSTADC		Analog ADC Reset. ADC reset will be asserted during RSTADC = 1.

3.3 Voice Codec Interrupt Enable (VC_INTEN) Register

The voice codec interrupt enable (VC_INTEN) register is shown in Figure 4 and described in Table 5.

Figure 4. Voice Codec Interrupt Enable (VC_INTEN) Register

31	8
Reserved	
R-0	

7	6	5	4	3	2	1	0
Reserved		WERRUDR	WERROVF	WDREQ	RERRUDR	RERROVF	RDRDY
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5. Voice Codec Interrupt Enable (VC_INTEN) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5	WERRUDR		Interrupt enable for Write FIFO underrun error
		0	Disable
		1	Enable
4	WERROVF		Interrupt enable for Write FIFO overflow error
		0	Disable
		1	Enable
3	WDREQ		Interrupt enable for Write FIFO Data request
		0	Disable
		1	Enable
2	RERRUDR		Interrupt enable for Read FIFO underrun error
		0	Disable
		1	Enable
1	RERROVF		Interrupt enable for Read FIFO overflow error
		0	Disable
		1	Enable
0	RDRDY		Interrupt enable for Read FIFO Data ready
		0	Disable
		1	Enable

3.4 Voice Codec Interrupt Status (VC_INTSTATUS) Register

The voice codec interrupt status (VC_INTSTATUS) register is shown in Figure 5 and described in Table 6.

Figure 5. Voice Codec Interrupt Status (VC_INTSTATUS) Register

31	8
Reserved	
R-0	

7	6	5	4	3	2	1	0
Reserved		WERRUDR	WERROVF	WDREQ	RERRUDR	RERROVF	RDRDY
R-0		R-0	R-0	R-0	R-0	R-0	R-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 6. Voice Codec Interrupt Status (VC_INTSTATUS) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5	WERRUDR		Interrupt status for Write FIFO underrun error
		0	No Interrupt
		1	Interrupt
4	WERROVF		Interrupt status for Write FIFO overflow error
		0	No Interrupt
		1	Interrupt
3	WDREQ		Interrupt status for Write FIFO Data request
		0	No Interrupt
		1	Interrupt
2	RERRUDR		Interrupt status for Read FIFO underrun error
		0	No Interrupt
		1	Interrupt
1	RERROVF		Interrupt status for Read FIFO overflow error
		0	No Interrupt
		1	Interrupt
0	RDRDY		Interrupt status for Read FIFO Data ready.
		0	No Interrupt
		1	Interrupt

3.5 Voice Codec Interrupt Status Clear Register (VC_INTCLR)

The voice codec interrupt status clear (VC_INTCLR) register is shown in Figure 6 and described in Table 7.

Figure 6. Voice Codec Interrupt Status Clear (VC_INTCLR) Register

31	8
Reserved	
R-0	

7	6	5	4	3	2	1	0
Reserved		WERRUDR	WERROVF	WDREQ	RERRUDR	RERROVF	RDRDY
R-0		W-0	W-0	W-0	W-0	W-0	W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 7. Voice Codec Interrupt Status Clear (VC_INTCLR) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5	WERRUDR		Interrupt status for Write FIFO underrun error
		0	No Interrupt
		1	Clear the Interrupt
4	WERROVF		Interrupt status for Write FIFO overflow error
		0	No Interrupt
		1	Clear the Interrupt
3	WDREQ		Interrupt status for Write FIFO Data request
		0	No Interrupt
		1	Clear the Interrupt
2	RERRUDR		Interrupt status for Read FIFO underrun error
		0	No Interrupt
		1	Clear the Interrupt
1	RERROVF		Interrupt status for Read FIFO overflow error
		0	No Interrupt
		1	Clear the Interrupt
0	RDRDY		Interrupt status for Read FIFO Data ready.
		0	No Interrupt
		1	Clear the Interrupt

3.6 Voice Codec Emulator Control Register (VC_EMUL_CTRL)

The voice codec emulator control (VC_EMUL_CTRL) register is shown in Figure 7 and described in VCIF emulator ControlTable 8.

Figure 7. Voice Codec Emulator Control (VC_EMUL_CTRL) Register

31	2	1	0
Reserved		SOFT	FREE
R-0		R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. Voice Codec Emulator Control (VC_EMUL_CTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved	0	Any writes to these bit(s) must always have a value of 0.
1	SOFT		Emulation soft bit. This bit is used in conjunction with FREE bit to determine the emulation suspend mode. This bit has no effect if FREE = 1.
		0	Voice codec halts immediately during emulation halt
0	FREE		Emulation free bit.
		0	Free-running mode is disabled. During emulation halt, voice codec halts immediately.
		1	Free-running mode is enabled. During emulation halt, the voice codec control module continues to operate.

3.7 Voice Codec Read FIFO Access (RFIFO)Register

The voice codec read FIFO access (RFIFO) register is shown in Figure 8 and descried in Table 9.

Figure 8. Voice Codec Read FIFO Access (RFIFO) Register

31	16	15	0
Reserved		RDATA	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 9. Voice Codec Read FIFO Access (RFIFO) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Any writes to these bit(s) must always have a value of 0.
15-0	RDATA		Read data

NOTE: When the RDSIZE bit in the VC_CTRL register is 1, then only lower byte data RDATA[7:0] is valid.

3.8 Voice Codec Write FIFO Access (WFIFO) Register

The voice codec write FIFO access (WFIFO) register is shown in Figure 9 and described in Table 10.

Figure 9. Voice Codec Write FIFO Access (WFIFO) Register

31	16	15	0
Reserved		WDATA	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 10. Voice Codec Write FIFO Access (WFIFO) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved		Any writes to these bit(s) must always have a value of 0.
15-0	WDATA		Write data

NOTE: When the WDSIZE bit in the VC_CTRL register is 1 then only lower byte data WDATA[7:0] is valid.

3.9 Voice Codec FIFO Status (FIFOSTAT)Register

The voice codec FIFO status (FIFOSTAT) register is shown in Figure 10 and described in Table 11.

Figure 10. Voice Codec FIFO Status (FIFOSTAT) Register

31	16
Reserved	
R-0	

15	13	12	8	7	5	4	0
Reserved		WDATACOUNT		Reserved		RDATACOUNT	
R-0		R-0		R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. Voice Codec FIFO Status (FIFOSTAT) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved		Any writes to these bit(s) must always have a value of 0.
12-8	WDATACOUNT		WFIFO stored data count
7-5	Reserved		Any writes to these bit(s) must always have a value of 0.
4-0	RDATACOUNT		RFIFO stored data count

3.10 Notch Filter 1 Parameter (VC_REG00) Register

The notch filter 1 parameter (VC_REG00) register is shown in Figure 11 and described in Table 12.

Figure 11. Notch Filter 1 Parameter (VC_REG00) Register

31	8	7	0
Reserved		NA1[7:0]	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. Notch Filter 1 Parameter (VC_REG00) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	NA1[7:0]		Notch filter 1 coefficient [7:0]

3.11 Notch Filter 1 Parameter (VC_REG01) Register

The notch filter 1 parameter (VC_REG01) register is shown in Figure 12 and described in Table 13. .

Figure 12. Notch Filter 1 Parameter (VC_REG01) Register

31	6	5	0
Reserved		NA1[13:8]	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. Notch Filter Parameter 1 (VC_REG01) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5-0	NA1[13:8]		Notch filter 1 coefficient [13:8]

3.12 Notch Filter 2 Parameter (VC_REG02) Register

The notch filter 2 parameter (VC_REG02) register is shown in Figure 13 and described in Table 14. .

Figure 13. Notch Filter 2 Parameter (VC_REG02) Register

31	8	7	0
Reserved		NA2[7:0]	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 14. Notch Filter 2 Parameter (VC_REG02) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5-0	NA2[7:0]		Notch filter 2 coefficient [7:0]

3.13 Notch Filter 2 Parameter (VC_REG03) Register

The notch filter 2 parameter (VC_REG03) register is shown in Figure 14 and described in Table 15.

Figure 14. Notch Filter 2 Parameter (VC_REG03) Register

31	6	5	0
Reserved		NA2[13:8]	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 15. Notch Filter Parameter 0 (VC_REG03) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved		Any writes to these bit(s) must always have a value of 0.
5-0	NA2[13:8]		Notch filter 2 coefficient [13:8]

3.14 Recording Mode Control (VC_REG04) Register

The recording mode control (VC_REG04) register is shown in Figure 15 and described in Table 16.

Figure 15. Recording Mode Control (VC_REG04) Register

31	4	3	2	1	0
Reserved		HPF	NTRST	NTEN	NTUP
R-0		R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 16. Recording Mode Control (VC_REG04) Field Descriptions

Bit	Field	Value	Description
31-4	Reserved		Any writes to these bit(s) must always have a value of 0.
3	HPF		High-pass filter enable or disable
		0	Enable
		1	Bypass
2	NTRST		Reset control for notch filter
		0	Not reset
		1	Reset
1	NTEN		Notch filter enable
		0	Enable
		1	Bypass
0	NTUP		Notch filter coefficient update
			Internal coefficients will be updated with values set in VC_REG00-VC_REG03 when this bit is transitioning from 0 to 1. It is highly recommended to write 0 to this bit after writing to it.

3.15 Programmable Gain Amplifier (PGA) and Microphone Gain Control (VC_REG05) Register

The programmable gain amplifier (PGA) and microphone gain control (VC_REG05) register is shown in Figure 16 and described in Table 17.

Figure 16. Programmable Gain Amplifier (PGA) and Microphone Gain Control (VC_REG05) Register

31	5	4	3	2	1	0
Reserved		ZCAEN	ZCREN	GAA	GAD	
R-0		R/W-1	R/W-0	R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

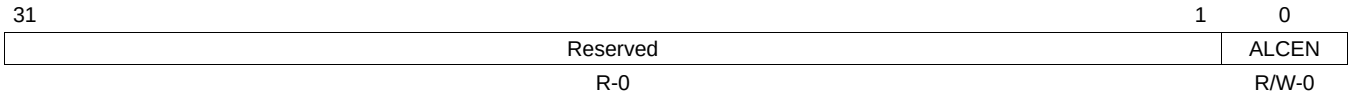
Table 17. Programmable Gain Amplifier (PGA) and Microphone Gain Control (VC_REG05) Field Descriptions

Bit	Field	Value	Description
31-5	Reserved		Any writes to these bit(s) must always have a value of 0.
4	ZCAEN		Zero cross enable for ALC
		0	Disable
		1	Enable
3	ZCREN		Zero cross detection enable for MIC gain and PGA update
		0	Disable
		1	Enable
2	GAA		Gain setting of MIC amplifier
		0	20 dB
		1	26 dB
1-0	GAD		Gain setting of digital PGA. GAD[1:0] must be set to 00 when ALC is enabled.
		00	0 dB
		01	6 dB
		10	12 dB
		11	18 dB

3.16 Automatic Level Control (VC_REG06) Register

The automatic level control (VC_REG06) register is shown in Figure 17 and described in Table 18.

Figure 17. Automatic Level Control (VC_REG06) Register



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 18. Automatic Level Control (VC_REG06) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved		Any writes to these bit(s) must always have a value of 0.
0	ALCEN		Automatic Level Control enable
		0	Disable
		1	Enable

3.17 Digital Soft Mute/Attenuation Control (VC_REG09) Register

The digital soft mute/attenuation control (VC_REG09) register is shown in Figure 18 and described in Table 19.

Figure 18. Digital Soft Mute/Attenuation Control (VC_REG09) Register

31	7	6	5	0
Reserved		PMUT	AT	
R-0		R/W-0	R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 19. Digital Soft Mute/Attenuation Control (VC_REG09) Field Descriptions

Bit	Field	Value	Description
31-7	Reserved		Any writes to these bit(s) must always have a value of 0.
6	PMUT		Digital soft mute for DAC
		0	Disable
		1	Enable (mute)
5-0	AT		Digital attenuation for DAC
		000000	-infinity (mute)
		000001	-62 dB
		000010	-61 dB
		000011	-60 dB
		000100	-59 dB
		000101	-58 dB
		000110	-57 dB
		000111	-56 dB
		001000	-55 dB
		001001	-54 dB
		001010	-53 dB
		001011	-52 dB
		001100	-51 dB
		001101	-50 dB
		001110	-49 dB
		001111	-48 dB
		010000	-47 dB
		010001	-46 dB
		010010	-45 dB
		010011	-44 dB
		010100	-43 dB
		010101	-42 dB
		010110	-41 dB
		010111	-40 dB
		011000	-39 dB
		011001	-38 dB
		011010	-37 dB
		011011	-36 dB
		011100	-35 dB
		011101	-34 dB
		011110	-33 dB
		011111	-32 dB
		100000	-31 dB

Table 19. Digital Soft Mute/Attenuation Control (VC_REG09) Field Descriptions (continued)

Bit	Field	Value	Description
		100001	-30 dB
		100010	-29 dB
		100011	-28 dB
		100100	-27 dB
		100101	-26 dB
		100110	-25 dB
		100111	-24 dB
		101000	-23 dB
		101001	-22 dB
		101010	-21 dB
		101011	-20 dB
		101100	-19 dB
		101101	-18 dB
		101110	-17 dB
		101111	-16 dB
		110000	-15 dB
		110001	-14 dB
		110010	-13 dB
		110011	-12 dB
		110100	-11 dB
		110101	-10 dB
		110110	-9 dB
		110111	-8 dB
		111000	-7 dB
		111001	-6 dB
		111010	-5 dB
		111011	-4 dB
		111100	-3 dB
		111101	-2 dB
		111110	-1 dB
		111111	0 dB

3.18 Zero Cross Detection Control (VC_REG10) Register

The zero cross detection control (VC_REG10) register is shown in Figure 19 and described in Table 20.

Figure 19. Zero Cross Detection Control (VC_REG10) Register

31	1	0
Reserved		ZCEN
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 20. Zero Cross Detection Control (VC_REG10) Field Descriptions

Bit	Field	Value	Description
31-1	Reserved		Any writes to these bit(s) must always have a value of 0.
0	ZCEN		Zero cross detection enable for DAC soft mute and attenuation update
		0	Disable
		1	Enable

3.19 Voice Codec Power Up/Down Control (VC_REG12) Register

The voice codec power up/down control (VC_REG12) register is shown in Figure 20 and described in Table 21.

Figure 20. Voice Codec Power Up/down Control (VC_REG12) Register

31							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
PDSP	PDLN	PDDA	PDAD	PDMC	PDBS	Reserved	PDCM
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 21. Voice Codec Power Up/down Control (VC_REG12) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved		Any writes to these bit(s) must always have a value of 0.
7	PDSP		Power up/down control for speaker amplifier
		0	Power down
		1	Power up
6	PDLN		Power up/down control for line amplifier
		0	Power down
		1	Power up
5	PDDA		Power up/down control for DAC
		0	Power down
		1	Power up
4	PDAD		Power up/down control for ADC
		0	Power down
		1	Power up
3	PDMC		Power up/down control for MIC amplifier
		0	Power down
		1	Power up
2	PDBS		Power up/down control for bias generator
		0	Power down
		1	Power up
1	Reserved		Any writes to these bit(s) must always have a value of 0.
0	PDCM		Power up/down control for VCOM
		0	Power down
		1	Power up

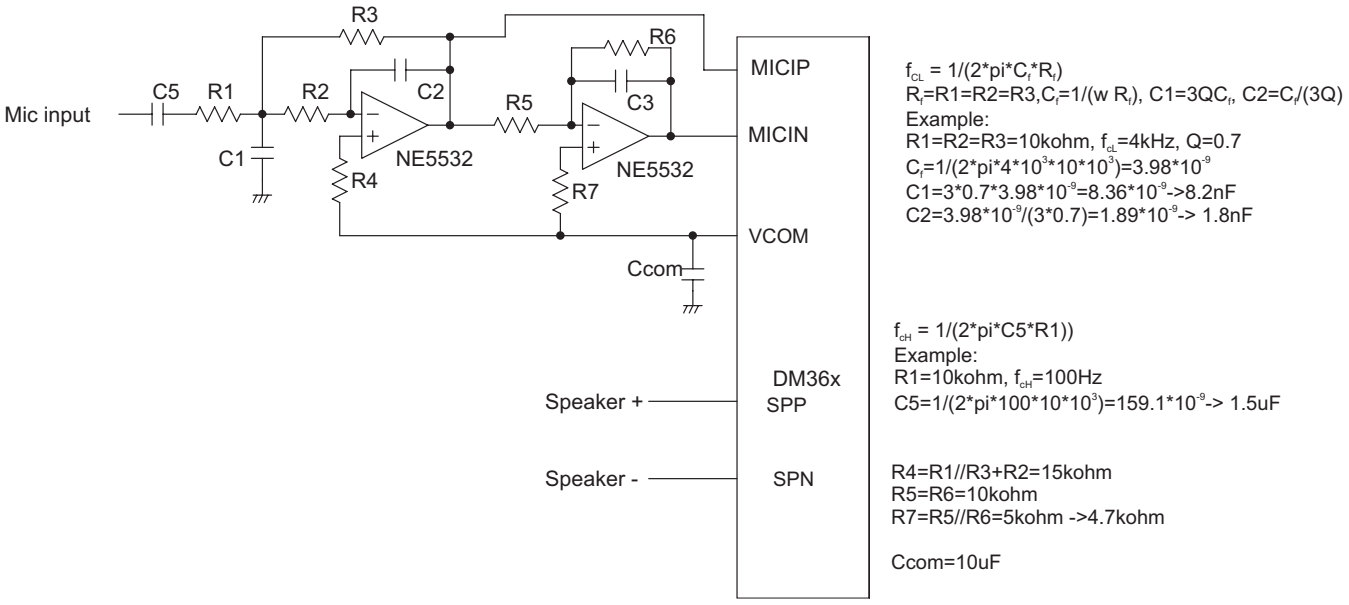
4 Application Examples

Figure 21 and Figure 22 illustrates the examples of the voice codec external connections for the microphone input and line out. See Section 1.2 for an overview of each major block of voice codec. See Section 4.1 for single-end input and Section 4.2 for fully differential input.

4.1 Single-End input

Figure 21 shows the data path of the voice codec application example for single-end input.

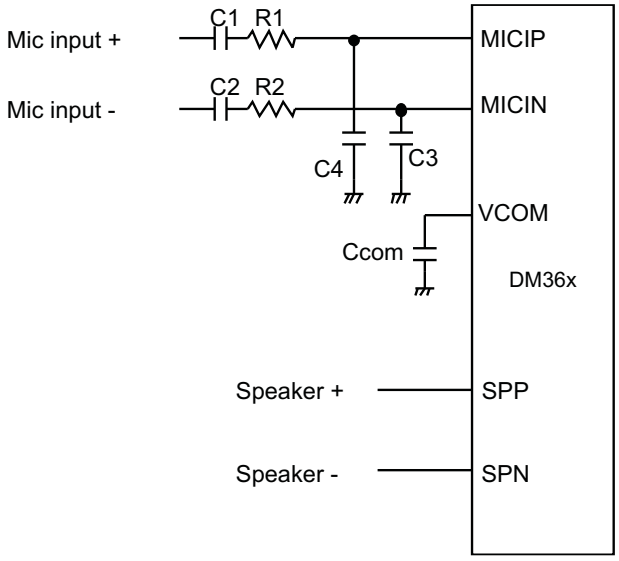
Figure 21. Single-End input Application Example



4.2 Fully Differential Input

Figure 22 shows the data path of the voice codec application example for fully differential input.

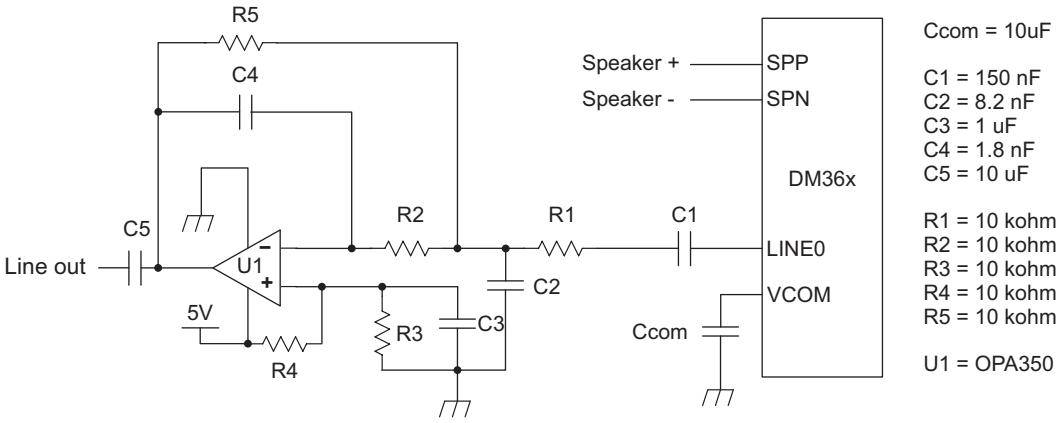
Figure 22. Fully Differential Input Application Example



4.3 Line Output Filter

Figure 23 shows the data path of the voice codec example for a line output filter.

Figure 23. Line Output Filter



Appendix A Revision History

This document has been revised from SPRUFI9A to SPRUFI9B because of the following technical change(s).

Table 22. Changes Made in This Revision

Location	Additions, Deletions, Changes
Section 2.4.1	Changed bullets 1 and 2.
Section 2.4.2	Changed bullets 1 and 2.
Figure 21	Updated figure.
Figure 22	Updated figure.
Section 4.3	Added section.

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