KeyStone II Architecture
IQNet2

User's Guide

Literature Number: SPRUHO6A
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Revision History

Changes from May 1, 2014 to October 1, 2014	Page
• Changed note for RAC Example	256

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Preface

About This Manual

This User Guide includes an overview of the IQN2 peripheral, and provides information on the features, operation, and use of the peripheral.

NOTE: The information in this document should be used in conjunction with information in the device-specific Keystone Architecture data manual that applies to the part number of your device.

Notational Conventions

This document uses the following conventions:

- Commands and keywords are in **boldface** font.
- Arguments for which you supply values are in *italic* font.
- Terminal sessions and information the system displays are in screen font.
- Information you must enter is in **boldface screen font**.
- Elements in square brackets ([ ]) are optional.

Notes use the following conventions:

NOTE: Means reader take note. Notes contain helpful suggestions or references to material not covered in the publication.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

CAUTION

Indicates the possibility of service interruption if precautions are not taken.

WARNING

Indicates the possibility of damage to equipment if precautions are not taken.

Related Documentation from Texas Instruments

Serializer/Deserializer (SerDes) for KeyStone II Devices User Guide	SPRUH03
Multicore Navigator for KeyStone Devices User Guide	SPRUGR9
TCI6630 Silicon Data Manual	SPRS893

Introduction

The information in this document should be used in conjunction with information in the device-specific Keystone Architecture data manual that applies to the part number of your device.

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1.1 Purpose

IQNet2 (IQN2) is a peripheral module that supports transfers of baseband IQ data between uplink and downlink baseband DSP processors and a high-speed serial interface.

This document describes:

- How to use IQN2
- Supported features
- Interface and implementation details
- IQN2 memory mapped registers
- IQN2 configuration example

1.2 Scope

The scope of this document is limited to the IQN2 IP. This version of the document includes information about internal IQN2 modules and features. It also includes information about Multicore Navigator which is included in the IQN2 subsystem and shows some examples of how to use it, but does not include detailed configuration of PKTDMA and QM. This document also explains AID and other IQN2 subsystems for DFE users but does not include DFE HW detail.

1.3 Terminology

The following sections list abbreviations, acronyms, and definitions of key terms that appear in this user guide.

1.3.1 Abbreviations and Acronyms

Table 1-1. Abbreviations in the IQN2 User Guide

Abbreviation	Description
3GPP	3 rd Generation Partnership Project
AIF2	Antenna Interface 2
AID	Antenna Interface for DFE
AIL	Antenna Interface Link
AP	Applications Processor
AT	IQN2 Timer (sub-module)
AxC	Antenna Carrier (stream)
AxC Container	Contains the IQ samples of one AxC for one chip (applied for CPRI)
Basic Frame	A CPRI basic frame consists of 16 words
BB	Base Band
BBM	Base Band Module
BCN	Base station Chip Number (BCN timer has same role like Phy timer)
BE	Big Endian
BER	SerDes Bit Error Rate
BF	Basic Frame
BFN	UMTS NodeB Frame Number
BTS	(Base Transceiver Station (Base Station)
C&M	Control and Management
CBA	Common Bus Architecture (SCR, VBUSP, VBUSM)
CDC	Clock Domain Crossing
CDMA	Code Division Multiple Access
CFG	Configuration
CorePac	A specific DSP core used (CPU)
CPRI	Common Public Radio Interface

Table 1-1. Abbreviations in the IQN2 User Guide (continued)

Abbreviation	Description
CRC	Cyclic Redundancy Check
CSL	Code Support Library
CSR	Control and Status Register
CW	Control Word (CPRI)
DDR3	Dual Data Rate Memory 3
DFE	Digital Front End
DL	Downlink
DMA	Direct Memory Access
DSP	Digital Signal Processor
EDC	Egress DMA Controller
EE	IQN2 Error Event handler (sub-module)
EFE	Egress Framing Engine
FDD	Frequency Division Duplexing
FIFO	First In First Out queue memory structure
FCS	Frame Check Sequence
FD	Finger Despreader
FM	Framing Module
GCCP	Generic Correlator Co-processor
HDLC	High-level Data Link Control
HFN	Hyperframe Number
HW	Hardware
Hyperframe	1 CPRI Hyperframe = 256 CPRI basic frames
ICC	IQN Core Component (Components mated with SI to create AIL and DIO)
IDC	Ingress DMA Controller
SD	SerDes
IFE	Ingress Framing Engine
I/O	Input & Output data flow
IQ	In-phase and Quadrature data
IQN2	IQ Net #2
IQS	IQ Switch
IP	Interface and Peripherals
K Codes	7-bit line codes representing 8b10b control characters
L2	CorePac DSP Level 2 SRAM
LE	Little Endian
LOF	Loss Of Frame
LOS	Loss Of Signal
LPSC	Local Power Sleep Controller
LUT	Look Up Table
LSB	Least Significant Bit
LTE	Long Term Evolution
MAC	Media Access Control
MAI	Multiple Access Interference
MMR	Memory Mapped Register
MOD	Modulo
MSB	Most Significant Bit
OBSAI	Open Base Station Architecture Initiative
OFDM	Orthogonal Frequency Division Multiplexing

Table 1-1. Abbreviations in the IQN2 User Guide (continued)

Abbreviation	Description
PIC	Parallel Interface Cancellation
PLL	Phase Lock Loop
PM	Path Monitor
PSI	Packet Streaming Interface
“r”	reserve bits (i.e. 0’s)
RAI	Remote Alarm Indication
RAM	Random Access Memory
RAC	Receive Accelerator Co-processor
RE	Radio Equipment (RF Module)
REC	Radio Equipment Control (BBM)
RF	Radio Frequency
RP1	Reference Point 1 (OBSAI)
RP3	Reference Point 3 (OBSAI)
RSA	Rake Search Accelerator
RTWP	Received Total Wideband Power of UMTS
RX	Receive
SAP	Service Access Point
SCR	Switch Central Resource (VBUS cross bar switch)
SDI	SAP Defect Indication
SDRAM	Synchronous Dynamic RAM
SerDes	SERializer / DESerializer
SI	IQN2 System Interface module
SIE_IQ	SI Egress IQ
SII_IQ	SI Ingress IQ
SOF	Start of Frame
	Chip rate = 1/3.84MHz
TBD	To Be Determined
TDD	Time Division Duplexing
TFCI	Transport Format Combination Indicator
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access (new China radio standard)
TPDMA	Third Party DMA
TX	Transmit
UE	User Equipment
UL	Uplink
UMTS	Universal Mobile Telecommunication System
VBUSM	Virtual Bus Multi-issue
VBUSP	Virtual Bus Pipeline
WCDMA	Wideband Code Division Multiple Access
WiMax	Worldwide Interoperability for Microwave Access
XAUI	10 Gigabit Attachment Unit Interface, IEEE 802.3ae
8b10b	Transmission code for high speed serial links

1.3.2 Definitions

Table 1-2. Definitions of Key Terms

Term	Definition
Channel	(same as stream)
Chip	WCDMA term indicating a sample of time. In WCDMA, one chip represents one clock cycle of 3.84MHz (appox 260 ns). Term is also used to indicate a 16-bit I /16-bit Q sample, or two 8-bit I/8-bit Q samples for UL 2x oversampled.
Egress	Data or control information that has or will **exit** IQN2
Ingress	Data or control information that has or will **enter** IQN2
Link (Lane)	A link is equivalent to a SerDes channel and the associated OBSAI or CPRI protocol that passes over that link. Links have an associated bit rate where the bit rate has some degree of programmability.
PKTDMA Packet	A PKTDMA packet consists of a PKTDMA header (called a descriptor) plus payload information (called a buffer) and optional protocol-specific data, which is an extension of payload information.
Stream	IQN2, CPRI, and OBSAI have the concept of multiple parallel contexts interleaved or arbitrated onto a single link. Stream is a term that is sometimes used to identify a single context (or series of packets). Channel is also used to identify the same concept. A given stream can either be streaming such as with ADC antenna data or on-demand as in packet date. The concept of stream is very important as IQN2 has unpacking and packing buffers dedicated per stream.
Wrap	IQN2 has circular ram, terminal count, and LUT; these fields use their own limited count value. If the count value reaches the terminal count value, it will automatically go back to the initial value or zero value. Wrap means this kind of circular repeating activity of a register field or memory.

1.4 Features

The following key features are supported:

- Supported Standards
  - OBSAI
    - OBSAI WCDMA
    - OBSAI LTE
    - OBSAI WiMax (all 802.16 formats)
    - OBSAI GSM/Edge
    - OBSAI Generic Packet Traffic
  - CPRI
    - CPRI WCDMA
    - CPRI LTE
    - CPRI WiMax (all 802.16 formats)
    - CPRI TDSCDMA support
    - CPRI GSM
    - CPRI Control Word (Ethernet)
- 2x AIL lanes
  - Link Rates
    - OBSAI {2x, 4x, 8x}
    - CPRI {2x, 4x, 5x, 8x, 10x, 16x}
  - PHY reset isolation
- Number of channel Supported (Ingress + Egress)
  - (48 + 48) PktDMA channels
  - (64 + 64) Each AIL AxC and (4+4) each AIL Control channel
  - (16 + 16) DIO AxC
  - (32 + 32) AID AxC and (16 + 16) AID Control channel

- Timing and Synchronization
  - Radio Timer
    - Programmable to handle supported radio standards
    - Counts OFDM symbol boundaries
  - Physical Interface Timer—10ms frame count for OBSAI/CPRI timing
  - Timer Synchronization
    - External synchronization
      - OBSAI RP01
      - Generic strobe
      - PA_COMP signal
    - Internal synchronization—Software (MMR) controlled synchronization
  - System Event
    - Internal System Event generation (total 24 events)
      - Synchronize software or EDMA to Radio Timing
      - Event generation based on Radio Timers
- Data Transfers and Formats
  - Autonomous DMA
    - RAC addressing format
    - TAC addressing format
    - WCDMA delayed stream format
    - Ping/Pong L2 data format for CorePac processing
    - WiMax—Symbol format with gap at Frame End
    - LTE symbol format
    - Optional and programmable system event to mark completion of {4chip, WiMax Symbol, Frame}
  - Big and Little Endian
    - Endian Entity size programmable per DMA channel
  - IQ or QI programmable ordering
  - 16-bit I and 16-bit Q—oversampling factor per AxC 1x
  - RSA UL Data Format 8-bit I and 8-bit Q
    - Over sampling factor per AxC 2x
    - Other Oversampling factors supported via multiple AxC
- Debug Support
  - Data tracing support
  - Clock stop and Emulation support
  - Error and Exception Interrupts (detection of many error conditions)
  - VBUS Configuration access to Data Buffer RAMs
- Frame Timing and Synchronization
  - OBSAI RP1 Support
  - OBSAI RP3-01 Support

System Requirements & Throughput:

- Mixed Radio Standards (and mixed DIO/PktDMA)
- VBUS_CFG
  - no substantial run-time throughput
    - 4 writes per 560 usec (for BB Hopping control)
  - other debug, diagnostic, and error handling traffic

- VBUS_Data
  - BW for all AxC and control traffic
  - Worst Case: 9Gbps Ingress + 9-Gbps Egress

Radio Standard configurations:

- LTE1.4: (32 + 32) AxC
  - 3.9 + 3.9 Gbps
  - 448k + 448k pkt/sec (normal cyclic prefix)
- WCDMA: (16 +16) AxC
  - 3.9 + 3.9 Gbps
  - DIO... no pkt/sec
- LTE20: (8 + 8) AxC
  - 7.8 + 7.8 Gbps
  - 112k + 112k pkt/sec (max ext. cyc prefix)
- GSM: (32 +32) AxC (not a formal requirement)
  - 3.9 + 3.9 Gbps (max GSM sample rate)
  - 55k + 55k pkt/sec
- Mix: LTE w/ WCDMA
  - combined BW not to exceed any spec above
  - combined pkt/sec not to exceed any spec above
- Mix: 8 + 8 LTE20 & 4 + 4 TDSCDMA
  - 8.0 + 8.0 Gbps
  - 112k + 112k pkt/sec (max ext. cyc prefix)
- plus (16 + 16) ctrl
  - undefined BW and pkt/sec

Overview of IQN2 Hardware and Software Components

Topic **Page**

2.1 Overview

IQN2 is a peripheral module that supports data transfers between uplink and downlink baseband processors through a high-speed serial interface. The IQN2 subsystem also supports digital front end interface for small cell BTS users. IQN2 directly supports the following radio standards:

- WCDMA/FDD
- LTE FDD
- LTE TDD
- WiMax
- TD-SCDMA
- GSM/Edge

The IQN2 supports both OBSAI RP3 and CPRI protocols. Much of the functionality of the IQN2 is not specific to either protocol. This document does not contain detailed information about OBSAI and CPRI protocols. For more information about these protocols, see the OBSAI RP3 spec. 4.2 and CPRI spec. 5.0.

IQNet stream data is the primary transferred data type and inter-device control data (or control data from/to the RF units) is the secondary transferred data type.

The internal IQN2 interface connects the IQN2 with multiple DSP cores, ARM cores, RAC, TAC, and the FFTC unit via the DMA Switch Fabric and Control Switch Fabric. The IQN2 internal interface connection to the switch fabric is the VBUS. The external IQN2 interface (sometimes called the SerDes interface) connects the IQN2 with either RF units and/or other Baseband OBSAI/CPRI devices. Another external interface connects the AID with Digital Front End (DFE) module in the device. A second internal IQN2 interface connects to the Configuration Switch Fabric for MMR read/writes.

The internal interface is based on two VBUS connections to the *DMA Switch Fabric* and the *Configuration Switch Fabric*. The 32-bit VBUS connection to the 32-bit Configuration Switch Fabric is mainly for configuration, status and error/alarm condition maintenance. The 128-bit VBUS connection to the 128-bit DMA Switch Fabric is mainly used for high data rate circuit-switched and packet-switched data that is sourced from or destined to the IQN2.

Both Configuration and DMA Switch Fabrics are a system of buses, switches, and internal communication protocols. The buses used by both switch fabrics are the TI proprietary VBUS and use a TI-specified VBUS protocol. The antenna interface is a slave endpoint on both the Configuration VBUS and master on the DMA Switch Fabric VBUS. Both switch fabrics use a crossbar switch (SCR) for connecting VBUS endpoints. This SCR (Switch Central Resource) allows multiple VBUS endpoints to communicate simultaneously.

IQN2 uses two basic data transport mechanisms (for data path). Data traffic is mastered by Multicore Navigator or Direct IO. Multicore Navigator is an internal packet DMA mechanism that is used for internal data transport (which is more packet-like) and non-antenna data. Direct IO is a custom state machine that transports WCDMA data to and from circular buffer in {RAC, TAC, L2, DDR3}. Circular buffering is a requirement unique to WCDMA and is not well-supported by Multicore Navigator.

IQN2 is a subsystem of scalable components. It has blocks that get data into the system from outside the SoC like AIL (one lane of CPRI or OBSAI) and AID (interface block that ties the DFE into IQNet. You put a maximum of four copies of AIL down depending upon the needs of the platform. The IQN2 AIL external interface is implemented with high-speed serialized links (max. of four). These links support OBSAI RP3 line {2x, 4x, 8x} rates and CPRI {2x, 4x, 5x, 8x, 10x, 16x} link rates.

IQN2 is intended to communicate with {FFTC, RAC, TAC, PA} subsystems without the need of constant supervision or control from application software. Application software would initially configure the interaction between IQN2 and these subsystems; however, in steady state no MIPS are required for this data interchange.

Communications with these subsystems falls into two basic categories:

- Direct IO: RAC & TAC
- Multicore Navigator: FFTC & PA/NETCP

Direct IO is used exclusively with WCDMA antenna traffic where the source and destination are circular buffers. Direct IO is similar to an EDMA solution except that the DMA is controlled by a custom FSM within IQN2. The change in approach between previous DSPs and the new KeyStone Architecture was motivated by the desire to make DMA changes dynamically.

Multicore Navigator is a packet-based DMA. In LTE (for example) each LTE symbol is treated as a packet. The packets are staged in L2/MSMC RAM. The IQN2 buffers are not large enough to hold whole LTE symbols, so the LTE symbols are slowly accumulated in L2 RAM. IQN2 marks the LTE symbol with the received IQN2 channel number and the LTE symbol index (count value starting at 0 on the radio frame boundary). The packet is then transferred to FFTC. The whole transfer of the LTE symbol from IQN2 to memory and finally to FFTC is performed with no interrupts of real-time action by any of the CorePac cores. (Packet exchanges between IQN2 and PA/NETCP occur in much the same way.)

FFTC requires configuration data in order to process LTE symbols. There are two different ways to configure FFTC:

- Dynamic: Send FFTC ahead of the packet payload (in the protocol specific region of the packet)
- Static: If no configuration is sent, use the last configuration sent (used by data sourced from IQN2)

FFTC has four different input queues all of which have their own static configuration memory. It is recommended that one of these queues be dedicated for reception of packet from IQN2.

NOTE: TAC has a channel aggregation feature which allows for RSA generated data to aggregate into TAC output buffers. This operation happens at earlier stages of TAC processing and are transparent to IQN2 DMA operation.

Radio Standard Requirements and IQN2 Handling

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3.1 WCDMA Requirements and Handling

- WCDMA AxC
  - 3.84 MHz sampling
  - Four bytes per sample
    - DL:
      - 16-bit I + 16-bit Q, 1x over-sampling -or-
      - 15-bit I + 15-bit Q, 1x over-sampling (CPRI only)
    - UL:
      - 8-bit I + 8-bit Q, 2x over-sampling -or-
      - 7-bit I + 7-bit Q, 2x over-sampling (CPRI only)
- Radio Frame Size
  - 10 ms
  - 38,400 chips (1x sample clocks for DL and 2x sample per clocks for UL)
- Data Sources/Destinations
  - RAC—Circular Buffer
  - TAC—Single Buffer, read every four chips. Treated as a circular buffer of one.
  - Memory (L2, MSMC, DDR3)
    - RSA processing of WCDMA data
    - Circular Buffer scheme

3.2 OFDM Requirements and Handling (LTE FDD, LTE TDD, WiMax, TD-SCDMA)

Both OBSAI and CPRI standards appear to have been developed with WCDMA sample rates in mind. The new emerging OFDM standards challenge these standards with a wide range of sampling rates. The OBSAI standard appears to be ahead of CPRI with the “Dual Bit Map” rate matching mechanism. CPRI has its own rate matching approach using the packing method 3 stuffing bit mechanism. Both of these mechanisms essentially rate matches as close to possible then insert bubbles to make up the difference. OBSAI specifies a precise mechanism and tables which show how to program the mechanism. CPRI specifies formulas which specify where the bubbles should be placed, but does not specify an implementation.

OFDM standards differ in data processing compared with WCDMA traffic. WCDMA traffic processing is a continuous streaming operation whereas OFDM processing is chunk-based processing. In OFDM, an FFT operation is performed on AxC data immediately after UL traffic enters the device. Likewise, IFFT is performed on AxC data just before exiting the device. In both cases, the most common FFT granularity is based on the OFDM symbol (grouping of samples).

3.2.1 OFDM DMA

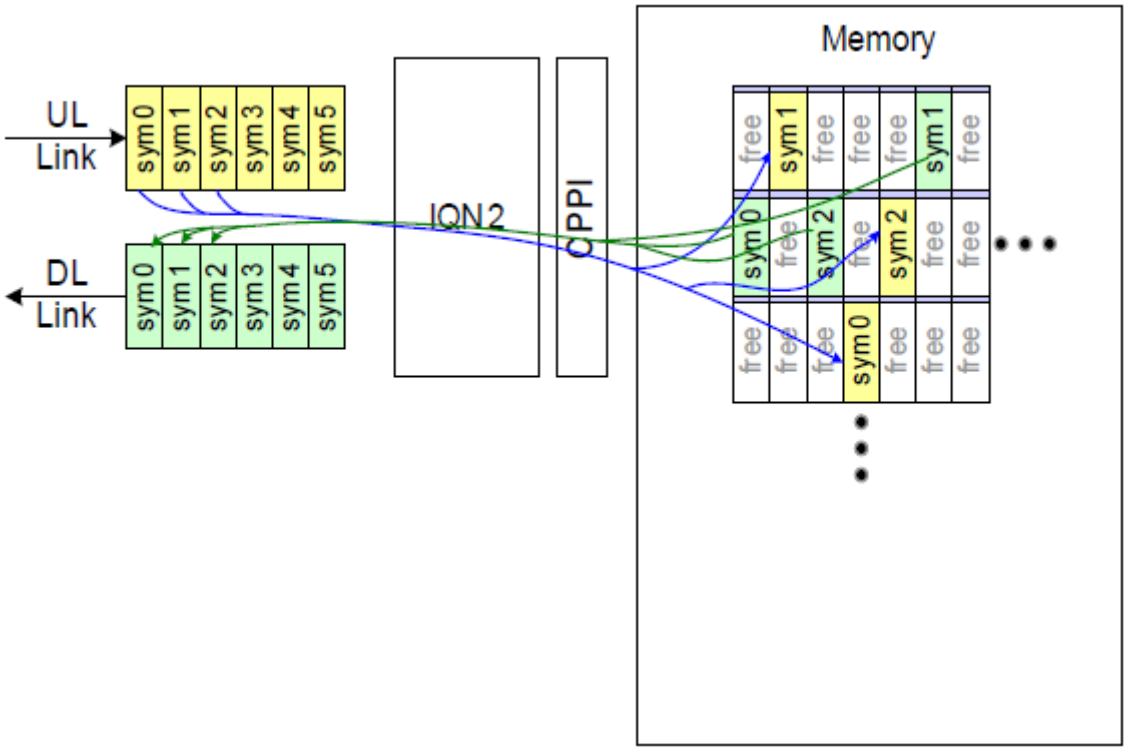
IQN2 AIL uses the Packet DMA (PKTDMA) methodology and hardware accelerators for handling internal data movement. OFDM data is stored in memory on OFDM symbol boundaries. Multicore Navigator adds a small header (descriptor) and protocol-specific field that provides some metadata for each OFDM symbol.

Multicore Navigator is a:

- DMA engine that is rate-controlled by IQN2
- Queue manager that can handle a backlog of packets to be transferred or consumed
- Memory management system

Multicore Navigator dictates (within a memory region) where to write OFDM symbols and frees memory resources after a transfer is complete.

Figure 3-1. OFDM PKTDMA



For OFDM traffic, IQN2 AIL identifies the symbol boundaries, segmenting the traffic into symbol sized packets. Data is internally DMA'ed and stored based on OFDM symbol packet basis. The Multicore Navigator packet header (PS field) contains such information as:

- AxC index
- OFDM Symbol number
- OBSAI header information (GSM BB hopping)
- Number of valid byte in packet (Info Word)

The Multicore Navigator packet payload consists of the OFDM symbol (including cyclic prefix).

The AT (IQN2 Timer) radio timer maintains the radio standard time. For OBSAI, each AxC is supported to have a time offset relative to the radio timer. In CPRI, the PHY (BCN) timer is used as the reference for AxC timing. The AxC offset is added to or subtracted from the system time calculating AxC slot boundaries and slot numbers.

The DMA buffering within the IQN2 AIL is intentionally shallow, intended only to handle small DMA timing differences and AxC alignments. The AIL begins partial DMA of the OFDM packet before receiving the entire packet. The user chooses which memory the packets are delivered to. For all active AxC, AIL in parallel forms whole OFDM packets into user-defined memory (L2, MSMC, or DDR3).

CAUTION

The normal traffic pattern of antenna traffic is for many parallel channels to stream data at radio rates. From a DMA perspective, this usually translates to bursts of 64 bytes for each given channel with rapid DMA context switching between channels. The nature of DDR devices imposes performance penalties when jumping around in address space, known as page thrashing. Because of DDR page thrashing, it is not recommended to have IQN2 directly target DDR with PktDMA AxC traffic. If use of DDR is required, it is recommended that IQN2 use L2 as a shallow PktDMA buffer (i.e., 3 symbol per AxC) then use infrastructure DMA to serially move whole packets to DDR, avoiding the rapid DMA context switching.

The user configures/programs the device with the location where IQN2 AIL will deliver packets and what should be done after the packets are fully formed in memory. The most likely next destination for a packet would be FFTC for FFT to be preformed on the packet. The Multicore Navigator subsystem can be controlled to automatically transfer (without CorePac intervention) OFDM packets (symbols) to FFTC after the packet is complete.

IQN2 AIL and Multicore Navigator deal with OFDM by using a fixed “buffer” size. A packet does not need to entirely fill a buffer, but it must not exceed the buffer size.

For LTE in particular, there can be three different packet sizes to process, as follows:

- Extended cyclic prefix packet size
- Normal cyclic prefix packet size (first symbol of frame/half-frame)
- Normal cyclic prefix packet size (other symbols of frame/half-frame)

When configuring the Multicore Navigator buffer size, the user must choose a buffer size that can accommodate the largest-sized packet. This represents a waste of memory, but it should be an insignificant percentage of RAM as cyclic prefixes tend to be much smaller than the samples of interest.

NOTE: In normal LTE cyclic prefix, the first symbol is a little bit bigger than the other symbols. Simply size the PktDMA buffer to accommodate the larger size.

3.2.1.1 OFDM TDD DMA {LTE TDD, WiMax, TD-SCDMA}

The OBSAI/CPRI links are full duplex (dedicated transmit and receive) and the air channel is half duplex in TDD (multiplexing between transmit and receive). The effect for the IQN2 AIL is that approximately 50 percent of the time traffic—depending on UL/DL ratio—is idle (sending messages for which the payload is not used, zero preferred) on a given link.

NOTE: RF modules may very well send non-zero data during these “idle” symbols/time_slots, but the Base Band will not use this non-zero payload. IQN_AIL will insert zeros for TDD OFF DL

While an AxC is idle (for either DL or UL), the links of the IQN2 AIL continue operating, but do not create OFDM packets or DMA any of the idle traffic within the SOC. Control of this operation is generalized by IQN2 AIL.

Each IQN2 AIL radio standard (8 Ingress & 8 Egress) is programmed with a bit map. Each bit in the bit map is intended to represent one OFDM symbol per frame/sub-frame. (In more general terms, each bit represents a DMA packet and the frame can represent a half-frame for the case of LTE TDD. Zeros in the bit map represent DTX (discontinuous transmission) and ones enable transmission.

On every frame (or sub-frame) boundary use of the bit map will rewind to the beginning. The bit map may be altered on-the-fly for support of changing the UL/DL ratio. The use of these TDD control bits is sampled only at the beginning of each symbol which allows for the possibility of SW updating the table in the middle of each symbol.

Alternately there is a second TDD mechanism which is a single bit per AxC. With this mechanism, the SW must modify the bit in real time prior to the beginning of each symbol. The HW samples and holds the value at each start of symbol giving the SW the largest possible time window to perform the update.

3.2.2 LTE

IQN2 directly supports all known/established LTE sampling rates. 100Mhz LTE or 80MHz LTE can be indirectly supported where the system partitions the traffic into multiple, separate LTE20 AxC (There is no special support to group, interleave, or merge the multiple AxC into a single entity).

Table 3-1. LTE Channels Supported

LTE Rate	Sample Rate	AxC per Link				Cyclic Prefix			FFT Size (payload)
		2x	4x	5x	8x	Normal 1 st	Normal 2 nd -7 th	Extended 1 st -6 th	
1.4MHz	1.92MHz	16	32	40	64	10	9	32	128
3.0 Hz	3.84MHz	8	16	20	32	20	18	64	256
5MHz	7.68MHz	4	8	10	16	40	36	128	512
10MHz	15.36MHz	2	4	5	8	80	72	256	1024
15MHz	23.04MHz	1	2	3	4	120	108	384	1536
20MHz	30.72MHz	1	2	2	4	160	144	512	2048

LTE1.4 and LTE3.0 both have cases where symbols are not quad word aligned. TI SOC buses and memories are naturally QWD(128 bit) in width. All other LTE rates have n x 4 samples per symbol which has the effect of being QWD aligned. The user simply programs packet symbols to the correct length. Specific AIL HW handles this complexity “under-the-hood” without special programming or handling required by the user. (AIF2 did not have this ability)

Oversampling of LTE is not directly supported, but may be achievable using the many degrees of programmability of IQN2.

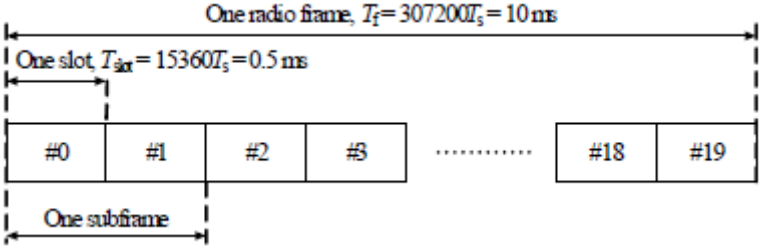
NOTE: IQN_AIL received and transmits full OFDM symbols, including the cyclic prefix. IQN_AIL has no distinction on cyclic prefix vs. payload region. In the SOC system, the FFTC module performs any cyclic prefix manipulations such as stripping it off, or generating it and adding it on.

- Sample bit-width of LTE is (IQN2 AIL supported):
  - OBSAI: 16-bit I and 16-bit Q
  - CPRI: 15-bit I and 15-bit Q

3.2.2.1 LTE Framing

3.2.2.1.1 LTE FDD Framing

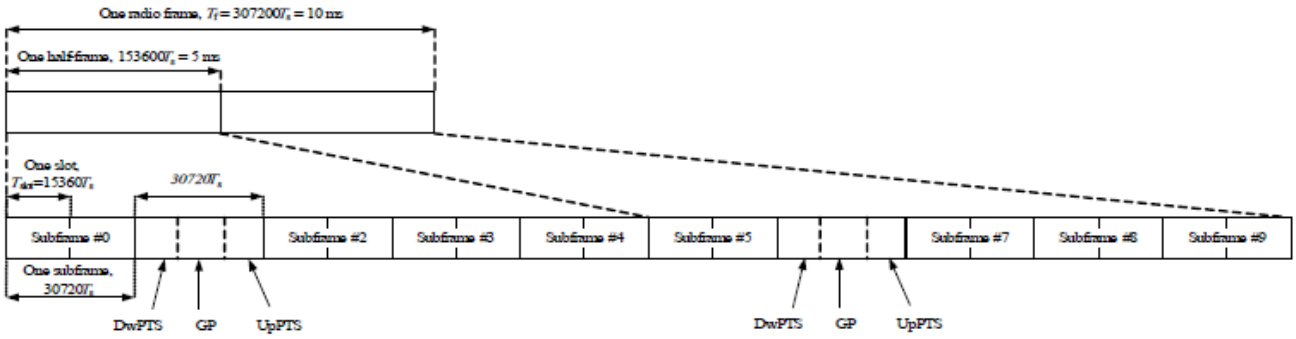
Figure 3-2. LTE FDD Frame Structure



- Framing
  - 10ms frame
  - 1ms subframe
  - 0.5 ms timeslot
  - Six or seven symbols per time-slot (that is, 20MHz LTE)
    - 307200 samples per 10ms frame
    - 15360 samples per 0.5ms timeslot
    - Extended Cyclic Prefix
      - Six symbols per timeslot
      - All same length
      - 2560 = 512 cyclic prefix + 2048
    - Normal Cyclic Prefix
      - Seven symbols per timeslot
      - 1 st symbol—2208 = 160 cyclic prefix + 2048
      - Other symbols—2192 = 144 cyclic prefix + 2048
  - Other Sampling rates
    - {0.75x, 0.5x, 0.25x} multiplication factor for sample rates of { *15MHz*, 10MHz, 5MHz}

3.2.2.1.2 LTE TDD Framing

Figure 3-3. LTE TDD Frame Structure (5ms Switch Point Illustrated)



- Framing
  - (same as FDD case)
  - Plus… half frame 5ms concept
- LTE cyclic prefix is static and can not be modified while a link is active.
- Dynamic change of UL/DL ratio—Switch Point: 5ms half frame boundary or 10ms frame boundary
- Special LTE TDD subframe
  - No implication for IQN2
  - Symbols are simply used for different uses
  - Symbols are same size as non-special timeslots
  - Two options for Switch Point
    - Case1 (5ms) one special frame per 5ms
    - Case2 (10ms) one special frame per 10ms
    - IQN2 AIL needs to support change in UL/DL ration on 5ms or 10ms basis
- TDD Muxing
  - Each timeslot can be either UL or DL

– Ratio can be changed at the switch point.

The IQN2 AIL has specific HW based on the sub-frame or slot concept. It simply counts n symbols within a frame/half-frame. An egress and ingress channel is allocated for each AxC. The TDD bit map per radio standard indicates on a symbol-by-symbol basis whether or not that symbol is to be DMA'ed or whether that symbol is empty. It is the programmer's responsibility to remap the LTE TDD UL/DL partition into the appropriate DMA control bit maps.

IQN2 AIL is likewise uninterested in the concept of special frames. The user programs the DMA bit maps so the DL symbols are handled by the Egress channel and UL symbols are handled by the Ingress channel. In this way, IQN2 AIL generalizes traffic, handling multiple radio standards with a single HW interface.

3.2.2.1.3 LTE MBSFN Framing

LTE MBSFN is a dynamic transition from normal to extended cyclic prefix with an unused gap between the two. The transition occurs part way through an LTE sub-frame. From the perspective of higher layer SW, the position of the transition is known; from the perspective of IQN2 AIL, it is programmed on a sub-frame basis on how it should process the next sub-frame.The MBSFN system operation translates to a dynamic modification of AIL framing engines and an agreed upon handling of the "gap."

Radio framing engines with the IQN2 sample and hold MMR configuration data at the beginning of each symbol. This allows SW to carefully modify the framing parameters while AIL HW is in mid-symbol. In this way, SW may re-configure the AIL to implement different radio framing from one sub-frame to the next.

From the perspective of the AIL, the "gap" is treated as an extremely short symbol. Application SW must index the symbol numbers accordingly, counting the gap as one of the symbols. SW may chose to TDD "OFF" the gap so that no dummy DMA data is required, but when SW writes the symbol index into the packets, it must increment the index as if the gap were an actual symbol. A SW wake-up routine is required to perform real-time MBSFN configuration of IQN2. An AT system event should be utilized in order to trigger the SW wake-up routine.

3.2.2.2 CPRI LTE (FDD and TDD)

3.2.2.2.1 CPRI LTE (FDD and TDD) Packing of AxC

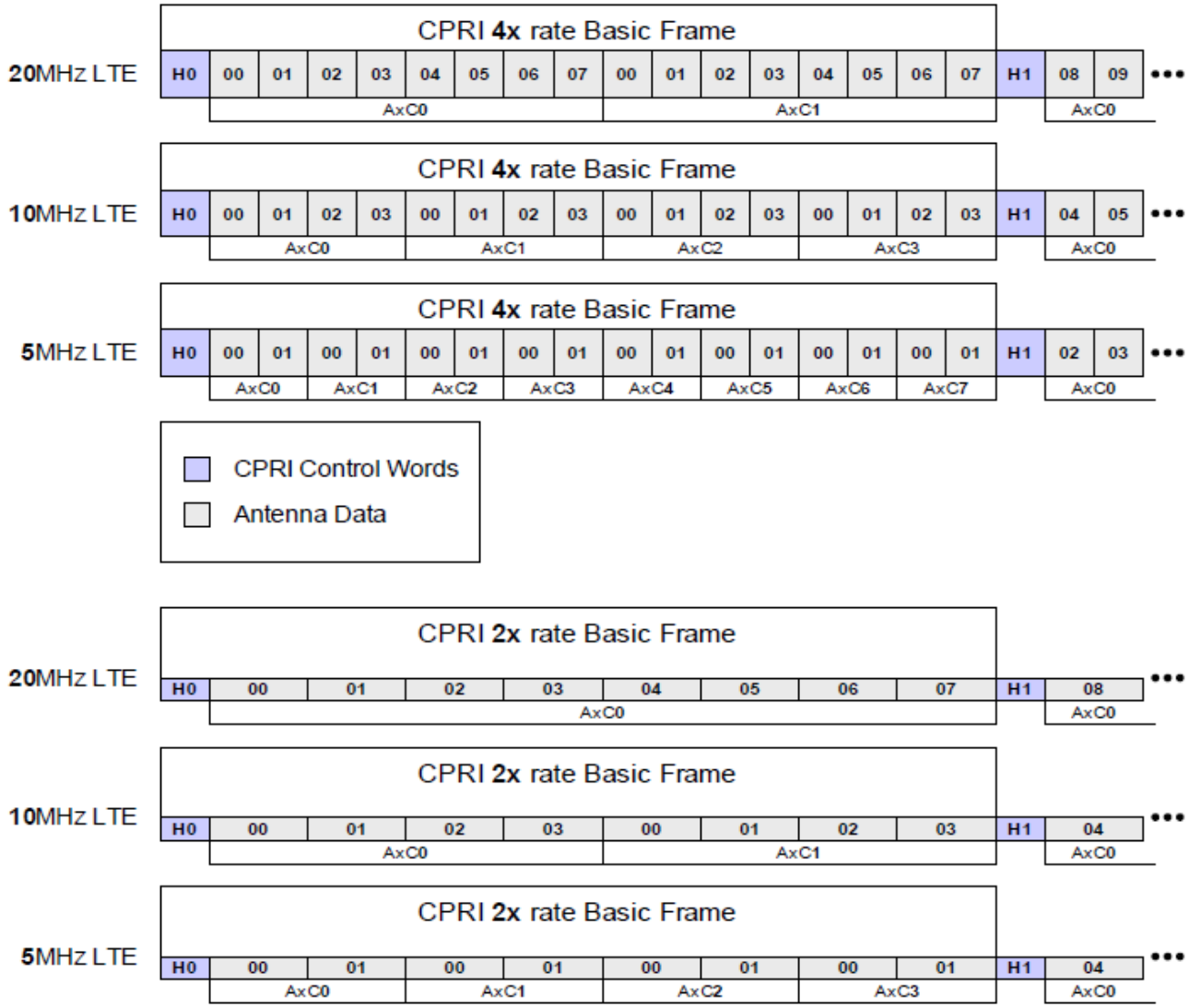
Primarily, the industry is using CPRI LTE sample bit widths of 15bit I + 15bit Q. At these sampling rates, the following number of LTE AxC are supported at the different rates.

Table 3-2. LTE AxC Supported Over Different CPRI Link Rates

	Link Rate					
LTE	**2x**	**4x**	**5x**	**8x**	**10x**	**16x**
1.4 MHz	16	32	40	64	64	64
3.0 MHz	8	16	20	32	40	64
5 MHz	4	8	10	16	20	32
10 MHz	2	4	5	8	10	16
15 MHz	1	2	3	5	6	10
20 MHz	1	2	2	4	5	8

The LTE15 link rate does not evenly fit into the CPRI link. The CPRI stuffing sample mechanism defined in Mapping Method 3 (see CPRI spec 5.0) is implemented to rate match the LTE15 into the CPRI PHY. Rate matching is the concept of inserting bubbles in order to match the rates of the dissimilar frequency requirement.

Figure 3-4. CPRI LTE Sample Packing {20MHz, 10MHz, 5MHz} vs. {4x, 2x} Link Rate



3.2.2.3 OBSAI LTE (FDD and TDD)

With 16-bit I + 16-bit Q sample sizes, exactly four samples fit into an OBSAI message; each OBSAI message contains four samples for one AxC.

The five-bit OBSAI timestamp starts at zero (on a radio frame boundary) and increments by one every four samples for a given AxC.

The AT (IQN2 Timer) is used to predict LTE (and other standards) frame boundary that is used in timestamp Tx generation and Rx checking. The IQN2 AIL contains a uAT timer which mirror the AT timers. In practice it is the radio timer in the uAT which is used for AIL operation.

OBSAI RP3 has done a really nice job of listing all the LTE channel bandwidths and listed the programming of the dual-bit-map FSM mechanism for rate matching.

See the OBSAI RP3 specification, Appendix F for details.

While the OBSAI RP3 standard does not specially call out LTE TDD, it is easily extrapolated that zero samples will continue to flow though the interface while either a UL or DL link is idle. During a TDD OFF symbol, OBSAI messages have zero payload with OBSAI message headers incrementing the TS field as if no TDD were implemented. The reception portion of IQN2 AIL continues checking the time stamp of TDD OFF symbols and expects proper headers of each message. The payload portion of Ingress TDD OFF symbols is discarded.

3.2.3 LTE 80 MHz and 100MHz Support

The LTE standards body has not fully developed the concept of 100MHz LTE. There are two possibilities:

- 80MHz: four times the bandwidth of 20MHz LTE
- 100MHz: five times the bandwidth of 20MHz LTE

3.2.3.1 80 MHz

Four times the bandwidth of 20 MHz LTE does fit into a single 8x rate IQN2 AIL link. IQN2 AIL does support modulo transmission rule (which is the way to program OBSAI for this AxC traffic rate).

3.2.3.2 100 MHz

One possible method of supporting 100 MHz LTE is for the sending device to segment the AxC into five parts, then send these parts over five different 20 MHz LTE AxC. If it is done correctly, the Multicore Navigator mechanism could be manipulated on the receiving device such that only Multicore Navigator headers would need to be modified in order to reconstruct the 100MHz AxC from the five 20 MHz AxC.

The manipulation of PktDMA can only concatenate multiple PktDMA packets together. It can not perform a sample-by-sample interleave. For this reason, an entire LTE 100MHz symbol needs to be pre-buffered at the source and segmented into five parts. This will result in the additional latency. It is up to the system designer to determine if this additional latency is acceptable.

To facilitate this reconstruction, the IQN2 PKTDMA channels involved should be programmed to use Multicore Navigator “Host Mode” instead of Multicore Navigator “Monolithic Mode.” Host mode separates the Multicore Navigator descriptor from the Multicore Navigator buffer. Host mode also allows for multiple descriptor/buffer pairs to be linked-listed into a larger packet structure. In the most optimal usage, the Multicore Navigator buffers should be sized such that a single LTE 20 MHz symbol fits into a buffer. In this way, there will be a single Multicore Navigator descriptor/buffer pair per 20 MHz Symbol. After all 20 MHz symbols are received, the application software can manipulate the buffer pointers linking all five descriptor/buffer pairs into a single LTE 100 MHz symbol packet.

3.2.4 TD-SCDMA

IQN2 AIL CPRI TD-SCDMA support is a comprehensive solution to TD-SCDMA. IQN2, in conjunction with Multicore Navigator, seamlessly transports and coordinates TD-SCDMA traffic with application software running on the CorePac core.

For TD-SCDMA, the DMA granularity may need to support two different modes:

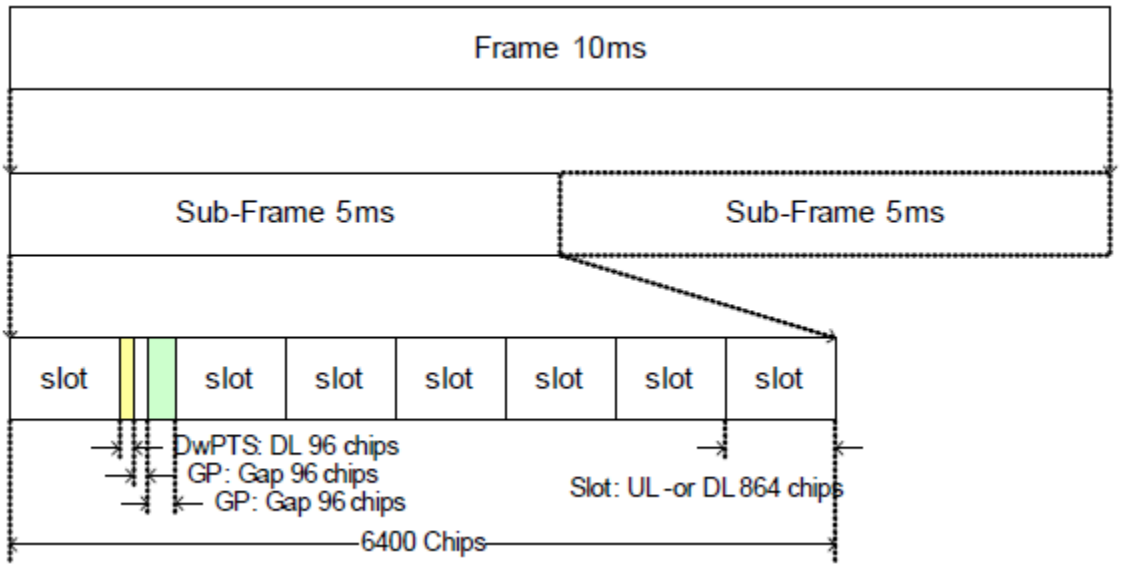
- DMA on Symbol Boundaries
- DMA on ½ Symbol Boundaries

½ Symbol Boundary DMA is not supportable with OBSAI.

3.2.4.1 TD-SCDMA Framing

TD-SCDMA is a TDD standard meaning that the Air channel is multiplexed between UL and DL.

Figure 3-5. TD-SCDMA Frame Structure



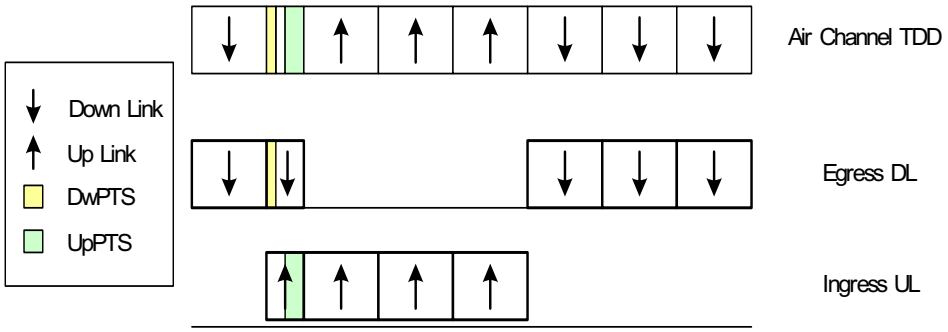
TD-SCDMA has a 10ms frame that is broken down into two 5ms subframes. Each subframe is further broken down into:

- Seven slots for transporting antenna traffic—Each are 864 chips
- Three special slots:
  - DwPTS: DL 96 chips
  - GP: Gap (unused) 96 chips
  - UpPTS: UL 160 chips

The first of the seven slots is always DL data. The special slots always follow the first normal slot in the subframe. The remaining regular slots can be configured to be either UL or DL information with the following restrictions:

- If there are any UL slots, the first UL slot follows the special slots
- All UL slots are grouped together with only one transition to DL slots
- All remaining DL slots are grouped together

Figure 3-6. TD-SCDMA Example DL/UL Mix



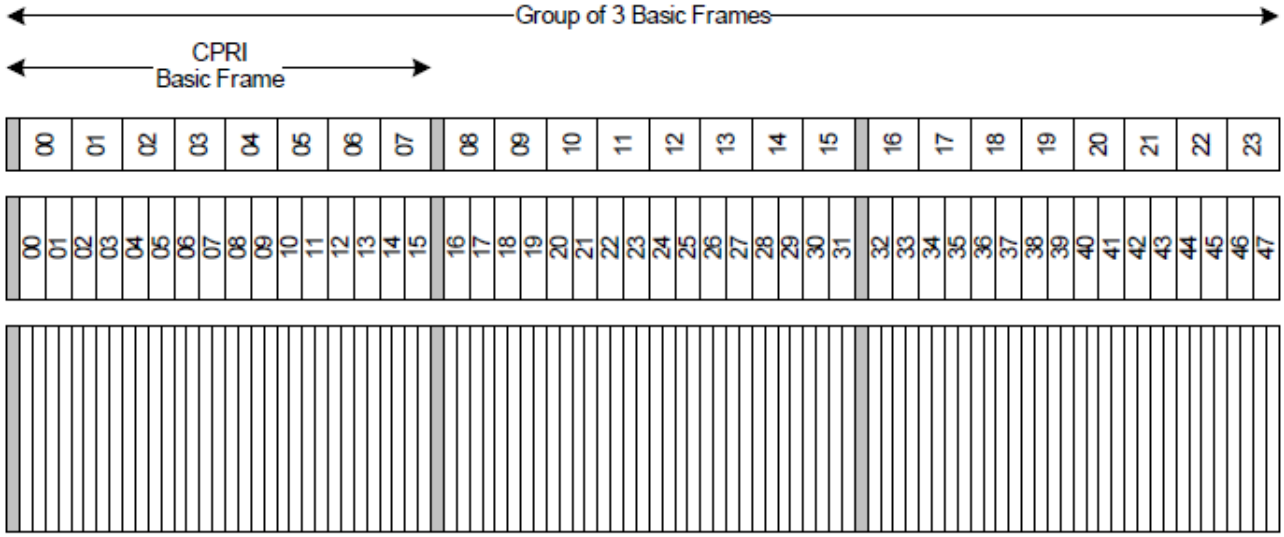
The air channel is TDD (simplex), but the CPRI SerDes are not simplex; the SerDes are full duplex. The SerDes have two half links (Tx and Rx) with DL traffic on one half (that is, TX) and the UL traffic on the other half (that is, RX). This has the unavoidable impact that only one half of the SerDes bandwidth is usable in TDD systems.

There are three separate “special slots” in TD-SCDMA, but for simplification, IQN2 AIL treats all three special slots as grouped together or a single slot. The next special handling aspect of IQN2 AIL is that the grouped special slot is handled redundantly for both UL and DL. This special handling is transparent at the RF card as the CorePac fills in zeros for all unused portions in the DL case and the CorePac disregards unused portions in the UL case.

The IQN2 AIL does not perform any special processing for 2x oversampling. The user would need to allocate two separate antenna carrier bins where IQN2 AIL would simply treat Odd and Even samples as separate antennas. If the user requires odd and even samples interleaved, the CorePac would be required to perform this function.

3.2.4.2 CPRI TD-SCDMA

Figure 3-7. TD-SCDMA AxCs Packed into Three CPRI Basic Frames



CPRI was developed initially for WCDMA and because TD-SCDMA is exactly one-third the sample rate, TD-SCDMA fits into the CPRI framing. For CPRI WCDMA (15-bit mode), a sample for each of {8, 16, 32} AxC fits respectively in a {2x, 4x, 8x} link rate basic frames; the same is true for TD-SCDMA. The difference between WCDMA and TD-SCDMA is:

- WCDMA: The next basic frame contains the next sample for those AxC
- TD-SCDMA: The next two basic frames contain a sample for other AxC. Effectively 3x more AxC are supported.

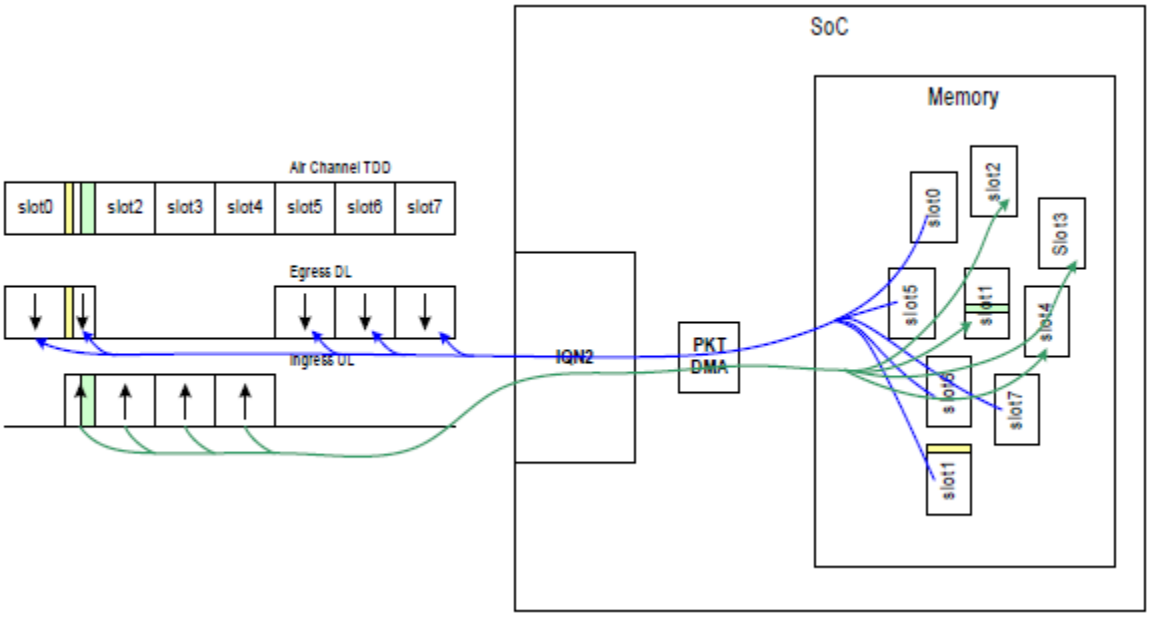
The CPRI link rates {2x, 4x, 8x} support {24, 48, 96} AxC. Even though the CPRI PHY supports up to 96 AxC, the IQN2 AIL only supports up to 64 DMA channels per link and PktDMA supports up to 48 DMA channels, so 48 will be the real maximum channel number supported.

There are a total of 38,400 basic frames per 10 ms frame. For TD-SCDMA support, these basic frames are grouped into threes giving a total of 12,800 basic frame groups per 10ms frame.

3.2.4.3 TD-SCDMA DMA

The DMA and memory storage of TD-SCDMA Data is slot-by-slot based. Each slot of TD-SCDMA data is stored in a contiguous memory block known as a buffer. While IQN2 AIL is receiving TD-SCDMA AxC data, it counts through the samples and identifies slot boundaries. IQN2 AIL tightly coordinates with the PKTDMA subsystem to transport the slot into memory.

Figure 3-8. TD-SCDMA Slots Transferred To/From Memory



Once the slot is completed in memory, the Multicore Navigator queue manager presents the buffer to the CorePac core. A pointer to the buffer is placed into a queue that is accessible to the CorePac core. The application software has great flexibility in configuring and use of these buffers. A system event can be programmed to alert the CorePac that an arrival queue is non-empty; the CorePac core can use this system event either as an interrupt or simply poll the event. The application software can consume the data very quickly or can allow multiple slots of data to accumulate in the arrival queues. A single arrival queue may be used for all AxC, or multiple arrival queues may be used to facilitate some form of priority scheme.

The separation of UL and DL has several degrees of freedom. Because UL and DL are separated by ingress and egress links, the IQN2 and Multicore Navigator can be programmed to place UL and DL traffic in separate memory regions such as different L2 regions for different CorePac cores.

The mixture between UL and DL traffic is also highly programmable. Even though TD-SCDMA only allows for two transition points (switch points) between UL and DL traffic within a subframe, the IQN2 is highly programmable and has no such limitation. IQN2 AIL allows the allocation of UL and DL slots to be programmed on-the-fly. From one TD-SCDMA frame to the next, the slots can be reallocated between UL and DL.

The IQN2 AIL TDD bit map per DMA channel is programmed with indication bits configuring IQN2 for:

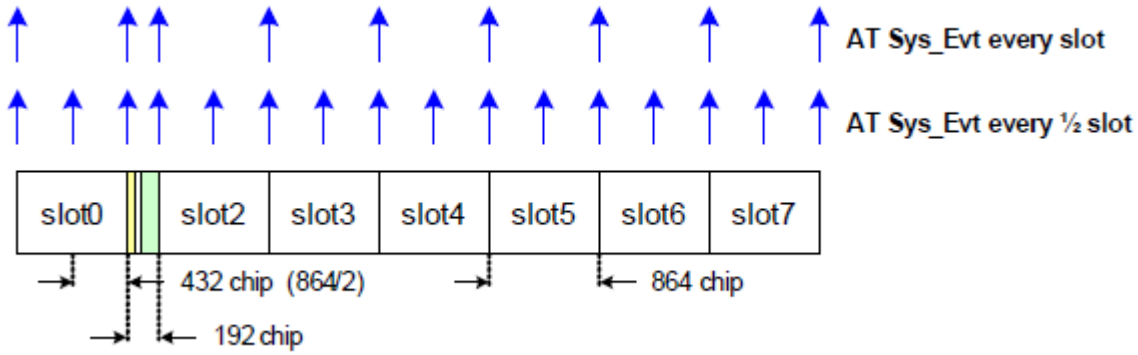
- 1’b1: slot is active and DMA data used
- 1’b0: slot is null, no internal DMA for slot
  - Tx: zeros filled into CPRI link
  - Rx: data is not extracted from CPRI link

The example TDD_EN bit field setup in AIL_IQ_EFE_TDD_EN_CFG0 and AIL_IQ_IFE_TDD_EN_CFG0 register looks like below.

AIL SI Egress or Ingress… bit0=0, 1, 1, 1, 1, 0, 0, 0, x, x, x, x, x, x, ...,x, bit31=x

3.2.4.4 TD-SCMDA Timer (AT) Operation

Figure 3-9. TD-SCDMA (AT) Timer-Based System Event Generation

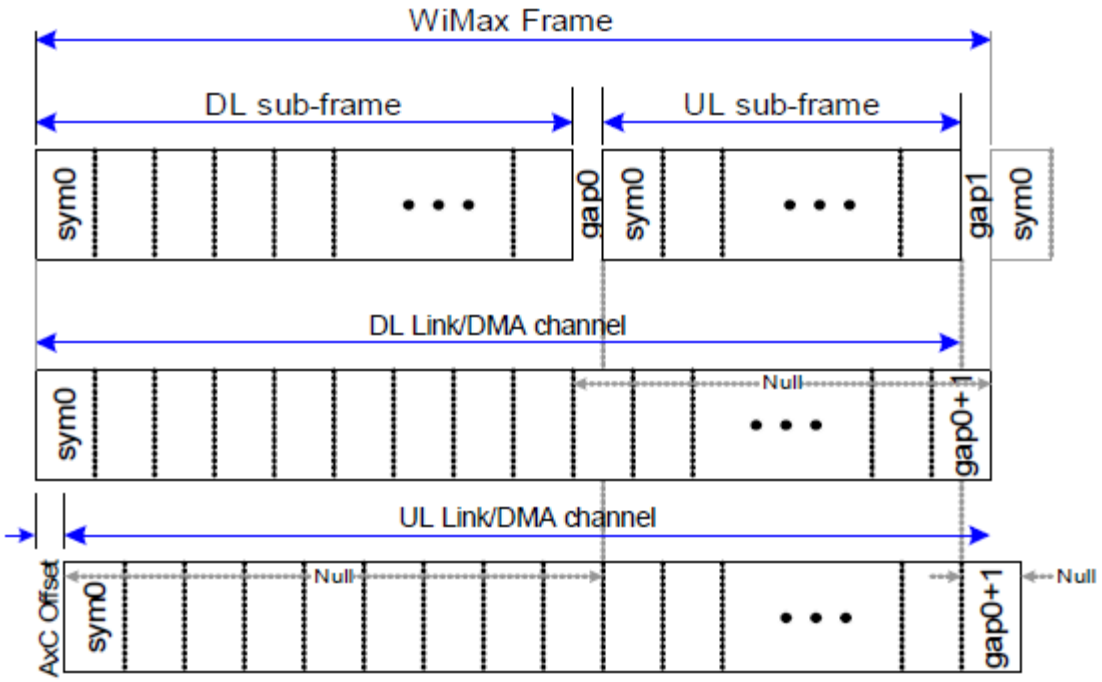


The IQN2 timer (AT) can generate system events for use by application software running on the CorePac cores. The AT is highly programmable. As a minimum requirement, it can supply timing strobes on TD-SCDMA slot or one-half slot boundaries by using modulus count register. A system event is generated at the beginning of the special region and at the end of the special region, but system events are not generated on special slot boundaries within the “special” region.

3.2.5 WiMax

3.2.5.1 WiMax Framing

Figure 3-10. WiMax Frame Structure



- OFDM samples n= {128, 512,1024,2048}
- cyclic prefix p= {n/4, n/8, n/16, n/32}
- Symbol size n + p
- sample rate 28/25 x {1.25MHz(128), 5MHz(512), 10MHz(1024), 20MHz(2048)}

  - 7MHz and 8.75MHz also have importance
- Over-sample 1x
- Data width 16-bit I and 16-bit Q

The WiMax TDD frame is partitioned into two subframes with a gap in between:

- DL subframe
- UL subframe

The DL and UL subframes are always an integer number of WiMax symbols in length. All symbols are the same length in WiMax and comprise an FFT length of samples plus a fixed-length cyclic prefix (combination of these two is referred to as a symbol in this document). The frame length MOD symbol length is the gap length (always smaller than a symbol in length).

On a frame-by-frame basis, the DL portion can shrink or grow by an integer number or blocks with the UL portion growing or shrinking by the amount. The gap between UL and DL does not change as the UL and DL portions are adjusted in duration.

3.2.5.2 WiMax, IQN2 Implementation

The IQN2 generic mechanism is used to implement WiMax. As with all TDD processing, IQN2 AIL uses two separate DMA channels to implement a single WiMax TDD antenna:

- UL: Ingress DMA channel
- DL: Egress DMA channel

Both channels are configured with n+1 symbols of length where:

- First n symbols programmed as symbol length
- Last symbol programmed as gap length (combined length of two gaps)

IQN2 has the generic concept of an AxC offset and Radio Standard offset which allows antenna carriers to be offset relative to the system timer (and each other). For WiMax, the offset mechanism is manipulated to create the sub-frame time offset between DL and UL. The DL AxC offset is programmed to be whatever the user requires. The UL Offset is programmed as the DL offset plus the time duration of the first gap; this is just to align the UL symbol boundaries.

Using AxC Offset for this purpose may pose a very small limitation on a user. IQN2 AIL supports a whole frame of AxC offset, but the UL offset will consume a small portion of this AxC offset. In OBSAI, the user could wait the entire RadT instead of using AxC_Offset MMR. In CPRI, the user should use the Group Offset (basic frame and hyper frame offset) which is effectively a radio standard offset for this purpose.

Just as with all other TDD standards, the PD IQN2 AIL bit map per DMA channel is programmed with indication bits configuring IQN2 for:

- 1'b1: symbol is active and DMA data used
- 1'b0: symbol is null, no internal DMA for symbol
  - Tx: zeros filled into OBSAI/CPRI link
  - Rx: data is not extracted from OBSAI/CPRI link

The bitmap may be modified on-the-fly allowing for changes in the DL/UL ratio on WiMax frame boundaries.

3.2.5.3 OBSAI WiMax

OBSAI RP3 lists all the WiMAx channel bandwidths and the programming of the dual-bit-map FSM mechanism for rate matching.

See the OBSAI RP3 specification, Appendix D for details.

3.2.5.4 CPRI WiMax

CPRI Mapping Method 3 Stuffing Sample mechanism can be used for rate matching WiMax into the CPRI PHY. See CPRI Spec 5.0 for more details.

3.2.6 GSM/Edge Requirement and Handling

- DMA and queuing
  - 1 packet per GSM time slot
- OBSAI specific
  - Each OBSAI message is 4 samples
  - GSM time slots are not n x 4 samples
  - OBSAI message partition is not exactly on GSM time slot boundary
- GSM Timing
  - GSM frame is 60ms/13
  - GSM time slot (60ms/13)/8
  - Need 3.5 hour timer… 26 x 51 x 2048 x frames
    - Need unique frame number in 3.5 hour timer
  - Each GSM Time slot is
    - CPRI 141,750 sys_clk (245.7MHz)
    - OBSAI uneven number of sys_clk (307.2MHz)
    - AT is programmed to approximate timing of GSM time slot timing to the nearest clock cycle.

System events are required on GSM time slot boundaries and 1/64 th GSM time slot boundaries. The GSM sample clock is not in a nice multiple of the OBSAI sys_clk rate, so an approximation is performed. It is observed that every 13 GSM frames, the GSM timer is an exact multiple of byte clock which occurs every 60 ms.

- 18432000 307.2MHz clocks every 60 ms
- 104 GSM timeslots per 60ms
  - 24 timeslots w/ 177230 clocks
  - 80 timeslot w/ 177231 clocks

Table 3-3. GSM Slot 307.2 MHz Approximations

	307.2MHz clocks per GSM slot (Approximations)							
	Slot0	**Slot1**	**Slot2**	**Slot3**	**Slot4**	**Slot5**	**Slot6**	**Slot7**
Frame0	177231	177231	177231	177230	177231	177231	177231	177231
Frame1	177230	177231	177231	177231	177230	177231	177231	177231
Frame2	177230	177231	177231	177231	177231	177230	177231	177231
Frame3	177231	177230	177231	177231	177231	177230	177231	177231
Frame4	177231	177231	177230	177231	177231	177231	177230	177231
Frame5	177231	177231	177230	177231	177231	177231	177231	177230
Frame6	177231	177231	177231	177230	177231	177231	177231	177230
Frame7	177231	177231	177231	177231	177230	177231	177231	177231
Frame8	177230	177231	177231	177231	177230	177231	177231	177231
Frame9	177231	177230	177231	177231	177231	177230	177231	177231
Frame10	177231	177230	177231	177231	177231	177231	177230	177231
Frame11	177231	177231	177230	177231	177231	177231	177230	177231
Frame12	177231	177231	177231	177230	177231	177231	177231	177230

- GSM sub-slot System Events
  - 64 system events per slot
  - 2769 307.2Mhz clocks per segment
  - Last segment of time slot is either 14 or 15 clocks longer than the 2769 clock segments

3.2.6.1 GSM Base Band Hopping

GSM Base Band Hopping is a scheme employed in GSM that can shift the frequency band allocated to a user.

- DMA
  - Have a fixed PktDMA channel per all possible AxC
    - App software chooses which DMA channel to write to
  - Have a single PktDMA channel for all Egress GSM control
    - Use Protocol Specific fields in Multicore Navigator header to pass OBSAI address or OBSAI header from application software to IQN2
- Data
  - Both UL and DL data have a (DTX) non-transmission portion at the end of each timeslot
  - DL has two forms, Compressed (mostly DTX) and normal (only a few DTX messages)
- Tx Rules
  - Use fixed DBM rules, mapping all possible antenna carriers
  - Fixed OBSAI adr and type per AxC (for AxC traffic)
  - Use OBSAI adr from packet (for GSM Control)
- Hopping
  - The TDD bit per AxC is dynamically configured by a SW wake-up routine each GSM time slot indicating weather the particular AxC is BB_Hop On/Off for that GSM time slot
- OBSAI msg Time stamp
  - MSB is 1 for beginning of time slot (0 else)
  - Five LSBs count up normally, wrap every 32
  - DL, first message MSB is active first message
  - UL, first four messages, MSB is “1”
- Error conditions
  - If last message of time slot is corrupted, need watchdog or other timer to close out EOP
  - If first message of UL is corrupted/lost, cannot lose whole packet

Normally, one device will process a set number of fixed antennas of data. In baseband hopping, this antenna contribution is dynamically mapped to different physical antennas on the RF card.

The basic radio concept is that multiple GSM frequency bands are supported by a single radio tower. Some of these frequencies have lower noise floors than others. With Baseband hopping, the “good” and “not-as-good” GSM frequency bands are TDM shared by all the active antenna traffic.

The implications on IQN2 transmission are:

- The mapping of PktDMA streams can be dynamically reassigned on GSM time slot boundaries. All possible transmission rules are predefined at configuration time (even though only some of these will be active at any point in time)
- The App software will dynamically map which antenna to transmit on simply by targeting a different Multicore Navigator queue. IQN2 is tolerant of data being present (or not) on a time slot by time slot basis.
- For GSM control data, Multicore Navigator passes the OBSAI address to allow for the OBSAI address to dynamically remap. App software writes the OBSAI address fields into a Multicore Navigator field. The PE will use this OBSAI address when building messages (not using the default OBSAI address programmed for the channel).
- IQN2 AIL PE needs to be programed every GSM time slot by using the TDD bit so that the next time slot will be BB_Hop ON or OFF. When OFF, no DMA data is expected and the Egress circuits will output OBSAI emtpy_msg or CPRI zeros.
- IQN2 AIL PD is also tolerant of whole missed GSM time slots.

Example:

If the baseband pool is supporting 36 AxC, each IQN2 AIL in each device will have 36 identically mapped transmission rules. If each device is supporting only eight of the 36 AxC, the application software will write data to eight of the 36 Multicore Navigator queues with GSM data for each GSM time slot. The IQN2 will process only those channels that have data for that particular time slot.

For each time slot of egress GSM data, the application software also supplies control data associated with the RF destination of the AxC data. The application software controls or routes the transfer of the control packets by writing the appropriate OBSAI address into a protocol-specific word attached to the Multicore Navigator header. IQN2 AIL inserts this software-written information into the OBSAI header when constructing the OBSAI message.

BB hopping has the specific requirement that a single device can dynamically target different RF destinations with control information. IQN2 has a very specific feature that allows this behavior; application software can dictate the OBSAI address in the header of the control message (when the message is in L2). When using this mechanism, a single OBSAI transmission rule can be used for many different control messages with different destination addresses.

In most cases, GSM samples are not 16-bit or 8-bit. IQN2 should be programmed to treat GSM data as generic 32-bit data in these cases so any endianess swap logic will not corrupt the samples. GSM Timestamping is not frame-based, but timeslot-based. This enables whole time slots to be omitted without regard for maintaining gaps in timestamp generation/checking. It is highly advisable that all GSM channels/AxC within a hopping group have the same AxC offset. The IQN2 AIL would probably work with different AxC offset, but this makes no sense from a system perspective.

3.2.6.2 GSM Time Slot Compression

IQN2 is required to handle both compressed and non-compressed GSM. The high level concept of compression is that DL data is sent as only 1bit I + 1 bit Q. The Radio module then applies a gain and expands the resolution of the samples. From the perspective of the IQN2 AIL, the concept of compression is simply that some portion of the end of a time slot is not populated with antenna data.

The implications on transmit.

- (OBSAI) AIL PE will not fail the link if the DMA data does not fully fill the GSM Time Slot. The PE will transition to empty messages or zero antenna data
- (CPRI) AIL PE will not fail the link if the DMA data does not fully fill the GSM Time Slot. The PE will commence with the next packet at the beginning of the next GSM time slot.

The implications on ingress/reception are nearly identical:

- (OBSAI) the AIL PD is programed to accept a very short time slot.
- (CPRI) the HW packetizes frame-based AIL data into full length GSM time slots. The received packets result with zero padding and user application truncates packets to real size.

The AIL module does not natively support the GSM mantissa/exponent format. Also, special care should be taken by the user if a mantissa/exponent format is to be transmitted or received over the CPRI link, since the AIL module performs sign extension to all 7-bit and 15-bit quantities. The user would have to be cognizant of this sign extension and make the necessary adjustments for it, such as ignoring the sign extension during reception and sign extending the data on transmission so that it is not saturated by the AIL module.

3.2.7 Dynamic Configuration

IQN2 supports dynamic configuration in run time as listed below:

- AIL lane Add/Delete
- AxC channel Add/Delete
- GSM Baseband Hopping
- LTE (TDD) and WiMax (TDD)
  - Change UL/DL ratio (on-the-fly)
  - LTE MBSFN support

- Timing
  - System Event Add/Delete

IQN2 supports several forms of dynamic changes that support changes to the base station radio configuration. These types of changes could be split into two basic categories:

- On-the-fly: Change occurs from one frame to the next without any OFF or error period. Requires special ping/pong buffering of configuration data where the ping/pong will toggle on the next frame boundary.
- Normal Changes: An antenna carrier is torn down, later rebuilt to accomplish a change. There is the expectation that some small amount of time of no transmission will elapse.

Basic operation of links and antenna carriers allow Add/Delete support. On-the-fly modification is generally not supported. To perform a Modify operation, delete the AIL lane/AxC followed by an Add with the new characteristics.

When Adding or Deleting a channel, there are three levels of configuration required:

- PHY: Links need to be enabled and preferably up and running
- Protocol: OBSAI address, type, transmission rules setup
- DMA: DMA channels assigned and turned on

WCDMA AxC Add/Delete should incorporate the Add/Delete of the assigned DirectIO DMA configuration. With PktDMA, the user has the choice to Add/Delete Multicore Navigator channels when performing Add/Delete of AxC, or simply keep the Multicore Navigator channel active always (as no data will transfer when the AxC is OFF).

The GSM Base Band hopping special requirements are not handled as reconfiguration, but rather by allowing software to direct where data goes. For antenna data, all DMA channels are allocated, and software steers data into the appropriate DMA channel FIFO. For control data, software writes the destination OBSAI addressing into the Multicore Navigator packet.

The standards that support TDD have separate UL and DL regions. On-the-fly update of the DL/UL ratio is required. On-the-fly update requires IQN2 to ping-pong buffer control information and transition to new control information at a precise timing (that is, on frame boundary).

Table 3-4. OFDM On-The-Fly Update Requirements

	On-the-fly Update		
Radio Standard	**UL/DL Ratio**	**Symbol Size**	**Sample Freq or Bandwidth**
LTE FDD	N/A	No	No
LTE TDD	Yes	No	No
WiMAX TDD	Yes	No	No
TD-SCDMA	No	N/A	No

LTE supports extended and normal cyclic prefix length in symbols and multiple bandwidth. It is expected that some users will support multiple LTE configurations on the same device (and even on the same link). LTE bandwidth change (for example from 20 MHz to 10 MHz) or change of cyclic prefix length is a radical re-configuration of an antenna carrier.

The user has a choice of handling Multicore Navigator when supporting multiple LTE bandwidths simultaneously. The easiest (and most practical) solution is to allocate the Multicore Navigator buffer size to accommodate the largest symbol size supported. When an antenna of lesser bandwidth uses these buffers, only a fraction of the memory is actually utilized. When using this simple approach to Multicore Navigator memory management, there is no Multicore Navigator reconfiguration required when changing LTE bandwidth.

The IQN2 is designed to handle 8 radio standard variants simultaneously (each LTE sampling rate and cyclic prefix is considered a variant). The AT has 8 different Radio timers. Each AIL has 8 different radio framing engine configurations. Each AIL PHY can handle at least 8 different radio standards (and Ingress and Egress can each have different radio standards). The AIL CPRI implementation supports up to 8 different groups and AIL OBSAI implementation supports up to 32 Egress transmission rules. The IQN2 is very well positioned to simultaneously support a complex mixture of radio standard traffic.

Changes of system event generation are supported by first turning a system event off, reconfiguring the system event, then turning it on. As a rule, system events are mainly used by application software and having an OFF period of time is required for software to re-sync to the difference in system event timing. Each system event is independent of the others, giving the flexibility to change one without corrupting any others.

Dynamic AxC channel reconfiguration example :

Egress:

- Stop pushing packets into the Tx queue
- Allow PktDMA and AIL channel to starve by waiting some time
- Disable the AxC channel at DIO SI EFE (for WCDMA)
- Disable the AxC channel at AIL EFE
- Wait for at least 1 radio frame of time
- Reconfigure AIL channel
- Reconfigure DIO channel (for WCDMA)
- Enable DIO channel if it was disabled
- Enable AIL channel
- Start pushing Tx data before the next frame boundary

Ingress:

- Disable AIL IFE channel
- Wait for at least two radio frames of time and confirm if the channel status is low
- If the channel status doesn't go low, use force channel shutdown
- Disable DIO SI IFE channel (for WCDMA)
- Disable PktDMA channel if needed
- Reconfigure AIL channel
- Reconfigure DIO channel or PktDMA Rxflow if needed
- Enable PktDMA and DIO if it was disabled
- Enable AIL channel

Disabling or enabling PktDMA for Rxflow reconfiguration is not a must. It could be safely done in run time. BW change requires Channel LUT value change and this should be done only when all related AxC channels are disabled. Force channel shutdown is a useful feature when unexpected packet EOP loss occurs like cable de-insertion or hot-swap.

IQN2 Timing Information

Topic **Page**

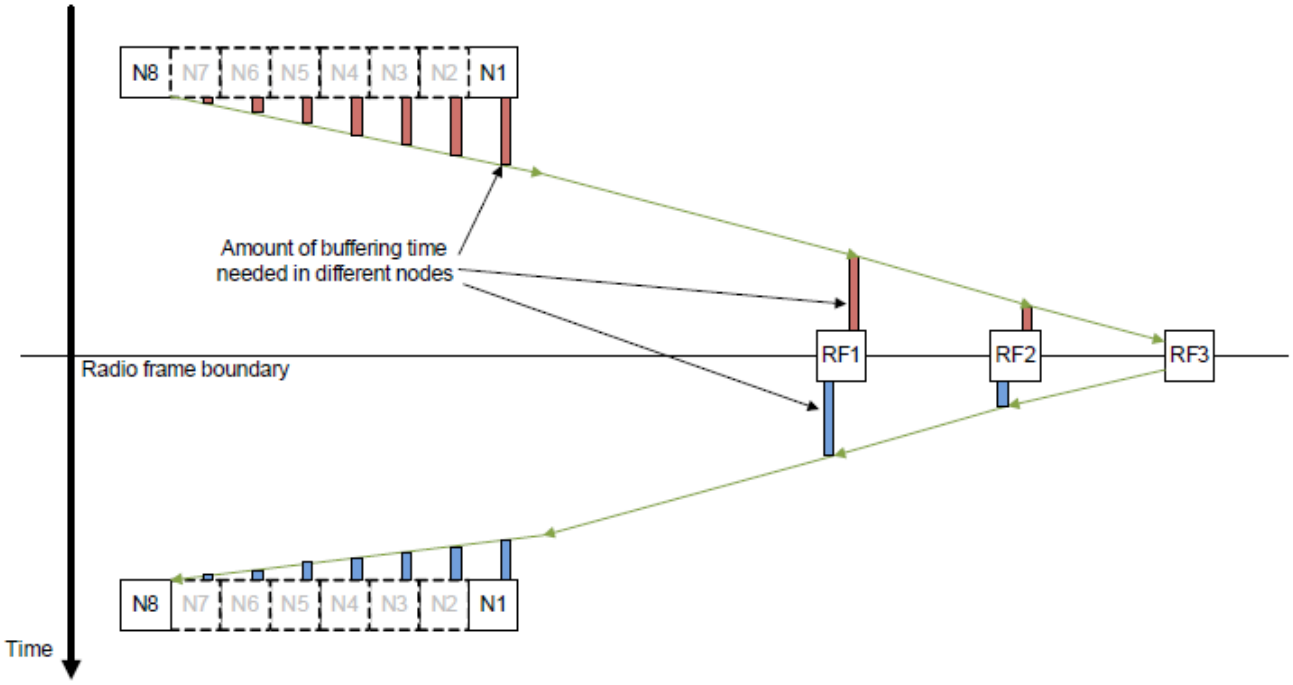
4.1 Timing and Topology

Within the daisy chain, the user needs to define the timing reference. One logical choice is to define time equal to zero at the radio head. This would yield all DL timing to be negative time and all uplink timing to be positive time. An alternative is to define time=0 at the first DL node in the chain; this way, all offsets are positive.

With any approach, each device in the chain has some amount of propagation delay between its input and output links. This translates into approximately 228 ns (around WCDMA one chip) of timing difference between adjacent devices in the chain. IQN2 AIL has sufficient buffering capability in most topology cases.

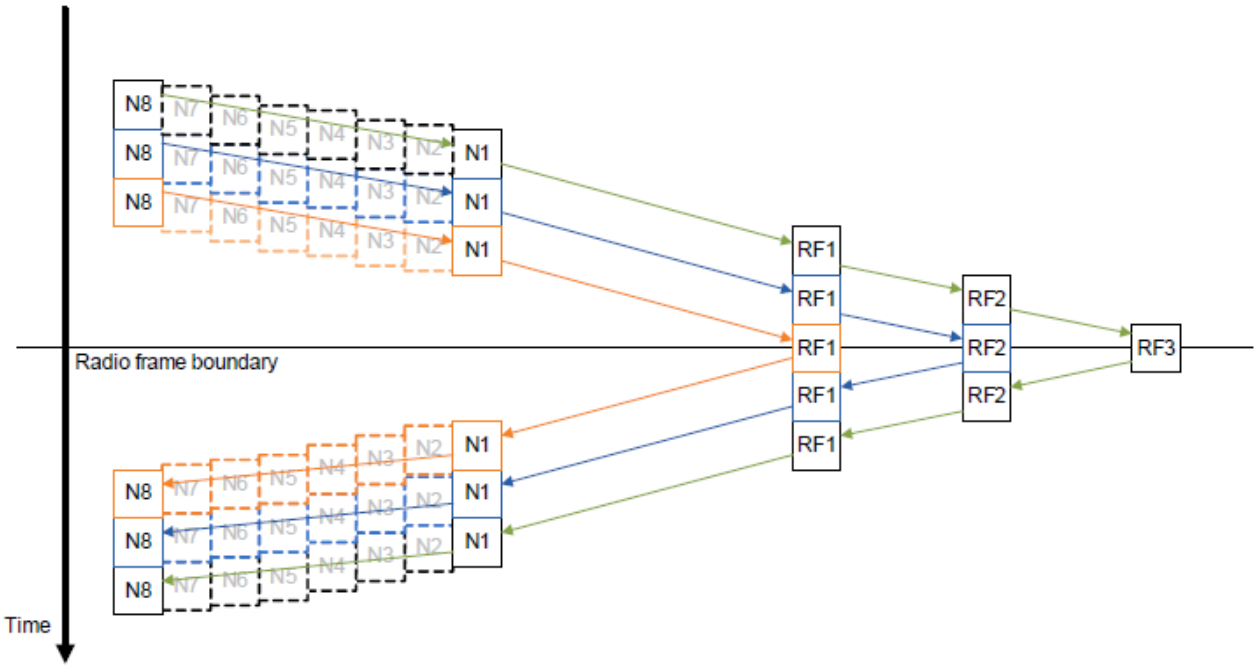
Figure 4-1 illustrates that each node in the chain has separate radio timing alignment. Node RF3 is defined with radio time equal to zero, where DL offsets are negative (red) and UL offsets are positive (blue). The offset differs at each point in the chain correlating to the propagation delay through the devices. In this example, there are three RF units in the serial chain. RF1 and RF2 both are implementing offsets because they are not defined to be equal to zero timing references.

Figure 4-1. Timing Topology, Multiple RF, Common Alignment



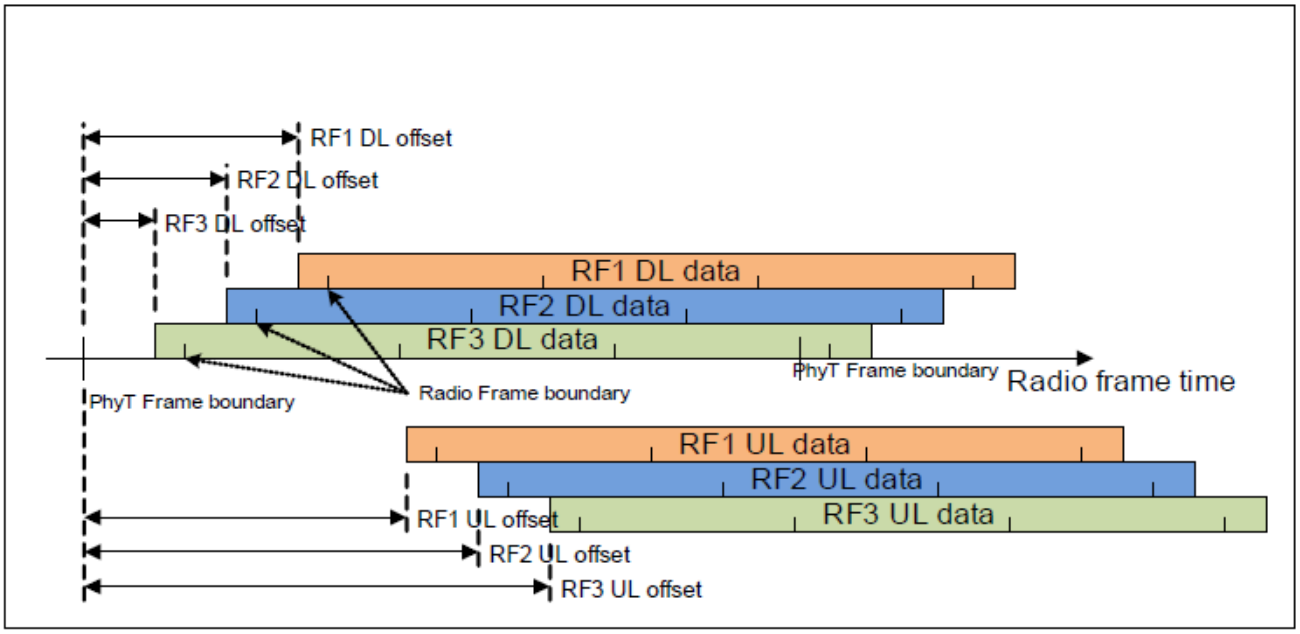
In topologies with multiple chained RF radio heads, the definition of time equal to zero can be further confused. Optionally, the furthest radio head from the baseband card can be defined with time equal to zero. In this case, the closer radio heads would delay DL data locally such that all radio heads would have synchronized transmission alignment. The radio heads would also result in synchronized reception timing, where closer RF heads would delay UL signals, compensating for any fiber delay to the furthest radio head.

Figure 4-2. Timing Topology, Multiple RF, Independent Alignment



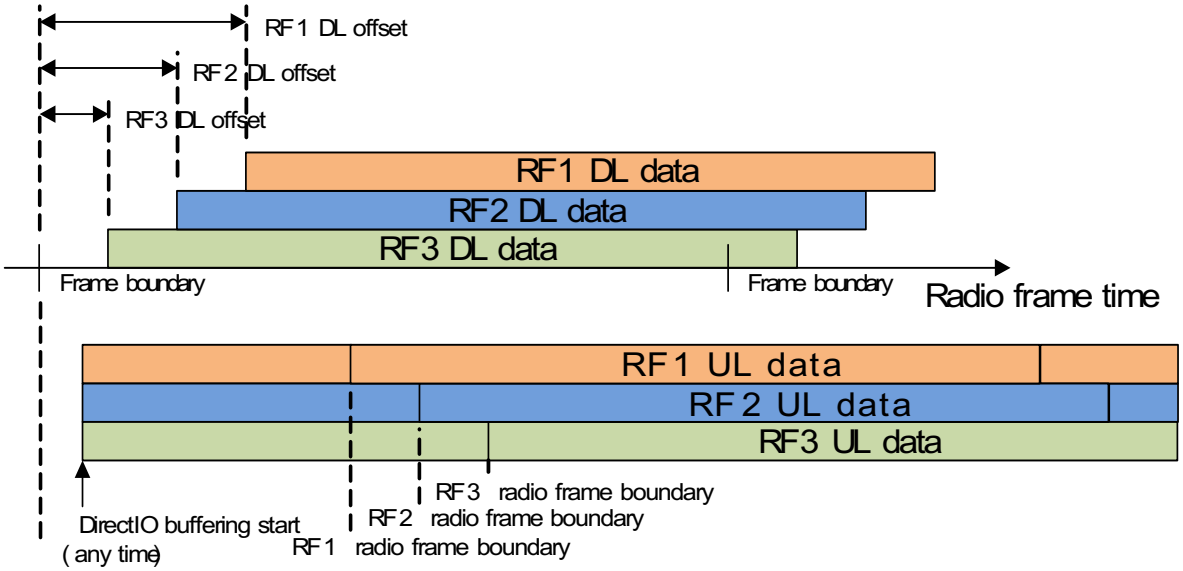
Optionally, each RF head could have its own unique concept of time equal to zero relative to itself. In this case, it is envisioned that radio head traffic is separated by an AIL link, where each link has a different reference point for timing. This is a good example to show why each AIL link supports independent timing.

Figure 4-3. OFDM/GSM/Edge2 Timing



For all radio standards other than WCDMA, DMA is aligned to radio time. For {LTE, WiMax, TD-SCDMA} DMA is started on the radio frame boundary of each AxC where each OFDM symbol is separated into a unique packet. For {GSM, Edge2}, alignment is initially made at the 60 ms boundary, but then each timeslot is separated into a unique packet.

Figure 4-4. WCDMA Timing



Neither IQN2 nor RAC have sufficient buffering to align input data to the radio frame boundary. As a result, IQN2 DIO performs a continuous DMA of WCDMA data to RAC with only alignment programmed to the granularity of 32 or 64 chips. The DMA is not aware of the radio frame boundary and can start with somewhat random alignment to radio framing.

TAC always begins transmission on radio frame boundaries. The DMA is not aware of radio framing, where DMA may start reading TAC output even before the beginning of the radio frame.

4.2 AxC Offset

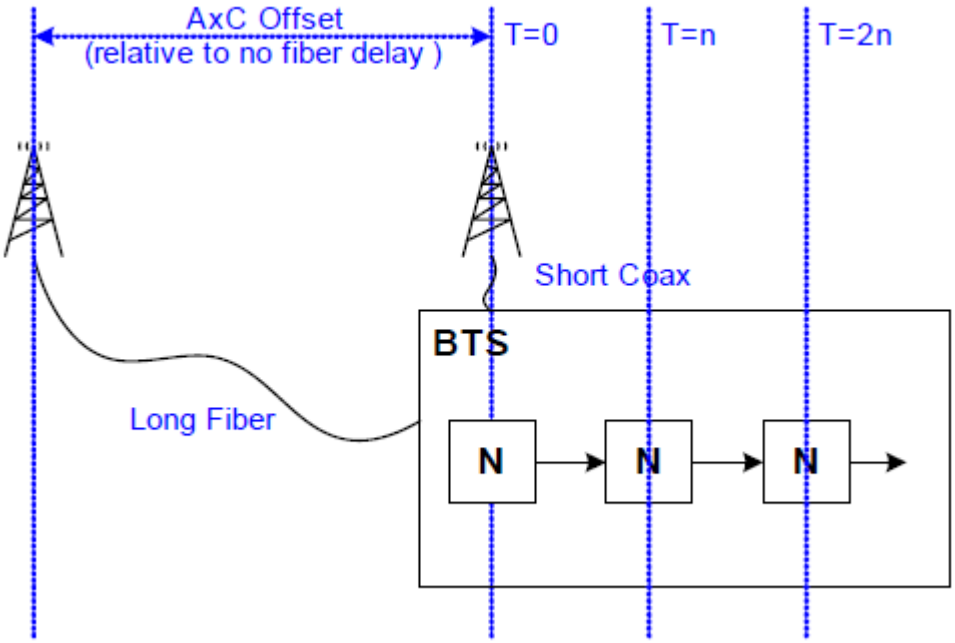
If all antennas are co-located with the base station, there is no antenna carrier offset. The coaxial or optical cable delay is treated as an extension of the air-propagation delay where the sampling at the RF card is considered to be time=0.

The first device in the daisy chain is considered to receive the antenna data with a time=0. Each subsequent “hop” in the daisy chain has a time offset relative to the delay through the previous device.

The concept of IQN2 antenna carrier offset is similar to AIF2. The minor difference is that the AxC offset is configured by multiple MMRs. For OBSAI, AxC offset MMR in PE, PD can be used to control each channel timing with sys_clk unit. For CPRI, QWD level AxC offset MMR is in PE, PD and additionally, the SI module has fine AxC offset which controls word-level offset. This fine offset is programmed to be zero for OBSAI. For legacy support of BTS with no fiber delay, the AxC offset is programmed to be zero.

For a centralized BTS that is supporting remote radio heads, there is a long fiber delay between the radio head and BTS (Figure 4-5). The time it takes for the signal to propagate through the fiber is the antenna carrier offset and is relative to a perfect connection (as if there were no delay at all).

Figure 4-5. BTS AxC Offset



The programming of AxC offset is a fixed value. For each hop of the daisy chain, the AxC offset is programmed with a different value to compensate for the time propagation through each daisy chain node.

If Ingress AxC offset is zero, PD will start processing when it detects the first AxC data within the AxC offset window boundary. If PD fails to find the first correct AxC data within the window, the PD link will not work until it meets the next radio frame boundary. On the Egress side, the minimum AxC offset cannot be zero for OBSAI, because the PE channel should be turned on after the channel data transfer is ready; so the min AxC offset will be the PE_STB offset from AIL uAT and additional fiber delay (4 sample, 8 sample, ...) is added based on that value.

The AxC offset usage is different depending on the user's protocol (OBSAI, CPRI) and radio standard (WCDMA, OFDM). For AIL OBSAI, both Egress and Ingress AxC offset unit is sys_clk and AxC offset window is used to check receiving frame boundary and if it has TS = 0 value OBSAI slot inside the window range. Ingress AxC offset is the center of the window and the user can flexibly expand the range of the window.

For AIL CPRI, the AxC offset unit is a CPRI sample for both sides. Normally, ingress AxC offset MMR in PD is programmed to be zero, because there is a radio standard level offset (BFRM, HFRM offset) which is defined by the CPRI 5.0 spec. and that offset is mainly used to control timing. Ingress AxC offset is not used for WCDMA. Instead, DIO_AXC_OFFSET (offset within circular buffer) and RAC control the external data delay. The AxC offset window concept is not used for CPRI.

For DIO/AID, the AxC offset unit is four CPRI samples (same to QW per AxC) and Ingress AxC offset is not used for WCDMA either like AIL CPRI. Fine AxC offset per channel is used for word-level offset. Normally, DIO AxC offset MMR in SI does not need to be programmed if AIL or AID controls the AxC timing.

4.3 IQN2 Internal Timing Details

4.3.1 DMA Timing

In a qualitative sense, RAC and TAC are local resources with dedicated access to DIO. L2 or shared memory are accessed by many peripherals with greater chance of contention. Users need to dedicate more slack timing for shared endpoints and less slack for dedicated endpoints.

For Egress, it is up to the user to ensure that DMA data is available prior to beginning AIL PE message construction (AIL PE_STB). Breaking real time on DMA has similar effects to breaking CorePac MIPS real time. Specifically, IQN2 will fail each affected AxC until the beginning of the next radio frame boundary.

For Ingress, it is important that DMA is efficient enough that the IQN2 internal input buffers never overflow.

For DIO (WCDMA), the Ingress DIO circular buffer size is 8 QW and can have up to a 32-chip time delay before it wraps.

The Multicore Navigator mechanism {LTE, GSM, WiMax, TD-SCDMA} manages input and output buffering more automatically, while the DIO DMA {WCDMA} is a much more manual and deterministic flow.

4.3.1.1 PKTDMA Timing

The IQN2 is a real-time system, meaning that there is a limited window of opportunity for transmission. Missing this window of opportunity is known as *Breaking Real Time*. In IQN2, it specifically is *Breaking DMA Read Time*. The penalty for breaking real time is fairly severe; the effected antennas stop transmission until the beginning of the next radio frame (in many cases 10 ms). During this time, it is likely that all calls on the effected antennas will be dropped. As such, Egress has much more interesting timing problems than Ingress.

QMSS (Queue Manager Sub-System) is the central resource for queuing free packet storage resources (memory management) and queuing packets that are ready for transport or consumption by endpoints. As a central resource, the QMSS blocks access to one resource while servicing other resources. The length of time for which QMSS blocks an access adds to the overall transport time of a packet.

Typically, engineers look at DMA bandwidth (and QMSS bandwidth) on an average basis because average bandwidth is the best understood criteria in our radio system. However, peak conditions are the usual source for breaking real time and peak conditions are difficult to characterize.

PUSH/POP: When a peripheral or CorePac wants to create a packet, it needs a memory location to start writing the data. Multicore Navigator manages memory by having a queue of free memory location (buffers) to write to. The peripheral needs to POP a location from QMSS to receive this address.

After the CorePac or peripheral creates the packet, it passes the packet to either a DMA engine or software thread for processing. The Pass operation is performed by posting a pointer to this packet on a queue. This operation is known as a PUSH and takes 12 clock cycles when 32 descriptors are used.

Table 4-1. QMSS Back-to-Back Performance

Operation	VBUS Cycles
PUSH	12
POP	45

Congestion: There are many parallel peripherals and CorePac cores that can all be performing Multicore Navigator packet operations. Congestion occurs either when there are either multiple simultaneous requestors or with a single requestor rapid firing or consuming packets. The user must handle these congestion issues in one of two ways:

- Add slack or a timing margin
- Carefully calculate and predict Multicore Navigator QMSS congestion to avoid failing cases

All modules (even a well-behaved module such as FFTC) will perform a single PUSH and POP in close proximity to each other when processing back-to-back packets.

Poorly-behaved peripherals will have peak packet flooding conditions where packets are machine gun fired into the system. There are two different conditions that can cause this type of behavior:

- Small packets: 16-byte packets are a worst-case offender, requiring a PUSH and a POP for relatively low interface or VBUS bandwidth. Both SRIO and IQN2 are built to handle small packets (or large) as small as 16 bytes.
- Many parallel channels: IQN2 is a worst-case offender for parallelism. IQN2 has up to 48 parallel channels. If these channels are all time-aligned, there is an amazing congestion of QMSS accesses.

While hardware peripherals tend to have a Multicore Navigator characteristic, software use of Multicore Navigator can be of either extreme (or more likely a mixture). 16-byte packets that are received by either SRIO or IQN2 are likely delivered to the CorePac. The CorePac software needs to access QMSS in much the same way as the hardware peripherals. Even for the otherwise well-behaved uses of CorePac (such as generating FFTC traffic) there is a danger of being organized into peak QMSS accesses. To save MIPS, a software user may like to cache Multicore Navigator descriptors in an effort to expedite packet creation.

The first-order worry of QMSS congestion is breaking IQN2 real time on the transmit side (Egress side) and a lesser worry is of overrunning the IQN2 receive buffers. Once Multicore Navigator packets have been started, the IQN2 implements a fair share scheduling algorithm to even out the traffic among channels.

4.3.1.2 DIO DMA Timing

Internal system events from uAT trigger the DIO Core (up to three engines) to transfer data. The user calculates how much time gets allocated for the DMA transfer after the internal system event triggers.

To start, the user calculates the ideal DMA transfer time (assuming no contention). In Table 4-2 and Table 4-3, look up the number of VBUS cycles and multiply by the number of VBUS bursts.

Table 4-2. Egress (Tx) DIO Core Performance

Burst Length (QW)	Bubbles (waste)	VBUS Cycles
4	1	5
2	2	4
1	3	4

Table 4-3. Ingress (Rx) DIO Core Performance

Burst Length (QW)	Bubbles (waste)	VBUS Cycles
4	2	6
2	3	5
1	4	5

Then take the ideal value and apply a derating factor. For local RAC or TAC access, +50 percent derating factor is suggested. For L2 or MSMC, +200 percent is recommended. DDR access is so heavily dependent on loading that a simple rule of thumb is not supplied.

Example: Assuming a 1 GHz CPU clock, the resulting VBUS clock is 3.3ns, yielding 157 vbus_clk allocated for the transfer.

- 32 UL AxC (8x), 8 chip iteration, two QW per AxC, 4-burst, RAC destination
  - 16 bursts of 4 = 16 x 6 = 96 VBUS clock
  - Derate by 50% = 144 vbus_clk
  - 475.2 ns + 518.1 ns (157 vbus_clk) = 306 sys_clk (307.2 MHz)
- 32 DL AxC (8x), 4 chip iteration, 1 QW per AxC, 4-Burst, TAC source
  - 8 bursts of 4 = 8 x 5 = 40 VBUS clock
  - Derate by 50% = 60 vbus_clk
  - 198 ns + 518.1 ns = 221 sys_clk (307.2MHz)

4.3.2 IQN2 Internal Delay

4.3.2.1 DIO or PktDMA => IQS =>AIL PE_STB Timing

This egress path is processed based on a request from the scheduler, and there is no intermediate buffer that causes a large amount of delay, so user does not need to care too much about delay. Sufficient amount of DMA delay (PktDMA or DIO) will cover all internal minor delays within sub-modules.

4.3.2.2 PE_STB =>RT_STB=>TM_STB (Delta) Timing

The minimum distance between the PE_STB and TM_STB (Delta) is 60 clock cycles for CPRI and 100 clock cycles for OBSAI. The minimum spacing between these system events represents the time it takes for PE to create link data prior to the TM beginning transmission. The PE_STB is the starting point for link construction.

The RT_STB is the starting point for link retransmission, insertion, or aggregation of RT. The minimum distance between PE_STB and RT_STB is 10 sys_clk and the minimum distance between RT_STB and TM_STB is 20 sys_clk. RT_STB moves between those two boundaries to better sync with incoming data from RM.

4.3.2.3 TM(Delta) and PE Event Offset Calculation

Delta and PE event offset is measured by sys_clk (307.2MHz for OBSAI and 245.76MHz for CPRI). There are several time delay factors in the egress side. They are Multicore Navigator data transfer delay, DIO DMA delay, and Egress IQN2 internal delay.

Delta (DL case) = DMA time (Multicore Navigator or DIO) + PE_STB =>TM_STB timing

- There is approximately one chip (260 ns) of minimum latency between reception and retransmission of a link.
- The distance between TM (Delta) and RT is approximately 15 sys_clk.
- Pi time could be the same to RT_STB event time in case of aggregation or retransmission.
- The distance between PE_STB and TM_STB (Delta) is 60 sys_clk or more for CPRI and 100 sys_clk or more for OBSAI

4.3.2.4 RM => RT timing (Retransmission or Aggregation)

The propagation delay from RM to RT is around 15 clock cycles. This is the time from Pi arrival as measured at the uAT until data is available to aggregate with PE.

RT_STB is the latest moment that RT will wait for PE and CI SOF contribution before

progressing without either input. Set RT_STB equal to Pi_{Max} + 15 where Pi_{Max} represents the latest time at which the frame boundary is expected.

4.3.2.5 AIL RM =>IQS =>PktDMA or DIO (UL Case)

The largest component of ingress timing has to do with packing the PHY standard {OBSAI, CPRI} and DIO SI buffer 4-sample data control and RSA data format control. In CPRI (non-RSA), a full quad word is accumulated before writing to PktDMA or DIO SI, because AxCs are interleaved on a word-by-word basis. With OBSAI, the AxCs are interleaved qwd-by-qwd — again, within four samples of time.

With RSA data format, AIL PD will wait until two quad words of data for a given AxC are received before writing to DIO, then PD will write out both quad words sequentially.

In practice, setting 400 clocks for all these kinds of internal delay and fuzzy factors avoids complex calculation. Therefore, the total Min Ingress Delay before starting First Ingress DIO SI 4-sample event will be **Pi + 400 clock time margin for AIL internal processing and data transfer to DIO SI buffer.** The delay for final DIO core DMA start depends on the burst size per AxC (4-sample, 8-sample, 16-sample). DMA delay for 4-sample can be simply approximated as 240 clocks for CPRI and 300 clocks for OBSAI and it can be doubled for 8-sample and 16-sample cases.

NOTE: In DIO mode of operation, DMA is triggered by precise timed internal system events and therefore has to be correctly timing characterized. In Multicore Navigator modes of operation, the DMA is triggered by data arrival making these timing calculations mostly unnecessary.

4.3.2.6 AID => DFE & DFE => AID timing

Only the AID requires per-radio standard frame timing strobe derived from the uAT for ICC Transmit and receive timing.

On egress, the AID scheduler wakes up for each 4 sample iteration strobe from uAT for each radio standard variant and starts a read of TDM LUT for all assigned channels. this 4-sample event with frame boundary strobe can be started after a certain amount of DMA time from PktDMA or DIO (this delay might be similar to the AIL case). The DFE module should be activated and wait for frame strobe from AID before starting data transmission.

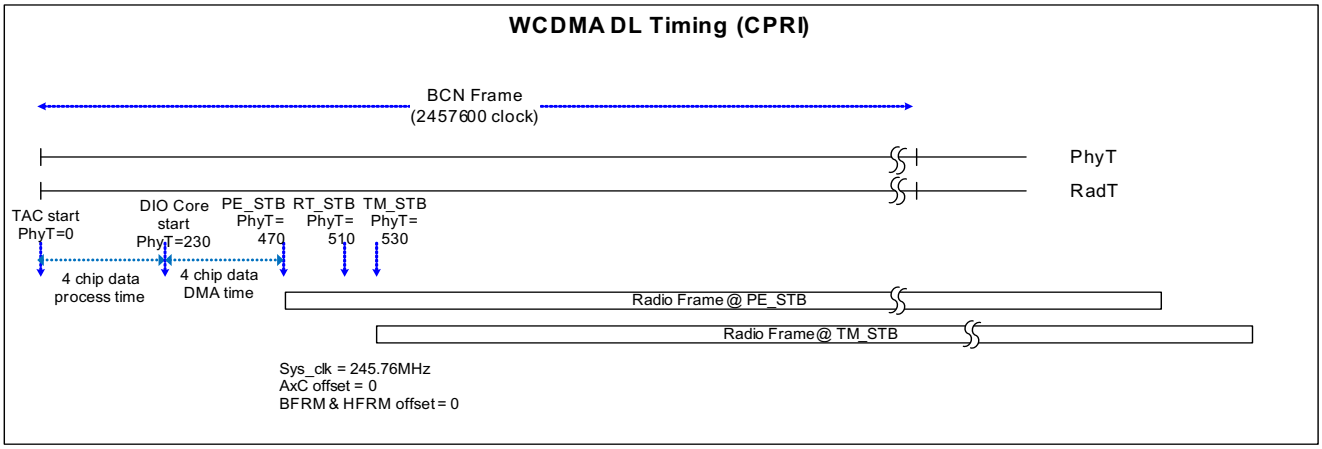
On Ingress, The AID is a timing slave of the ICC (DFE) it is attached to. Operations are paced as data is made available to the IFE of AID. The frame start signal from the DFE is the only synchronization mechanism required. The user application should know the exact frame start delay from DFE and the delay must be matched with AID IFE 4-sample strobe start timing. In case of WCDMA, DIO SI event and DIO Core event timing must be paced with this strobe with a certain amount of delay. The delay for DIO events are the same to the AIL/DIO case. (See Section 4.3.2.5 for details.)

4.3.3 WCDMA Timing Example

4.3.3.1 WCDMA DL CPRI

The first example is a WCDMA using DIO for Egress TAC emulation (Section 4.3.3.2). The TAC process starts at PhyT=0 and RadT =0 and at PhyT = 230, Egress DIO DMA starts, where approximately four chips of time are given to allow the DMA to complete (which is an excessively large amount of time for the transfer to complete).

Figure 4-6. WCDMA DL Egress Timing (CPRI)



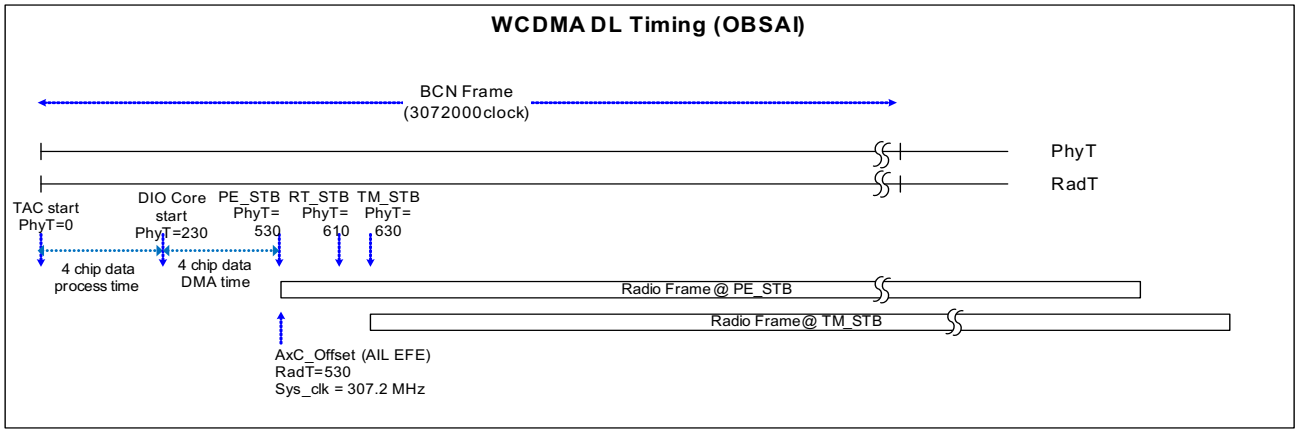
At PhyT=470, the AxCs are activated. The AxC_Offset is chosen using the exact method, a value of 470 which is the same to PE_STB. The exact method is chosen for simulation purposes such that the AxC starts up exactly when the link turns on. Using the approximate method is recommended for field use where it is not critical to start real traffic in the first frame of boot.

The RT_STB event in this example proved non-critical as there is no aggregation in this example. The distance between PE_STB and TM_STB (Delta) has been chosen as the minimum (60). It is recommended to use the Min values always (no reason to vary this timing).

4.3.3.2 WCDMA DL OBSAI

In case of OBSAI (Figure 4-7), the main difference is using the sys_clk rate of 307.2 MHz. One WCDMA chip length is 80 clocks instead of 64 clocks (CPRI) and requires 300 clock cycles for a 4 sample DMA to complete. This makes the AxCs activated at PhyT = 530. The distance between PE_STB and TM_STB (Delta) has been chosen as the minimum (100).

Figure 4-7. WCDMA DL Egress Timing (OBSAI)



4.3.3.3 WCDMA UL (Ingress)

This example is a WCDMA using DIO for Ingress RAC emulation. The Pi_Min is set to zero and the Pi_Max is set to 20, providing some slack in reception timing.

With reception, (after PiMax) an overall ingress timing margin of 400 clocks is added before starting the DIO SI 4 sample strobe. This 400 clock margin includes all AIL pipe and processing delay + IQS switching delay + DIO SI buffer delay. Finally, an additional 480-clock delay is added before starting the DIO Core 8-chip strobe for UL data. This delay between DIO SI strobe and DIO core DMA strobe will be doubled if 16-sample burst per AxC is chosen for delayed stream.

RAC strobe can be started after 32-chip time since the Ingress DIO DMA 8-chip event is activated. IQN2 does not have UL and DL Radio timer like AIF2. Instead, the AT supports a max. of 8 radio timers. Some of the timers are used to support real radio standards and the remaining ones might be used as UL or DL timing creation for certain radio standards. For CPRI, Ingress AxC offset is not used and all external antenna delay will be controlled by RAC.

Figure 4-8. WCDMA UL Ingress Timing (CPRI)

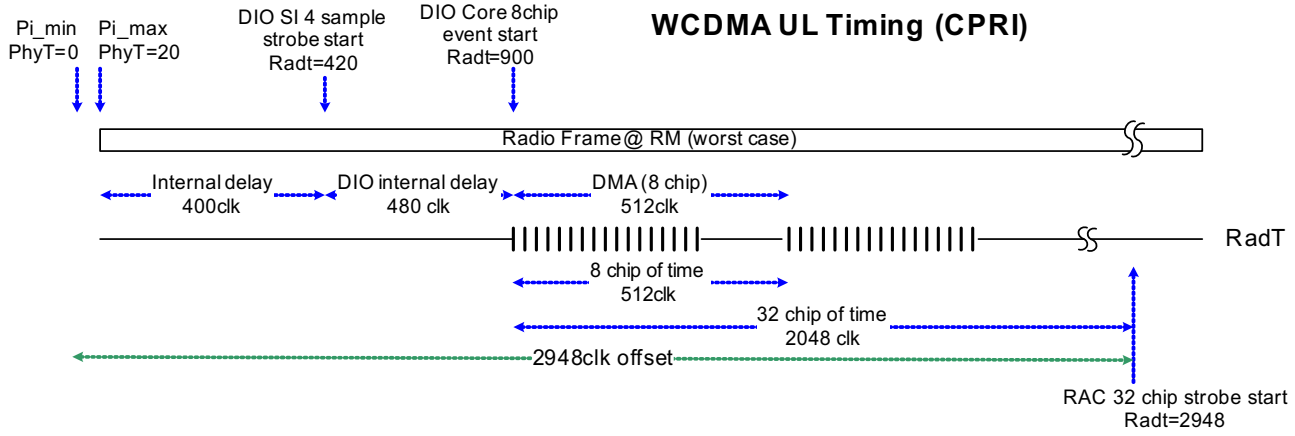
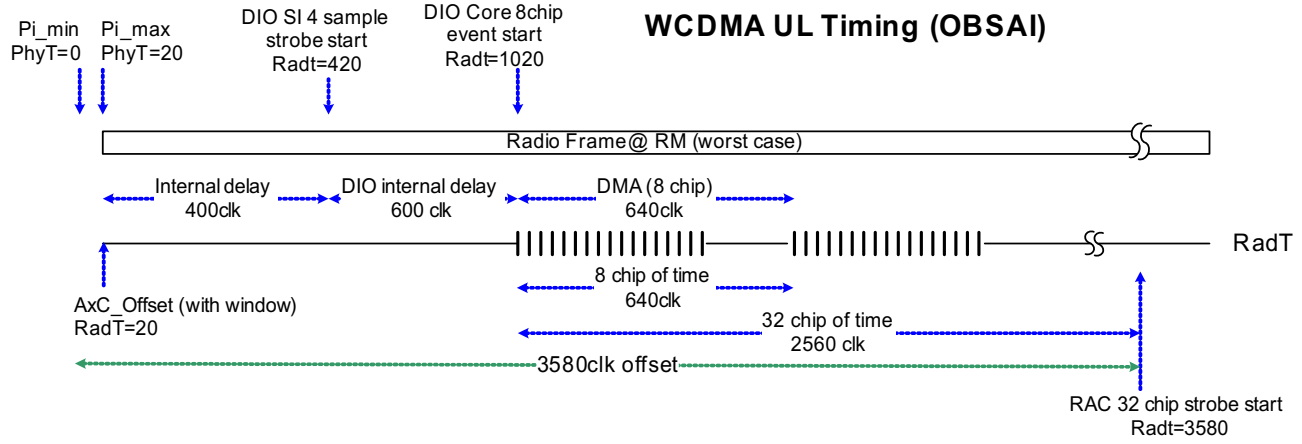


Figure 4-9. WCDMA UL Ingress Timing (OBSAI)



4.3.4 LTE Timing Example

The LTE example is simpler than the WCDMA case because Multicore Navigator controls data transfer automatically. The IQN2 PKTDMA packet pop operation starts before PhyT=0 and RadT =0 and at PhyT = 0 both the link and the AxC are activated by PE_STB. The AxC_Offset is chosen as a value of 0 (same to PE_STB). The TM_STB value was set to 100 to cover both OBSAI (100 clock) and CPRI (60 clock) case.

Figure 4-11 shows the re-transmission insertion timing. If captured Pi on ingress link is 360, a CI and RT pipe delay of 15 clocks is added for egress RT_STB on egress to make a perfect daisy chain. PE_STB and TM_STB are calculated based on RT_STB.

Figure 4-10. LTE Egress Timing

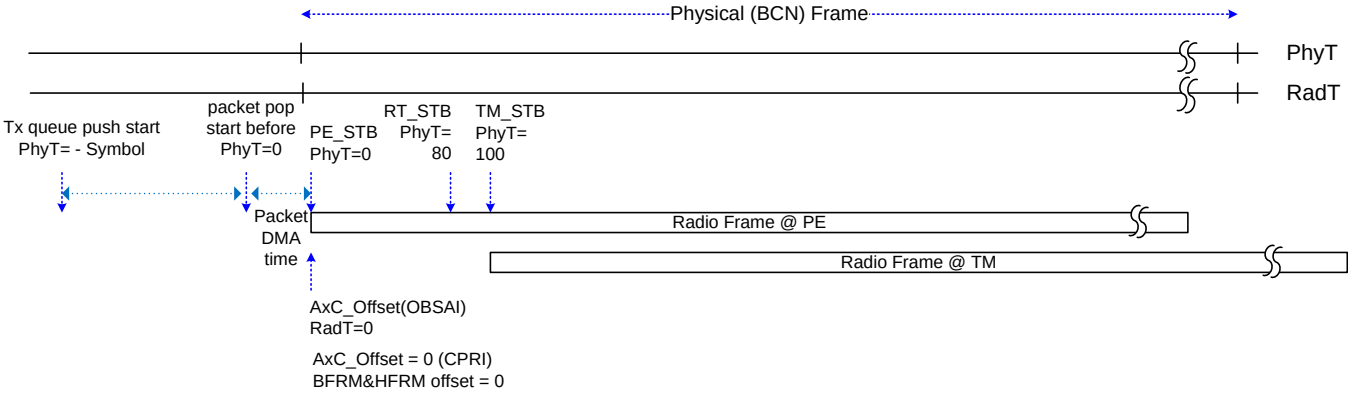
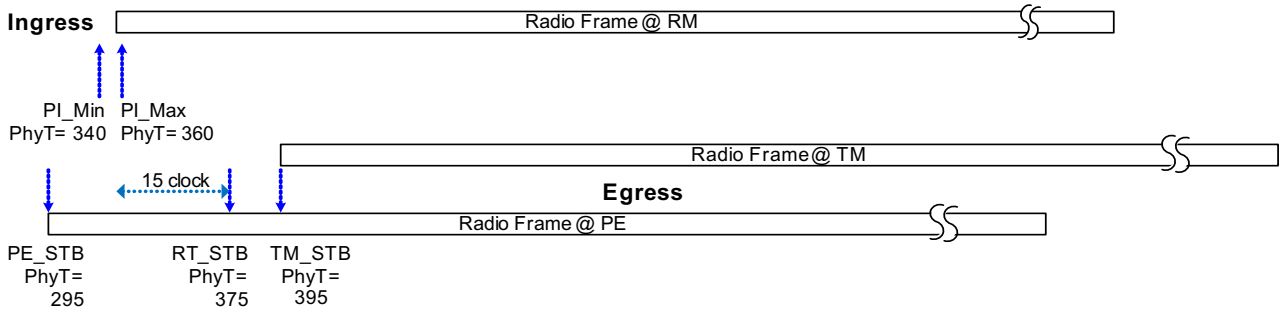


Figure 4-11. Retransmission, Insertion Timing



Interface Standards CPRI, OBSAI Specifics

Topic **Page**

5.1 CPRI Specifics

Table 5-1. CPRI Link Rates

Link Rate	Gbps	sys_clk	Bytes per CW	30-bit AxC Containers per Basic Frame (Max)	32-bit AxC Containers per Basic Frame (Max)
2x	1.2288	245.7MHz	2	8	7
4x	2.4576	245.7MHz	4	16	15
5x	3.0720	307.2MHz	5	20	18
8x	4.9152	245.7MHz	8	32	30
10x	6.144	307.2MHz	10	40	37
16x	9.8304	245.7MHz	16	64	60

5.1.1 AIL CPRI Support Overview

The AIL module supports a large majority of the CPRI v5.0 protocol over a single transmit and a single receive serial link. The AIL supports the 2x, 4x, 5x, 8x, 10x, and 16x line bit rates. It should be noted that the 1x bit rate is not supported by the AIL. The line bit rate of the AIL transmit and receive path is set through a Memory Mapped Register (MMR).

There are some limitations on the mix of link rates that can be supported with CPRI links using the same SerDes macro. The 2x and 16x CPRI link rates cannot be supported by the same SerDes macro. Also, the 5x and 10x CPRI link rates cannot be mixed with any other CPRI link rate within a SerDes macro. The banking of AIL links is an SoC-level architectural decision.

At bit line rates of 8x and higher, the AIL supports scrambling which is applied to the data stream before 8b/10b encoding as described in Section 6.5 of the CPRI v5.0 specification. The scrambling seed is provided to the AIL transmit link via an MMR, while the AIL receive link will recover the scrambling seed using at least the first 32 bits of control bytes #Z.0.2 to #Z.0.(T/8-1). The AIL supports the use of zero as a scrambling seed, which essentially disables scrambling while allowing the protocol version in the L1 in-band control sub-channel to be set to 2.

The AIL module offers three synchronization mechanisms to the user. All of these mechanisms will provide a reference point for the CPRI 10 ms frame. The user can choose to provide a pulse to a pin, utilize the IEEE 1588 protocol to provide a timing base, or the user can perform a software write to an MMR inside of the IQN2 subsystem. The accuracy of these synchronization methods should be understood by the user when determining which method is best suited for the application. In all three sync mechanisms, once AT BCN timer is started the timer can effectively be measured and adjusted.

Multicore Navigator transmission timing is set via the “delta.” CPRI reception of the PHY SOF (Start of Frame) is measured via the “pi” MMR. Both of these are BCN timer values. Higher-layer SW can use the transmission and reception timing of all nodes in the system to calculate RTT timing. Once RTT timing is known, the network can be reconfigured to compensate for long fiber transmission delays.

5.1.2 CPRI IQ Data Handling

The AIL module supports up to 64 AxCs (Antenna Carriers) to be transmitted per link and up to 64 AxCs to be received per link. The actual number of AxCs that the link can support may be reduced due to the line rate and the type of AxC (i.e., only 1 LTE20 AxC can be transmitted/received on a 2x link).

The AIL requires that these AxCs be mapped into a maximum of 8 groups. Each group will define important characteristics of the AxCs (many users will choose to simply have one group per link). These characteristics are the number of bits per container, the number of containers, and the offset in bits from the previous group. CPRI defines the container size to be either 30-bit or 32-bit. In some 30-bit container usages some bits are unused. The AIL supports 7, 8, 15, or 16-bit samples (i.e., 15-bit I + 15-bit Q).

The AIL will always send either 16 or 8-bit data to the DMA layer, so sign extension is performed on all 15 and 7-bit samples. The offset in bits from the previous group allows the user to space the groups in the IQ data block portion of the CPRI basic frame however they would like. Within these groups the containers are packed as densely as possible, without any reserved bits between containers.

The AIL supports mapping method 3 as described in Section 4.2.7.2.7 of the CPRI v5.0 specification. This means that the concept of stuffing samples is supported and the location of these stuffing samples is determined by the formulas described by mapping method 3. The use of stuffing samples is effectively the concept of rate matching. Since, the pattern of stuffing samples can be influenced by the grouping of AxC, it is important that care is taken to program these groups accordingly. Also, since there are only 8 groups available to the user, it may be necessary to program these groups with a number of AxC that is greater than zero.

Each of these 8 groups would correspond to a radio standard or radio standard variant. As an example, one group could be created for LTE20MHz traffic, while another group is created for LTE5MHz traffic, and a third group created for WCDMA traffic. CPRI requires all AxC within the same group to have the same stuffing sample pattern, for this reason it is cleaner to group radio standard variants separately from one another.

If AxC offsets are to be used, these are to be programmed on an AxC-by-AxC basis. The AxC offset feature allows for the start of each AxC to be delayed by an integer number of samples relative to the group offset. The group offset is programmed in basic frames and is relative to the CPRI PHY SOF. When an AxC is programmed to use the AxC offset feature, the AxC will initially turn on later than those without an AxC offset. While an AxC is OFF, zeros are transmitted. On reception, traffic for AxCs which are OFF is discarded.

A Group turns On/Off relative to its group offset. Initially, all AxCs are OFF when a group is OFF. Once the group is ON, AxC may turn ON/OFF based on the programming of those channels. SW enables AxCs, and once the radio SOF is reached for that channel it will turn ON. Once SW disables an AxC, it will turn OFF once the next radio symbol/slot boundary is reached. It is the responsibility of the user to only disable a group once all AxCs are OFF. Likewise, it is the responsibility of the user to turn OFF the PHY only after all groups are OFF.

The AIL module supports TDD radio standards by allowing symbols/slots to be marked as TDD off. When a symbol/slot is marked as TDD off, all samples will be filled with zeros when transmitted, and all samples received will be dropped. The AIL module expects that DMA data is provided only for TDD ON symbols/slots.

In all cases, AIL checks that DMA data matches the expected radio traffic. AIL checks the symbol/slot length of DMA data as well as the symbol/slot index provided in the PacketDMA packet headers. In cases where DMA does not match the FSMs running in AIL TX, the AIL considers the DMA data to be “bad.” AIL Drops all DMA packets until DMA SOF is encountered and AIL will then re-synchronize the use of DMA data with PHY usage on the next radio SOF calculated by AIL FSMs.

5.1.2.1 TX Radio Timing

In CPRI, the radio timing of AxC traffic is always relative to the PHY SOF. CPRI is a little vague on the concept of offsets. It comes up in two places in the standard. For GSM, they clearly call out a need for the radio standard to be time offset from the PHY SOF. The other place where offsets come up is the RE UL Chaining. While the standard does not call out the need for radio standard offset, the result of RE UL Chaining clearly requires it. In order to generalize the CPRI concepts, AIL supports a separate offset for each of eight supported groups.

From looking at the way CPRI segments the basic frames into groups and the way the bubble insertion mechanism works, it is clear that group offset must always be whole basic frames. (The stuffing sample mechanism starts on “container blocks” and a container block can span PHY frame boundaries).

The AIL implementation supports two different forms of radio standard timing offset:

- Radio Standard Offset: AIL supports up to eight groups within the single link. It is intended that AxCs with similar timing requirements (radio standard) are grouped together. Each group is supported with an offset, programmed in units of basic frames and even hyper-frames, relative to the PHY SOF. The Ingress path and Egress paths are supported with independent offset values giving the user flexibility to support normal vs. RE UL chaining -or- completely independent Ingress/Egress operation.
- AxC Offset: This concept is strong in OBSAI, but not specified at all in CPRI. Each AxC may have an independent offset (delay) relative to the group (radio standard) offset. The AxC offset is programmed in units of samples (unlike group offset which is programmed in basic frames). Most CPRI users will program the AxC_Offset to zero, which means disabling the feature.

The IQN2 Antenna Timer (AT) tends to be the centralized timing source for the entire SoC. The AT has system events which are used to control RAC, TAC, and APP SW. These system events are generated from eight different radio timers in the AT. The AIL CPRI implementation does not use the AT radio timers directly, rather it only uses the BCN timer (which effectively is a PHY timer). The user must be aware of the timing relationship between PHY time and radio time, and the ability to convert between them.

In particular, the RAC and TAC are paced by the radio timers in AT. A DMA is constantly performing the export of the AT timer values to RAC and TAC in order for those IP modules to control where they are in their WCDMA frame timing. The CPRI links only use the BCN timer value, so the user must know the programmed relationship between these different timers.

The radio timing at the CPRI interface is extremely tight and precise. The radio timing concept at the APP SW is rather loose, but still aligned to radio time. One of the primary functions of IQN2 AIL is to tighten, or re-align the DMA data from the APP SW to the CPRI PHY.

5.1.2.2 CPRI IQ, link construction

CPRI uses a mechanism of precise placement within the CPRI PHY. CPRI hard partitions the link into control vs. AxC bandwidth. For each CPRI basic frame, the first 1/16th of each basic frame are CW while the remaining 15/16 of each basic frame is BW for IQ or AxC traffic. The placement of AxC samples within this region is essentially done by a series of FSMs. Both the transmitter and receiver must have exactly identical placement and extraction strategies. The placement must be exact on both ends. (This operation is complex.)

Placement of AxC traffic is complicated by different radio sample rates and even a few different sample widths. A single CPRI link contains many AxC and may contain several radio standards.

CPRI AxC placement strategy is a layered approach:

- Radio Standard (Group) Offset
  - The 2nd and 3rd “layer” (Rate Matching & AxC TDM) operations are aligned to the radio standard frame boundary (relative to a PHY frame boundary)
  - (i.e.,) the 60ms GSM radio frame (13 GSM frame boundary)
    - APP SW chooses the appropriate (one of six) PHY frame boundary
    - APP SW chooses the number of Basic Frame offsets relative to the chosen PHY frame boundary
    - IQN2 AIL starts the operation precisely at this programmed point.
- Layer 1: Grouping of AxC of similar characteristics
  - A sensible thing to do is to group AxC of same radio standard
  - AxC samples within a group must have the same number of bits per sample
    - 32-bit container: (16-bit I + 16-bit Q) -OR- 2x (8-bit I + 8-bit Q)
    - 30-bit container: (15-bit I + 15-bit Q) -OR- 2x (7-bit I + 7-bit Q)
      - CPRI pre-defines reserved bit location if not all 30 bits are utilized
  - AxC samples within a group must have same rate matching (stuffing sample)
  - Gaps are permitted between Groups, but no gaps are permitted between containers within a Group.
    - Gaps sizes are a programmable even number of bits
- Layer 2: Rate Matching (Stuffing Samples)
  - Rate matching is performed independently on each Group
  - Bubble insertion formulas are precisely defined in the CPRI standard
  - These Bubbles or “stuffing samples” are wasted CPRI containers (samples)
  - Without Rate Matching, some radio standards (i.e., GSM) cannot exactly fit in the CPRI PHY
- Layer 3: AxC TDM
  - Within the Group, after the Rate Matching, the resulting stream of containers simply represent a TDM of AxC.
    - (i.e.,) if 3 AxCs fit into the Group, a pattern of 0, 1, 2, 0, 1, ... simply repeats over and over again

- The TDM pattern must wrap on every radio frame (else the user has created an illegal pattern)

5.1.2.3 Group Programming

When programming the eight groups, the user is encouraged to maximize the group size. This means that the user should call out the largest number of containers to be used for the radio standard variant. The user will then be able to enable each container in the group. The enabled containers per group will be used as the N_C variable in the mapping method 3 equations from the CPRI v5.0 specification.

The other necessary variables such as number of AxCs per group (N_A), the number of samples per block (S), the number of basic frames over which a block is transmitted/received (K), and the number of stuffing samples per block (N_V) are to be programmed by the user per group. These values will be used to properly insert stuffing samples where needed. The sequence of AxC numbers must be provided by the user, allowing the IQ samples in a group to be flexibly ordered.

Each group must start on an even-numbered bit, and the groups cannot overlap.

The parameters controlling the eight groups can be changed during operation of the AIL. The changes will only take effect on 10 ms CPRI frame boundaries. This effectively allows a user to add/delete a group with the caveat that all effected AxCs in that group must be in the OFF state. Modifying a group with active AxCs will likely corrupt current traffic and may not be recoverable.

5.1.2.4 Group & Stuffing Sample Example

Figure 5-1 shows an example where three groups are identified within a 8x CPRI link. The first group contains a single LTE20 AxC, the second group contains two LTE5 AxCs, and the third group contains four WCDMA AxCs. In this example, all of the groups have been defined with 30-bit container sizes, and the radio standards do not require stuffing samples to be inserted into the IQ data stream. It should be noted that to optimally program this grouping into the AIL, the user should program the first group to consume 16 containers, the second group to consume 12 containers, and the third group to consume four containers. The first group would only have the first eight containers enabled, the second group with four containers enabled, and the third group with all four containers enabled. Each disabled container will be filled with reserved bits, which are zero. This mapping of more containers than are currently being used allows for AxCs to be added/removed without changes to the grouping configuration.

Figure 5-1. Multiple Radio Standard Group Mapping

B \ W	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Control Byte (BZ.X.0)	I-0	I-2	I-4	I-6					I-1	I-3					I-13
1		Q-0	Q-2	Q-4	Q-6					Q-1	Q-3					Q-13
2		I-1	I-3	I-5	I-7					I-2	I-4					I-MSB
3		Q-1	Q-3	Q-5	Q-7					Q-2	Q-4					Q-MSB
4		I-2	I-4	I-6	I-8					I-3	I-5					I-0
5		Q-2	Q-4	Q-6	Q-8					Q-3	Q-5					Q-0
6		I-3	I-5	I-7	I-9					I-4	I-6					I-1
7		Q-3	Q-5	Q-7	Q-9					Q-4	Q-6					Q-1
8	Control Byte (BZ.X.1)	I-4	I-6	I-8	I-10					I-5	I-7				I-0	I-2
9		Q-4	Q-6	Q-8	Q-10					Q-5	Q-7				Q-0	Q-2
10		I-5	I-7	I-9	I-11					I-6	I-8				I-1	I-3
11		Q-5	Q-7	Q-9	Q-11					Q-6	Q-8				Q-1	Q-3
12		I-6	I-8	I-10	I-12					I-7	I-9				I-2	I-4
13		Q-6	Q-8	Q-10	Q-12					Q-7	Q-9				Q-2	Q-4
14		I-7	I-9	I-11	I-13					I-8	I-10				I-3	I-5
15		Q-7	Q-9	Q-11	Q-13					Q-8	Q-10				Q-3	Q-5
16	Control Byte (BZ.X.2)	I-8	I-10	I-12	I-MSB					I-9	I-11				I-4	I-6
17		Q-8	Q-10	Q-12	Q-MSB					Q-9	Q-11				Q-4	Q-6
18		I-9	I-11	I-13	I-0					I-10	I-12				I-5	I-7
19		Q-9	Q-11	Q-13	Q-0					Q-10	Q-12				Q-5	Q-7
20		I-10	I-12	I-MSB	I-1					I-11	I-13				I-6	I-8
21		Q-10	Q-12	Q-MSB	Q-1					Q-11	Q-13				Q-6	Q-8
22		I-11	I-13	I-0	I-2					I-12	I-MSB				I-7	I-9
23		Q-11	Q-13	Q-0	Q-2					Q-12	Q-MSB				Q-7	Q-9
24	Control Byte (BZ.X.3)	I-12	I-MSB	I-1	I-3					I-13					I-8	I-10
25		Q-12	Q-MSB	Q-1	Q-3					Q-13					Q-8	Q-10
26		I-13	I-0	I-2	I-4					I-MSB					I-9	I-11
27		Q-13	Q-0	Q-2	Q-4					Q-MSB					Q-9	Q-11
28		I-MSB	I-1	I-3	I-5					I-0					I-10	I-12
29		Q-MSB	Q-1	Q-3	Q-5					Q-0					Q-10	Q-12
30		I-0	I-2	I-4	I-6					I-1					I-11	I-13
31		Q-0	Q-2	Q-4	Q-6					Q-1					Q-11	Q-13
32	Control Byte (BZ.X.4)	I-1	I-3	I-5	I-7				I-0	I-2					I-12	I-MSB
33		Q-1	Q-3	Q-5	Q-7				Q-0	Q-2					Q-12	Q-MSB
34		I-2	I-4	I-6	I-8				I-1	I-3					I-13	I-0
35		Q-2	Q-4	Q-6	Q-8				Q-1	Q-3					Q-13	Q-0
36		I-3	I-5	I-7	I-9				I-2	I-4					I-MSB	I-1
37		Q-3	Q-5	Q-7	Q-9				Q-2	Q-4					Q-MSB	Q-1
38		I-4	I-6	I-8	I-10				I-3	I-5					I-0	I-2
39		Q-4	Q-6	Q-8	Q-10				Q-3	Q-5					Q-0	Q-2
40	Control Byte (BZ.X.5)	I-5	I-7	I-9	I-11				I-4	I-6					I-1	I-3
41		Q-5	Q-7	Q-9	Q-11				Q-4	Q-6					Q-1	Q-3
42		I-6	I-8	I-10	I-12				I-5	I-7					I-2	I-4
43		Q-6	Q-8	Q-10	Q-12				Q-5	Q-7					Q-2	Q-4
44		I-7	I-9	I-11	I-13				I-6	I-8					I-3	I-5
45		Q-7	Q-9	Q-11	Q-13				Q-6	Q-8					Q-3	Q-5
46		I-8	I-10	I-12	I-MSB				I-7	I-9					I-4	I-6
47		Q-8	Q-10	Q-12	Q-MSB				Q-7	Q-9					Q-4	Q-6
48	Control Byte (BZ.X.6)	I-9	I-11	I-13					I-8	I-10					I-5	I-7
49		Q-9	Q-11	Q-13					Q-8	Q-10					Q-5	Q-7
50		I-10	I-12	I-MSB					I-9	I-11					I-6	I-8
51		Q-10	Q-12	Q-MSB					Q-9	Q-11					Q-6	Q-8
52		I-11	I-13	I-0					I-10	I-12					I-7	I-9
53		Q-11	Q-13	Q-0					Q-10	Q-12					Q-7	Q-9
54		I-12	I-MSB	I-1					I-11	I-13					I-8	I-10
55		Q-12	Q-MSB	Q-1					Q-11	Q-13					Q-8	Q-10
56	Control Byte (BZ.X.7)	I-13	I-0	I-2					I-12	I-MSB					I-9	I-11
57		Q-13	Q-0	Q-2					Q-12	Q-MSB					Q-9	Q-11
58		I-MSB	I-1	I-3					I-13	I-0					I-10	I-12
59		Q-MSB	Q-1	Q-3					Q-13	Q-0					Q-10	Q-12
60		I-0	I-2	I-4					I-MSB	I-1					I-11	I-13
61		Q-0	Q-2	Q-4					Q-MSB	Q-1					Q-11	Q-13
62		I-1	I-3	I-5					I-0	I-2					I-12	I-MSB
63		Q-1	Q-3	Q-5					Q-0	Q-2					Q-12	Q-MSB

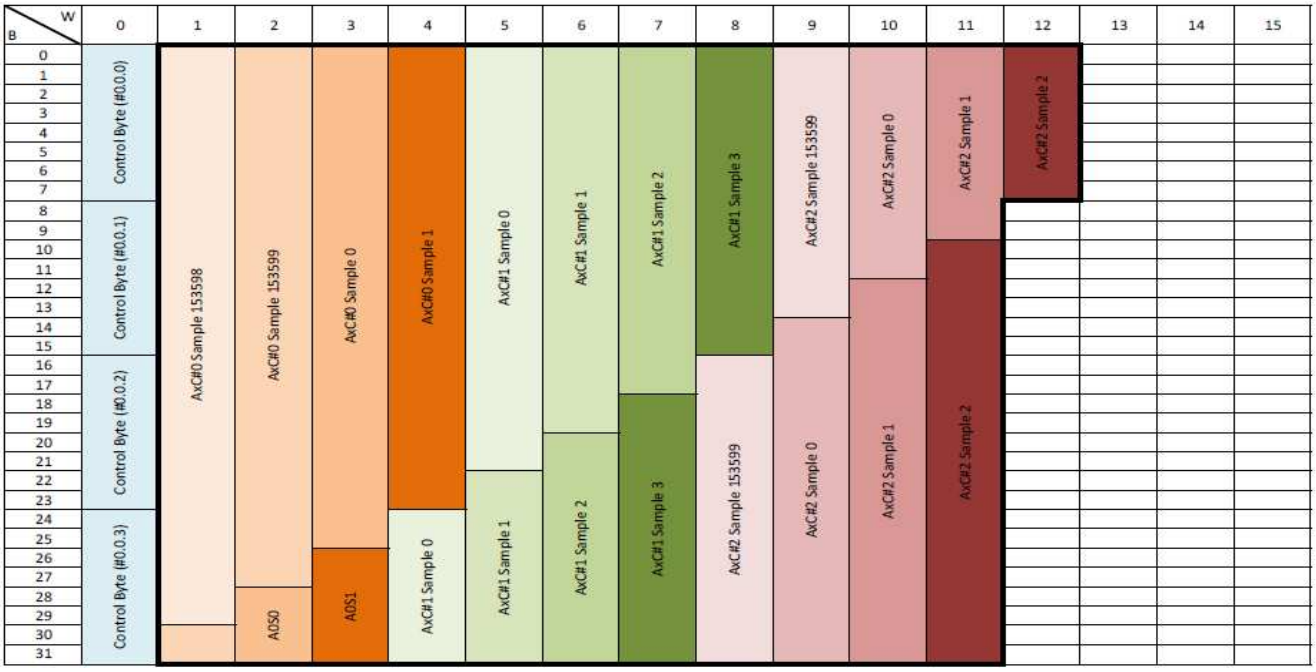
Figure 5-2 shows an example where groups with different container sizes are mapped onto a 4x CPRI link. Each AxC in this example is mapped to a different group. They are packed as closely as possible for illustrative purposes, since it would be better to configure the group mapping for the easy addition of AxCs to groups without having to touch the mapping configuration. It should be noted that the container size is always either 30 or 32 bits, and that sample size selection of seven or eight bits will indicate a container size of 30 bits and 32 bits respectively. Also, the user should be aware that the use of 32-bit containers will lower the number of AxCs that can be supported per AIL.

Figure 5-2. Sample Size Options in Group Mapping

B \ W	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Control Byte (#Z.X.0)	I-0	I-1	I-1	I-2											
1		Q-0	Q-1	Q-1	Q-2											
2		I-1	I-2	I-2	I-3											
3		Q-1	Q-2	Q-2	Q-3											
4		I-2	I-3	I-3	I-4											
5		Q-2	Q-3	Q-3	Q-4											
6		I-3	I-4	I-4	I-5											
7		Q-3	Q-4	Q-4	Q-5											
8	Control Byte (#Z.X.1)	I-4	I-5	I-5	I-6											
9		Q-4	Q-5	Q-5	Q-6											
10		I-5	I-6	I-6	I-7											
11		Q-5	Q-6	Q-6	Q-7											
12		I-MSB	I-MSB	I-7	I-8											
13		Q-MSB	Q-MSB	Q-7	Q-8											
14		I'-0	I'-0	I-8	I-9											
15		Q'-0	Q'-0	Q-8	Q-9											
16	Control Byte (#Z.X.2)	I'-1	I'-1	I-9	I-10											
17		Q'-1	Q'-1	Q-9	Q-10											
18		I'-2	I'-2	I-10	I-11											
19		Q'-2	Q'-2	Q-10	Q-11											
20		I'-3	I'-3	I-11	I-12											
21		Q'-3	Q'-3	Q-11	Q-12											
22		I'-4	I'-4	I-12	I-13											
23		Q'-4	Q'-4	Q-12	Q-13											
24	Control Byte (#Z.X.3)	I'-5	I'-5	I-13	I-14											
25		Q'-5	Q'-5	Q-13	Q-14											
26		I'-MSB	I'-6	I-MSB	I-MSB											
27		Q'-MSB	Q'-6	Q-MSB	Q-MSB											
28		r	I'-MSB	I-0												
29		r	Q'-MSB	Q-0												
30		I-0	I-0	I-1												
31		Q-0	Q-0	Q-1												

Each AxC can be offset by an integer number of samples. This means that the first sample of an AxC does not have to arrive/depart at the same time as the first sample of other AxCs within the same group. Figure 5-3 depicts an example where AxC#0 is offset by 2 samples, AxC#1 is offset by zero samples, and AxC#2 is offset by one sample on a 4x CPRI link. These AxCs are LTE10 AxCs, so each basic frame holds four samples. Also, it is not required for AxC numbers to be incrementing within a group.

Figure 5-3. AxC Sample Offset Mapping



When a radio standard is used that requires stuffing samples, the AIL follows equation 16 from the CPRI v5.0 specification. The following four figures are examples of a 4x CPRI link with four groups. The first group is an LTE5 group with two AxCs, the second group is an LTE1.4 group with three AxCs, the third group is a GSM (960 kHz sample rate) group with one AxC, and the fourth group is a WCDMA group with four AxCs. These four figures show the pattern of how stuffing samples would be inserted for this grouping. This pattern would be repeated every four basic frames, with the sample numbers incrementing accordingly.

Figure 5-4. Basic Frame 0 of Stuffing Sample Mapping

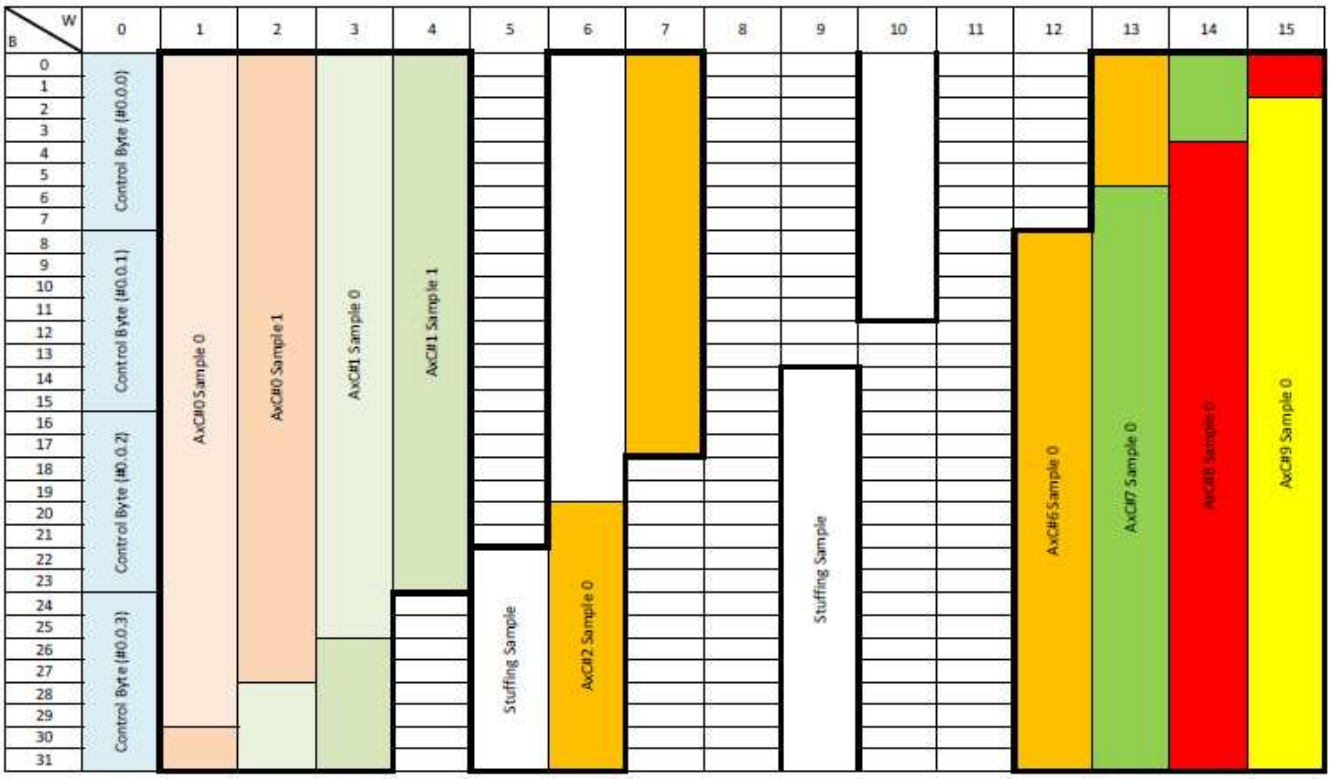


Figure 5-5. Basic Frame 1 of Stuffing Sample Mapping

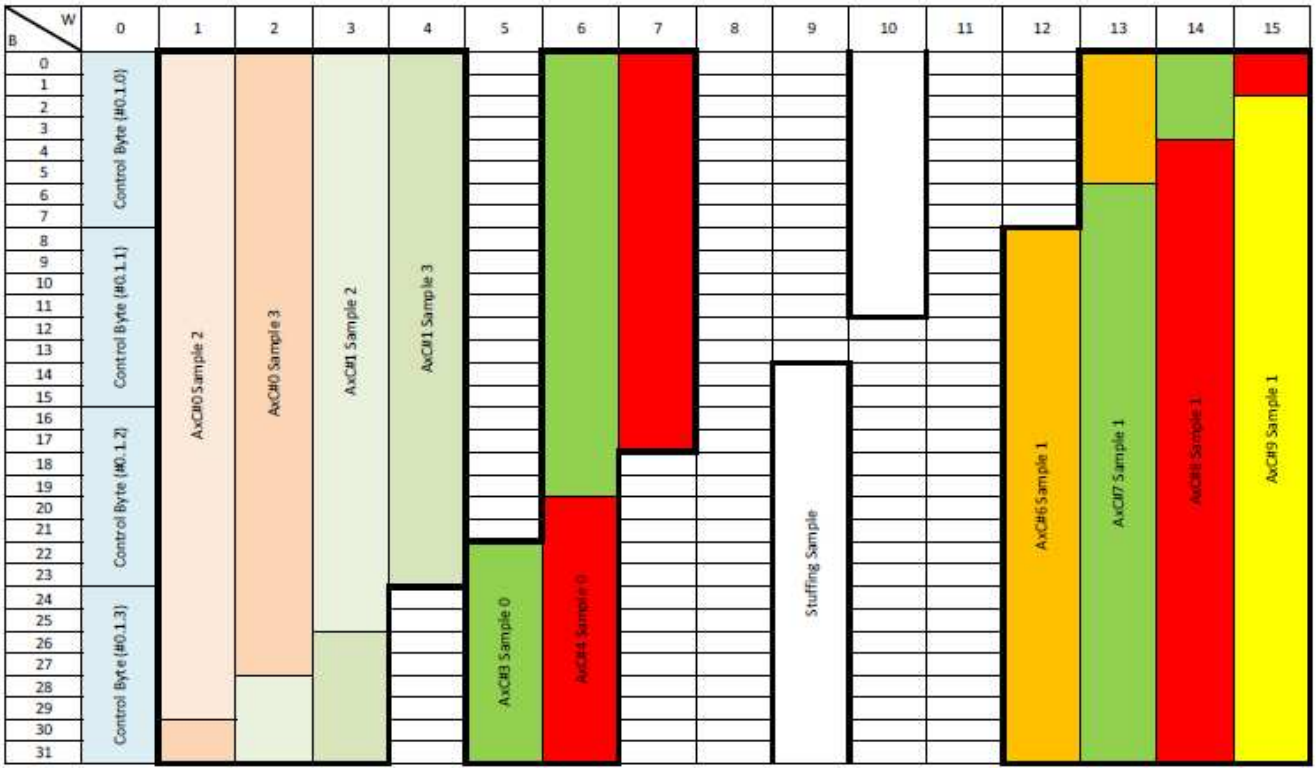


Figure 5-6. Basic Frame 2 of Stuffing Sample Mapping

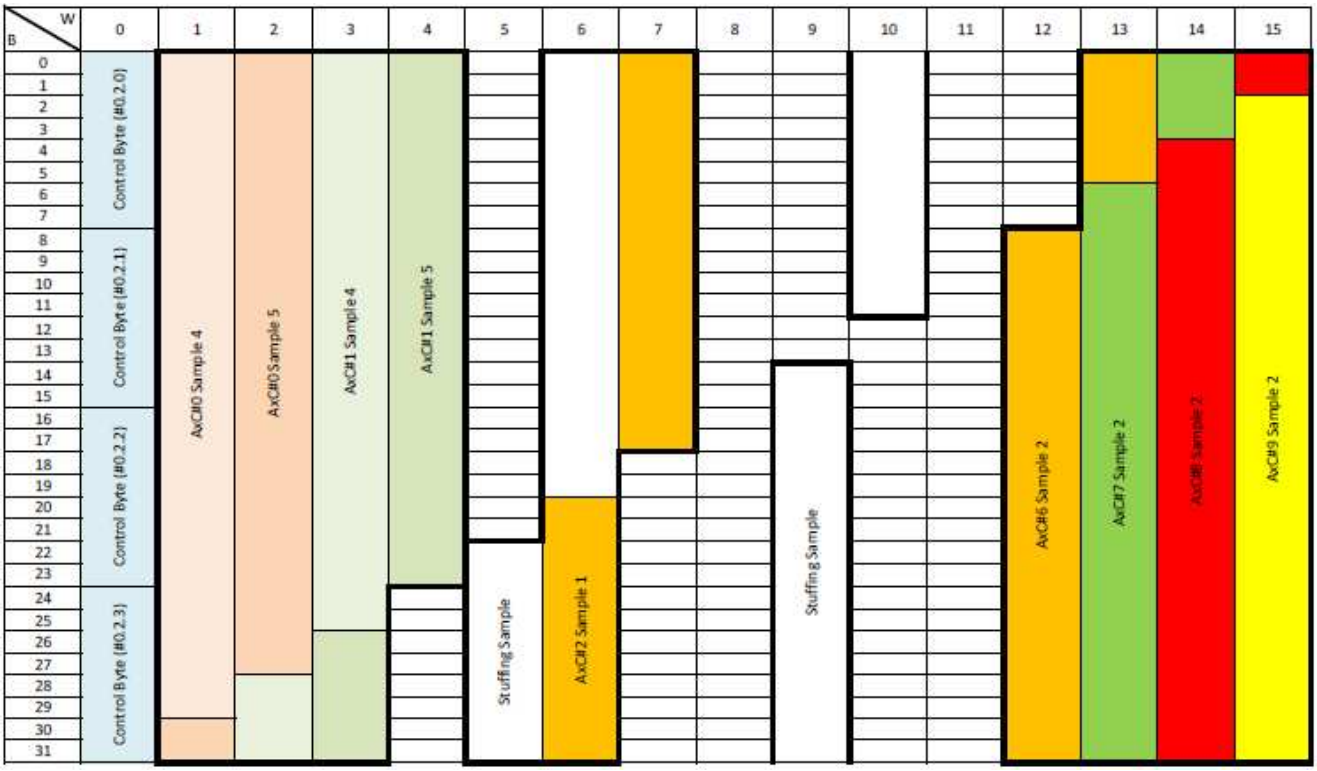
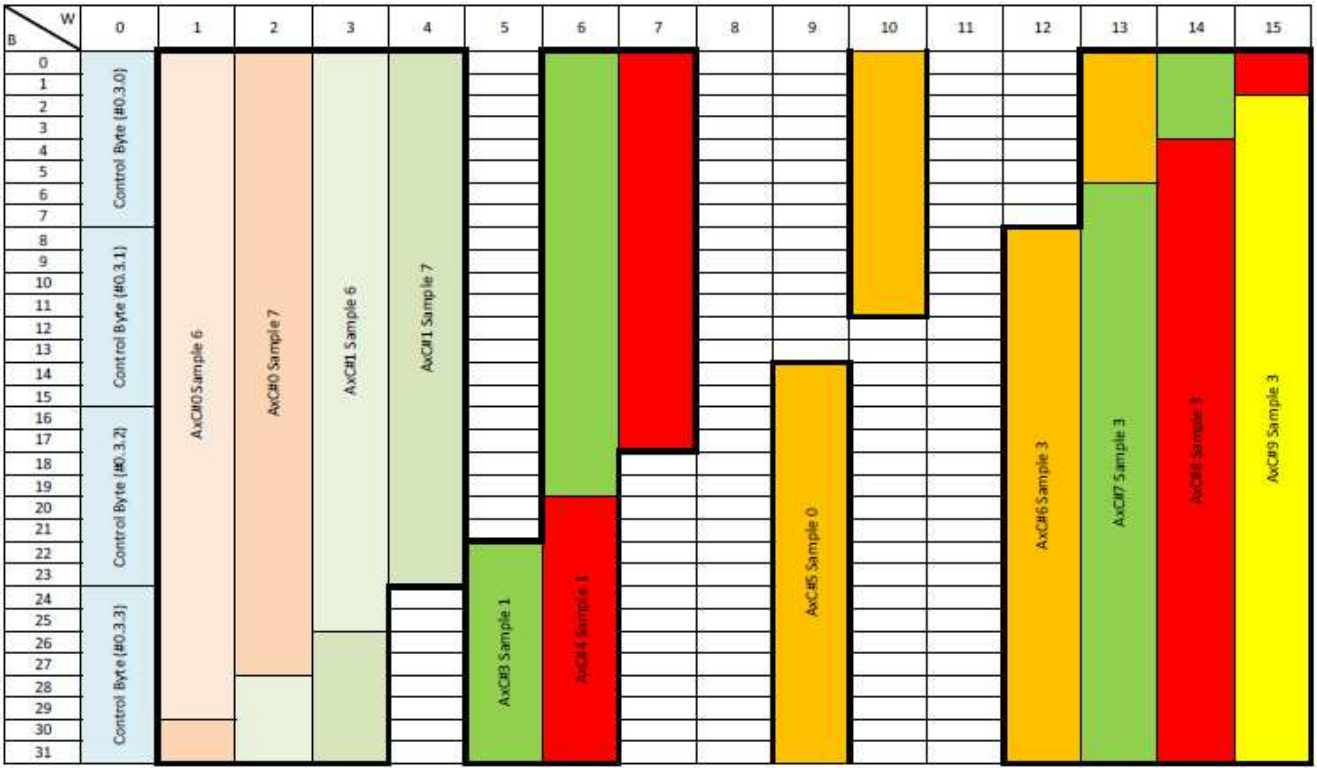
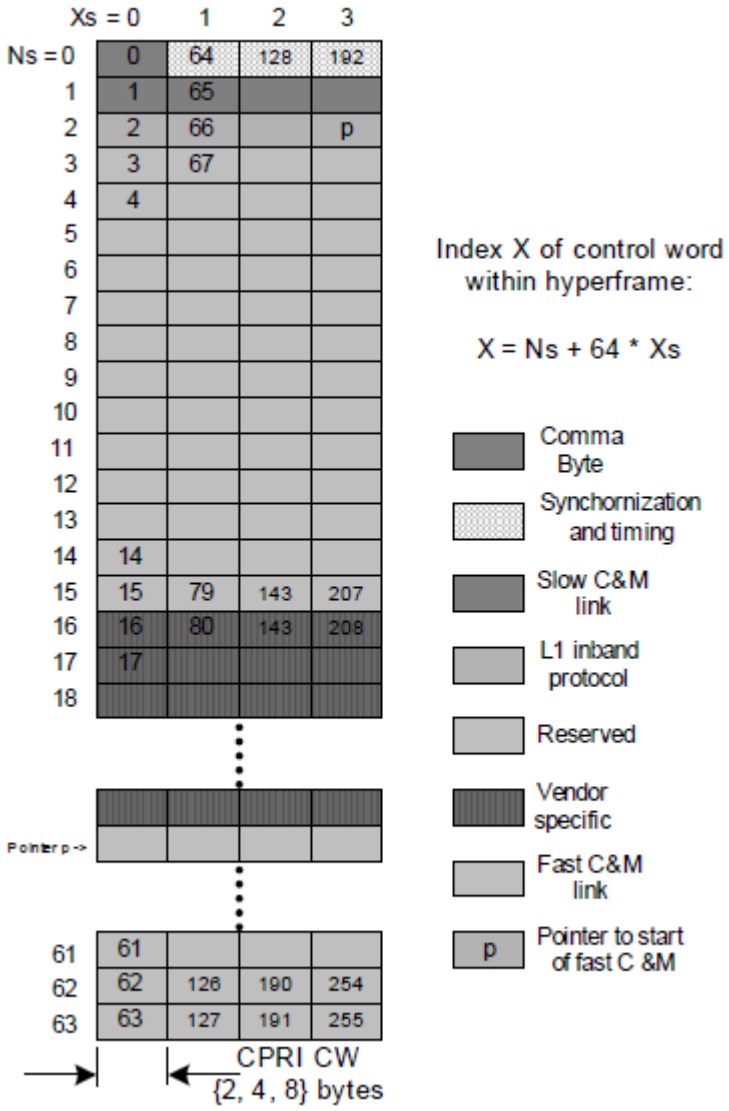


Figure 5-7. Basic Frame 3 of Stuffing Sample Mapping



5.1.3 CPRI Control Data Handling

Figure 5-8. CPRI Control Words Mapping



Many mechanisms for CPRI CW (Control Word) are supported by the TI implementation:

- Slow C&M (HDLC)
- Fast C&M (Fast Ethernet)
- L1 inband, Predefined CW (specific HW control for special bytes)
- Hyperframe delineated insertion
- Null Delimiter

The AIL module can extract/insert up to 4 user defined streams of control words, along with other fixed control words that the AIL captures to/inserts from MMRs.

All other information from control words such as slow C&M, fast C&M, RTWP (Received Total Wideband Power) measurements, and vendor-specific control words are to be mapped to one of the four available control flows. Each control word flow will allow the user to extract or insert into the control words of any of the 256 basic frames. The user will also be able to define the number of bytes per control word that are to be used per control word flow. This byte selection feature along with the basic frame selection feature can be used to implement all of the slow C&M link rates.

The user also may instruct a control word flow to only insert/extract control data during specific hyperframes. This is a hyperframe filter for the control flow. The user will indicate into which hyperframe(s) the control word data is to be inserted/extracted. This feature allows the user to implement the RTWP control word flow, where the RTWP information is only sent every 30 hyperframes. It should be noted that a single hyperframe filter is made available per AIL module direction (one for transmit, one for receive). Each control word flow can either use the hyperframe filter, or be active during all hyperframes.

The user must set the receive and transmit C&M channel rates as well as the C&M channel type through an MMR. The rate and C&M channel type will not be auto-negotiated through hardware. The user must set the pointer-p value as well, since the AIL module does not use the pointer-p value to set the fast C&M channel rate. Although the hardware does not perform auto-negotiation for the C&M channel rates, a software routine can be written to perform this function. Also, it should be noted that if either C&M channel rate is changed during normal operation, data could be lost during the change and the change requires software assistance.

Each control channel flow can have the bit order, nibble order, or bit and nibble order reversed. This reversal can be done before or after the desired encoding. Each control channel flow has its own reversal control, so each control channel flow can be set differently. This flexibility at the hardware level allows the data to be presented in the correct and optimal format for other end users.

5.1.3.1 L1 In-Band Signals (HW MMR Handling of Special CPRI CW)

As noted previously, the AIL module extracts many of the L1 in-band signals on the receive link to readable MMRs. The AIL module filters the reset signal to make sure that at least five consecutive instances of this bit were set before reporting the signal as set. This will ensure that multiple bit errors in the reset bit location cannot cause a link to reset.

The LOS signal is set when the number of 8b/10b code violations exceed a programmable value per hyperframe. The CPRI v5.0 specification calls out at least 16 8b/10b code violations per hyperframe, but the AIL module leaves this up to the user.

The LOF signal is set when the K28.5 synchronization character is not found at location Z.0.0 consecutively greater than a programmable number of times.

The SDI signal cannot be forwarded from an AIL receive link, but it can be set by the reception of the filtered reset signal of a receive link, or through the use of an MMR.

For these signals on the transmit link, the user can choose to either force these signals to a value through the use of an MMR, or the signals can be forwarded from an AIL receive link. It should be noted that the reset signal cannot be forwarded. The RAI signal can also be set by a receive link LOS or LOF signal.

- Sub-channel 0
  - HFN (hyper-frame number)
  - BFN (nodeB frame number)
- Sub-channel 2
  - Protocol version
  - HDLC bit rate
  - Reset Status
  - RAI (remote alarm indication)
  - SDI (SAP defect indication)
  - LOS (loss of signal)
  - LOF (loss of frame)
  - Pointer p value
- Sub-channel 52 (52, 116, 180, 244 control slot)
  - Port ID (reserved for PORT ID and cannot be used for FastC&M)

The AIL will insert the following fields based on MMR settings:

- Sub-channel 2
  - Protocol version

  - HDLC bit rate
  - Pointer p value
- Sub-channel 52 (52, 116, 180, 244 control slot)
  - Port ID (reserved for PORT ID and cannot be used for FastC&M)

The LOS and LOF conditions are well defined and can occur at the receiver of the AIL. In addition to the LOS or LOF error occurring locally, the ingress and egress CPRI link has these bits in the Z.130.0. For purposes of clarification, TI defines variants of these signals with the following sub-scripts:

- XXX_{RX}: bit is received in Ingress link byte Z130.0
- XXX_{ERR}: Error has occurred locally at IQN_AIL receiver
- XXX_{TX}: IQN_AIL sets bit in Egress link byte Z130.0

At each AIL receiver (RM), each of the four received error bits {LOS_{RX}, LOF_{RX}, RAI_{RX}, SDI_{RX}} is received and extracted. The CorePac cores can be programmable alerted via the IQN2 AIL EE (Error Event) mechanism. The error bits {LOS_{RX}, LOF_{RX}, RAI_{RX}} as well as the locally detected errors {LOS_{ERR}, LOF_{ERR}} also are passed to the transmitters (TM) for possible propagation. SDI is not supported with HW propagation; SDI_{RX} is only supported via EE alert and MMR insertion which requires SW support.

The transmitter (TM) for each link receives {LOS_{RX}, LOF_{RX}, RAI_{RX},LOS_{ERR}, LOF_{ERR}} signals from each of six links as well as MMR control information and manual set of each transmitted bit {LOS_{TX}, LOF_{TX}, RAI_{TX},SDI_{TX}}

RAI_{TX} is defined as the aggregate of LOS OR LOF with the capability propagating. This is accomplished by the logic OR of {LOS_{ERR}, LOF_{ERR}, RAI_{RX}, and MMR bit}. Each possible input into the OR operation is MMR enabled/disabled.

5.1.3.2 Flexible Control Word Flows

The AIL module provides several options when defining a control word flow. These options are to control the encoding/decoding of the control words, as well as the delimitation of a message in the control word flow. Through the combination of these options, the AIL module provides a comprehensive solution for extracting control words from a CPRI link, be it one of the defined C&M channels or a vendor specific channel.

The user can define a control word flow with 4b/5b encoding, HDLC bit-orientated encoding, or no encoding. The insertion of preamble and SFD octets for fast C&M Ethernet is controlled via an MMR. These encoding/decoding options are included to facilitate the fast and slow C&M channels, but can be used in any control word flow.

The 4b/5b encoding code list is the same as called out in Table 14 of the CPRI v5.0 specification. This encoding is used to emulate the physical specification of 100BASE-T, described in IEEE 802.3-2005 Section 2. This encoding style provides control characters, such as the start-of-stream delimiter and end-of-stream delimiter that are used in determining packet boundaries.

The HDLC bit-oriented encoding is defined in ISO 13239 section 4.3.1, entitled “Synchronous Transmission.” This encoding scheme inserts a 0 bit after all sequences of 5 contiguous 1 bits. The encoding is performed on all of the content between the two flag sequences that indicate the start and end of message, including the last five bits of the FCS (Frame Check Sequence). The FCS is a 2-byte value, with an MMR that will provide the user with control of which byte to transmit/receive first. The FCS is a 16-bit CRC, and the user can control the initialization value of this CRC sequence. Also, the user has the option of sending constant flag sequences (0x7E) or the IDLE flag (0xFF) as inter-message fill.

5.1.3.3 CPRI Control Word Interleave/Deinterleave

IQN2 allows up to four independent control streams per CPRI link. Each control stream may have parallel control packets in flight at different stages of completion.

CPRI hyper-frames have exactly 256 control words. IQN2 provides a series of MMR registers (three bits per CW position) per link that map each CPRI control word position to:

- Enable bit
  - 1’b0: CW is not mapped to a control stream

  - 1'b1: CW is mapped to a control stream
- Mapping bits
  - 0-3: map to Control Streams {0, 1, 2, 3}

With this LUT method of assigning CPRI control words, the user has complete flexibility to either duplicate the CPRI separation between:

- {slow C&M, fast C&M, and vendor specific}
- Non-CPRI compliant usage of control works

NOTE: IQN2 AIL does not directly use the Pointer-P in assigning Control word BW. AIL does support HW extraction/insertion of Ingress Pointer-P to MMR. If the user wishes to use the Pointer-P for CW allocation, upper layers of SW need to implement this functionality.

5.1.3.4 Packet Parsing

The three key functions of packet parsing are:

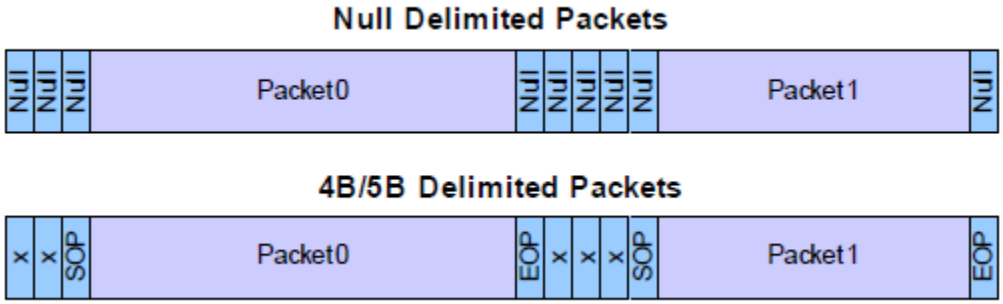
- Using the hyperframe boundary as a packetization boundary
- Separating valid control data from null character
- Separating control stream into valid packets
  - Identify SOP/EOP (start/end of packet)

IQN2 AIL has three mechanisms for packet parsing:

- Hyperframe FSM
- Programmable null delimiter
- 4B/5B coding

Each of four possible (per link) control streams is MMR configured as to which of the two options is used for that stream.

Figure 5-9. CPRI Packet Delimiters



The Programmable Null Delimiter is a unique character that identifies a null (empty byte). The value can be any byte or any non-comma K-character (e.g., K27.7 or K29.7). It is not permissible to have this character appear within a packet. IQN2 allows the user to choose which null value is to be used by programming a 9-bit MMR field. Any data that does not match the Null Delimiter is considered valid control data. There must be at least one Null Delimiter between "packets" of control data. All characters that do not contain valid control data should be filled with the chosen Null delimiter.

Alternately, the Fast Ethernet 4B/5B coding scheme can be used to identify SOP/EOP. 4B/5B may be used for non-Ethernet packets.

5.1.3.5 Fast Ethernet

Fast Ethernet is Ethernet that is 4B/5B encoded. 4B/5B encoding is the encoding on top of the SerDes 8B/10B encoding. In essence, IQN2 deals with 8B/10B encoding at the PHY layer and 4B/5Bencoding at the Protocol layer.

Figure 5-10. Ethernet Frame Structure

Preamble	Start of Frame	Dst Adr	Src Adr	Length	Payload	CRC
7 bytes	1 bytes	6 bytes	6 bytes	2 bytes	1-1500 byte	4 byte

- SSD/ESD: Appended and Stripped by AIL HW
- Preamble: Constant value: 8'b1010_1010
  - Ingress: Stripped off by IQN2 AIL
  - Egress: Added by IQN2 AIL
- Start of Frame: Constant value: 8'b1010_1011
  - Ingress: Stripped off by IQN2 AIL
  - Egress: Added by IQN2 AIL
- Length Field: IQN2 does not use or check the length field of Ethernet
  - Ingress: Ethernet frame is defined by either delimiter byte or 4B/5B encoding
  - Egress: Packet length is controlled by Multicore Navigator header
- Other Fields: Simply passed by IQN2
- Interframe gap (not shown in Figure 5-10)
  - Does not apply to CPRI, Gapping is not required over Phy
- Extension fields
  - Does not apply to CPRI, Not supported.

IQN2 performs the following operations:

- Ingress
  - De-interleave CPRI Streams
  - 4B/5B decode (SSD/ESD strip)
  - Parse stream into Ethernet packets
  - Strip Ethernet preamble and SOF fields
  - Encapsulation into Multicore Navigator packets
  - PKTDMA
- Egress
  - PKTDMA
  - Extract from Multicore Navigator Packet
  - Add Ethernet preamble and SOF fields
  - 4B/5B encode (SSD/ESD appended)
  - Insert into CPRI Stream
  - Interleave CPRI Streams

PA (Packet Accelerator) performs the following operations:

- Route to final internal or external destination

5.1.3.6 4B/5B Encoding

4B/5B encoding is part of Fast Ethernet, but IQN2 AIL allows for use of 4B/5B encoding simply as a packet delimiter. This special encoding also can be used as a packet delimiter for generic packet traffic that uses the AxC data slot in generic packet mode.

4B/5B encoding is a 20 percent overhead scheme where each byte is broken into two nibbles and each nibble is represented by five bits. With the extra redundancy, extra characters can be defined. IQN2 allows for the use of 4B/5B encoding only in CPRI mode and can be used for:

- Fast Ethernet (4B/5B required)
- Generic CPRI control packet delimiter

The SOP is uniquely identified by a pair SSD#1 and SSD#2 (bit pattern 11000_10001) which is used by AIL as a comma alignment character. The EOP is identified by the pair ESD#1 and ESD#2 (bit pattern 01101_00111).

Table 5-2. Fast Ethernet 4B/5B Encoding

Name	4b	5b	Description
0	0000	11110	hex data 0
1	0001	01001	hex data 1
2	0010	10100	hex data 2
3	0011	10101	hex data 3
4	0100	01010	hex data 4
5	0101	01011	hex data 5
6	0110	01110	hex data 6
7	0111	01111	hex data 7
8	1000	10010	hex data 8
9	1001	10011	hex data 9
A	1010	10110	hex data A
B	1011	10111	hex data B
C	1100	11010	hex data C
D	1101	11011	hex data D
E	1110	11100	hex data E
F	1111	11101	hex data F
I	-NONE-	11111	Idle
J	-NONE-	11000	SSD part1
K	-NONE-	10001	SSD part2
T	-NONE-	01101	ESD part1
R	-NONE-	00111	ESD part2
H	-NONE-	00100	Halt

The 4B/5B encoding occurs before stream serialization (CPRI PHY packing) and before 8B/10B encoding for SerDes transmission. (4B/5B encoding is in addition to 8B/10B; it does not replace 8B/10B).

4B/5B Corner cases and IQN2 handling:

- SSD#1 and SSD#2 form a pair that identify SOP
  - They are a unique code which give comma alignment
- ESD#1 and ESD#2 form a pair that identify EOP
  - Cannot be used for comma alignment
- Any non-data byte (except ESD) after an SSD
  - Bad Packet
  - Marked as bad packet in Multicore Navigator header (but still DMA'ed)
  - IQN2 will EOP packet immediately

- SerDes Byte Error during a packet
  - Marked as bad packet in Multicore Navigator header (but still DMA'ed)
- Packet too long
  - Not handled by IQN2 (handled by PA)
- Null Data
  - IQN2 will transfer "IDLE" when there is no control packet to send on a given control stream.

5.1.3.7 CRC

The AIL module provides several hardware CRC options for control word flows. A programmable 8-bit CRC, a 16-bit CRC (CRC-16-CCITT, x16 + x12 + x5 + 1), and a 32-bit CRC (CRC-32, x32 + x26 + x23 + x22 +x16 +x12 + x11 + x10 + x8 + x7 + x5 + x4 + x2 + x + 1) are available.

When a CRC is enabled for transmit, it is created and appended to the end of a control message. The user will have to leave space at the end of the packet sent over the DMA to the AIL module for the CRC to be placed. These bytes will be overwritten by the AIL module when sent out over the CPRI link. When a CRC is enabled for receive, the CRC is calculated and checked against the incoming CRC field. The CRC field is passed with the rest of the packet over the DMA. If the CRC fields do not match, the packet can either be marked as an errored packet or the packet can be dropped. The operation performed on a CRC mismatch will be user selectable.

5.1.4 Retransmit/Chaining

Although the AIL module only has visibility of 64 AxCs at the protocol layer, the AIL module can retransmit the entire CPRI link at the physical layer. The AIL module provides the capability to retransmit the received traffic from one of eight other CPRI links onto the transmit CPRI link.

The retransmission of a CPRI link cannot be dynamically changed. Once a CPRI link is chosen to be the retransmitted link, another link cannot be substituted while the AIL module is operational. The link rate of the received traffic from other AIL modules must be the same as the transmitter link rate. For the AxCs for which the AIL module does have visibility, the user can choose to have the AIL module transparently pass the value from receive to transmit, aggregate the received sample with another sample from memory and transmit the result, or overwrite by transmitting a different sample from memory.

During sample aggregation, the AIL module performs symmetrical saturation on any value that exceeds the sample size after aggregation. When retransmitting, the AIL module has enough buffering and bandwidth elasticity to compensate for +/- 833 ns of fiber drift.

The AIL module can be instructed to operate in CPRI uplink RE-Chaining mode. In this mode, the CPRI control words will be buffered until the next CPRI hyperframe so that they can be inserted at the correct basic frame. The user will program an MMR which instructs the AIL module to insert the IQ data at the appropriate basic frame number. This MMR value can then be communicated to the downstream CPRI receiver, so that the correct sample number can be recovered from the CPRI link. This feature meets the requirement in the CPRI v5.0 specification where each networking RE can change the frame position of an uplink AxC container in order to minimize delay.

It should be noted that when in CPRI uplink RE-Chaining, any control word messages that are to be extracted during specific hyperframes will be delayed by at least one hyperframe per hop. This must be taken into account by downstream receivers. When in the CPRI uplink RE-Chaining mode, the repositioning of the IQ data will consume a portion of the fiber drift buffer.

5.1.5 Bit-Rate Conversion

The AIL module does not support bit-rate conversion. The data would have to be extracted to the DMA layer, and then transmitted through normal means. This will increase latency and use switch-level DMA resources as well. This precludes the AIL module from performing bit-rate conversion.

5.1.6 Delay Measurement

The AIL module provides time measurements of when the incoming synchronization signal is received over the CPRI link and when the outgoing synchronization signal is transmitted over the CPRI link. These values are based on a central timer that both measurements share. The values are readable through an MMR. This method meets the link timing and round trip delay timing accuracy requirements detailed in the CPRI v5.0 specification, except when the AIL module is running at the 2x link rate. At this link rate, the uncertainty contributions due to clock domain crossings could exceed the requirement values defined in the CPRI v5.0 specification.

5.2 OBSAI Specifics

5.2.1 OBSAI Standard Overview

The OBSAI interface is primarily intended for passing antenna data between the RF card and the baseboard devices. Its secondary function is for passing user-specific control data between any devices.

The basic premises of the OBSAI interface are to time multiplex different streams (that is, antennas) of data on a single SerDes link. OBSAI segments each data stream into 16-byte segments and appends a simple header that is used on the receiving end to reconstruct/deinterleave the different streams.

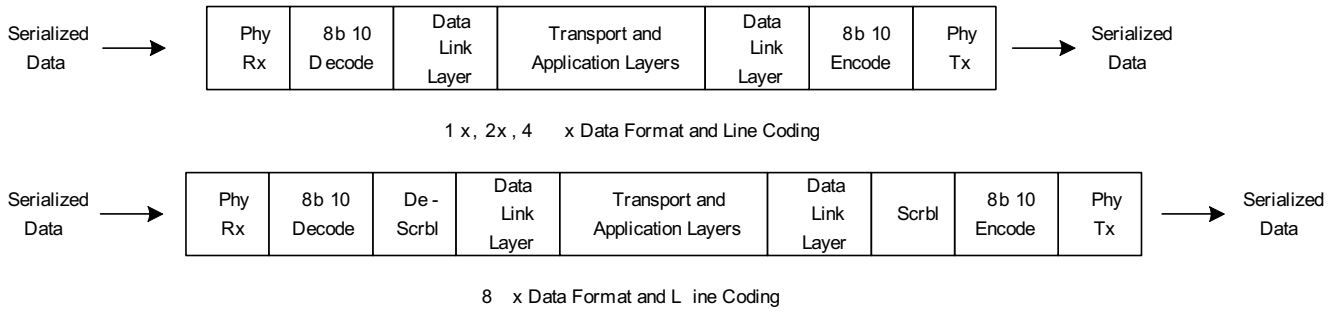
There are two basic parts of the OBSAI interface:

- OBSAI RP1: timing interface for synchronizing all nodes/devices within the base station
- OBSAI RP3: Data Interface for passing antenna and control data between nodes in the base station utilizing SerDes connectivity.

The RP1 physical interface is a simple LVDS serial data interface with corresponding LVDS 30.72MHz clock. The IQN2 AIL supports only reception/synchronization to RP1 sync bursts, but does not transmit RP1 sync bursts. The OBSAI RP1 spec. defines the serial burst stream pattern over the serial data interface and how IQN2 is to use this timing information.

The RP3 physical layer provides coding and serialization of the transmission path. An LFSR scrambling algorithm, applied to 8x links only, provides smoothing of the data stream before 8b10b encoding. The data link layer provides a method for creating messages of the bit stream. The transport layer utilizes the address field of messages to control message routing for processing of the application layer. The application layer terminates the payload of messages into packets.

Figure 5-11. OBSAI Data Format and Line Coding



The OBSAI RP3 standard supports multiple link data rates. SerDes data rates differ from usable data rates for the following reasons:

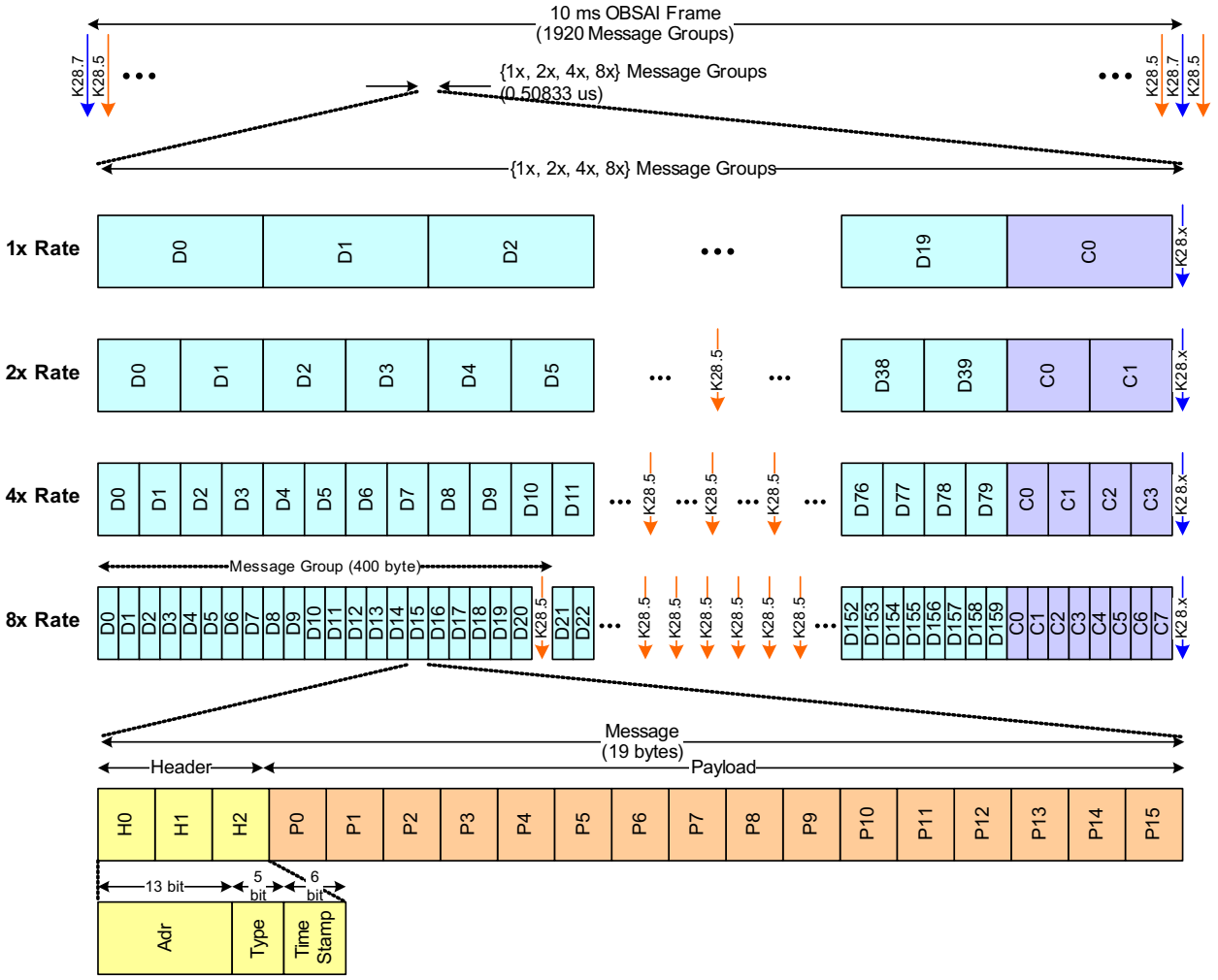
- Three bytes of header for each 16 bytes of payload
- 8B/10B SerDes encoding
- One dedicated control message for each 20 data messages
- K-character demarcating framing

Table 5-3. OBSAI RP3 SerDes Rates

Link rate	Line rate (Gbps)	Data Msg Payload Rate (Gbps)	Control Msg Payload Rate (Gbps)
2x	1.536	0.98304	0.049152
4x	3.072	1.96608	0.098304
8x	6.144	3.93216	0.196608

5.2.1.1 OBSAI Overview: Frame/Message Structure

Figure 5-12. OBSAI Frame/Message Structure



Regardless of link rate, OBSAI has a 10 ms frame structure. The frame boundaries are demarcated with a K28.7 character at the end of each frame. Each frame is further subdivided into *i*1920 message groups (where *i* depends on link rate *i*={1x, 2x, 4x, 8x}). Each message group is exactly 400 bytes containing exactly 21 messages ending with a single K-Character:

- K28.7 if it is the last message group in a frame
- K28.5 for other messages groups in a frame

Data Messages are grouped with Control Messages. First there are *i*20 Data messages then *i* Control Messages. These groups span multiple message groups (with K-characters ending each message group.

Table 5-4. OBSAI Data/Control Message Grouping

Link rate	*i* Message Groups	Data Messages	Control Messages
2x	2	40	2
4x	4	80	4
8x	8	160	8

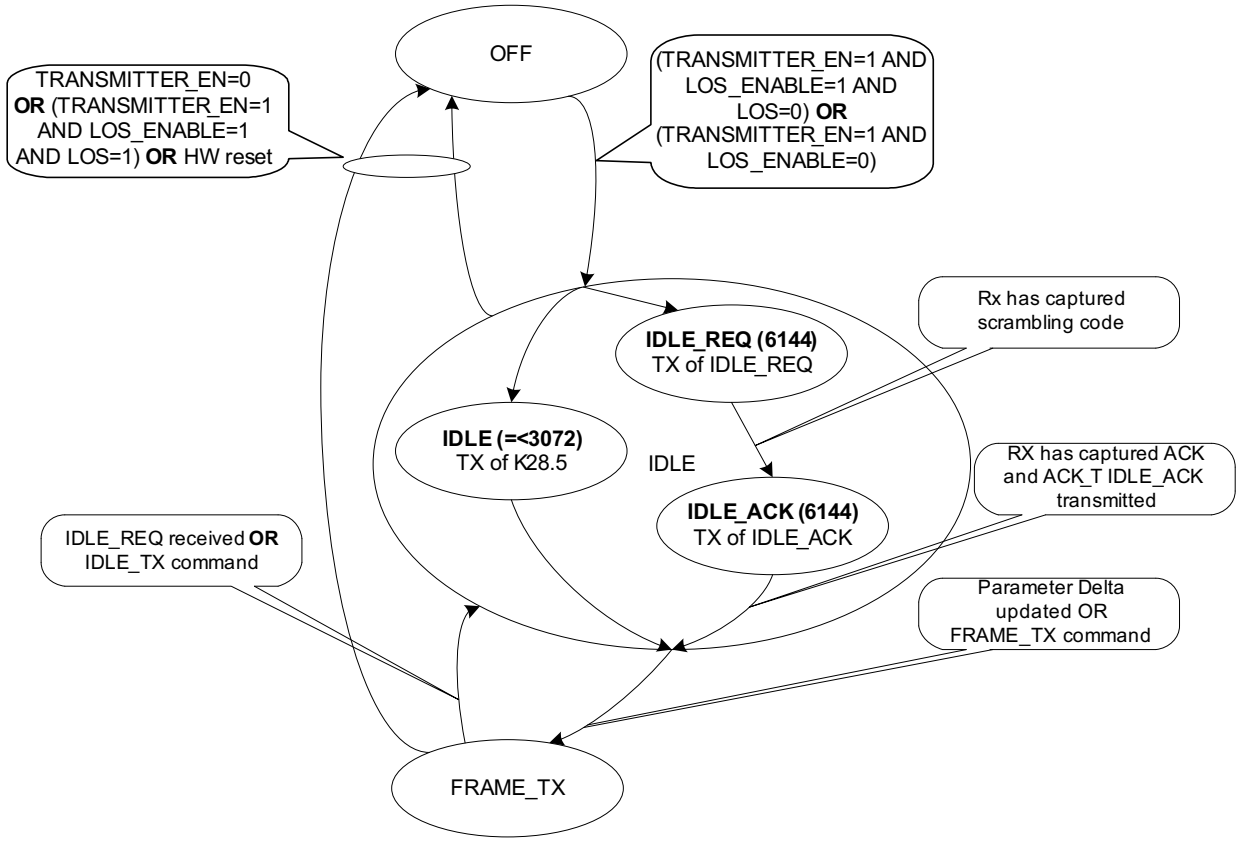
The special message type “Empty Message” is defined to indicate a control or data message is currently unused. “Empty Message” is indicated with the special OBSAI address of 13’h1fff. All other fields are “don’t care” but IQN2 fills all other fields with zeros.

Figure 5-13. OBSAI Empty Message (IQN2 Transmitted)

5.2.1.2 OBSAI Overview: RP3 Tx and Rx FSMs

Frame synchronization is achieved by adhering to defined state transitions in OBSAI RP3. For transmit, the state transitions are shown in Figure 5-14. The frame synchronization begins in the Off state. The transmitter is enabled by system control to transition the state machine to the Idle state. While in the Idle state, the state machine follows the scrambler protocol acknowledge sequence if the link is configured for 6144 Mbps. If the link is configured for less than 6144 Mbps, then while in the Idle state K28.5 characters are transmitted. Once the delta variable is known, the state machine can be transitioned to the FRAME_TX state, and valid frames are transmitted at the delta offset. Upon a reset, receiver loss of signal, or a system control disable of the transmitter, the state machine transitions back to the Off state.

Figure 5-14. OBSAI RP3 Transmit State Machine



The receiver state machine in Figure 5-15 consists of four states for 768, 1536, and 3070 Mbps line rates and six states for the 6144 Mbps line rate. The four states applied to all line rates are as follows:

- UNSYNC
- WAIT_FOR_K28.7_IDLES
- WAIT_FOR_FRAME_SYNC_T
- FRAME_SYNC

Two of these states, WAIT_FOR_K28.7_IDLES and WAIT_FOR_FRAME_SYNC_T, can be considered to form a single logical state called SYNC. The meaning of states UNSYNC, SYNC, and FRAME_SYNC is as follows:

- UNSYNC: Bus link is down. Many byte errors are detected.
- SYNC: Bus link is working, that is, connection exists.
- FRAME_SYNC: Normal operational mode. Frame structure is detected and messages are received.

Two additional states are applied for the 6144 Mbps line rate due to scrambling seed transfer from the transmitter to the receiver: WAIT_FOR_SEED and WAIT_FOR_ACK. These two states form a logical state called SCR_CAP (scrambling seed capture). It is expected, that the receiver can capture scrambling code both from IDLE_REQ and IDLE_ACK patterns. When in the state WAIT_FOR_K28.7_IDLES, IDLE_REQ is detected if every 17th byte of received data is a K28.5 and there are valid data bytes (no K-codes, no LCV errors) between K-codes. Contents of data bytes are not checked. This way it is possible to recognize IDLE_REQ, even if the scrambling code has been changed.

To reduce false recognition of IDLE_REQ, due to an errant K28.5, IDLE_REQ will not be detected in the WAIT_FOR_FRAME_SYNC_T and FRAME_SYNC states. If a scrambling code has been changed, many IDLE_REQs will be received. This will eventually cause FRAME_UNSYNC_T invalid message groups and force the transition to the WAIT_FOR_K28.7_IDLES state. IDLE_REQ will be detected in this state and cause a transition to the WAIT_FOR_SEED state.

The receiver state machine uses two separate criteria to determine the quality of a bus link. The first one monitors the signal quality by counting LCV errors and the second one monitors the validity of the received frame structure. Parameters BLOCK_SIZE, SYNC_T, UNSYNC_T, FRAME_SYNC_T, and FRAME_UNSYNC_T control the transitions.

On reset, the state machine enters the UNSYNC state. The UNSYNC state also is entered when the SerDes indicates a loss of signal. State transition from the UNSYNC state to WAIT_FOR_K28.7_IDLES (768,1536, and 3070 Mbps line rate) or WAIT_FOR_SEED (6144 Mbps line rate) is done if SYNC_T consecutive blocks of bytes have been properly received. In each block, there exists BLOCK_SIZE bytes and a block is considered to be valid if all the bytes were received correctly (i.e., no 8b10b decoding errors). Otherwise, the block is considered to be invalid.

In case of 6144 Mbps line rate, state transition from WAIT_FOR_SEED state to WAIT_FOR_ACK state is done when the scrambling seed is captured from the IDLE_REQ training pattern (or IDLE_ACK pattern) and verified over 16 sets of training patterns. Transition from the WAIT_FOR_ACK state to the WAIT_FOR_K28.7_IDLES state is done when an acknowledgement of the seed capture has been received (IDLE_ACK pattern).

Transition from state WAIT_FOR_K28.7_IDLES back to UNSYNC is done if UNSYNC_T consecutive invalid byte blocks are received or in case of HW reset or SerDes loss of signal. Transition from state WAIT_FOR_K28.7_IDLES back to WAIT_FOR_SEED occurs if an IDLE_REQ pattern is detected.

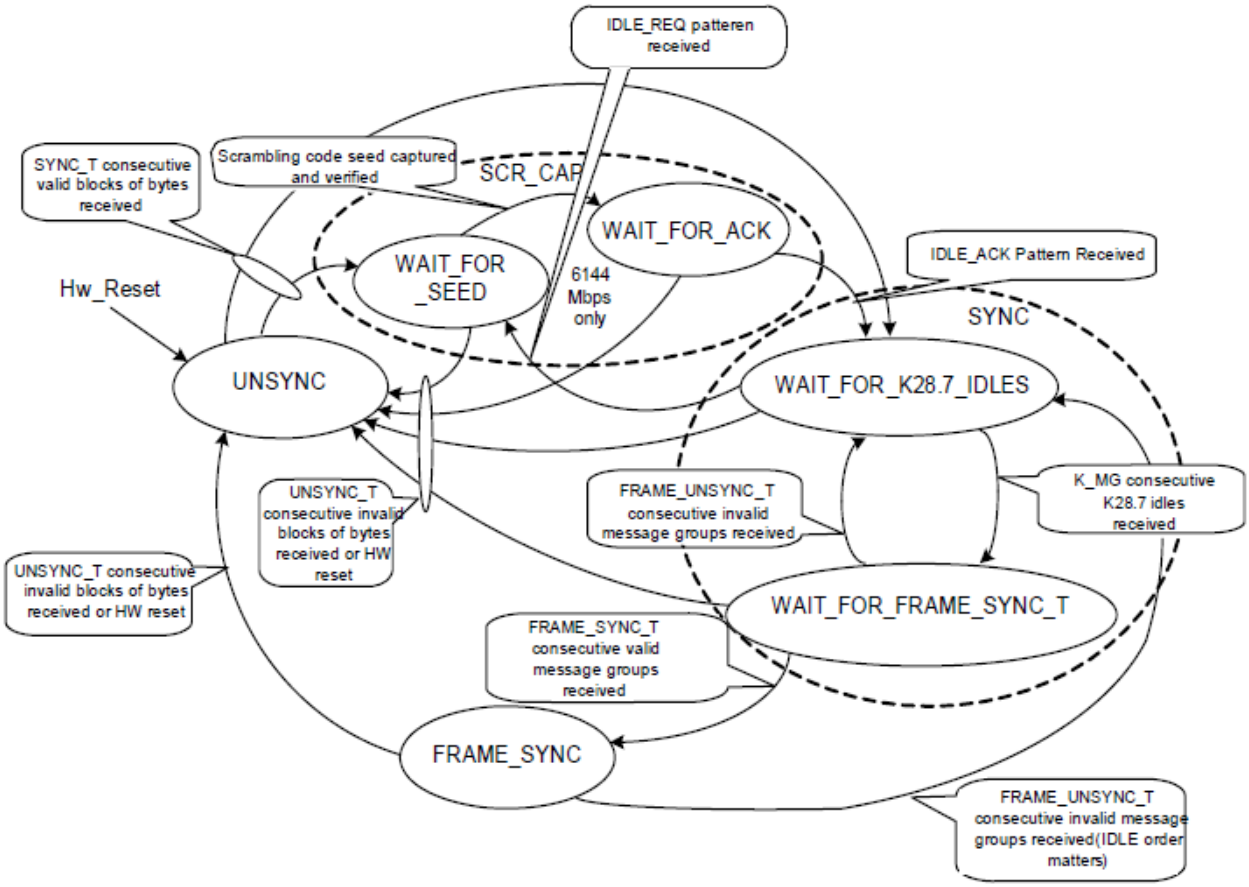
Master Frame boundary is indicated by a set of K28.7 IDLE bytes, i.e., it exists at the end of the block of K_MG consecutive K28.7 IDLEs (for purposes of the IQN_AIL, K_MG = 1). Transition from WAIT_FOR_K28.7_IDLES to WAIT_FOR_FRAME_SYNC_T is done when K_MG consecutive K28.7 IDLE bytes, i.e., a possible Master Frame boundary, is detected. In state WAIT_FOR_FRAME_SYNC_T as well as in state FRAME_SYNC, Master Frame timing is considered to be fixed (defined by the first set of received K28.7 IDLEs).

In WAIT_FOR_FRAME_SYNC_T state, validity of consecutive message groups is studied. When FRAME_SYNC_T consecutive valid message groups are received, FRAME_SYNC state is entered. If FRAME_UNSYNC_T consecutive invalid message groups are received, state WAIT_FOR_K28.7_IDLES is entered and search for a new set of K28.7 IDLE bytes is started immediately, unless the IDLE_REQ pattern is detected (6144 Mbps line rate), in which case the WAIT_FOR_SEED state will be entered.

State transition from FRAME_SYNC to WAIT_FOR_K28.7_IDLES is done when FRAME_UNSYNC_T consecutive invalid message groups are received and transition from FRAME_SYNC to UNSYNC is done when UNSYNC _T consecutive invalid blocks of bytes are received. If enabled, if a programmable number of 8b10b decoding error occurs, the UNSYNC state also will be entered.

A valid message group is defined as a block of 400 bytes where the first 399 bytes are of type data or an 8b10b decoding error occurs. IDLE codes K28.5 or K28.7 are not allowed. The last K_MG bytes must be either K28.5 or K28.7 IDLE bytes or an 8b10b decoding error. Furthermore, the order of the IDLE bytes matters. In the first N_MG-1 Message Groups of a Master Frame, all IDLE bytes of the Message Group must equal to K28.5 while in the last Message Group of the Master Frame, K_MG (=1) IDLE codes equal to K28.7.

Figure 5-15. OBSAI RP3 Receive State Machine



The receiver synchronization state machine has several outputs. Current state of the receiver will be available for the Application layer. An interrupt may be generated from each state change. Signal loss_of_signal is active (has value 1) in state UNSYNC while it is inactive in other states. Synchronization block also indicates bytes that contain 8b10b decoding error as well as the location of the Master Frame boundary. For the 6144 Mbps line rate, scramble seed capture and acknowledge training pattern received is also indicated.

5.2.1.2.1 OBSAI Overview: General

Streams/Messages are classified into different types, and these types are indicated by the type field of the message headers. OBSAI supports several different types of traffic. These are identified by the “Type” field in the OBSAI header where the different types are predefined as a five-bit encoded fields. For the different types, the usage of the “Timestamp” fields varies. Table 5-5 shows the “Timestamp” usage for the different OBSAI types. An “X” indicates that there is an algorithm for filling the Timestamp. A “#” indicates that Timestamp bits are being used to extend the addressing. In other cases, a fix value is written.

Table 5-5. OBSAI RP3 Types

Payload data Type	Content of Type Field	Timestamp #: address extension X: Timestamp Protocol
Control	00000	000000 –or- 000001
Measurement	00001	XXXXXX
WCDMA/FDD	00010	XXXXXX
WCDMA/TDD	00011	XXXXXX
GSM/EDGE	00100	XXXXXX
TETRA	00101	undefined
CDMA2000	00110	XXXXXX
WLAN	00111	undefined
LOOPBACK	01000	undefined
Frame Clock Burst	01001	000000
Ethernet	01010	XXXXXX
RTT message	01011	000000
802.16	01100	XXXXXX
Virtual HW reset	01101	000000
LTE	01110	XXXXXX
Generic Packet	01111	XX####
Not Used	10000-11111	undefined

CRC error check is provided for the following types:

- Control Messages: 16-bit CRC
- Generic Packet Type: 16-bit CRC
- Ethernet Type: 32-bit CRC

5.2.1.3 OBSAI Overview: Timestamp

The OBSAI header has a six-bit field that is labeled Timestamp. For transport types that are streaming antenna traffic, this timestamp field is used to indicate the progression of samples moving in/out of the RF card. Additionally, the TS field carries framing information indicating radio frame boundary for all standards except for GSM/Edge where the timeslot boundary is indicated.

5.2.1.3.1 Non-GSM AxC Timestamp

The six bits of Timestamp start at 6'b000000 at the radio frame boundary and increment by one every OBSAI message. Timestamp is maintained separately for each AxC. The timestamp value ranges from 0-to-63, wrapping when reaching the max. count. Timestamp equal to 0 can either mean radio frame boundary, or a simple wrap of the counter.

5.2.1.3.2 GSM Timestamp

GSM/Edge has a custom Timestamp where the MSB represents the beginning of a GSM timeslot (1'b1 identified timeslot beginning). The remaining LSBs start at zero (at the beginning of a timeslot) and increment one for each message of the timeslot. There is one slight difference between UL and DL:

- DL: The MSB is held high for only the first OBASI message of the timeslot
- UL: The MSB is held high for the first four OBSAI messages of the timeslot

5.2.1.3.3 Ethernet Timestamp

- SOP: 6'b100000
- MOP: 6'b000000
- EOP: 6'b1XXXXX (XXXXX: indicates the number of bytes from the start of RP3 payload containing MAC frame data (counting started from the byte after the header)

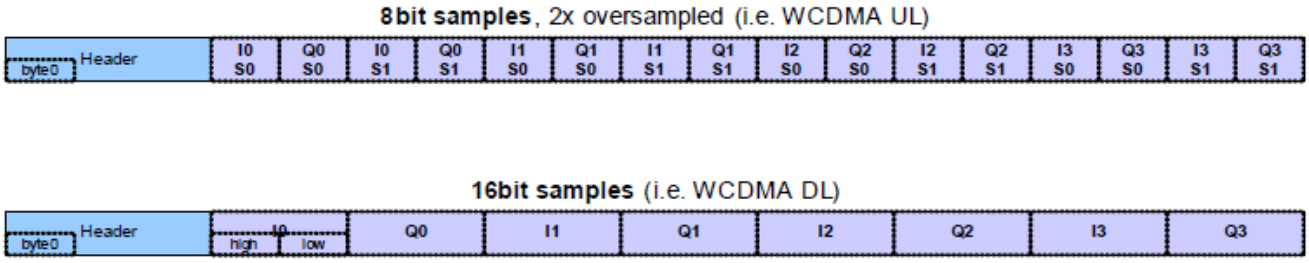
5.2.1.3.4 Generic Packet Timestamp

- SOP: 6'b10XXXX
- MOP: 6'b00XXXX
- EOP: 6'b11XXXX (XXXX: is an extension of OBSAI address and is the same for all elements within the packet)

5.2.1.4 OBSAI Overview: Message Payload Formats

See Figure 5-16 for data alignment within the OBSAI message payload.

Figure 5-16. OBSAI Message, Payload Sample Packing



Two different payload formats are supported for antenna traffic:

- 8-bit I + 8-bit Q, 2x over-sampled
- 16-bit I + 16-bit Q, not over-sampled

5.2.2 OBSAI: Header Based Processing

5.2.2.1 DMA Channel Index

OBSAI Header information is used to map ingress stream data with the appropriate ingress DMA channel. There are a total of 64 possible ingress DMA channels per IQN2 AIL. The total address space of an OBSAI header is too large to implement with an exhaustive RAM LUT. 64 parallel comparison circuits are built corresponding to the 64 possible ingress DMA channels. When one of these 64 comparison circuits activates, the corresponding DMA channel is indexed.

NOTE: It is the user's responsibility to ensure that each unique DMA channel LUT is programmed uniquely such that only one comparison will fire at a time.

This indexing function is based mostly on the OBSAI Address and Type comparison. The exception to this rule is the OBSAI Generic Packet indicated by type 5'b01111; the address space is effectively extended by using the four LSBs of the Timestamp field in Generic Packet Mode. In Generic Packet Mode, there is no valid concept of timestamp and so this field is used to extend addressing.

While IQN2 AIL has 64 different DMA channels allowing for unique handling and destination addressing of all 64 streams, IQN2 PktDMA only allows 48 channels to be mapped to PKTDMA channels. An additional 16 channels can be supported by DIO but those channels are only used for WCDMA traffic.

5.2.2.2 8B/10B Code Violation and Bad OBSAI Message Header

A SerDes bit error is expected to occur once every 10^{15} bits (results in an 8B/10B code violation). Although infrequent, it happens regularly enough that it needs to be handled properly. Each 10 bits across the SerDes map to an eight-bit byte; a single bit error results in the complete corruption of the entire byte.

For antenna traffic, an infrequent bad byte at the phy level has much lower error contribution than the cellular air channel. For control data, a bad byte in the payload fields is assumed to be unimportant, caught by CRC check, or corrected by higher layers. The IQN2 handling of bad bytes in the OBSAI payload (of the message) is to convert it to a 0 (8'h00) and simply pass it along.

5.2.2.2.1 IQN2 Operation

- The IQN2 RM (Rx Mac) drops packets with:
  - 8B/10B code violations in the OBSAI Header –or-
  - K30.7 in the OBSAI Header
  - Dropped packet is replaced with empty message
- The IQN2 RM will replace bad payload bytes with 8'h00. A bad byte is identified by either:
  - 8B/10B code violations in the OBSAI Payload –or-
  - K30.7 in the OBSAI Payload

Retransmission occurs after RM, so the above actions dictate the handling.

5.2.2.3 OBSAI: Missing Timestamp

IQN2 expects a constant stream of correct OBSAI messages for each AxC stream. IQN2 checks the incoming stream by examining the OBSAI message header timestamp field. Timestamps are expected to be zero on radio frame boundary and increment by one for each OBSAI message of a given AxC.

Due to the handling of 8B/10B code violations in OBSAI headers, whole OBSAI messages can be dropped. IQN2 has handling mechanisms that tolerate one or two consecutive missing messages. If there are more than two consecutive missing messages, the entire AxC is failed; resynchronization occurs on the next radio frame boundary.

5.2.2.3.1 IQN2 Operation

- PD Performs TS check
  - PD predicts TS and FB
  - Checks TS against Expected
  - Writes packet boundaries and Error signals into FIFO w/Data
- DMA interface block (while reading DMA Channel FIFO)
  - Insert 0, one, or two extra empty data phases
  - Close/Open packet as indicated by packet boundaries

The IQN2 partitions the handling of missing TS information among several submodules. The PD (Protocol Decoder) writes whole messages into the DB FIFO and identifies missing timestamps and missing packet boundaries. PD performs this check using predicted timestamps and symbol boundaries.

5.2.2.3.2 Failed AxC

- AIL restarts the TS predictor circuit
- AIL close out any open packet (by writing a EOP with zero data)
- AIL will activate Fail_Pkt signal marking packet as bad
- DMA
  - Direct IO: DIO stops capturing data until next Radio Frame Boundary; DIO DMA continues to transfer junk
  - Multicore Navigator: Discard current packet for DMA channel

The mechanisms for detecting missing TS (messages) is reactive. Not until new, valid messages have arrived will the error mechanism for the missing messages be activated. In the event that a missing message would have been the EOP (end of packet), the DMA of the packet is effectively delayed until a valid message is received for that particular AxC. It is the responsibility of the user to analyze their system to ensure that these timing differences do not have a detrimental effect.

The AIL_PD WatchDog timer can help improve the latency of packet completion due to missing OBSAI messages. In particular, there is a special case of GSM BB Hopping or GSM Compressed Mode where a missing EOP will not be pushed out by good traffic for a very long time.

5.2.3 OBSAI: 6 GHz Scrambling

Bit-level scrambling is performed on 8x rate links to reduce cross talk between links as well as to reduce inter-symbol interference (ISI). The RP3 transmitter applies a seven-degree polynomial to data bytes and the inverse operation is performed by the RP3 receiver. Scrambling only pertains to 6 GHz operation (8x link rate). Link rates {2x, 4x} are backward compatible with no scrambling applied.

Cross talk between transmitters through the local SerDes power supply is the main concern. With all transmitters having differing scrambling offsets, randomness between transmitting lanes is achieved. The assignment of unique scrambler offsets for receivers is optional as cross talk between receivers and transmitters is non-critical.

The RP3 transmitter is configured by higher layers with a starting value of the seven-degree polynomial scrambling code generator. Higher layers should configure unique seed values for adjacent RP3 Tx links. Table 5-6 lists the available seed values to be used; these seed values represent nx7 position offsets (nx7 has been specifically chosen to give an odd offset between adjacent links). The RP3 receiver is a slave to the transmitter, receiving the seed value in a training sequence.

Table 5-6. Scrambler Seed Values

Nx7 Index	X^7	X^6	X^5	X^4	X^3	X^2	X^1
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	1
2	0	0	0	0	1	0	1
3	0	0	0	1	1	1	1
4	0	0	1	0	0	0	1
5	0	1	1	0	0	1	1
6	1	0	1	0	1	0	0
7	1	1	1	1	1	0	1
8	0	0	0	0	1	1	1
9	0	0	0	1	0	0	1
10	0	0	1	1	0	1	1
11	0	1	0	1	1	0	1
12	1	1	1	0	1	1	0
13	0	0	1	1	0	1	0
14	0	1	0	1	1	1	0
15	1	1	1	0	0	1	1
16	0	0	1	0	1	0	1
17	0	1	1	1	1	1	1

The scrambler is a seven-degree polynomial, linear feedback shift register (LFSR). The polynomial is $X^7 + X^6 + 1$. K28.5 or K28.7 characters reset the LFSR to the seed value. The bit pattern repeats every 127 bits.

5.2.4 OBSAI: Generic Packet Mode

Generic Packet is an OBSAI mechanism that allows multiple OBSAI messages to be grouped together to form a larger packet. The packet size is n × 16 bytes where the last two bytes are the CRC16.

Generic Packet

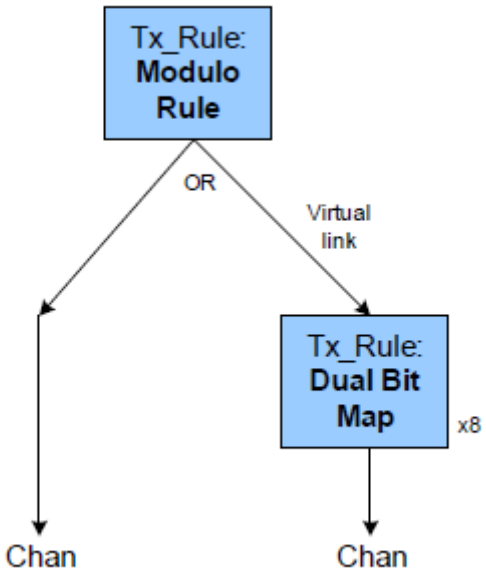
- Type fields = “5’b01111”
- Timestamp field
  - Bit[5:4]
    - 2’b10: SOP start
    - 2’b00: MOP mid-point
    - 2’b11: EOP end

– Bit[3:0]: extension of address field

5.2.5 OBSAI: RP3 Transmission

Modulo and Dual Bitmap Rules are used in conjunction with each other to flexibly allocate the Link bandwidth between multiple streams of antenna or control data.

Figure 5-17. OBSAI Transmission Rules



5.2.5.1 OBSAI Tx: Modulo Rules

Data Messages and Control Messages are separated into two different control flows. A counter is maintained for each where the counter is zeroed at the beginning of each PHY (RP3) frame boundary. A modulo value is chosen and different streams are given unique indexes into that modulo.

The modulo technique is used to share bandwidth between different streams sharing the same link or virtual link. It is used for either antenna traffic or control traffic, but it was not intended that a single stream be shared between Control Message slots and Data Message slots.

The Modulo technique works very well for WCDMA, LTE, and TD-SCDMA where the sample rate is an exact divisible rate relative to the OBSAI Data Message rate. The Modulo technique does not work for WiMax where the sample rate does not have a clear relationship to the OBSAI rates.

Historically, Modulo Rules where the only form of transmission rule. Dual bit map rules were added later to support rate matching. Along with DBMR, the concept of TDM is added permitting a single rule to support n AxC. TI advocates using a single DBMR per radio standard, enabling a great simplification of the AxC_Offset concept.

5.2.5.2 OBSAI Tx: Dual-Bit Map Rules

The Dual Bit Map approach is a rate matching algorithm for mapping streams into links (with dissimilar frequencies). In summary, *X* AxC with the same sampling frequencies are mapped into *X* sequential Data Messages. At the end of *X* sequential Data Messages one empty message is inserted according to the programming of the Dual Bit Map control fields. Dual Bit Map Rules are not intended to be applied to Control Messages.

If the bit map contains:

- 1: length = *X* + 1 (*X* data message for *X* AxC + one empty message)
- 0: length = *X*

The index into the bit map is incremented each X or X+1 data messages. The empty message gaps constitute the rate matching where the whole purpose of the Bit Map Algorithm is to place these empty messages in meaningful locations.

OBSAI RP3 specifies programming values of the Dual Bit Map FSM in the RP3 specification, Appendices D and F.

5.2.6 OBSAI RP3-01 Standard Overview

The OBSAI RP3-01 is a late addition to the OBSAI standard specifically intended to support remote radio heads. At that moment in time, Ethernet over OBSAI was added to the standard where Ethernet proves to be useful for both Macro and RRT BTS. The ability to send remote sync to an external node is more specific to RRH applications, though it has also been used for expansion modules of a macro BTS.

5.2.6.1 RP3-01 RTT Message

The OBSAI RP3-01 message is not supported by AIL. Users need to use Pi reception measurement in conjunction with prior knowledge of Delta transmission timing at source in order to calculate RTT (round trip timing) for the link.

5.2.6.2 RP3-01 Timing Synchronization

The RP3-01 is a mechanism to remotely synchronize a timer from a master node to a slave node via the RP3 interface. The master node is assume to have an active RP1 interface to a timing board which is supplying an RP1 serial FCB burst. The last bit of the RP1 timing burst is the exact time which the RP1 timing FCB is to take effect.

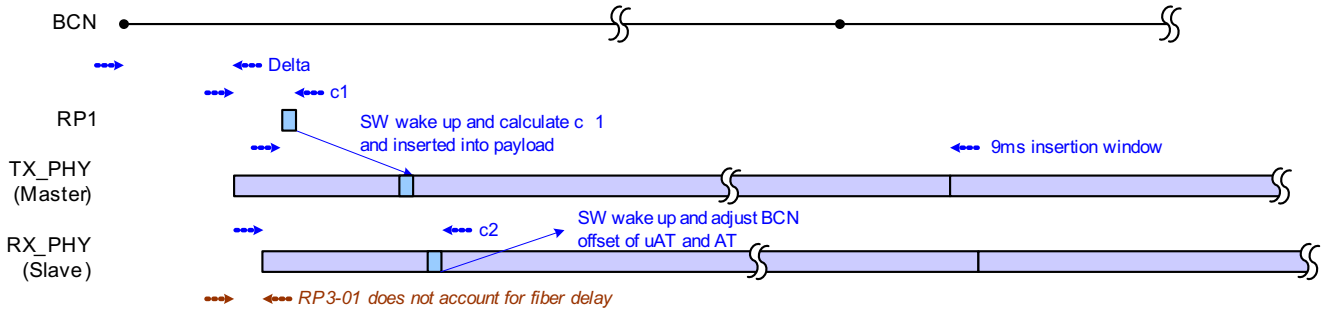
In normal RP1, the timing burst will synchronize a timer (several timers exist); in case of RP3-01, the RP1 FCB is passed to the remote slave node for use. When passing the FCB across, the timing precision of the last bit is lost, so the RP3-01 protocol passes additional information in order to facilitate the synchronization.

Master operation:

The IQN2 implementation of the RP3-01 differs slightly from the OBSAI spec. Whenever an RP1 FCB is received over the RP1 bus, the AT BCN value is captured. In addition, the TM delta value (TM event offset) is a known quantity. The delta is simply added to the measured FCB arrival time to calculate the value of c1. This c1 value is multiplied by 2 prior to use. SW is alerted into action upon reception of the RP1 FCB via an EE system event. The SW wake-up task performs this c1 calculation and builds up the payload of the OBSAI FCB message.

The calculated c1[26-bit] value plus the two FCB fields system_type[8] and system_frame_number[64] are packed into an OBSAI message with a CRC16 appended to the end. This specially constructed message is inserted into the outgoing OBSAI link and must be transmitted within 9 ms of time. The complete operation is controlled via a mixture of initialization SW and run-time “wakeup” SW. At initialization time, the SW allocates a PktDMA channel and PE channel dedicated to the FCB messaging. SW sets up an OBSAI transmission rule which allocated OBSAI BW for this RP3-01 flow (at least a few OBSAI message slots per frame guarantee the 9 ms transmission). The runtime SW forms a packet from the OBSAI message and pushes the packet onto the appropriate queue manager channel. Once the AIL_PE (triggered by the OBSAI transmission rule) visits the channel, the packet will be fetched and the RP3-01 message sent over the OBSAI link to the slave device. The SW may use the CRC16 option in the PE circuit or may simply calculate and append the CRC16.

Figure 5-18. OBSAI RP3-01 Timing c2 > c1



Slave operation:

On reception of every OBSAI frame boundary, the AIL_RM creates an internal strobe which captures the AIL_SI_uAT BCN counter value. The measurement is extremely accurate. This measurement is referred to as “Pi Measurement” and is the time synchronization reference point. Effectively, the “Pi Measurement” plus the passed c1 value is the intended sync point passed FCB information. There are two complications for this:

- The operation is non-causal: It took some amount of time to pass the FCB from master to slave so the precise application of the original RP1 FCB has passed. The slave must apply the information for a future sync point.
- c2 > c1 -or- c1 > c2 : depending on whether the FCB message was transmitting in the same link frame as the RP1 message was received or if it was transmitted in the next link frame, there is a possible correction factor which needs to be applied

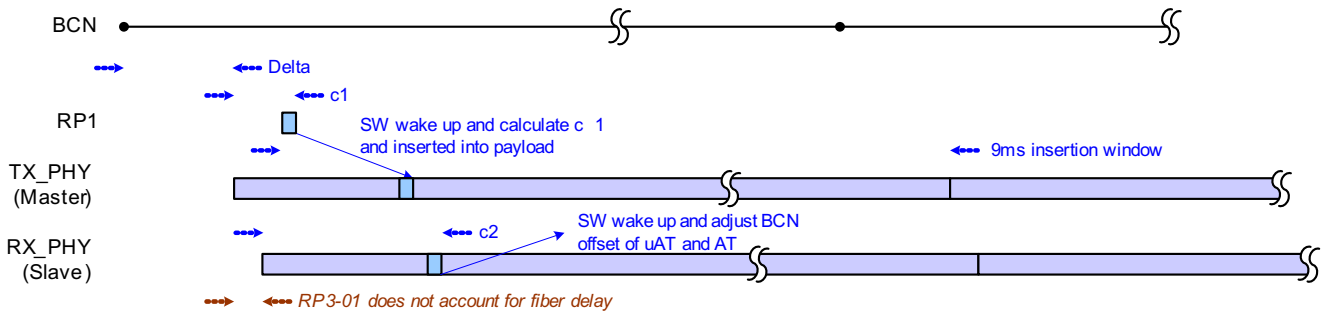
The AT BCN counter and the uAT BCN counters are simply up counters which roll over at the 10 ms boundary. Each of these is an OFFSET MMR which immediately offsets the count value. Many of these have Frame_Cnt which increments every frame boundary wrap and this Frame_Cnt can be instantaneously written (overwritten) by SW at any time. At the beginning of time, the RP3-01 slave starts up it’s BCN counters with random alignment to the radio system. Once an RP3-01 FCB BCN message is received, the local BCN value is corrected. The correction value is the two parts, partial frame and whole frame values.

Assuming that c2 > c1 and that the FCB is synchronizing BCN: The BCN counter was supposed to be zero at the “Pi_Measurement” + c1. In other words if the “Pi_Measurement” + c1 is zero, then the BCN is already properly aligned. If it is off in either direction, then a correction factor is calculated.

In cases where a RadT is being synchronized, the RadT alignment to the BCN is known. The RadT-to-BCN offset is added to the above algorithm in order to calculate the correction factor specific to the RadT.

For the case of the BCN counters and simple RadT counters in the uAT, the offset value is simply adjusted. In case of the complex RadT counters in the AT, a future sync point is calculated and programmed into the RadT sync circuit (the complex RadT timers are started at a specified value of the master AT BCN).

Figure 5-19. OBSAI RP3-01 Timing c1 > c2



The c2 value is simply the number of clocks between the received frame boundary and the received RP3-01 FCB message. In cases where the master measured c1 in one RP3 frame and transmitted the c1 in the next RP3 frame, a correction factor is calculated and used. In this case the ("Pi_Measurement" - 10 ms) + c1 should be equal to zero. Since the BCN is already modulo10ms, the extra 10 ms factor has no effect on the fine grain adjustment of the BCN or simple RadT. For RadT frame lengths which are not 10 ms (WiMax 4 ms in particular) the fine adjustment is complicated by this c1 > c2 case.

The IQN_AIL_PD strobes a signal to the uAT when the FCB message is received; the uAT captures its local BCN value to an MMR. SW creates a c2 value by subtracting the Pi measurement capture from the FCB BCN capture.

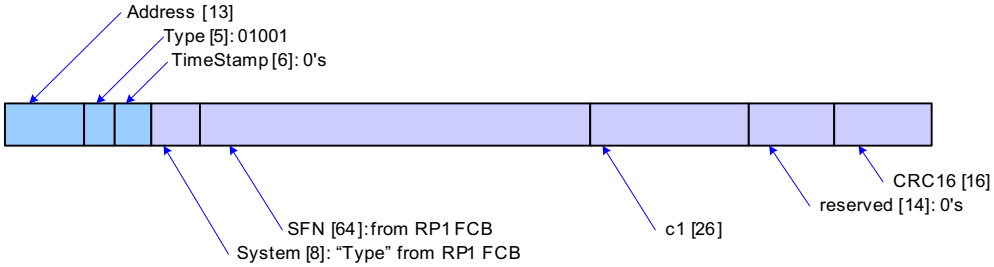
NOTE: The Pi measurement is triggered at the AIL_RM from the reception of the K28.5 on the OBSAI PHY. The FCB message capture is triggered at the AIL_PD which is many clocks away from the RM measurement. It is unfortunate that the measurements are taken in different places in the pipeline, but necessary since only the protocol layer is capable of decoding an OBSAI message. In practice, the user should compensate for the difference in measurement positions to avoid corner case errors in the RP3-01 algorithm.

5.2.6.3 OBSAI RP3-01 Message

The RP3-01 requires the sender (master) to transmit the FCB message within 9 ms of receiving the RP1 FCB; this coupled with max fiber latencies of 200 us (40km) guarantee that the SFN (frame number) is current for the current operation. In case of the simple BCN counters, simply update the counter offset value with the correct fine adjustment, then overwrite the current Frame_Cnt with the value supplied by the FCB SFN.

In cases of modifying the complex RadT timers of the AT, the SW must choose a future BCN value to be a sync point and calculate what the Frame_Cnt will be at the time of that sync point. (This operation is similar to the RP1 sync of these timers and may actually invoke the same SW routines.)

Figure 5-20. OBSAI RP3-01 Timing c1 > c2



The OBSAI header for the FCB message has a specific OBSAI Type of 5'b01001 and the OBSAI TimeStamp of 6'b000000 (effectively the OBSAI TimeStamp field is unused).

A remote radio head (RP3-01 slave) requires both the RP3-01 sync and the ability to generate a radio frequency exact clock. The clock source for the RRH is beyond the scope of the IQN2 and not discussed in this document.

IQN2 DMA (Multicore Navigator and DIO)

Topic **Page**

6.1 VBUS Data Formats

6.1.1 IQN2 16-Bit Sample DMA (OFDM and WCDMA DL)

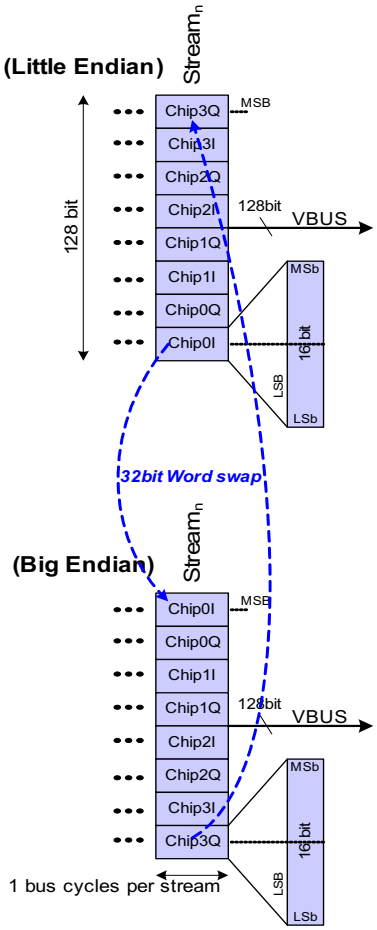
Four samples of 32 bits each conveniently fit into a single 128-bit VBUS cycle. For this reason, VBUS packing and IQN2 PSI FIFO packing are orientated as 128-bit (eight 16-bit values). Endianess handling is performed on the 32-bit entity size where word alignment swapping is implemented. IQN2 SI (DIO,AIL,AID) IDC and EDC has this special feature to swap data in word level. In case of WCDMA DL, DIO SI EDC swap feature can be chosen to swap data.

This data format is used for:

- WCDMA DL
- LTE, WiMax, TD-SCDMA

Figure 6-1 shows a WCDMA chip, but the same figure applies to OFDMA standards by replacing the word "chip" with "sample."

Figure 6-1. 16-bit Sample VBUS Transfer Format



Endianess handling is performed on the 32-bit entity size where word alignment swapping is implemented. IQN2 SI (DIO, AIL, AID) IDC and EDC has this special feature to swap data in word level. In case of WCDMA DL, DIO SI EDC swap feature can be chosen to swap data.

This data format is used for:

- WCDMA DL
- LTE, WiMax, TD-SCDMA

Figure 6-1 shows a WCDMA chip, but the same figure applies to OFDMA standards by replacing the word "chip" with "sample."

In many cases, CPRI data arrives as 15-bit I + 15-bit Q. The Protocol layer converts between 15-bit and 16-bit data prior to the DMA layer.

WCDMA DL data has two possible sources:

- TAC
- L2 (RSA processed DL data)

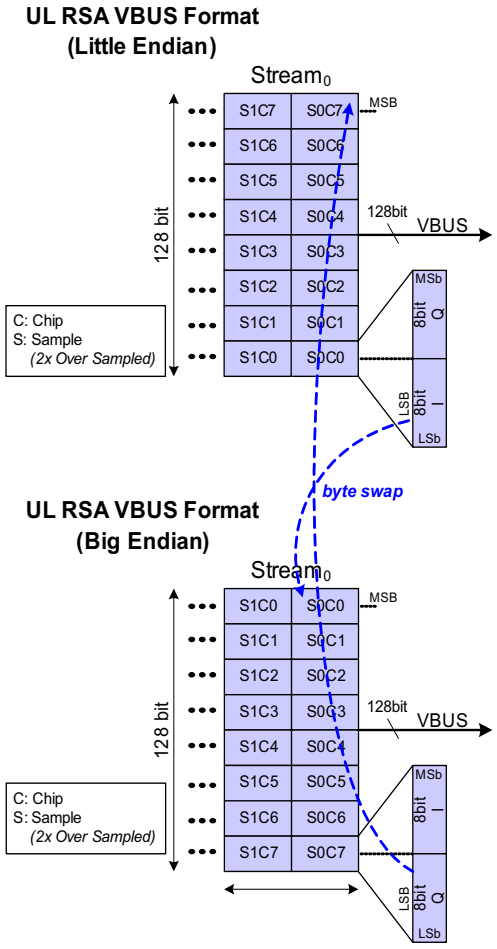
6.1.2 WCDMA UL DMA

Figure 6-2 shows:

- Odd samples: S0xx
- Even Samples: S1xx

RSA Data format is shown in diagrams. This RSA data format is the WCDMA UL data format used by both CorePac RSA and RAC. The figure shows Odd/Even samples sequentially transferred over the VBUS (in separate data phases). This is the way the RAC FEI requires input data.

Figure 6-2. Uplink VBUS Transfer Format



The uplink data flow is somewhat more complex than the Downlink scenario. Predominately, Uplink symbol data originates in the Inbound RAM and is written to both the RAC (Receive Accelerator Coprocessor) and the RX DSP L2 RAM. Delayed streams are formed by writing Antenna Data to the external RAM and then retrieving it at a later time. Retrieved data is sent both to the RAC for receive processing and out the Antenna Interface for broadcast to other devices in the system.

WCDMA Uplink DMA transfers are always bursts of eight chips *(the DL transfer burst format is four chips)*. Uplink data is eight bits I and eight bits Q with an oversampling rate of 2x. The RSA (which can perform some Uplink processing such as Preamble Detect or Path Monitoring) requires the oversampled input data to be separated into even and odd samples. All this coupled with a VBUS width of 128 dictates an optimal transfer burst of eight chips.

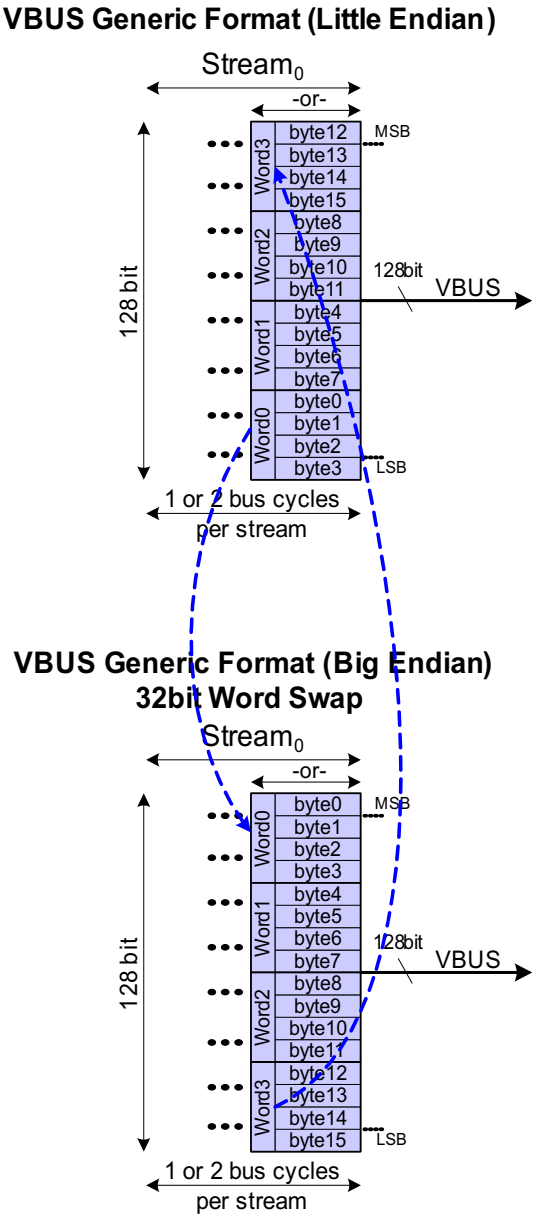
Endianess handling is performed on the 16-bit entity size where byte alignment swapping is implemented. IQN2 DIO has a special feature to swap data in byte level by programming **DIO_GLOBAL_CFG.RSA_BIG_ENDIAN**. See Section 7.7 for more detail about this feature.

6.1.3 Generic Format DMA

Generic Format:

- CPRI Ethernet
- CPRI Control Data
- OBSAI 16 byte (mode) Control Message
- OBSAI or CPRI Generic Packet of Control Slot
- OBSAI Generic usage of AxC data Payload

Figure 6-3. VBUS Format Generic (Byte Numbers Relative to PHY Arrival)

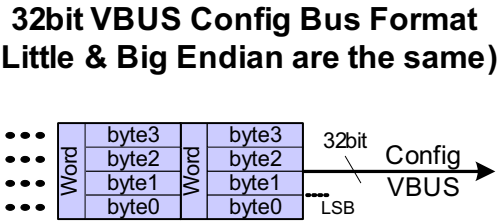


The Generic format supports all packet switch messages (including control messages) and is used to facilitate inter-device communication traffic. The Generic format is differentiated from other formats with its word (four-byte) orientation matching the width of the DSP core data path.

6.1.4 VBUS Config Bus

The 32-bit VBUS config port is used for reading and writing MMRs within IQN2 as well as accessing the IQN2 data path for emulation.

Figure 6-4. MMR VBUS_Config Data Format



All MMRs within IQN2 are defined as 32-bit words and therefore have identical Big Endian and Little Endian representation on the 32-bit VBUS config.

While users are debugging code using Code Composer Studio, it is possible to place various memories into a watch window. To achieve this, CCS is actually performing reads (and writes) of various memory-mapped locations.

6.2 Direct IO

The term Direct IO means that a peripheral has dedicated custom logic that implements data movement (as apposed to using EDMA or CPU reads/writes). For IQN2, custom circuitry is built to handle data movement requirements unique to WCDMA.

The Packet DMA (PKTDMA) module has a Direct IO support feature that allows IQN2 to pass VBUS reads/writes to the VBUS, using the 128-bit VBUSM master port on the PKTDMA.

Direct IO is a state machine that is triggered to transfer data when DIO internal uAT RadT events fire. Example transfer times could be every {4, 8, 16} chips of time. The time granularity of the data transfer does depend on UL/DL and the preferred packing at the destination (that is, DDR3 prefers 64-byte read/write bursts). The amount of data to be transferred is equal to the accrued number of samples buffered during the transfer time chosen above.

The PKTDMA module in IQN2 megamodule assigned 48 channels for packet style data transfer like LTE, WiMAX, TD-SCDMA, GSM and also assigned separate 16 channels for Direct IO purpose. There is no need to enable Rx and Tx channels before sending or receiving DIO data and PKTDMA internal data loopback mode setup can be ignored for DIO mode. (There is nothing to be set for DIO operation.)

6.2.1 IQN2 DIO

The IQN2 DIO allows for Direct I/O, i.e., non-packet-based DMA for WCDMA applications. It uses a common DMA engine design that is constructed specifically for WCDMA-based transfers. The DIO consists of the following major components:

- Ingress DIO
- Egress DIO
- Data Trace
- SI
  - Ingress SI Interface
  - Egress SI Interface
  - Micro AT module (uAT)
- VBUSM Interface (master)
- Error Event (EE) Module

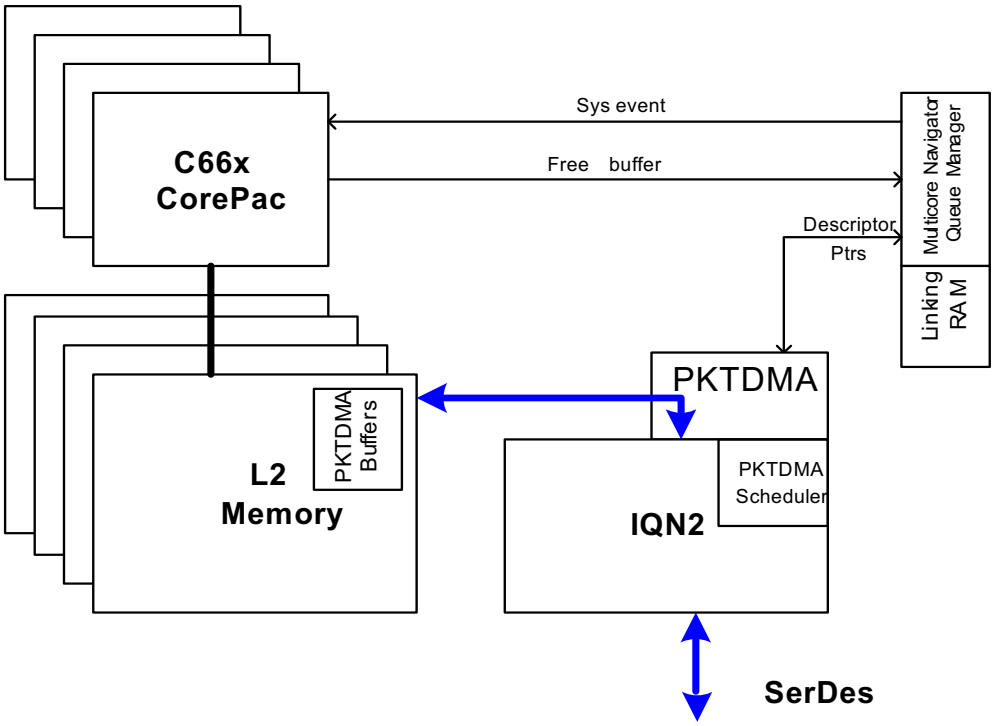
The DIO module controls the WCDMA IQ data coming from and going to the PSI bus with minimum latency. The DIO also implements RSA (RAC WCDMA UL format) Data Format Conversion for both the Ingress and Egress directions.

6.3 PKTDMA

Multicore Navigator is a methodology and a series of hardware accelerator modules that allow DSP cores and peripherals to effectively transfer packets. It is a safe and managed way that memory can be used to pass data. The Multicore Navigator hardware accelerators decouple DSP cores from the actual transfers elevating what would otherwise be a heavy interrupt and MIPS burden from the DSP core.

Multicore Navigator hardware accelerators use the VBUS infrastructure to implement DMA movement and Queue maintenance. The PKTDMA connection to VBUS is a VBUSM master port and for IQN2, the PKTDMA connection is 128 bits wide.

Figure 6-5. IQN2 Multicore Navigator



The DSP host allocates blocks of memory and configures the Multicore Navigator hardware to utilize the memory region. A key aspect of the Multicore Navigator solution is that the memory is broken up into small grain buffers that are linked listed together via the Multicore Navigator hardware creating virtually any size packets. This approach utilizes the memory space very efficiently minimizing “white space” overhead. While the processing burden of this linked list approach is significant, much of it is performed in hardware accelerators minimizing any impact on DSP MIPS or peripherals.

There is a trade-off when choosing the buffer size. Small buffers give finer grain usage of memory, but may require more buffers to be linked together to store a packet (creating more overhead in storing/retrieving packets). Larger buffer size would require fewer buffers, but the last buffer in a linked list is likely to be only partially full (wasting memory).

Multicore Navigator has a large degree of flexibility. Some applications are not tolerant to breaking up packets into multiple buffers. For these applications, Multicore Navigator has an alternate operation where only a single fixed size buffer is used per packet. Clearly the buffer size needs to be chosen in advance to handle the largest possible packet size. (Each memory region supports only one buffer size.)

Figure 6-6. Multicore Navigator Host Mode Example

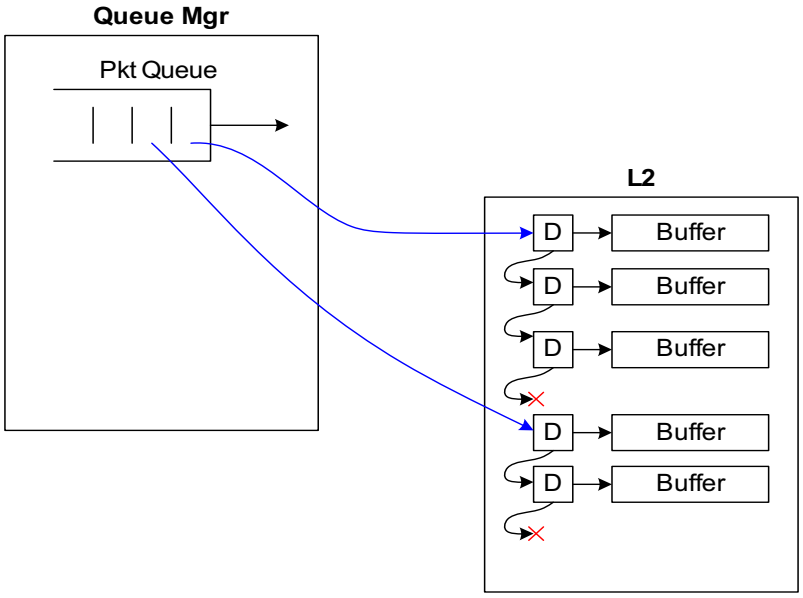
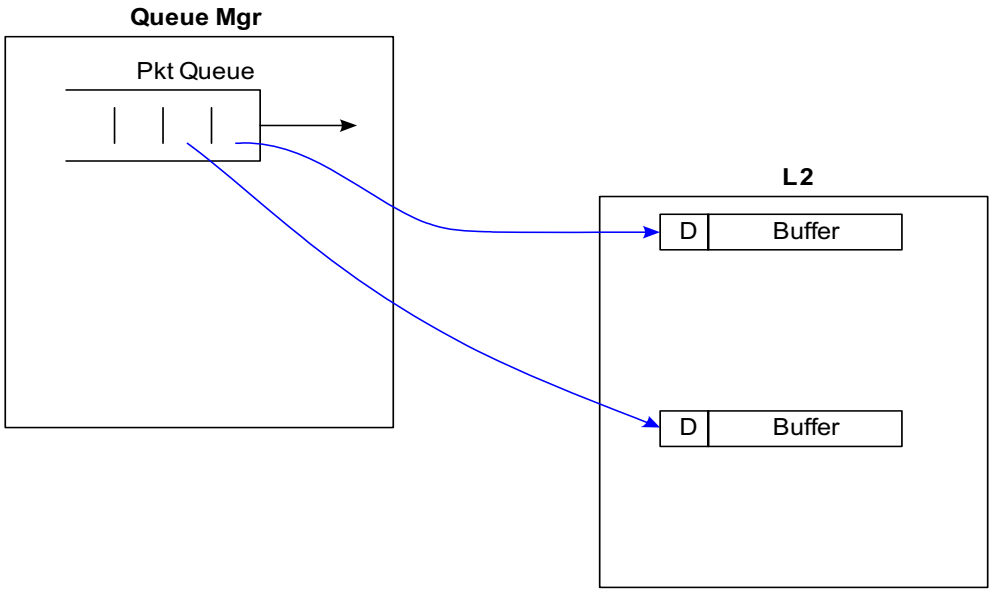


Figure 6-7. Multicore Navigator Monolithic Mode Example



6.3.1 Multicore Navigator Buffers and Descriptors

Multicore Navigator includes the concept of Buffers and Descriptors:

- **Buffers**: Buffers hold raw data. The CorePac core allocates a region of memory for buffers and the CorePac core dictates the fixed size for all buffers in this memory region. Multicore Navigator can support multiple memory regions, but each region can support only one buffer size. (Monolithic mode will use exactly one of these buffers per packet. Host mode can use one or more buffers chained together in a linked list.)
- **Descriptors**: Descriptors are a form of packet header or buffer header which contains information specific to Multicore Navigator. Pointers to buffers (differing from linked list) are contained in Descriptors as well as many other useful fields both for software and the PKTDMA engine. Descriptor fields vary depending on the Multicore Navigator packet type being supported:
  - **Host Mode Descriptor:** As well as other information, holds an additional pointer to the “next” Host

Mode Descriptor in the packet (forming a linked list). The Descriptor and Buffer are separate entities stored in separate areas of memory.

– **Monolithic Mode Descriptor:** Descriptor and Buffer are merged into one contiguous portion of memory (basically, the Buffer contains the Descriptor in the first n words). PKTDMA is aware of the offset between descriptor and beginning of payload.

NOTE: AxC & Packet Tx Buffers must be in same memory region. All traffic for a given IQN2 egress DMA channel must be sourced from the same memory region (i.e., the same L2). The issue which is being avoided is re-ordering of VBUS read requests due to different memory targets. Assume that there are back-to-back memory requests for a single AxC where the first memory read is for a highly loaded L2 and the 2nd memory read is for a lightly loaded L2. PktDMA is a high speed interface and will pipeline issue these read requests prior to the first read request receive data. If the latency of the first read is higher than the pipelined issue and round trip return of the 2nd read request, the data will be presented out of order to the IQN2. This would corrupt the traffic for that AxC, possibly scrambling the order of up to 32 consecutive samples. This is not an issue for consecutive requests to the same memory region as all consecutive requests will be returned in order even if read requests experience stalls.

6.3.2 Multicore Navigator Queues

Queues are at the heart of the Multicore Navigator concept. There are several types of Multicore Navigator Queues.

- **Free Queue**: At the time of initialization, all Descriptor/Buffer pairs are pushed onto a Free Queue. Each memory region should be given its own Free Queue. As Descriptor/Buffer pairs are allocated, they are popped off the Free Queue. When Descriptor/Buffer pairs are no longer needed, they are deallocated by popping off the appropriate queue and pushing them onto the Free Queue.
- **Receive Queues**: Receive and Transmit Queues are packet queues that are used for scheduling PKTDMA transfers. Multiple Queues are useful to implement a Priority scheme. When the host receives an interrupt from PKTDMA that a packet has arrived and populated Receive Queue, the host will pop packets from the receive queue for processing and the receive queue could be popped into Free Queue for recycling. (This should be done by the host. PKTDMA will not do this automatically.)
- **Transmit Queues**: The host Pushes Packets on a Transmit Queue for DMA and PKTDMA will automatically recycle the queue when the packet is fully transferred.

When App software shuts down a channel, there could be residual packet data in the Multicore Navigator buffers for that channel. AIL will stop generating Multicore Navigator packet data once the AxC is disabled, but if the App software stops reading this Multicore Navigator traffic, it would be the responsibility of the software to move all the descriptor pointers to a free queue.

6.3.3 Multicore Navigator and DIO Scheduling

The arbitration scheme allows for programmable priority between the following:

- Multicore Navigator Traffic
- Direct IO Traffic

When only one form of traffic has pending data, that traffic is serviced. If both forms of traffic have pending data, the state of the MMR bit indicates which one will be serviced. The higher priority traffic is serviced exclusively until all pending data is transported, then and only then is the other form of traffic serviced.

For the two different modes of DMA, the scheduling is performed in a very different way:

- Direct IO: An internal system event from uAT triggers the DIO FSM to burst transfer all DMA activity programmed into the engine.
- Multicore Navigator: Data transfer is scheduled based on the PHY rate of data reception/transmission.

6.3.4 Multicore Navigator Packet Types

Multicore Navigator is extremely general and flexible; the intended use of IQN2 is to use Multicore Navigator in a very specific and limited way, using only two Multicore Navigator packet types:

- Monolithic: Used for {LTE, WiMax, TD-SCDMA, GSM} Antenna data and Control data
- Host: Used for {Control data, Generic packet, Ethernet} traffic that requires a large data buffer

NOTE: It is possible to use Host Mode for antenna traffic instead of Monolithic. If this is desired, please be aware the Host Mode has more descriptor fetch overhead than Monolithic. Make sure that system performance will not suffer.

NOTE: The Monolithic Descriptor type has a variable length. IQN2 uses only a 12-byte descriptor (with an optional four bytes of protocol specific) in order to keep the Descriptor VBUS overhead to one bus cycle.

The Host mode packets are the most general and widely used packet (in other IP peripherals) as it handles variable packet length by chaining *n* buffers together in a linked list fashion. Clearly, if the packet does not completely fill the last buffer, the unused area is wasted. Host mode descriptors are separate from the buffers where each descriptor contains a pointer to a data buffer and a second pointer to the next descriptor in the linked list.

Host mode has a lot of performance overhead with many descriptor and pointer operations. In Host mode, the first descriptor is known as the packet descriptor and only this descriptor is placed on a transport (DMA) queue in the QM.

During configuration, the Host is responsible to prelink Host Mode descriptors and buffers by writing a buffer pointer to each descriptor. After this operation, all descriptors are placed on a free queue. Once on a free queue, Multicore Navigator can randomly assign buffers as needed, performing memory management.

At the time of configuration, it is the responsibility of the user to program how much memory to allocate and how large the buffers should be. If the buffers are too large, then the memory is not used efficiently. If the buffers are too small, there is a higher performance overhead for increased linking operations.

The Monolithic packet type is mainly envisioned for the purpose of passing OFDM symbol data. It is designed for maximum performance in both clock cycles and memory utilization.

Multicore Navigator Monolithic packet types have the descriptor and buffer concatenated in one contiguous memory buffer. Because the descriptor and buffer are in contiguous memory, the PKTDMA operations are simplified when addressing memory. Monolithic packet types do not support linked list chaining and therefore must be sized correctly to accommodate the largest possible packet.

The Monolithic packet descriptor header for IQN2 is exactly 16 bytes (one VBUS 128 data phase). Many of the fields are required by Multicore Navigator, and some of the remaining bits (4 bytes) are allocated for protocol specific use. The Monolithic packet type uses some of the protocol specific bits for Radio Standard specific information:

- Ingress/Egress selection
- AxC number
- Symbol Number (or GSM timeslot number)

In the special case of GSM Base Band Hopping where App software is assigning OBSAI address to Control Packets, the protocol specific word contains:

- OBSAI address (13 bits)

In the special case of GSM Base Band Hopping where App software is assigning full OBSAI header to Control Packets, the protocol specific word contains:

- OBSAI address (13 bits)
- OBSAI type (6 bits)
- OBSAI time stamp (5 bits)

Packets that are sourced by the CorePac core are expected to have the Multicore Navigator descriptors properly populated. IQN2 requires the CorePac to fill in {Ingress/Egress, AxC num, Symbol num} fields for transmit AxC packets. IQN2 PSR will check and fail packets that do not match expected timing. If the AxC num and Symbol num are not matched with the expected timing, the AIL link will be halted until the end of the Radio frame.

FFTC or any other operations after CorePac core that creates packets are expected to maintain these protocol-specific fields of information as IQN2 requires this metadata. The PKTDMA Tx configuration register has a special bit field called AIF_MONO_MODE. This bit should be set to one if the user wants to use four bytes protocol specific field.

NOTE: It is possible for the FFTC to send output packets directly to the IQN2 without any DSP intervention. In that case, the AIF_MONO_MODE should be turned off and FFTC uses a descriptor size field of 16 bytes as normal mode, because FFTC cannot set 64 bytes to DESC_SIZE field before pushing the descriptor into the IQN2 TX queue.

PKTDMA loopback mode also should be disabled because the default value is loopback enable. The PKTDMA emulation control register in the Global control register region has this bit field.

In the event that Monolithic is used for non-AxC data, IQN2 will fill Egress protocol specific fields with zeros and Ingress protocol specific fields will be disregarded.

At time of Configuration, the user should choose the smallest Monolithic packet to fit the OFDM Symbol or GSM timeslot. Monolithic packets can be allocated in $n \times 16$ bytes. Choose the size to be the symbol size plus 16 bytes for descriptor header (rounded up to the nearest 16 bytes). For LTE, the first, largest symbol size should be chosen.

The following tables show examples of monolithic descriptor fields.

Table 6-1. Monolithic Packet Descriptor Word 0

Bits	Name	Description
31-30	Packet ID	Monolithic packet descriptor type. Value is always 2 (0x02) for monolithic descriptors.
29-25	Packet Type	This field indicates the type of this packet and is encoded as follows: 0-31 = To Be Assigned by User
24-16	Data Offset	This field indicates the byte offset from byte 0 of this descriptor to the location where the valid data begins. On Rx, this value is set equal to the value for the SOP offset given in the Rx DMA channel's monolithic control register. When a monolithic packet is processed, this value may be modified in order to add or remove bytes to or from the beginning of the packet. The value for this field can range from 0-511 bytes, which means that the maximum NULL region can be 511-12 bytes, because byte 0 is the start of the 12-byte packet info area. Note that the value of this field must always be greater than or equal to four times the value given in the Protocol Specific Valid Word Count field. Set to 0x10 for IQN2 (16 bytes)
15-0	Packet Length	The length of the packet in bytes. The valid range is from 0 to 65536 bytes.

Table 6-2. Monolithic Packet Descriptor Word 1

Bits	Name	Description
31-24	Source Tag - Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field as specified in the rx_src_tag_hi_sel field in the flow configuration table entry.
23-16	Source Tag - Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field as specified in the rx_src_tag_lo_sel field in the flow configuration table entry. Normally, this field is used as an index of Rx flow.
15-8	Dest Tag – Hi	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field as specified in the rx_dest_tag_hi_sel field in the flow configuration table entry. Not used for IQN2.
15-0	Dest Tag - Lo	This field is application specific. During Packet reception, the DMA controller in the port will overwrite this field as specified in the rx_dest_tag_lo_sel field in the flow configuration table entry. Not used for IQN2.

Table 6-3. Monolithic Packet Descriptor Word 2

Bits	Name	Description
31	Extended Packet Info Block Present	This field indicates the presence of the Extended Packet Info Block in the descriptor. • 0 = EPIB is not present (set zero for IQN2) • 1 = 16-byte EPIB is present
30	Reserved	
29-24	Protocol Specific Valid Word Count	This field indicates the valid # of 32-bit words in the protocol specific region. For IQN2, this should be 1. This is encoded in increments of 4 bytes as follows: • 0 = 0 bytes • 1 = 4 bytes • … • 16 = 64 bytes • ... • 32 = 128 bytes • 33-63 = Reserved
23-20	Error Flags	This field contains error flags that can be assigned based on the packet type. Not used for IQN2.
19-16	Protocol Specific Flags	This field contains protocol specific flags / information that can be assigned based on the packet type. Not used for IQN2.
15	Reserved	
14	Return Push Policy	This field indicates how a Transmit DMA should return the descriptor pointers to the free queues. This field is encoded as follows: • 0 = Descriptor must be returned to tail of queue • 1 = Descriptor must be returned to head of queue This bit is only used when the Return Policy bit is set to 1.
13-12	Packet Return Queue Mgr #	This field indicates which of the four potential queue managers in the system the descriptor is to be returned to after transmission is complete. This field is not altered by the DMA during transmission or reception and should be initialized by the host.
11-0	Packet Return Queue #	This field indicates the queue number within the selected queue manager that the descriptor is to be returned to after transmission is complete.

Table 6-4. Monolithic Packet Descriptor Word 3 (Protocol Specific Info)

Bits	Name	Description
31-16	Reserved	
15	Ingress/Egress	0 = Ingress 1 = Egress
14-7	Symbol Number	Symbol number (0x00 – 0xFF)
6:0	AxC Number	AxC number (0x00 – 0x7F)

Table 6-5. Monolithic Packet Descriptor Word 3 (Protocol Specific Info Alternate Mode for OBSAI Address Only)

Bits	Name	Description
31:16	Reserved	
15	Ingress/Egress	1 = Egress Only
14:13	Reserved	
12:0	OBSAI address	13-bit OBSAI address that will be inserted in OBSAI header for GSM frequency hopping

Table 6-6. Monolithic Packet Descriptor Word 3 (Protocol Specific Info Alternate Mode for Full OBSAI Header)

Bits	Name	Description
31:24	Reserved	
23:11	OBSAI address	13-bit OBSAI address that will be inserted in OBSAI header for GSM frequency hopping
10:5	OBSAI type	6-bit OBSAI type that will be inserted in OBSAI header for GSM frequency hopping
4:0	OBSAI time stamp	5-bit OBSAI time stamp that will be inserted in OBSAI header for GSM frequency hopping

6.4 Multicore Navigator Examples

QM: Multicore Navigator Queue Manager

Packet DMA: PKTDMA Controller

6.4.1 Ingress (IQN2 Reception DMA-to-L2 RAM)

- CorePac Initializes Multicore Navigator (PKTDMA, QM)
  - Buffer Allocated
    - The CorePac core allocates a portion of L2 memory for data sharing between the IQN2 and CorePac.
    - The CorePac programs Multicore Navigator hardware accelerators with the location and size of these buffers.
  - Monolithic and Host Descriptors filled out (Initialized)
    - CorePac core writes a link-pointer in each descriptor pointing to its associated buffer
  - Queue Manager notified of all available resources
    - Buffer region, number of buffers, and buffer size are programmed into queue manager
  - Free Descriptor Queue filled with all Descriptors
    - Free Queue is a virtual queue inside queue mgr. (shared)
    - Free Queue is implemented with Linking RAM as are all other Queues
    - CorePac writes all descriptors addresses to Free Queue essentially “pushing” them onto the queue
  - Enable PKTDMA Rx, Tx channels, and disable loopback mode
    - Enable each Rx or Tx channels with AIF_MONO_MODE option in case of OFDM.
    - Disable PKTDMA loopback mode.
    - Enable PKTDMA Rx, Tx channels should be executed after IQN2 sub-module (AIL, AID, DIO) channels are enabled. (different from AIF2 operation)
- **IQN2 starts receiving** packet over OBSAI or CPRI interface
  - Multicore Navigator/IQN2 DMA Scheduler
    - Once a programmable number of bytes are in the IQN2 buffer, IQN2 DMA Scheduler passes a “credit” to PKTDMA controller.
    - Each DMA Channel has a default Rx Queue that will be the next destination of the packet.
    - IQN2 Scheduler has an internal queue of “credits” indicating a requested DMA transfer, the

channel number, and number of bytes to be transferred.
- IQN2 has several categories of packets that are managed. Each category has its own FIFO and is considered a Multicore Navigator channel.
- IQN2 will usually request 64-byte transfers.

– PKTDMA Control
- If SOP, PKTDMA read (fetch from QM) descriptor over VBUS
- (QM) allocates a descriptor for the new packet
  - This is considered a “packet descriptor” (being the first descriptor per packet)
  - For large packets, multiple descriptors are allocated. Subsequent descriptors are simply called descriptors and also requested by Packet DMA (PKTDMA).
- (PKTDMA) writes to Descriptor (in L2). Fills in Descriptor with information about Packet.
- (PKTDMA) Reads pointer to buffer (from Descriptor in L2)
- (PKTDMA) Writes data to data buffer

– PKTDMA transfers data
-
- DMA reads data across Multicore Navigator FIFO I/F (similar to VBUS)
- If packet is larger than a single buffer, QM and PKTDMA work together to:
  - Assign a new descriptor
  - Link list, link the new descriptor to the old descriptor
  -
  -
  - DMA the partial packet FIFO data to the new buffer
- If EOP, Write descriptor contents
  - (PKTDMA) writes Descriptor to Packet Queue
  - (QM) create system event

- CorePac
  – CorePac either polls or waits for interrupt from system event
  – CorePac reads “Packet Queue”
  – Pointer to descriptor
  – Either reads Descriptor, or for monolithic skips header and uses data
  – Host Mode… CorePac will follow links in Descriptors…
  – When CorePac is done with packet
    - CorePac navigates Packet Linked List
    - Writes Descriptors to Free Queue for recycle.

6.4.2 Egress (L2 RAM DMA-to-IQN2 Transmission)

This section is abbreviated. See Ingress example for greater detail.

- CorePac Initializes Multicore Navigator
- CorePac packet create
  – CorePac pops descriptors from Free Queue
  – CorePac fills in descriptors and buffers, popping and filling new descriptors as needed.
  – CorePac fills in first SOP descriptor and pushes onto Transport Queue
- IQN2 DMA Scheduler controls PKTDMA to transfer packet
  – QM gives IQN2 a constant status of queue not_empty for each of 48x queues
  – Scheduler monitors IQN2 output buffer depth, if space available
  – If EOP, Scheduler indicates EOP and number of bytes in last transfer

- PKTDMA performs transfer
  - PKTDMA fetches Descriptor address from QM
  - PKTDMA fetches Descriptor from L2
  - PKTDMA (uses Buffer Address from Descriptor) fetches Buffer from L2
  - PKTDMA writes Buffer info to IQN2 input buffer
  - As Buffer boundaries are encountered (for Host Mode)
    - PKTDMA will push freed descriptors/buffers onto Free Queue for recycle
    - PKTDMA use link in descriptor to fetch next descriptor in linked list
  - As EOP is encountered PKTDMA will close out packet

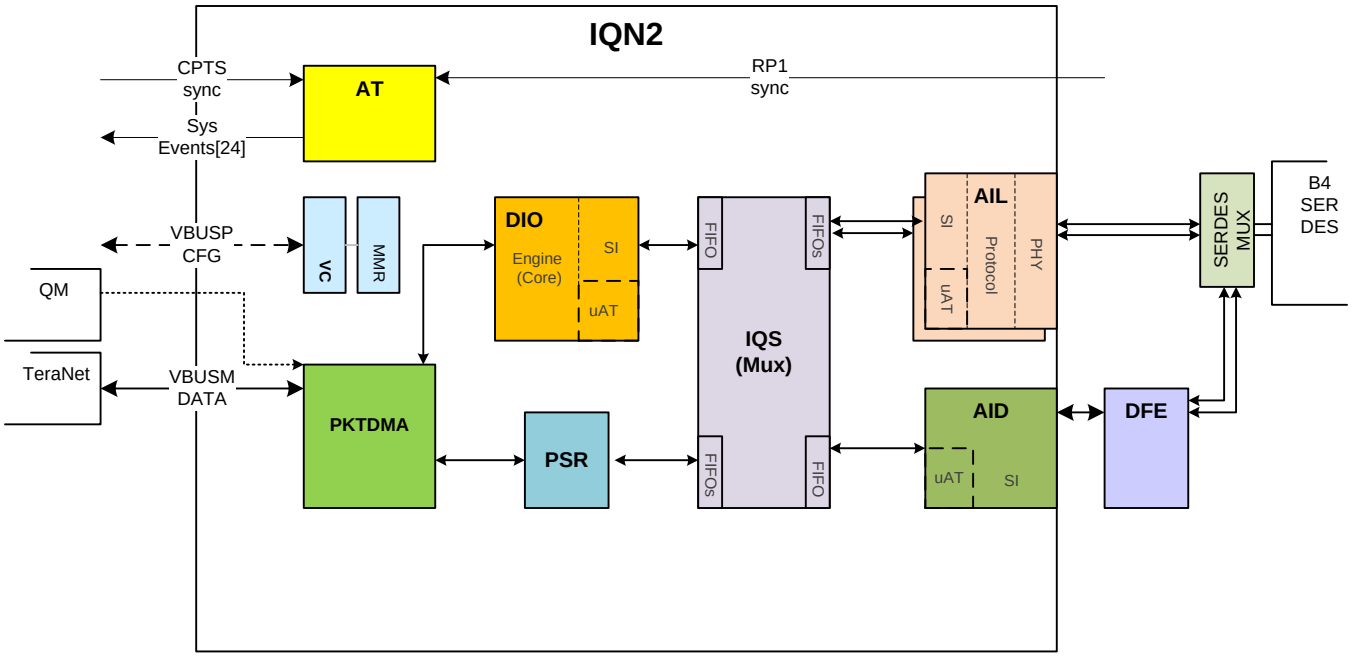
Implementation Details and Application for Sub-Modules

Topic **Page**

7.1 IQN2 Top

Figure 7-1 shows the top level IQN2 internal hardware architecture.

Figure 7-1. IQN2 Top Level Block Diagram



Key High-Level Features:

- VBUSM DATA connection
  - VBUS_CLK (CPU_CLK/3)
  - connection is to the PktDMA
- 2x VBUSP CFG
  - VBUSP CFG0 (IQN2):
  - VBUSP CFG1 (DFE):
- Number of channels supported (Ingress + Egress)
  - (48 + 48) PktDMA channels
  - (68 + 68) Each AIL
  - (16 + 16) DIO2
- PktDMA
  - (48 + 48) channel support
    - allocation between Control and AxC is soft/flexible
- AID
  - (32 + 32) AxC channels
  - (16 + 16) Control Channels
- AIL(2x)
  - OBSAI
    - (64 + 64) any AxC/Ctrl mixture channels
    - link rates {2x, 4x, 8x}
  - CPRI
    - (64 + 64) AxC channels
    - (4 + 4) control channels

    - link rates {2x, 4x, 5x, 8x, 10x, 16x}
  - Allows link-to-link PHY level forwarding (defined in OBSAI/CPRI)
  - PHY reset isolation
- AT
  - 24 System Events
  - 1 BCN counter and 8 complex RADT (Radio Timers)
  - Timing Sync Sources {RP1, generic input pins, CPTS(10gE), SW}
- DIO
  - Core (Engine, VD): DIO engines + VBUS DMA controller
  - 3 DIO engines
    - Up to 3-way Ingress multi-cast
    - Each engine independently programmed DMA profile, Each engine can have different burst length and SOC addressing scheme
- IQS
  - DMA-to-Peer & Peer-to-DMA mapping only
- PSR/Flush Controller
  - Provides packing/unpacking of PSI PS_DATA
  - Provides peer requested flush of packets from the PKTDMA. Flushes packets to the PKTDMA if a PKTDMA channel is over full.
  - limits VBUS peak BW during packet Flush
- VC(VBUS CFG)
  - Top Level MMRs
- SERDES 2:1 Mux (share AIL SERDES w/DFE) is done at chip level (not in IQN2)

7.1.1 Chip level IO mapping and Clock

Table 7-1 describes the clocks required for IQN2.

Table 7-1. Clocks

CHIP Pin Name	Frequency	Description
sys_clk	307.2 MHz (OBSAI and CPRI 5x, 10x), 245.76 MHz (CPRI)	This is used in symbol rate processing of IQ data and AT/uAT timers use this clock as a counter unit. CPRI 16X gets a 491.4 MHz txbclk. It is divided by 2 in the AIL and used to drive all other internal AIL logic and selected as sys_clk for IQN2 logic outside of AIL. In modes other than CPRI 16X, the txbclk input is used unchanged, without the clock divider in AIL.
vbus_clk	CPU/3	Typically 400MHz, could be as low as 233MHz
rp1_clk	30.72 MHz	This clock is only used for OBSAI RP01 clock source. This clock comes from an external LVDS device pin pair.
dfe_sys_clk	245.76MHz, 368.64MHz	This clock comes from an external PLL which drives DFE. This clock is derived from the same source which drives the reference clock for the JESD SERDES.

The VC_CLKCTL_SYSCLK_SEL_CFG register has AT_DFE_CLK_SEL and SYSCLK_SEL field. if AT_DFE_CLK_SEL is set, it selects dfe_sys_clk as a clock source of ATand uAT instead of IQN2 sys_clk. This is only valid when DFE is used but AIL is not used. Remember AID always uses def_sys_clk for its sys_clk area operation.

When IQN2 AIL is used, the SYSCLK_SEL field, bits 0 and 1 are used to select which SERDES txbclk is used for the IQN2 internal system clock (sys_clk). Bit 2 is set when selecting the divide-by-2 txbclk in CPRI 16X mode. Otherwise it will be 0. The AIL PHY section further describes the SERDES clocking when using the AIL.

Example 7-1. KeyStone II SerDes Link Rate Configuration Example:

```
OBSAI(2x,4x,8x) and CPRI5x,10x: Use 6.144GHz SerDes configuration
TX : Full rate
RX : Full rate for 8x and CPRI 10x,
Half rate for 4x and CPRI 5x,
Quad rate for 2x
CPRI(2x,4x,8x): Use 4.9GHz SerDes configuration
TX : Full rate
RX : Full rate for 8x,
Half rate for 4x,
Quad rate for 2x
CPRI 16x: Use 9.8GHz SerDes configuration
TX : Full rate
RX : Full rate
and Set SYSCLK_SEL bit[2] in VC_CLKCTL_SYSCLK_SEL_CFG register
CPRI 8x,4x lane when 9.8GHz SerDes configuration used:
TX : Half rate
RX : Half rate for 8x,
Quad rate for 4x,
and Set SYSCLK_SEL bit[2] in VC_CLKCTL_SYSCLK_SEL_CFG register
```

7.1.2 SerDes Serial Bit Ordering

The serial coding provides the 20-bit encoded symbol to the SerDes module such that it follows the bit order defined for both the OBSAI RP3 and CPRI standards. These bit orderings for each 10 bits of the 20-bit pair are shown in the following figures. The SerDes module expects that the first bit transmitted or received is bit 0 of the parallel interface of the module.

Figure 7-2. OBSAI Serial Bit Ordering

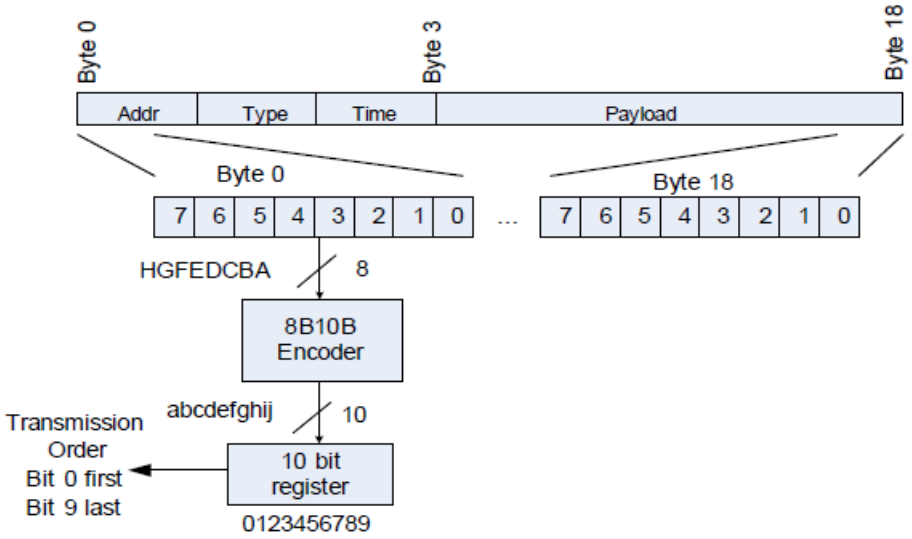
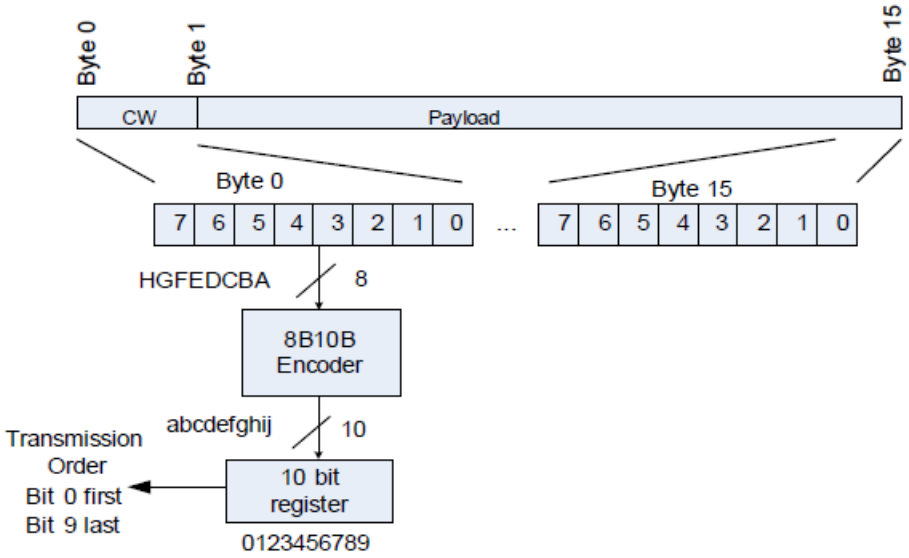


Figure 7-3. CPRI Serial Bit Ordering



NOTE: SerDes module information for KeyStone II devices is not provided in this user guide. See KeyStone II SerDes User Guide on the device product web page for more information.

7.1.3 PSR (PS Reformatter)

The PSR module reformats PS data between PKTDMA PS data transfers and the IQN2 internal INFO word under MMR control. Packets in the Egress direction may pack the PS data word from the PKTDMA needed for AxC data into the INFO word. For Ingress, it can take the INFO word and transfer to the PKTDMA as a PS_DATA.

Flush (for Failed Packet from PKTDMA) in the Egress direction is done if requested by the Egress peer (AIL or AID), because PKTDMA cannot flush the error packet for itself. If this flush is not done correctly for the error packets, it may cause serious memory problem like losing descriptors. In either direction, the flush function drops all data for a channel until the next SOP is seen. BW limiting (by MMR) is provided on the Egress path to minimize the effect on the system VBUS.

Egress data is read from the PKTDMA with packets that may or may not contain PS data. An MMR will indicate if that PKTDMA channel will have a PS _DATA word available in the cycle after an INFO word. If there was no PS_DATA expected, only the INFO word would be loaded. If a peer indicates a channel needs to be flushed, data from that channel is dropped until an SOP is seen. Flush transfers will have lower priority than all other AxC or packet data transfers and will be bandwidth limited based on an MMR setting.

7.1.3.1 Configuring the Flush Rate

The IQN2 needs to limit the BW used during flushes. The flush rate algorithm is based on VBUS utilization within a 16-clock cycle window. When a flush transfer starts, a state machine starts which allows a selectable number of transfers to be made at certain times over the following 16 cycles. The available transfer times are spread as evenly as possible over the 16 cycles so if four cycles are allowed over 16 cycles, the accesses are spaced four cycles apart from each other rather than four back-to-back followed by 12 unusable cycles. Normal data transfers have priority over flush transfers so if both are possible on a clock cycle the flush transfer is ignored.The **PSR_EGR_CFG.BW_LIMIT** selects the rate with a value of 0 allowing one transfer every 16 cycles.

With a VBUS clock at 400 Mhz, the maximum data rate of the VBUS is 51 Gbit/second. We want to flush at a higher rate than the normally-used data rate on the bus, but not so fast as to cause problems in other parts of the system. The percentage bandwidth of flush should be set based on the percentage of the bus expected to be in non-flush operation and the estimated available bandwidth based on the system level VBUS utilization.

If a system is configured to support 6Gbit of traffic, that is 12 percent of the entire VBUS throughput. Due to activity in the other parts of the chip, we may be limited to the use of a peak bandwidth of 9Gbit which gives us a maximum rate of 1.5 times the normal operating bandwidth. This is 3/16 of the full VBUS bandwidth so we would set the **PSR_EGR_CFG.BW_LIMIT** to a 2 so there are three possible transfers every 16 cycles. In a larger system that supports a 12Gbit bandwidth, we would need a higher number to just match the average bandwidth, a setting of 3 which means four possible transfers every 16 cycles (12Gbit) gives just enough for this bandwidth, if no additional BW is allowed from the system.

Also assume all other activity leaves very little available bandwidth on the above examples, such as only 5Gbit is unused. Since each 1/16 of the VBUS bandwidth is 3Gbit, then we would set a value of 0 in the register which is one transfer every 16 cycles.

7.1.4 VC (VBUS CFG)

Table 7-2. Memory Map of Register Region Addresses

Module	Sub-module	IP Level Address	Sub-Module LevelAddress
Top			
	VC MMR	0x00_0000	0x00_0000
	EE	0x00_4000	0x00_4000
	PSR	0x00_8000	0x00_8000
	IQS	0x02_0000	0x02_0000
AT2			
	AT MMR	0x01_0000	0x00_0000
	AT EE	0x01_8000	0x00_8000
AID2			
	SI sysclk	0x04_0000	0x00_0000
	SI vbusclk	0x04_8000	0x00_8000
	EE sysclk	0x05_0000	0x01_0000
	EE DFE	0x05_1000	0x01_1000
	EE vbusclk	0x05_2000	0x01_2000
DIO			
	SI sysclk	0x06_0000	0x00_0000
	SI vbusclk	0x06_8000	0x00_8000
	DIO mmr	0x07_0000	0x01_0000
	DIO EE	0x07_8000	0x01_8000
PktDMA			
	gcfg	0x10_4000	0x00_0000
	tcfg	0x10_6000	0x00_2000
	rcfg	0x10_8000	0x00_4000
	txs	0x10_A000	0x00_6000
	rflow	0x10_C000	0x00_8000
AIL_0			
	SI sysclk	0x20_0000	0x00_0000
	SI vbusclk	0x20_8000	0x00_8000
	PE	0x22_0000	0x02_0000
	PD	0x22_8000	0x02_8000
	PHY	0x23_0000	0x03_0000
	EE vbusclk	0x23_2000	0x03_2000
	EE sysclk	0x23_4000	0x03_4000
AIL_1			
	SI sysclk	0x24_0000	0x00_0000
	SI vbusclk	0x24_8000	0x00_8000
	PE	0x26_0000	0x02_0000
	PD	0x26_8000	0x02_8000
	PHY	0x27_0000	0x03_0000
	EE Vbus	0x27_2000	0x03_2000
	EE Sys	0x27_4000	0x03_4000

7.1.4.1 Reset

The VC_SW_RESET_STB MMR gives the programmer the ability to reset specific sections of the IQN2. The SW reset feature typically is used in initial bring-up and debug, not typically in normal operation.

The following endpoints will each have one bit associated with its software reset:

- AIL_0: PHY & PROTO/DMA
- AIL_1: PHY & PROTO/DMA
- AIL_2: PHY & PROTO/DMA
- AIL_3: PHY & PROTO/DMA
- AID
- DIO
- PktDMA
- SW RESET resets all of the above with one bit.

Great care must be taken when implementing RESET. It has always been possible to hang the VBUS_DATA or VBUS_CFG. Importantly, it is possible to hang the PktDMA with a partial reset of either AIL0/1 or AID. So, care must be taken not to create a serious situation, and to bring down links gracefully. (Stop traffic and shutting down channels first.)

7.1.4.2 Power Gating & Reset Isolation

Power Gating, Known Use Cases :

- DFE-only operation: In this use case, the dual AIL sub-chip is not used and power gated OFF
- AIL-only operation: The DFE is power gated OFF.
- SOC Deep Sleep (AIL use): For BTS overnight power savings, some SOCs in the daisy chain are put into extremely low power state and not contributing to the OBSAI/CPRI daisy chain. During this operation, only the AIL sub-chip is power gated ON while most of the remaining SOC is power gated OFF (DFE is also power gated OFF). IQN2_TOP is power gated ON, although the VBUS clock may be turned off. The AIL_PHY remains active to prevent crashing the OBSAI/CPRI daisy chain. Prior to waking up the SOC, it is likely that an isolated HW reset is performed on the SOC omitting a HW reset to the AIL_PHY.

Reset Isolation :

In IQN2 there is a need to allow for the AIL PHY to remain up and running while the remainder of the IQN2 is reset after recovering from a deep sleep (overnight power savings for example).

IQN2 has two separate HW reset pins. One input is used for resetting non-isolated hardware and the other input is used for resetting all hardware including non-isolated and isolated. Control of these pins is exercised through a low-power sleep controller (LPSC) outside of IQN2.

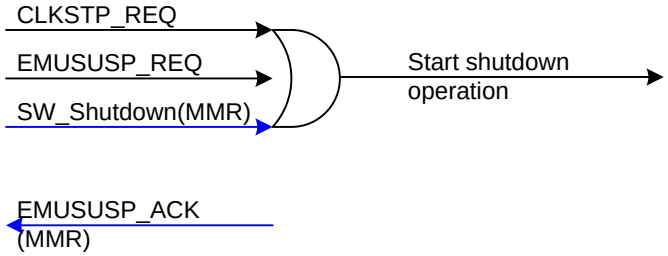
To simplify the design, the entire AIL is on the reset isolation area. The reason for this is that the Micro AT is instantiated in parts of the AIL which are not easily separated from the PHY vs. Protocol. The Micro AT must still be up and running while the PHY is running. The AT must also be up and running during PHY operation since it is the main time keeper. The VC MMRs are also on the reset isolation area, since it controls the clock selection, reset, and some of the SerDes related functions.

The SerDes logic must also be controlled externally by the LPSC to be treated as isolated logic. The user is required to gracefully shut down all IQN2 channels and DMA traffic prior to resetting the device.

7.1.4.3 Shutdown Controller (SC)

The shutdown controller orchestrates clock-stop-request and emulation-suspend. While from the user's perspective, these are two different mechanisms. From the perspective of the IQN2, CLKSTP and EMUSUSP are handled nearly identically. For both of these mechanisms, IQN2 shuts down DMA and Protocol layer traffic as cleanly as possible.

Figure 7-4. Conditions That Start Shutdown



The shutdown process is started when either the external clock stop REQ or the emulation suspend signal to the IQN2 is asserted, or if a FRC_SHUTDOWN from a VC MMR is set. The SC is in essence the master shutdown controller which orchestrates shutdown operations between all sub-modules. Most subsystems have a slave shutdown controller which orchestrates the smaller grain shutdown operations contained within that sub-module.

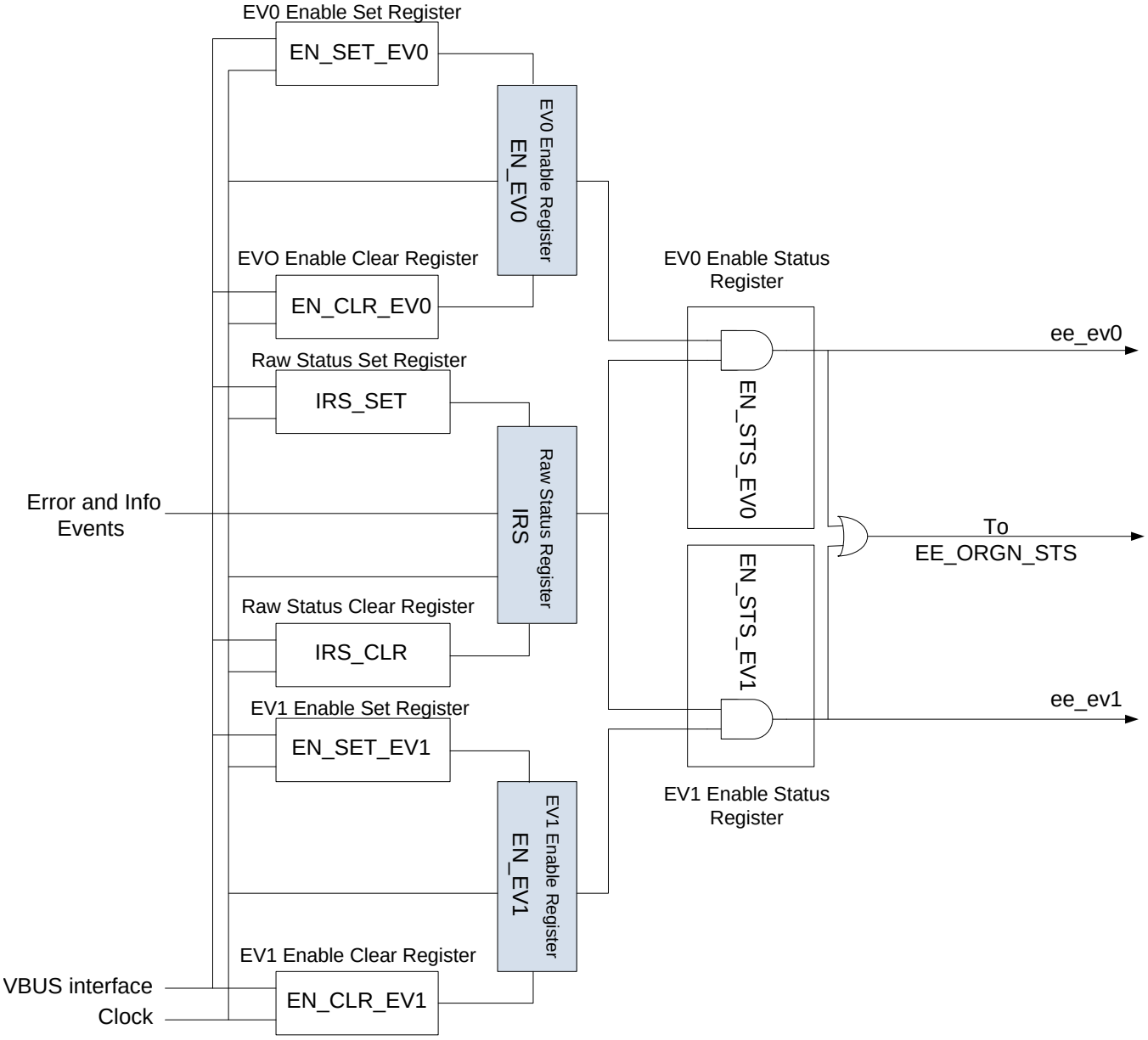
7.1.5 EE Methodology & Implementation

The IQN2 EE is comprised of two major components. The EE Handler provides event enable registers (mask registers) and a Status “register” that indicates the status/origination (ORGN) of the enabled events. Also provided is the EOI register and write pulse logic required by the INTD to create a pulsed interrupt. The enabled events are aggregated (ORed) down to a single, active high-level event. There are two identical versions of these sets of registers in order to be able to generate independent interrupts that may contain a different “mix” of masked events.

The INTD is a Highlander 0.1 compliant, Interrupt Distributor. This component accepts active high-level events from the EE Handler and creates a pulsed interrupt in conjunction with the EOI logic. This pulse is stretched, as needed, for the host and synchronized to the host clock.

Each IP module provides two active high-level outputs that are a selection of error or info events from that IP. Figure 7-5 shows event handling and interrupt generation at the Top IQN2 level.

Figure 7-5. Top Level Exception Event Handler and Interrupt Generator



7.1.5.1 EE Handler

For each interrupt path (EV0 and EV1), there is a separate set of origin (ORGN) status registers. This is equivalent to the Interrupt Vector (*intr_vector*)

End of Interrupt Register (**EOI**)

- The End of Interrupt Register allows the software to acknowledge the servicing of a handshake interrupt so that another interrupt can be generated. Software should clear the interrupt, using the Interrupt Clear Shadow Register.
- The EOI mechanism involves an extra register write by the host after clearing the interrupt in the IP. This write is to an EOI register. Writing to the register triggers an EOI handshake. The data written to the register indicates which group to handshake with so different groups will look for different EOI values. When an EOI handshake is seen with the correct EOI value, the group of interrupts is re-evaluated and if any interrupt in the group is pending, then another interrupt is sent to the host. If there are no pending interrupts, the group waits for the next interrupt to generate the system interrupt to the

host. This extra register write guarantees that the previous write to clear the interrupt has been received by the IP and stabilized that interrupt's status before the re-evaluation occurs.

NOTE: The IQN2 consists of three independent interrupt sources from the IP (ee_cppi, ee_ev0 and ee_ev1) with corresponding interrupt destinations. As such, the EOI Vector (eoi_cppi_vector, eoi_0_vector and eoi_1_vector) values for each of these interrupt paths is 0x00.

7.1.5.2 Mapping an IP Module to a Single Interrupt

The following is an example of mapping an IP module to its own interrupt. In this example, we will map the DFE events to interrupt *iqn_ee_int0*.

Set the following register in the AID (AID2_IQN_AID2_DFE_EE_SYSCLK_EE):

- AID2_DFE_EE_A_EV0_EN_SET

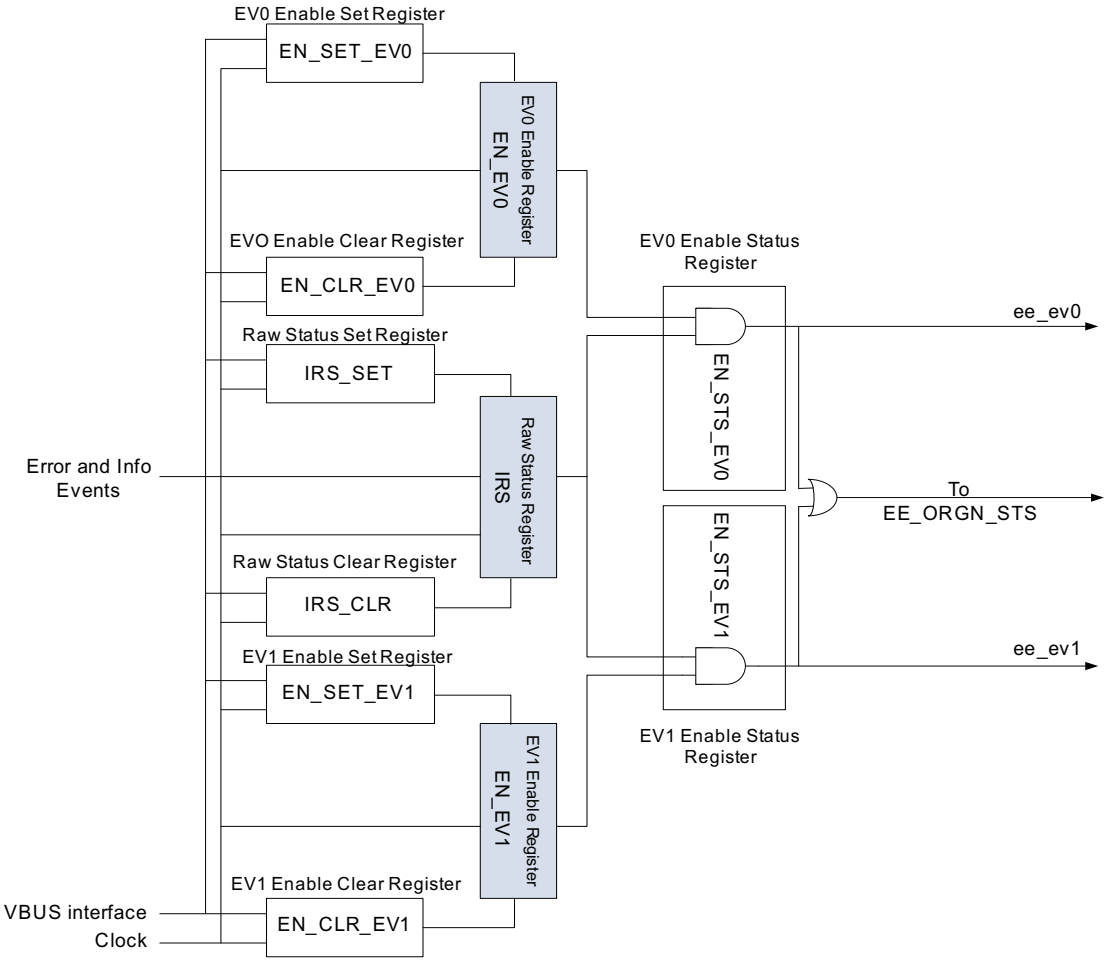
Do not set any other IP EE registers to EV0. In this way, only events generated by the DFE will create an interrupt on *iqn_ee_int0.*

7.1.5.3 EE Register Description

The following comprise the IQN2 EE register set:

- Interrupt Raw Status Register (**IRS**)
  - The Interrupt Raw Status Register captures the current active status of the error/info events before any processing (one bit per error/info event).
    - Raw status of active error/info events (0 = inactive, 1 = active)
- Interrupt Set Register (**IRS_SET**)
  - The Interrupt Set Register provides a software interface for setting interrupts. It is a shadow register and does not have any bits but modifies the **IRS** register.
    - Write a 1 in a bit position to set the error/info event active (writing a 0 has no effect)
- Interrupt Clear Register (**IRS_CLR**)
  - The Interrupt Clear Register provides a software interface for clearing interrupts after they have been serviced or for debug purposes. It is a shadow register and does not have bits but modifies the **IRS** Register.
  - Write a 1 in a bit position to clear the error/info event to inactive state (writing a 0 has no effect)
- Enable Status Register (**EN_STS_EV**)
  - The Enable Status Register captures the current active status of the error/info event after the enabling function (one bit per error/info event). This register does not require any flop bits.
    - Enabled status of active error/info event (0 = inactive, 1 = active)
- Enable Register (**EN_EV**)
  - The Enable Register allows the software to enable individual error/info events. This register reads the current state of the enables for the error/info event.
    - Enabled status of active error/info event (0 = inactive, 1 = active)
- Enable Set Register (**EN_SET_EV**)
  - The Enable Set Register allows the software to enable individual error/info events. Since it is a shadow register there are no physical bits but rather it operates on the **IRS** value.
    - Write a 1 in a bit position to set the enable (writing a 0 has no effect)
- Enable Clear Register (**EN_CLR_EV**)
  - The Enable Clear Shadow Register allows the software to disable individual error/info events. It is a shadow register and does not contain any bits but modifies the Enable Register.
    - Write a 1 in a bit position to clear the enable (writing a 0 has no effect)

Figure 7-6. Exception Handling Register Set



7.1.5.4 EE Interrupt Support

The EE aggregates all of the Error and Info event signals for an IP into two, active high level signals (*ip_ee_ev0* and *ip_ee_ev1*) that are sent to the Top EE module to be further aggregated. These two signals can ultimately be used as interrupt sources to the Host.

Each internal error/info event is reported to the IP EE as a one *vbus_clk* wide pulse and results in a unique bit being set to a 1 in an Interrupt Raw Status Register (**IRS**) in the EE. This bit remains set until cleared by the Host via the VBUSP configuration bus.

All error/info event signals can be routed to either or both of the *ip_ee_ev0* or *ip_ee_ev1* interrupts, and the user can configure the subset of error/info event signals that are associated with each of the *ip_ee_ev0* and *ip_ee_ev1* interrupts via individual enable registers (**EN_SET_EV**) for each of the signals inside the EE. If the error/info event signal is enabled via the enable registers (**EN_EV**), it will cause an interrupt on the *ip_ee_ev0* or *ip_ee_ev1* signal it is routed to when the error/info event signal occurs.

After the interrupt occurs on *ip_ee_ev0* or *ip_ee_ev1*, subsequent event signals that are received for this same *ip_ee_ev0* or *ip_ee_ev1* interrupt will not cause another interrupt until the Host has acknowledged the interrupt by clearing the associated interrupt raw status register (**IRS_CLR**). The Host must also write to the End of Interrupt Register (**EOI**) in the top EE after it clears the source of the interrupt from the IP before a new interrupt can be generated to the system from the *ip_ee_ev0* or *ip_ee_ev1* that created the previous interrupt.

Here are some additional rules that the EE follows:

- If an error/info event signal is received and the corresponding error/info event interrupt raw status bit is

already set to a 1, the occurrence of the second signal will not be saved.

- If the Host attempts to clear an error/info event at the same time that a new error/info event signal is received on the same error/info event input, the new error/info event will cause the status bit to remain set to a 1.

7.1.5.5 Error / Info Event Mapping

To map an error/info event to the *ip_ee_ev0* output interrupt, the user would write a 1 to the enable bit corresponding to the error/info event in the **EN_SET_EV0** register. This action would allow the error/info event to pass to the *ip_ee_ev0* aggregation logic. Mapping an error/info event to *ip_ee_ev1* output interrupt is done in the same manner described above except a 1 would be written to the **EN_SET_EV1** register.

If a user wanted to test the mapping of an error/info event to the *ip_ee_ev0* interrupt without actually generating the error/info event signal from the source module, the user would write a 1 to the corresponding bit in the **EN_SET_EV0** register (to enable the bit to pass) and then write a 1 to the bit in the **IRS_SET** register. The **IRS** bit corresponding to the error/info event would then have to be cleared from the **IRS** by writing a 1 to the corresponding bit in the **IRS_CLR** register. Finally the user would write the **EOI** register in the top EE to acknowledge the servicing of the interrupt. The same process can be applied to map an error/info event to the *ip_ee_ev1* interrupt by writing a 1 to the corresponding bit in the **EN_SET_EV1** register.

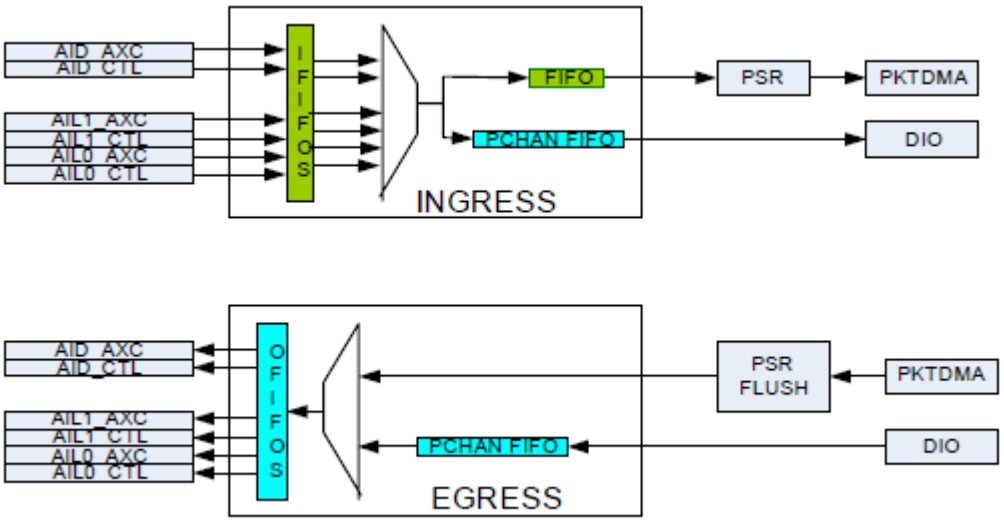
7.1.5.6 EE Event Origination Support

The EE module contains an origination register (**EE_ORGN_STS**) that is designed to help the user minimize the number of register reads required to investigate which error/info event caused an interrupt to occur. This register contains an indication of which **EN_STS_EV** register contains an error/info event that may have caused the initial interrupt. It is the OR of **EN_STS_EV0 | EN_STS_EV1.**

7.2 IQS (IQ Switch)

The IQN2 Switch (IQS2) connects and arbitrates traffic between a DIO and a PKTDMA with an AID and up to four AIL modules (only two AIL modules are instantiated). The IQS2 uses most of the standard PSI signals and timing plus some additional sideband signals. It supports transfers between the DIO or PKTDMA and the AID or AIL. Transfers between AILs and the AID are not supported. All data comes from or goes to the VBUSM interface.

Figure 7-7. IQN2 IQS2 Block Diagram



7.2.1 Ingress Arbitration

Round Robin Arbitration rotates requests so the last granted request is the lowest priority. Then it generates the priority and re-adjusts the result based on what the last granted request was. This provides equal sharing of accesses between all requesting devices.

Fixed arbitration allows the highest priority thread, thread 0, to win out over any lower priority thread, even if that thread has been waiting. Lower priority ports cannot be granted until all higher priority requests have completed.

The IQS2 combines both Round Robin and fixed priority arbitration to provide multiple fixed levels of arbitration between channels with Round Robin arbitration done for channels at the same priority. Which channel was granted last is kept separately for each fixed level of priority. Priorities can be modified at any time regardless of any arbitration activity.

7.2.2 Egress Arbitration

Arbitration in the egress will allow only one channel to have a data transfer on each cycle. It will rely on per-channel empty flags from the egress output port FIFO and the PKTDMA or DIO channel data available signals to decide if a transfer is needed.

Each egress PKTDMA and DIO channel has an MMR specifying which of the output ports it is going to and which channel in that port to write to. It will also have an enable and a 3-bit priority select field so each channel can be assigned to one of eight priority levels.

Whichever source wins the arbitration, either the PKTDMA or DIO, has its data muxed onto a bus that is distributed to all the egress output FIFO modules along with the channel and destination that won the arbitration. Each output FIFO module monitors its data valid indication and takes the data if it was selected.

7.2.3 Push back

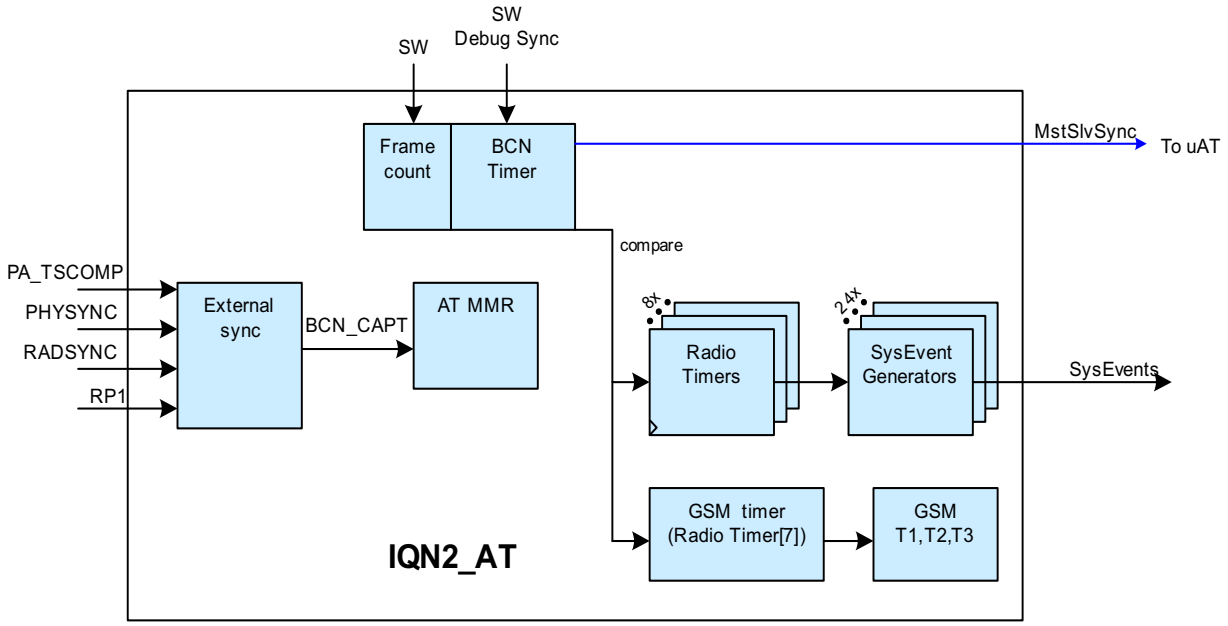
Pushback from the PKTDMA FIFO is supported for those input ports that have their **ALLOW_PUSHBACK** MMR bits set. The PKTDMA pushback point on these ports is selectable at either 1/2 or 3/4 full. The DIO does not support pushback since it only handles AxC traffic. Pushback is intended for traffic such as control packets.

7.3 AT

The Antenna interface Timer (AT) is meant to mark frame boundaries so that events can be generated which are synchronized with this time. Frame synchronization is flexible and currently-known required framing boundaries are {1ms, 4ms, 5ms, 10ms, 60ms}.

There are two basic timer types which are used as a reference for PHY and radio timers (BCN and RADT). All timer synchronizationis based on the offset BCN, which needs to be synchronized with the system. The radio timer RADT is used as a reference basis for radio standard event generation. This timer is synchronized to a particular standard that is chosen. Figure 7-8 shows basic block diagram of AT.

Figure 7-8. AT Block Diagram



The RADT (radio) timers will be used by the system software to mark radio time. All timers are CPU readable. One specialized radio timer (RADT[7]) can be used for counting GSM frame timing. There are a total of 24 external events and event[0] is connected to the external output signal EXT_FRAME_EVENT. This will typically be used for debug purposes. This event is in the native AT sys_clk domain.

There is a synchronization section that detects synchronization from an external source. This detected sync is used as a basis for the timers to capture the BCN count. Software may then adjust the BCN offset as needed for the RADT timing synchronization. The difference in sync selection between AIF2 and IQN2 AT is that the PHY timer is replaced by the BCN timer which is always started by software. The BCN value is captured when there is an input synchronization event (Physync, Radsync, PA_TSCOMP, RP01). An interrupt is generated upon the sync event and SW may then read the captured offset BCN value. Software will then program a BCN offset register which will be used to sync a RADT by using the BCN sync compare value register.

7.3.1 AT BCN Timer

The BCN timer works similarly to the previous PHY timer in AIF2 and it is used for synchronization with GSM time and for marking frame boundaries. The function of the timer is straightforward. There is a clock counter which runs at the basic IQN2 system clock rate which is 307.2MHz (OBSAI) or 245.76MHz (CPRI) and a frame counter which increments upon wrap of the clock counter.

The clock counter will count up to a full frame in OBSAI or CPRI mode. The terminal count for this counter is 25 bits wide and is programmable to count up to **33,554,432** clock ticks. This allows for a 60 ms frame timing at 500MHz. A 10 ms frame for example is **3,072,000** clock ticks at a system clock of 307.2MHz and **2,457,600** clock ticks at a system clock of 245.76MHz.

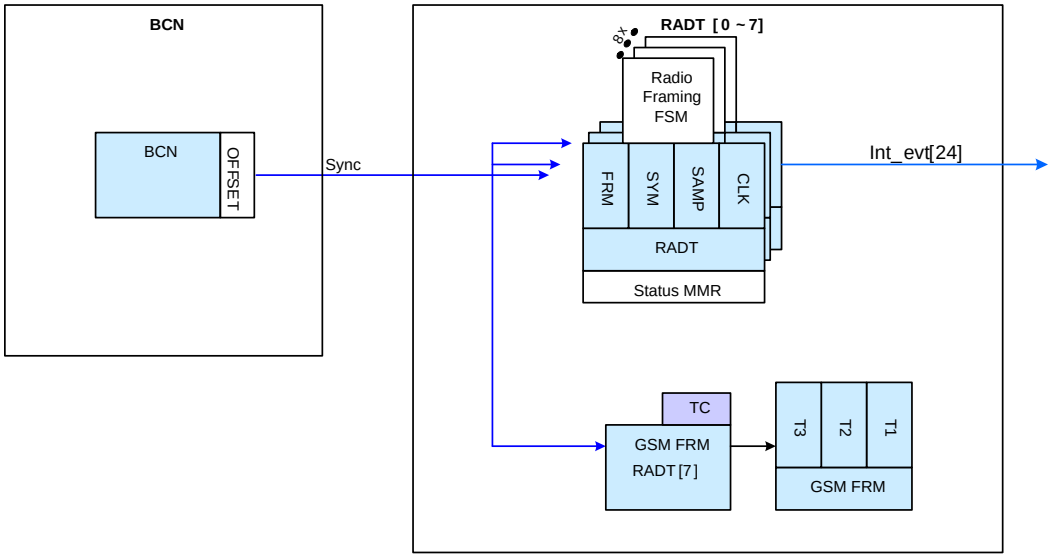
The frame counter is 40 bits in width. The initial value of the frame is set by software.

The BCN receives its synchronization from a number of possible sync sources. Each sync is used for capturing its offset BCN time. Initially, the SW programs the BCN offset to be 0. BCN terminal count is programmed. The BCN is enabled and starts free-running. When a sync occurs, an EE event interrupts the SW for that sync and the offset BCN is captured. SW then adjusts the BCN offset according to the captured BCN time by writing the BCN offset MMR. If the sync is an RP1 sync, the frame number is captured by the RP1 interface. The SW uses this value to initialize the 40-bit BCN Frame counter.

The BCN counter has a terminal count MMR which is used for both the free-running for frame compare and strobe generation (mst_slv_sync for uAT synchronization).

7.3.2 AT Radio Timer

Figure 7-9. AT2 RADT Block Diagram



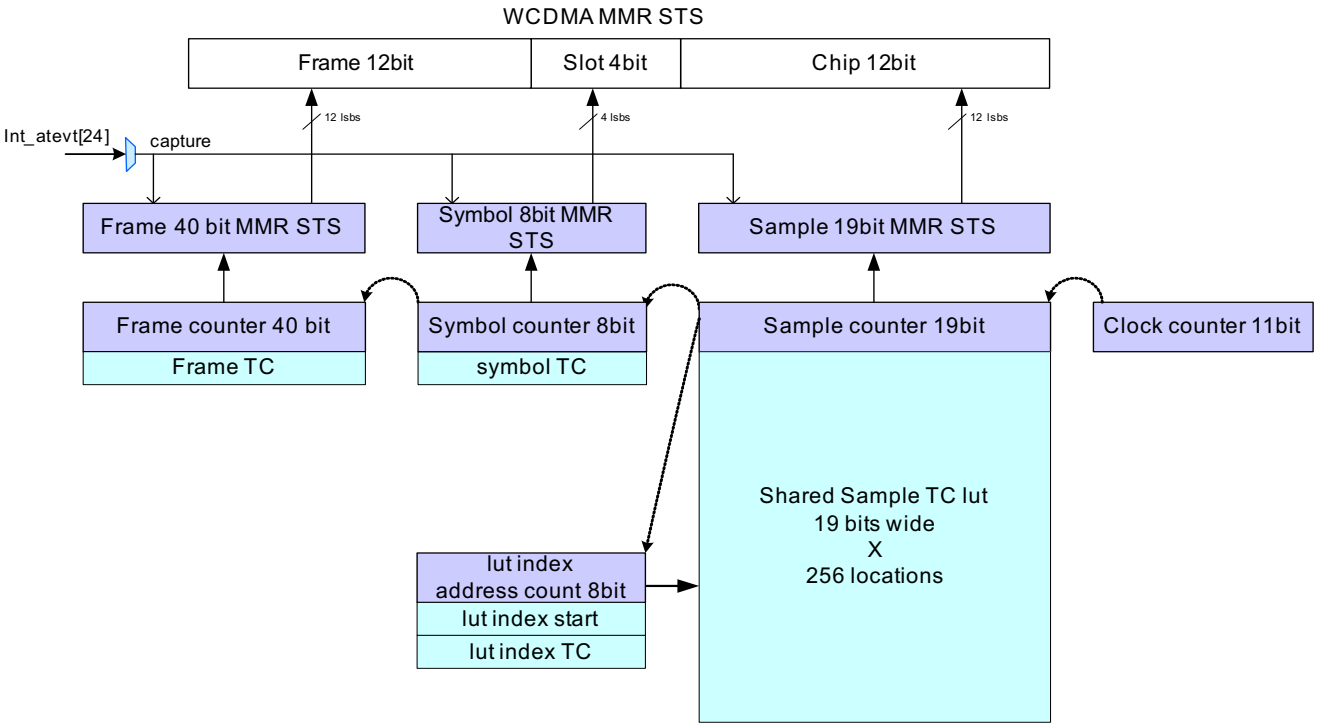
Radio Timers have the ability to count symbols and frames of various sample counts. Symbol or frame boundary will be used to drive event generators. These events will be used by the internal modules and external to IQN2. These events will typically interrupt CPUs but may be used by other system components. The IQN2 AT supports eight simultaneous radio standards with eight RADTs and a special GSM frame counter.

Timer symbol counting is accomplished with the use of a lookup table (LUT) programmed to represent the radio standard time. This allows for timing a regular pattern of symbols of variable size as in some TDM standards. Each RADT will have its own BCN comparator. SW programs the compare value which effectively offsets the individual RADT from the BCN frame boundary.

To start the RADT, SW must first enable the particular RADT by setting enable MMR. Once enabled, the RADT starts counting once the associated BCN compare value is met from an initial value of 0 for all but the frame counter. The frame counter may be initialized by SW.

The RADT basic counter setup is as diagrammed in Figure 7-10.

Figure 7-10. RADT Basic Counters



RADT is a fine-grain reference timer clocked off of the system clock (sys_clk). This time is converted to its selected standard through the use of the Clock TC LUT. The LUT is populated (programmed) with terminal counts that represent all of the symbol terminal counts within the desired standard's frame or group of frames.

The sample LUT consists of a single RAM that is shared among eight RADTs. A separate symbol LUT index counter is used to select the clock counter terminal count value for that particular symbol. It will increment whenever it sees a symbol boundary and will wrap on the number of symbols per frame counted. The wrap value is programmed per standard. Typically, the wrap value of the LUT index is equal to the wrap value of the symbol TC plus the index start offset. If all of the symbol sizes are equal for a particular standard, only one location in the LUT will be used for that RADT. An exception is in LTE which has a repeating pattern or either 6 or 7 symbols within a group of 120 or 140 symbols.

The clock counter, sample counter, and symbol counter all start from a count of zero. The Frame counter starts from whatever initial value was loaded by SW.

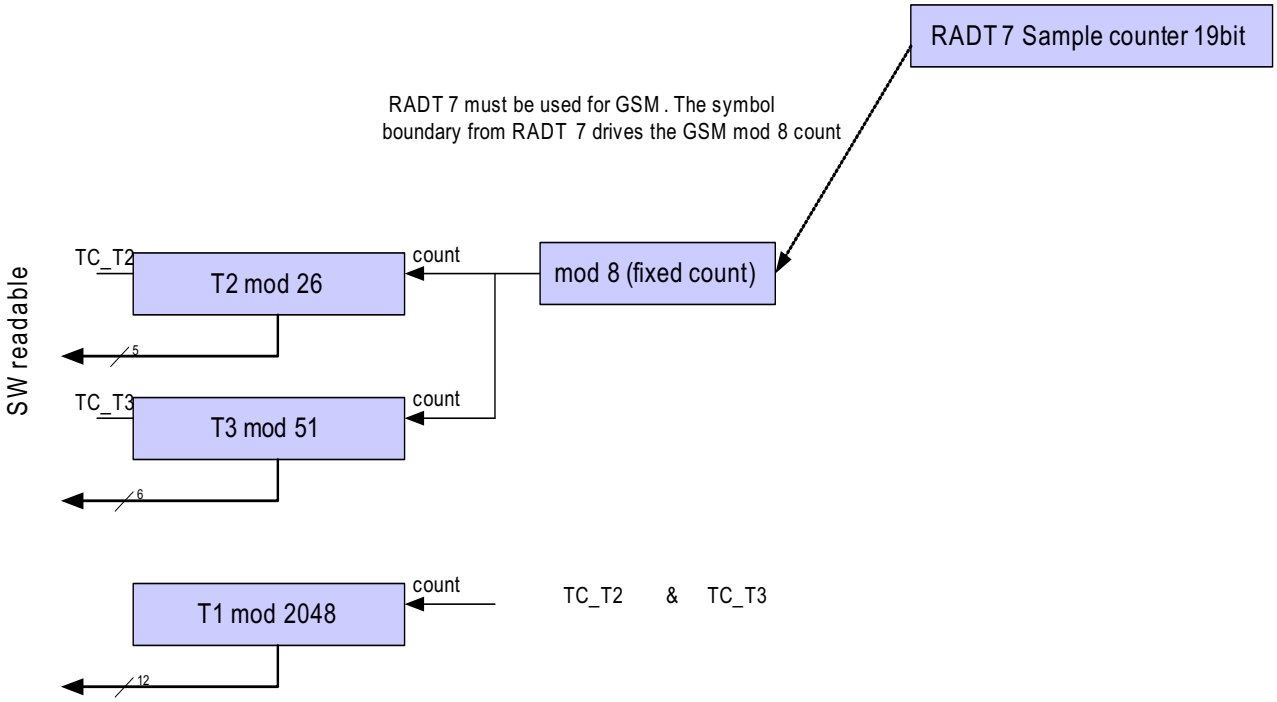
RADT has a status MMR for WCDMA format time. All RADTs have this although only some of the RADTs are used for this purpose. This format is needed for doing a DMA of the value to the RAC or TAC upon an event that drives an EDMA.

There is an additional GSM timer triggered off of the RADT 7 every eight symbol boundaries. This marks T1, T2, and T3 frame times. These counters count GSM frames which are a duration of 1/13th of a 60 mS period. The modulo count for the three timers is as follows:

- T1 = modulo 2048
- T2 = modulo 26
- T3 = modulo 51

Software must initialize the T1, T2 and T3 counters based on the current FCB received. The software application must calculate T1,T2 and T3 based on a received RP1 FCB frame burst and then load these T counters. T2 and T3 both count GSM frames. T1 counts every time when both of these counters wrap. Max count for T1 is 2047 before it wraps to 0.

Figure 7-11. GSM Frame Timer



7.3.3 AT: Synchronization

Synchronization is detected from an external source and is meant to determine a time within a UMTS or other frame boundary. This synchronization would typically happen on the frame boundary, but may happen at an offset into the frame boundary. Detected Frame synchronization is referenced to the selected sync clock, but will be re-synchronized to the 307.2MHz or 245.76MHz sys_clk domain in which the timers and events reside.

This detected sync is used as a basis for the timers to capture the BCN count. Software may then adjust the BCN offset as needed. The difference in sync selection between AIF2 and IQN2 AT is that the PHY timer is replaced by the BCN timer which is started by software. The BCN value is captured when there is an input synchronization event. Each synchronization input has its own separate BCN capture register. An interrupt is generated upon the sync event and SW may then read the captured offset BCN value. Software will then program a BCN offset register to adjust the frame timing.

Captured offset BCN value shows the time distance between current free running BCN frame boundary and the sync triggered timing. Software then calculates BCN frame length - Captured offset BCN and the result can be set as a BCN offset value. This offset value is added to the current clock counter right away. For example, if the BCN frame size is 2457600 clocks and captured offset BCN was 2100000, then 2457600 - 2100000 = 357600. This 357600 can be set to BCN offset register and the current clock counter will jump to the new clock counter value as amount of 357600 as soon as the offset is set.

There is no synchronization source selection. Instead, the sync sources have their own BCN capture register. When a sync occurs, an interrupt may be generated for that sync and the SW can then read the captured BCN value for that sync and make adjustments in timing accordingly.

7.3.3.1 AT: OBSAI RP1 Synchronization

OBSAI RP1 specifies that the CCM (Clock and Control Module) provides a 30.72MHz System Clock and periodically sends synchronization bursts to the BaseBand Modules. The RP3 and System Frame Numbers, Frame boundary timing, and Time of Day information is passed in the synchronization bursts.

The OBSAI synchronization burst is serially transmitted over a single differential input (differential signaling) which is clocked in via the differential SCLK. Each bit of the serial transfer is held for eight System Clock (SCLK) periods; this is approximately 260 ns. For fields with more than a single bit, the least significant bit (LSB) is sent first.

The first field is the “Start” bit which marks the beginning of the synchronization burst. The 8-bit “Type” field follows and identifies the type of information which is contained in the synchronization burst payload. The 64-bit “Information” or Payload field contains the relevant data (either frame number or time of day). The CRC field is used for data integrity and the “End” field terminates the synchronization burst packet.

The falling edge of the END bit based on the RP1 clock determines the frame synchronization boundary. This boundary is resynchronized to the AT2 sys_clk domain (clock which is used for the BCN anb RADT timers) which adds one to two sys_clk pipeline delays. This is one sys_clk period of uncertainty due to synchronization plus one pipeline delay. This synchronized RP1_SYNC is then used for capturing the BCN counter which software can read and determine if an adjustment is needed by writing to the BCN offset configuration register.

Figure 7-12. Synchronization Burst Format

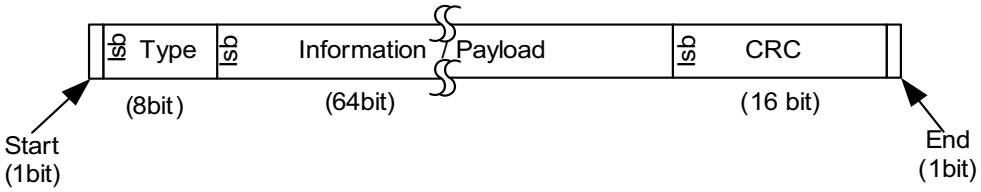


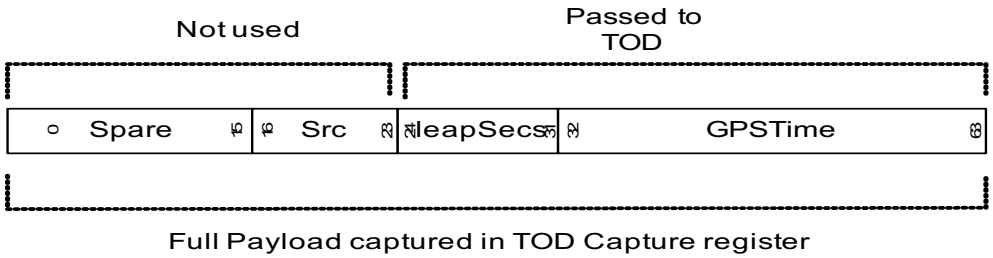
Table 7-3. RP01 Type Field Definition

Type	Supported	Value
Not Used (1)	N/A	00h
RP3 Bus (FDD) Frame Number	Yes	01h
WCDMA/FDD Frame Number	Yes	02h
GSM/Edge1 Frame Number	Yes	03h
GSM/Edge2 Frame Number	Yes	04h
GSM/Edge3 Frame Number	Yes	05h
WCDMA/TDD Frame Number	Yes	06h
CDMA2000 Frame Number	Yes	07h
Time of Day	Yes	08h
Reserved (1))	N/A	09h – 7Fh
802.16 Frame Number, 2ms Frame	Yes	80h
802.16 Frame Number, 2.5ms Frame		81h
802.16 Frame Number, 4ms Frame	Yes	82h
802.16 Frame Number, 5ms Frame	Yes	83h
802.16 Frame Number, 8ms Frame	Yes	84h
802.16 Frame Number, 10ms Frame	Yes	85h
802.16 Frame Number, 12.5ms Frame		86h
802.16 Frame Number, 20ms Frame		87h
3GPP LTE Frame Number	Yes	88h
Spare (2)	No	89h – FFh

(1) Reserved” and “Not Used” Types will cause an Alarm/Error condition.
(2) Spare” Types are disregarded

Figure 7-13 shows the payload used for the Time of Day timer.

Figure 7-13. Payload Use for Type Time Of Day



7.3.3.1.1 AT: RP1 CRC

The CRC process does a modulo2 polynomial divide of the input data stream. The resulting remainder of that division is compared with the sent CRC and is equal provided that the data or CRC value has not been corrupted.

"OBSAI Reference Point 1 specification" specifies the divisor polynomial to be:

$$x^{16} + x^{12} + x^{5} + 1 \quad (1)$$

The initial value of the CRC shall be 0xFFFF

The CRC checking circuit recursively processes every bit of the "Type," "Information," and "CRC" fields and then on 16 trailing 0 bits. If the remaining result equals the sent CRC, the CRC passes. The checking circuit must first be initialized to either all 0s or all 1s before the checking process begins.

Flexibility has been designed into the CRC checker since the OBSAI RP1 spec. has had some ambiguous interpretations and was in a state of changing as this document was written. There are four bits in Control Register 1 that control the behavior of CRC checking:

- "CRC_use" = 1 will use the CRC, = 0 will not.
- "CRC_flip" =1 will change the MSB/LSB order, = 0 will keep MSB/LSB order (default).
- "CRC_init_ones" controls initialization where the default value of "0" will initialize the CRC calculator to all 0s. For true OBSAI compliance, this bit must be set to "1" to initialize the CRC calculator to all 1s.
- "CRC invert" =1 inverts the CRC for comparison, = 0 does not invert the calculated CRC for comparison (default).

The order in which the frame_burst CRC is received is programmable with the CRC_flip bit of a control register. When CRC_flip =0, the CRC register bit-16 value should be received first in the frame_burst CRC. When CRC_flip=1, the CRC register bit-1 value should be received first in the frame_burst CRC. The received value is loaded into a shift register, then compared to the calculated CRC.

CRC is enabled by setting a CRC_use bit. When enabled, a CRC failure will discard the sync_burst. The CRC fail will generate an error or alarm using the error/alarm mechanism. If the CRC passes, the contents of the sync burst are used and normal operation will continue. If the CRC is disabled by clearing a CRC_use bit, the contents of the sync_burst are used regardless of the CRC.

7.3.3.1.2 AT: Time of Day

The RP1 interface receives a frame burst of type TOD and the payload value is captured. The type and payload is SW readable after the RP1 sync is detected. SW determines that this is of type TOD and uses the TOD payload.

7.3.3.2 AT: Sync Boundary Detect and Resynchronization

When synchronization has already been established and a new sync arrives while the BCN and RADT timers are counting, there may be an interrupt on sync (if enabled) and the SW will determine if the BCN offset has changed from the original sync time. If it has, the SW may then readjust BCN offset or offset comparators for RADTs and uATs.

7.3.3.2.1 AT Re-synchronization Process

- When new external sync arrives, one of the BCN sync capture status registers will show new captured value.
- Calculates new offset based on captured value and update BCN offset register.
- It takes more than one frame time to make both BCN and RADT fully synchronize and run correct with new offset.
- New mst_slv_sync signal will be delivered to uATs (AIL, AID, DIO) for uAT BCN and RADT synchronization

7.3.3.2.2 Micro AT Re-synchronization Process (Applied to AIL, AID, DIO)

- New mst_slv_sync sync from AT arrives, all BCN and RADT sync capture status registers will show new captured value.
- Calculates new offset based on captured value and update BCN or RADT offset register if required. AID, DIO requires RADTs, AIL OBSAI requires BCN and RADTs and AIL CPRI only requires BCN.
- It takes more than two or three frame time to make both BCN and RADT fully synchronize and run correctly with new offset.
- In case of AID, all AID EFE, IFE channels must be disabled before updating the micro AT timer offset registers and enabled again after the re-sync process is fully done.

7.3.3.2.3 DIO Module Re-synchronization

There are two restrictions to make DIO run correctly after re-synchronization.

- DIO engine should be disabled before updating the micro AT timer offset registers and enabled again after the re-sync process is fully done.
- All DIO EFE channels (used for SoC level ingress) must be disabled before updating the micro AT timer offset registers and enabled again after the re-sync process is fully done.

7.3.4 Adjusting Radio Timer Terminal Counts on the Fly

Antenna interface Timer (AT) will allow adjusting of the radio timers on the fly with some restrictions.

System software needs to wait for an event from the particular radio timer which marks the start of a period of time in which that timer can be updated. The event needs to be a frame boundary event for the particular radio timer.

If all radio timers are to be adjusted, there need to be separate events, each referenced to their associated timer.

Upon detection of the event, the software update window is one minimum symbol of time minus event latencies, processor latencies, and VBUS latencies. Preference for standards with variable symbol length would be to use a frame boundary event since the clock counter terminal count will already be known for the first symbol.

In this time, SW needs to write the new terminal count into the symbol LUT.

Any updates of TC or actual counter value must be done with the same event mechanism, on a frame event boundary.

Assumptions:

- Update of radio timer LUT index is not allowed.
- Update only allowed on a frame event for the particular timer.
- Update of sample TC LUT allowed.
- Update of symbol TC allowed.
- Update of Frame TC allowed.

7.3.5 Modifying the 40-bit Frame in BCN and RADT Timers

Antenna interface Timer (AT) allows for a programmable software modification of the frame in the BCN and RADTs.

SW then reads/modifies/writes the new frame value. The upper 28 bits of the frame can be modified with one 28-bit register write. If there is a need to modify the lower 12 bits, a second register write is needed for the frame LSBs of that timer. For BCN and RADT, there is a window of one frame minus event latencies, processor latencies, and VBUS latencies.

The safest way of updating a RADT is to wait for a symbol-based system event for the particular timer and do the modification within the symbol minus latency (above) time. Software must account for symbol count wrapping.

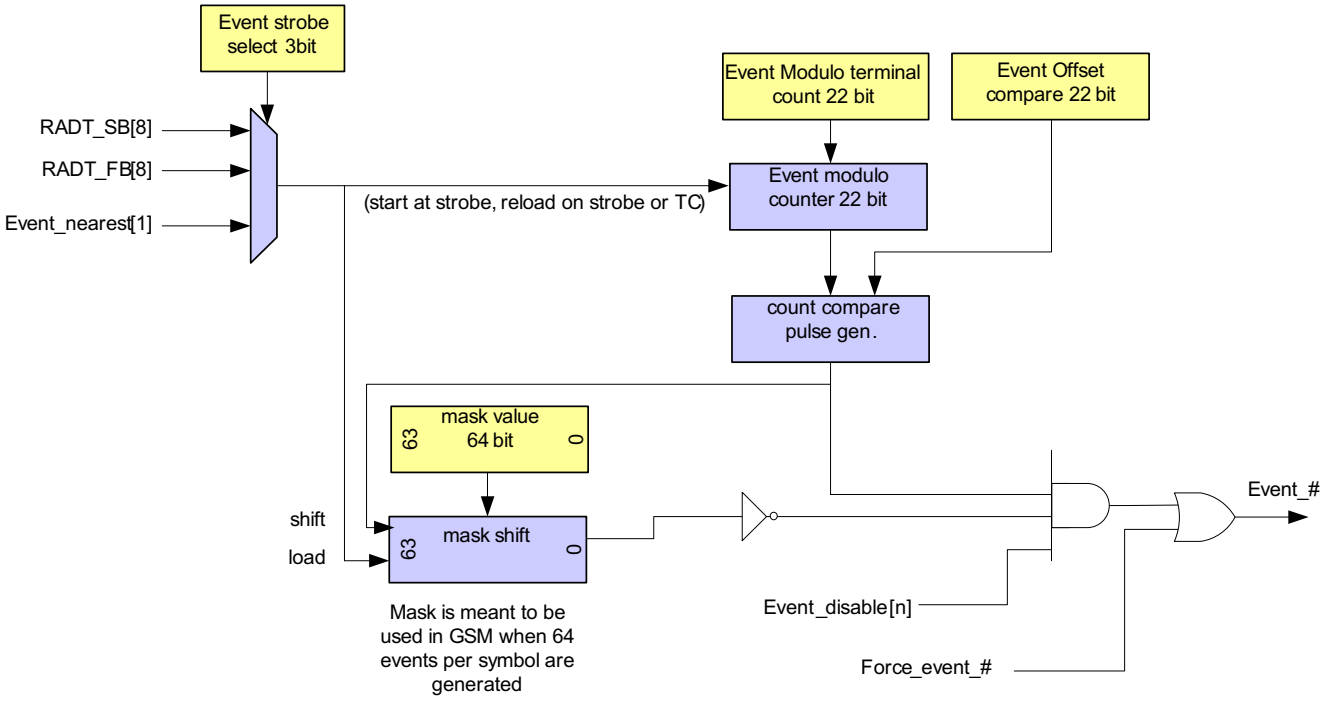
Assumptions:

- Update for RADT allowed on symbol boundary event.
- Update of frame number allowed.
- Update of clock counter on the fly is not allowed.
- Update of sample counter on the fly is not allowed.
- Update of symbol counter on the fly is not allowed.

7.3.6 AT: Event Generation

There are a total of 24 events used by the system outside of AT and event[0] output is also connected to an external pin. These events are referenced to the radio timers (RADT timers). Events for internal IQN2 use are based on the RADT timer and explained in more detail in uAT chapter in SI.

Figure 7-14. Event Generator



Each event generator for the 24 events used outside of IQN2 is based on an event modulo counter and an event count compare. These two values are set in software. There is a boundary detect signal from its selected RADT. This boundary is typically a symbol boundary, but may also be a frame boundary. An event start boundary may also be based on the nearest neighbor event (next higher event).

Detection of the boundary starts the modulo timer. Events will occur upon compareison of the modulo timer with the event count compare, provided that the particular event is not masked. There is a 64-event mask register that is set to mask any combination of 64 events in a symbol, provided that 64 events per symbol are programmed in the event modulo and compare. This is meant to be used in GSM and can be set to 0xFFFFFFFF for all other radio standards.

Event count compare (offset) and event modulo TC should be less than the event symbol (or frame) period. Event count compare must be less than or equal to the event modulo TC. **Event modulo minimum is mod 16.** This will allow for crossing synchronization boundaries into the VBUS clock domain which is CPU clock/3. The event output will be a positive pulse of one VBUS clock width.

Since all of the events are counter-based, each event can have the flexibility to have a modulus that is not necessarily a power of two.

Events may be disabled or enabled on the fly while events are being generated. Disabling an event will cause the event to be removed on the next available selected timer frame boundary (frame or symbol). An event that is enabled during event generation will start generation upon its programmed offset after the next detected boundary. Also, events can be forced in software. This feature may be used for system debug.

The external system event, EXT_FRAME_EVENT, is a chip output event based on at_event[0]. The requirement for this event is to generate a frame pulse that is a minimum of eight clock cycles long. AT system Event0 is used for driving the EXT_FRAME_EVENT and will be synchronized to the sys_clk and extended a minimum of eight clock cycles.

Table 7-4. Use of Timer Fields for Different Radio Standards

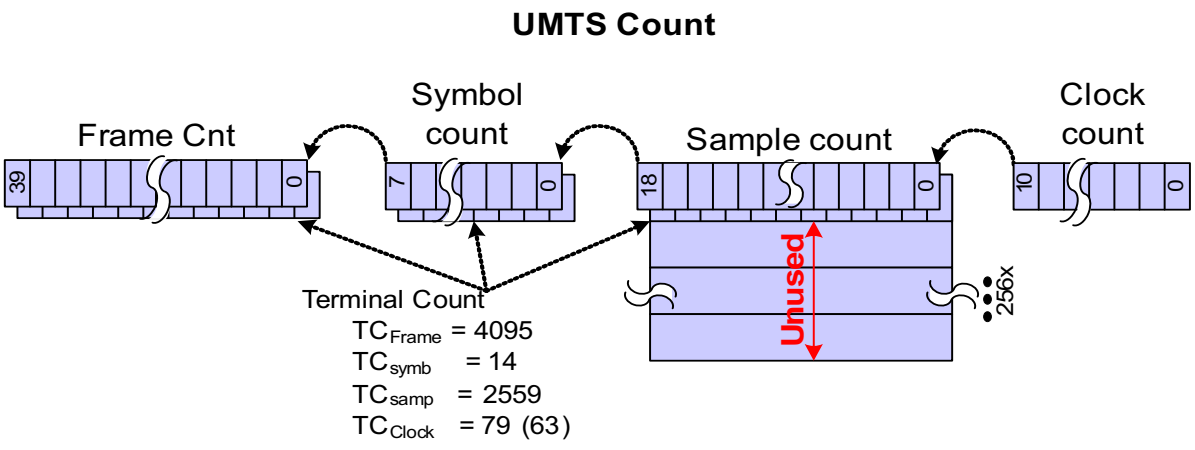
Radio Standard	Frame_Cnt	Symbol_Cnt	sample_Count	Clock_Count
WCDMA	10ms	Time Slots	Samples per Slot	Clocks per Sample
LTE	10ms	Symbol Count	Samples per Symbol	Clocks per Sample
WiMax (TDD/FDD)	Frames	Symbol Count	Clocks per Symbol	Not used (zero)
TD-SCDMA (TDD)	Frames	Symbol Count	Clocks per Symbol	Not used (zero)
GSM	60ms	Time Slots per 60ms	Clocks per Time Slot	Not used (zero)

7.3.6.1 AT WCDMA

The RADT timers are programmed as shown for WCDMA.

The LUT index will always point to one location. This location will have the terminal count value so that the sample counter will count to 2560. The clock counter will count to 80 clocks for OBSAI, CPRI 5x,10x and 64 for other CPRI.

Figure 7-15. WCDMA RADT Timer Setup



Symbol count TC is 14, allowing for 15 slots per frame. The frame counter will count up to 4095 then wrap. RADT events will be triggered by either a symbol boundary or frame boundary. Once triggered, there could be up to 640 events per symbol (UMTS slot), representing one event for every four UMTS chips for downlink and eight UMTS chips for uplink. The BCN clock timer is set to count 3072000 clocks at 307.2MHz and 2457600 clocks at 245.76MHz. This represents one full 10 mS frame.

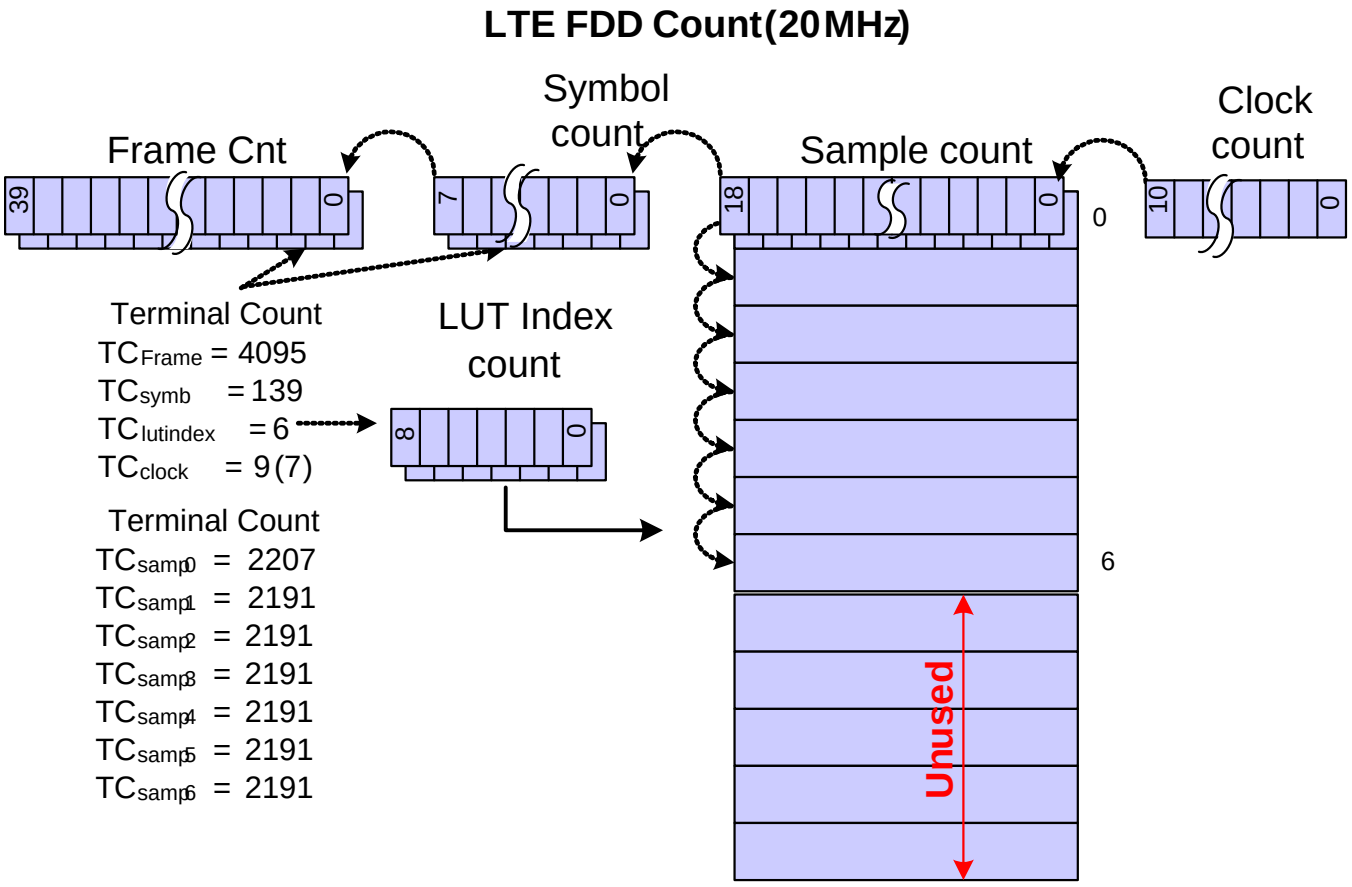
7.3.6.2 AT LTE

For LTE FDD count, the clock counter LUT index is programmed to six and sample count will be repeated every seven symbols. The clock counter will count to 10 clocks for OBSAI, CPRI 5x,10x and 8 clocks for other CPRI(LTE 20MHz). Table 7-5 shows how the clock counter can be set for each radio standard. Symbol count TC is 139, allowing for 140 symbols per frame when normal cyclic prefix is used. The frame counter will count up to 4095 then wrap.

Table 7-5. Clock Count Within One Sample

Radio Standard	Clocks in sample (OBSAI, CPRI5x10x)	Clocks in sample (CPRI 2x4x8x16x)
WCDMA	80	64
LTE 20 MHz	10	8
LTE 10MHz	20	16
LTE 5MHz	40	32
LTE 3MHz	80	64
LTE 1.4MHz	160	128

Figure 7-16. LTE RADT Timer Setup for FDD

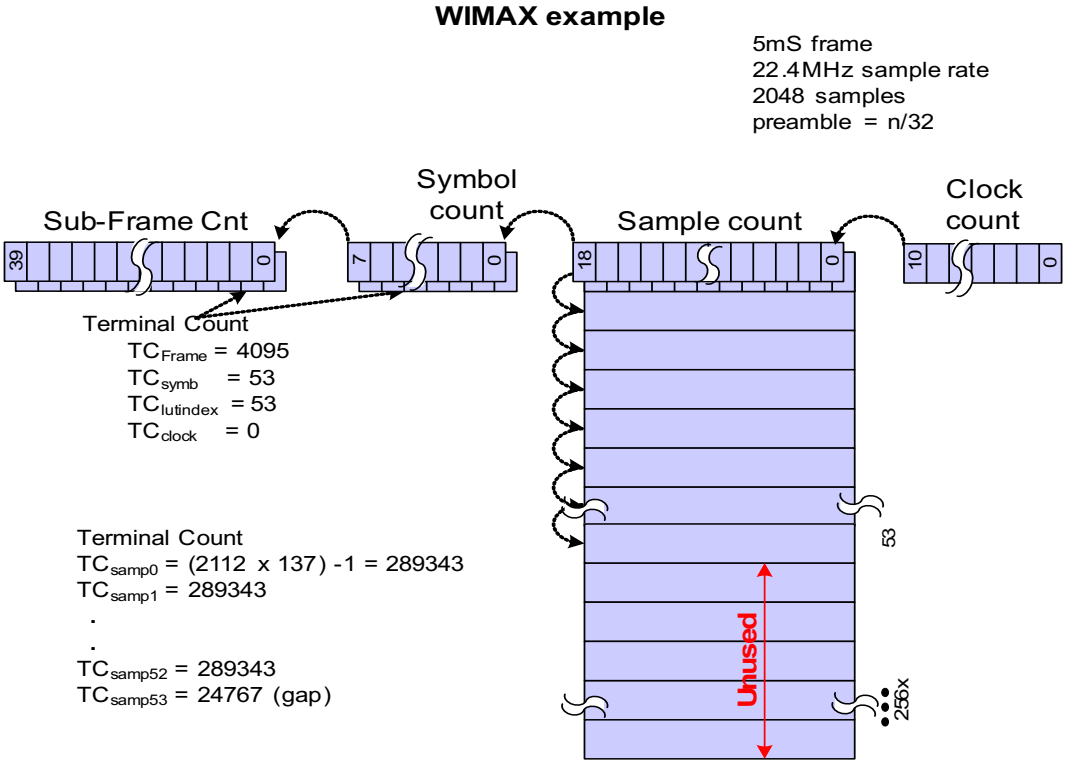


7.3.6.3 AT WiMax

The RADT timers have the flexibility needed for the various WIMAX rates. The following example is for a 5 ms frame, 22.4MHz sample rate. The clock counter LUT index will be programmed with the same value as the Symbol count TCsymb. Since the WIMAX sample clock is not an integer multiple of the 307.2MHz RADT timer clock, an approximation must be made for time-slot counts or for gap.

In the following example setup (Figure 7-17), error is accumulated in the gaps. Clock counter is not used and sample counter shows the nmber of clocks within symbol. Setup of sample TC may be modified to distribute the error among time-slots as is done in the GSM example.

Figure 7-17. WIMAX Timer Setup 5 ms Frame,22.4MHz Sample Rate



Events may be generated for uplink or downlink separately, or both combined. Events would be triggered by symbol boundaries (OFDM packets). The event counter could be set to have one event per symbol. If separate events for uplink and downlink are desired, the mask for the particular event could be configured to select only uplink while masking out downlink events. The same could be done for downlink. When the UL and DL ratio changes, the mask can be reprogrammed on the fly to change this event ratio.

7.3.6.4 AT TD-SCDMA

The RADT timers are programmed as shown for a 5 ms TDSCDMA subframe. The clock counter LUT index is programmed with the same value as the symbol count TCsymb.

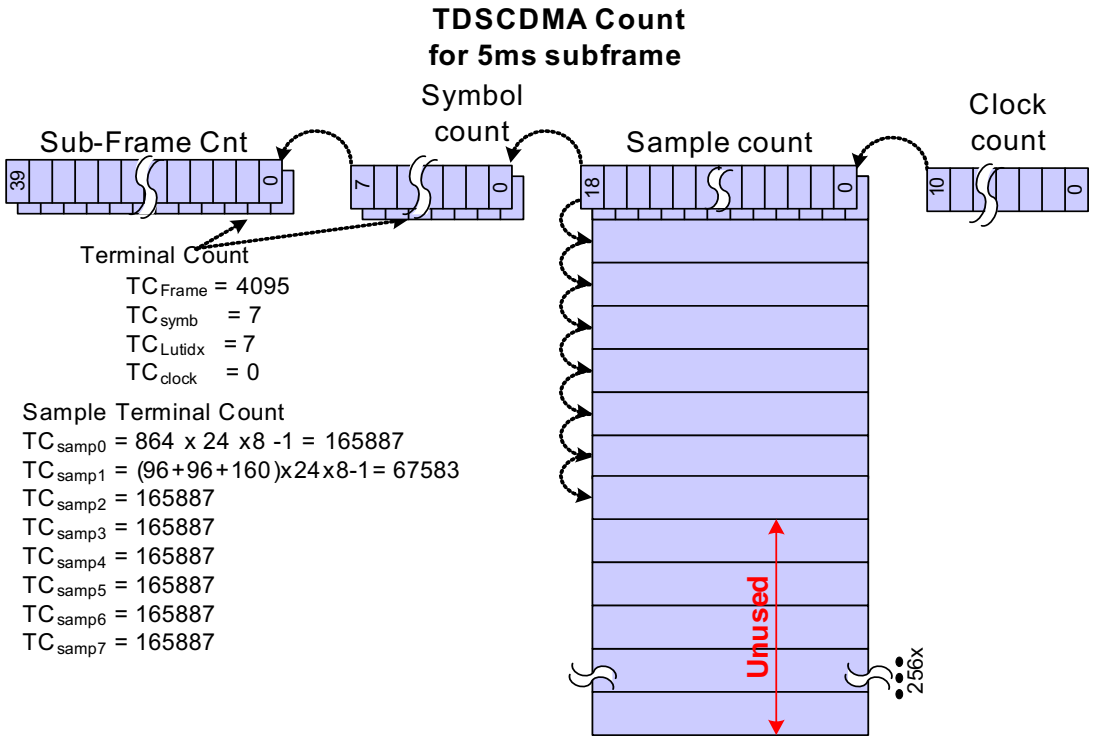
For TDSCDMA, there are various slot sizes. The LUT is programmed to have the configuration shown in Figure 7-18. For example, the first terminal count for the clock counter (Sample TC in this case) is programmed to be 165887, the second location 67583, third location 207359, etc. This accounts for the various but repeatable symbol sizes in TDSCDMA.

Symbol count TC is set to seven in order to count eight symbols per subframe.

Each sub-frame in this case is 5 ms.

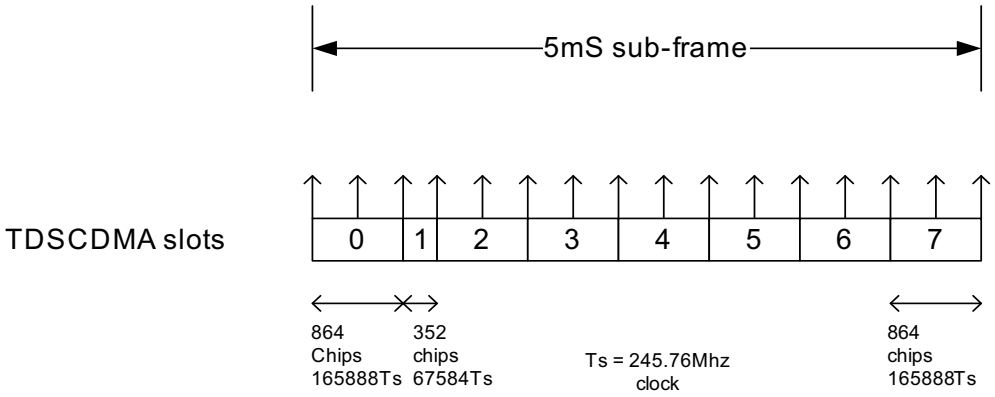
If a 10 ms frame boundary is needed, the programmer has the option of doubling the depth used in the LUT and doubling the symbol count.

Figure 7-18. RADT TDSCDMA Counter



Events are generated on a ½ slot boundary as shown. Slot1 is a special slot, actually made up of DwPTS, GP, and UpPTS. No event is generated in the middle of this slot. The event counter has a 432 chip as a modulo and a period of 67584 clocks @ 245.76MHz, so it does not create a mid-slot event.

Figure 7-19. TDSCDMA events

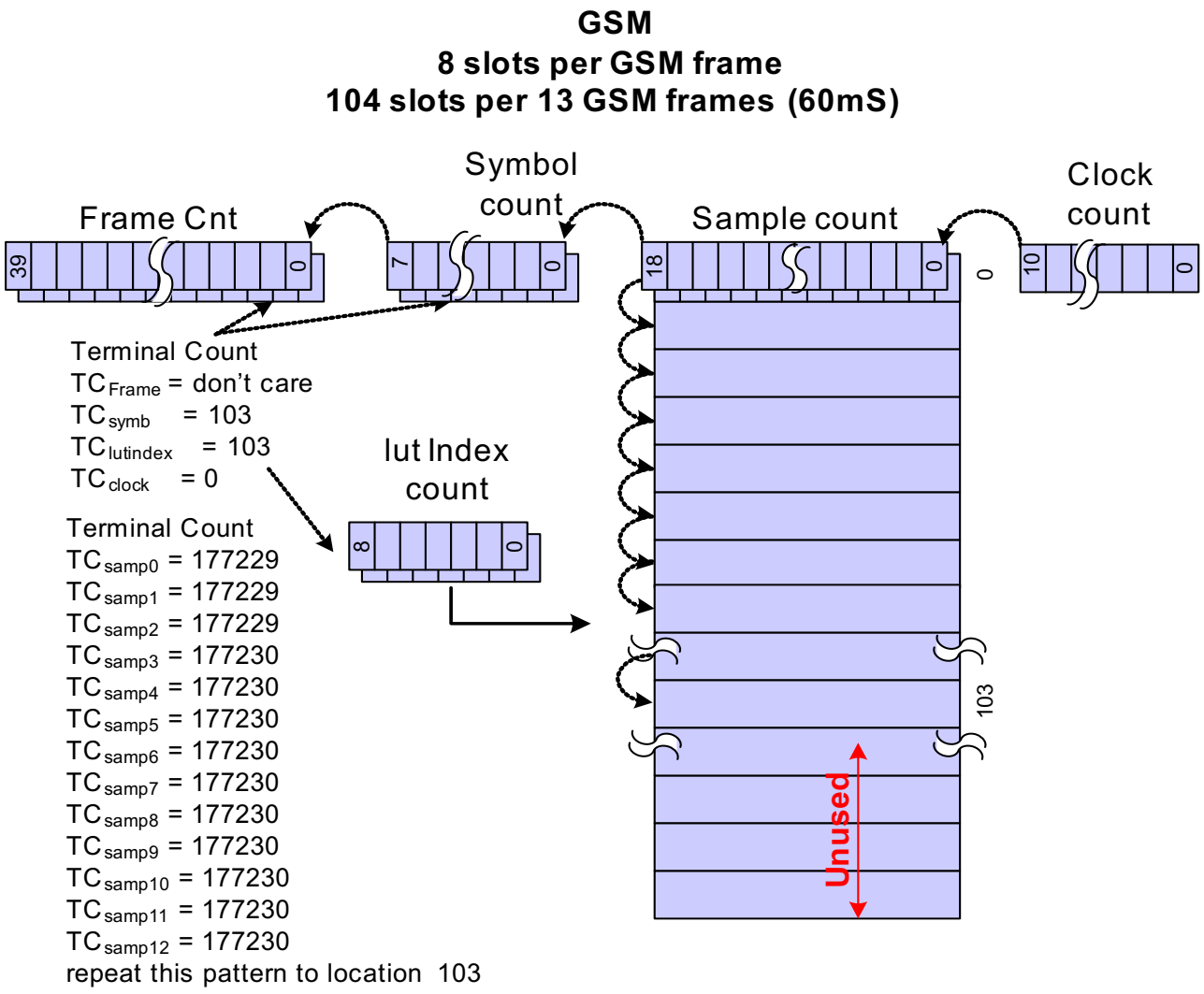


7.3.6.5 AT GSM/Edge

Since the GSM sample clock is not an integer multiple of the RADT timer clock, an approximation must be made for time-slot counts. Fortunately, every 60 ms, the GSM timer is an exact multiple of the 307.2MHz clock. This allows for minor adjustments of the slot size, +/- one clock. Since there are eight slots per GSM frame and there are 13 frames in 60 ms, we need to be able to have 104 timeslots (sample). Clock terminal counts are available in the sample count lookup table. The 256 locations of the sample count LUT can accommodate this. 104 locations are loaded with the various slot sizes of either 177230 or 177231 clocks (307.2MHz case). In a series of 13 slots, three slots would count 177230 clocks and 10 slots would count 177231 clocks. This pattern of terminal counts will exactly allow for a 60 ms count for 13 GSM frames.

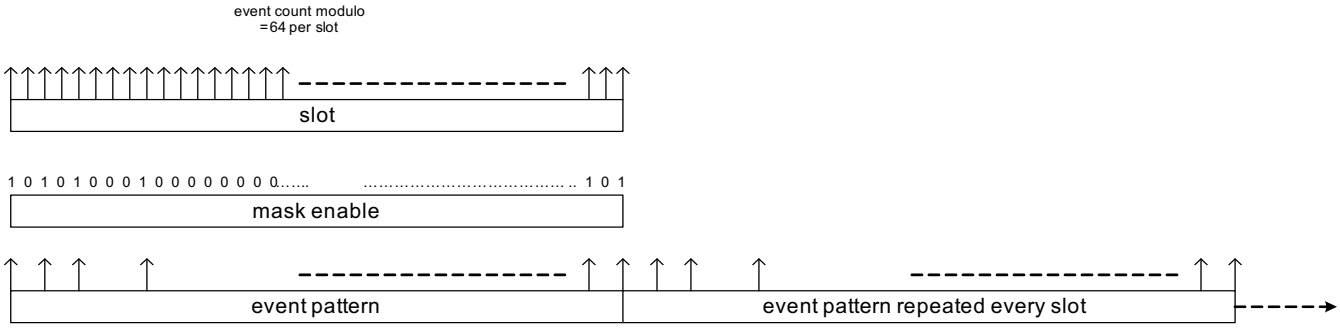
The symbol counter needs to count 104 slots per 13 GSM frames, or 60 ms. The 104 locations will account for clock count distribution among 13 GSM frames. T1, T2, and T3 counters are initialized by software and are used to count GSM frames. Typically, the value in the Frame Count field is not used, rather the T1, T2, T3 values are read by software. A fixed eight-symbol counter indicates a GSM frame boundary and increments the T2/T3 counters.

Figure 7-20. GSM RADT Setup



Events are generated based on slot boundaries where there are 64 possible events per slot. The desired event counter is programmed to be modulo64 with an index of 0. The 64-event mask is programmed to enable the desired event pattern within the slot period. All slots for that particular event counter will have an identical event pattern.

Figure 7-21. GSM Maskable Events



GSM also has another group of three timers which are increased on a GSM frame-by-frame basis. They will be increased every time the symbol (GSM slot) counter wraps. These are the T1, T2, and T3 timers fixed as:

- T1 = modulo 2048
- T2 = modulo 26
- T3 = modulo 51

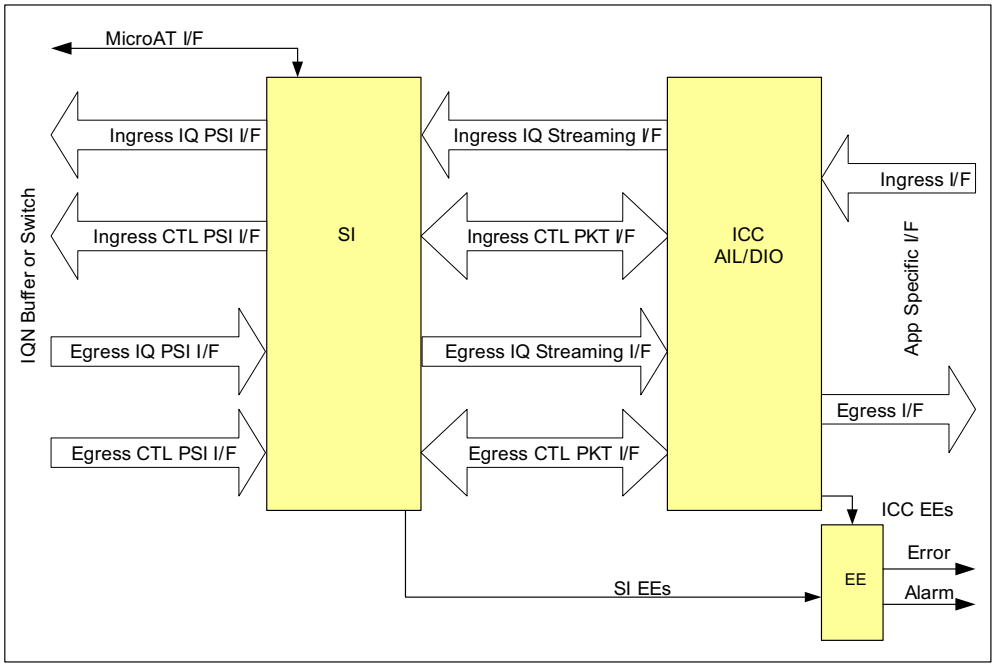
These timers will not generate events but are readable by software. Software must initialize the T1, T2, and T3 counters based on the current FCB received.

7.4 SI

The SI (IQN2 System Interface) module provides a common interface between the components of an IQN2 (i.e., AIN, AIL, and DIO) and the IQN2 buffer or IQS for both the Ingress and Egress paths. The SI can accommodate both IQ data and control packets, if required, via separate interfaces. Some IQN2 components require special signals that the SI also accommodates. Since each IQN2 component can have different AxC capacity requirements, the SI can be configured differently for each application.

A block diagram of an IQN2 component using the SI and an IQN2 core component (ICC) is shown in Figure 7-22. The AID, AIL, and DIO are all implemented in this manner. The AID is implemented with only a standalone SI, MMRs, Shutdown Controller, and an EE module.

Figure 7-22. IQN2 Component Block Diagram (AIL,DIO)



NOTE: For purposes of this chapter, an IQN2 component (e.g., AIL, AID, DIO) consists of an IQN2 core component (ICC) and an accompanying SI block. Refer to the AIL, AID, and DIO chapters for further details on the top level block diagrams of each of these IQN2 components.

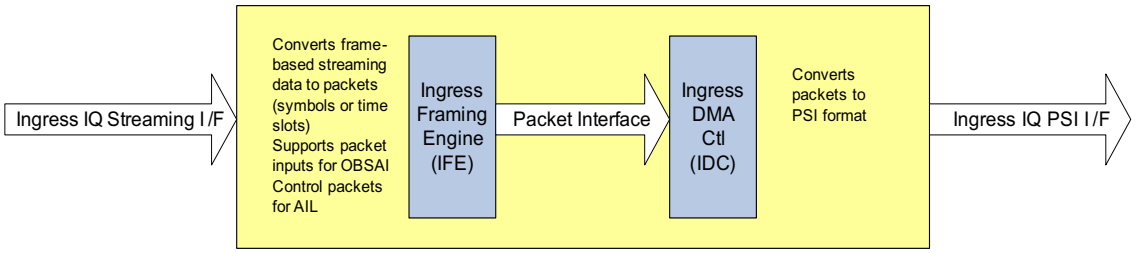
An IQN2 component has a single VBUSP configuration port that is connected to the SI via a SCR (not shown) so that all of the SI MMRs are located in the SI. The IQN2 component also aggregates the EEs from both SI and ICC. A Shutdown Controller is also included that orchestrates a safe shutdown of all of the blocks to support clock stop and emulation. This local Shutdown Controller is controlled by the Shutdown Controller in the IQN2 component.

Depending on the characteristics of the IQN2 that the SI will be used in, the PSI interfaces will connect to either a custom buffer, or IQS. The rest of this chapter will use the term “IQN buffer (IQNB)” when referring to the IQN2 element that connects to the SI PSI interfaces.

7.4.1 Ingress IQ

Figure 7-23 shows a block diagram of the SI Ingress IQ block. It consists of an Ingress Framing Engine (IFE) and an Ingress DMA Controller (IDC).

Figure 7-23. SI Ingress IQ Block Diagram



7.4.1.1 Ingress Framing Engine (IFE)

The IFE receives radio frame based streaming IQ data from the ICC that it is attached to and partitions it into packets which are framed with an SOP and an EOP. For all radio standards except WCDMA, the packets are OFDM Symbols or GSM Time Slots. For WCDMA, the packets are WCDMA Time Slots (i.e., 2560 chips or 640 QWDs).

Channels are enabled or disabled by SW. The actual Channel ON/OFF activity is controlled by radio frame timing. Once enabled via writing **IQ_IFE_CHAN_CFG[N].CHAN_EN**, a channel turns on when the next SOF is received from the ICC for that channel. Once disabled, the channel turns OFF on the next SYM/TimeSlot boundary for that channel. SW may read the ON/OFF status of each channel via **IQ_IFE_CHAN_ON_STS[N].CHAN_ON[N]**.

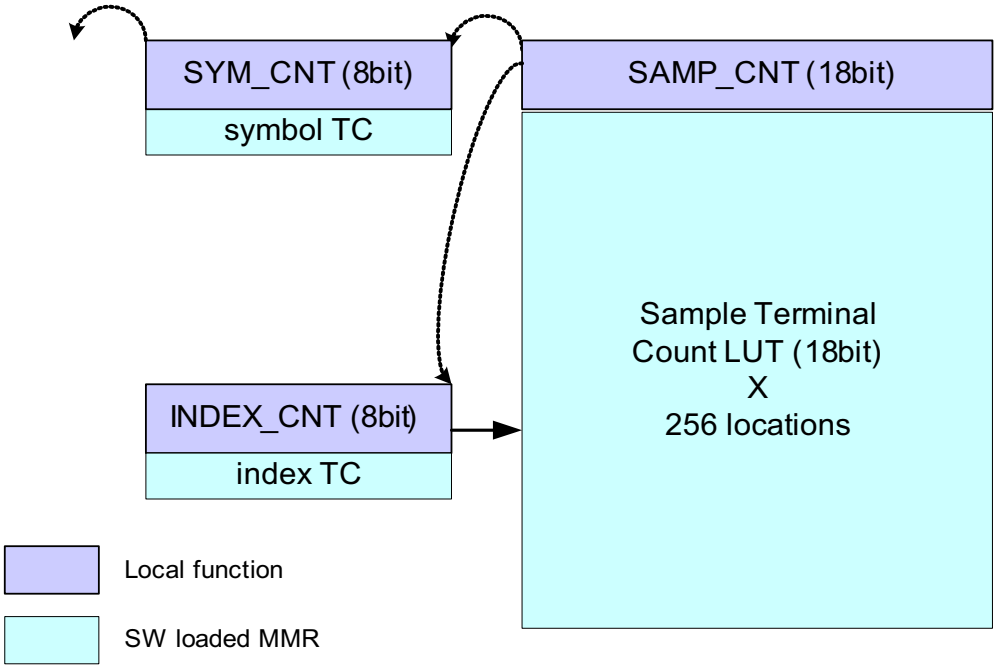
In the case of Global Disable, the channel ON/OFF behaves as if all channels are disabled and turns OFF on the next SYM/TimeSlot boundary for each of the channels. Global Disable is initiated by an MMR write of **IQ_IFE_GLOBAL_EN_CLR_STB**

In addition to tracking channel ON/OFF status, “in packet” status also is tracked. Every SOP written to the IDC places a channel “in packet.” Every EOP written to the IDC places a channel “out of packet.” **IQ_IFE_IN_PKT_STS[N].IN_PKT[N]** provides this packet status. For AxC channels, **IN_PKT[N]** is low for only the small period of time between the EOP and SOP. For TDD OFF channels, **IN_PKT[N]** is low for the duration of all OFF symbols.

7.4.1.1.1 Radio Framing FSM

The primary purpose of the Radio Framing FSM is to break up the streaming data from the ICC into smaller portions which make sense to the DMA system and the radio processing application SW or HW processing modules. The streaming data is partitioned into packets framed with SOP and EOP indicators. The packets are partitioned into OFDM Symbols, GSM Time Slots, or WCDMA Time Slots of 2560 chips (or 640 qwd).

Figure 7-24. SI_IFE: Radio Framing FSM



The Radio Framing FSM is used to support all channels. The IFE has a separate set of framing controls per radio standard variant (i.e., eight total), and the Radio Framing FSM uses the set that is assigned to the channel. The framing state of each channel is separately maintained.

The Radio Framing FSM configuration is radio-standard specific and used for {LTE, WCDMA, WiMax, TD-SCDMA, GSM} and their variants (e.g., LTE20Mhz, LTE10Mhz, etc.). The IFE has eight sets of framing counter configurations to support up to eight radio standard variants. The high degree of programmability is to satisfy all the special requirements of all the different radio standards.

The Radio Framing FSM has three fields or counters:

- **SAMP_CNT**: A per-channel, count down, sample counter that loads a terminal count value from the Sample Terminal Count LUT (**IQ_IFE_FRM_SAMP_TC_CFG[256].FRM_SAMP_TC)** at the start of every symbol **.** Since the Radio Framing FSM stores the value of **IQ_IFE_FRM_SAMP_TC_CFG[256].FRM_SAMP_TC** at the start of each symbol, SW can dynamically change the MMR value.
- **SYM_CNT**: A per-channel, count up symbol counter that increments by one each time the SAMP_CNT under flows.The state of SYM_CNT is presented to external circuits for the purpose of creating the symbol index for the PKTDMA. The Radio Framing FSM stores the value of **IQ_IFE_FRM_TC_CFG[8].FRM_SYM_TC** when it reaches the terminal count indicated by **IQ_IFE_FRM_TC_CFG[8].FRM_INDEX_TC** and SAMP_CNT under flows. This provides SW with a window where it can dynamically change **FRM_SYM_TC.**
- **INDEX_CNT**: A per-channel, count up index counter that increments by one each time the SAMP_CNT under flows. When it reaches the terminal count indicated by **IQ_IFE_FRM_TC_CFG[8].FRM_INDEX_TC** and SAMP_CNT under flows it wraps back to **IQ_IFE_FRM_TC_CFG[8].FRM_INDEX_SC**. The intent is that INDEX_CNT be either identical to SYM_CNT or wrap an even number of times within the total SYM_CNT. The INDEX_CNT is used to index the Sample Terminal Count LUT that supplies the length of each symbol to SAMP_CNT. This allows a set of different SYM/SLOT lengths to be supported.
- The Radio Framing FSM stores the value of **IQ_IFE_FRM_TC_CFG[8].FRM_INDEX_SC** and **IQ_IFE_FRM_TC_CFG[8].FRM_INDEX_TC** when it reaches the terminal count indicated by **FRM_INDEX_TC** and SAMP_CNT under flows. This provides SW a window where it can dynamically change **FRM_INDEX_SC** and **FRM_INDEX_TC**.

7.4.1.1.2 TDD s upport

Two modes of TDD are supported by the Radio Framing FSM. The first is called the TDD LUT mode, and it is controlled on a per-radio standard variant basis with a separate enable/disable control and TDD LUT for each variant. When it is enabled via **IQ_IFE_RAD_STD_CFG[8].TDD_LUT_EN**, the associated 160 entry TDD LUT (**IQ_IFE_TDD_EN_CFG[8][5].TDD_EN[32])** indicates which symbols are enabled/disabled for DMA. **SYM_CNT** is essentially used as an index into the TDD LUT.

The Radio Framing FSM makes use of the TDD configuration MMRs by storing the **TDD_EN** for the next symbol and the value of **TDD_LUT_EN** when the SAMP_CNT under flows. This provides SW a window where it can dynamically change **TDD_EN** and **TDD_LUT_EN**.

The second TDD mode is controlled on a per-channel basis via the **IQ_IFE_CHAN_CFG[N].CHAN_TDD_FRC_OFF** bit. This bit forces the channel into TDD OFF regardless of the TDD configuration of the radio standard variant the channel is assigned to (i.e., **TDD_EN** and **TDD_LUT_EN**). The channel enters TDD-OFF on the next symbol (i.e., SAMP_CNT under flows) after **CHAN_TDD_FRC_OFF** is set to a 1.

7.4.1.1.3 Multiple Radio Standard Support

The IFE can support eight simultaneous radio standard variants. These include the various standards and their variants (i.e., LTE3Mhz and LTE5Mhz are variants of LTE).

Each AxC is associated with one of the eight possible radio standard variants via the **IQ_IFE_CHAN_CFG[N].CHAN_RADIO_SEL** parameter. As an example, **IQ_IFE_CHAN_CFG[0].CHAN_RADIO_SEL** is programmed to 0x0 to associate it to radio standard variant #0.

The value of **CHAN_RADIO_SEL** selects the following parameters that control the framing and TDD behavior of each AxC:

- FRM_SAMP_TC
- FRM_SYM_TC

- FRM_INDEX_TC
- TDD_LUT_EN
- TDD_EN

7.4.1.1.4 OBSAI Control Message Support for AIL Applications

Channels can be configured to support OBSAI Control Message packets via **IQ_IFE_CHAN_CFG[N].CHAN_OBSAI_CTL**, which only exist for AIL applications. Since OBSAI Control Message packets are provided as packets by the ICC, the IFE handles these in an entirely different manner than AxC traffic. Wherever possible, the functions that already exist for AxC traffic are overloaded to support these messages.

7.4.1.2 Ingress DMA Controller (IDC)

The IDC receives packets from the IFE and converts them to a RX PSI format that drives the common IQNB which is in the VBUS_CLK domain. Since the IFE operates in the SYS_CLK domain in some applications, a clock domain crossing FIFO (CDC FIFO) is provided to interface the two clock domains. The IDC MMRs operate in both clock domains.

7.4.1.2.1 Data Swapper

The first stage of the IDC is the Data Swapper which performs programmable endian independent data and IQ swapping logic on a per-channel basis. This logic is controlled by **IQ_IDC_CH_CFG[N].DAT_SWAP** and **IQ_IDC_CH_CFG[N].IQ_ORDER**.

The internal format of the data before the data swapper is big endian since the IFE is natively big endian. Figure 7-25 shows an example of the data swapping schemes supported by the IDC. The CPUs in the system can be configured to operate in either big or little endian mode.

Figure 7-25. Data Swap

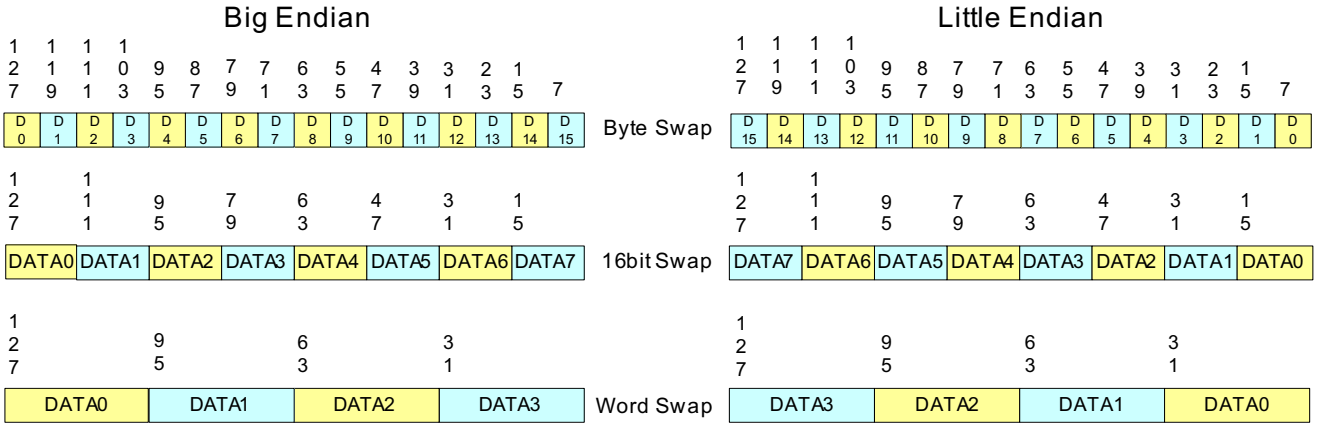
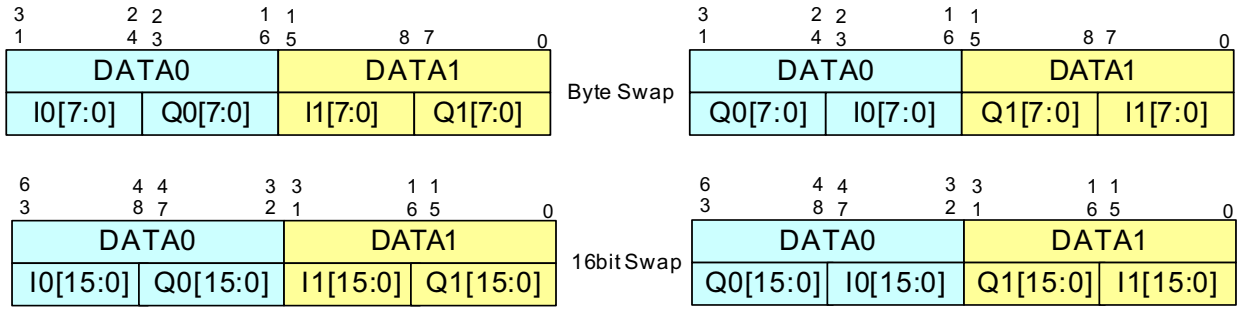


Figure 7-26 shows example of the IQ swapping schemes supported by the IDC.

Figure 7-26. IQ Swap



7.4.1.2.2 Force off controller

The SII_IQ can force off all of the channels or a single channel without waiting for a Symbol/TimeSlot boundary for AxC channels or an EOP for OBSAI control channels. This feature allows channels to be shut off in cases where the input data is abruptly lost and cannot be shut down in the normal, traffic-driven manner.

When channels are truncated, the PktDMA can be left with “open packets” for those channels. This is a problem, because buffers allocated in the SoC for those channels will not be available for other uses, and also the PKTDMA will not respond to RX tear-down requests for those channels. These issues are solved by having the Force Off Controller (FOC) close out any channels with “open packets” by generating an EOP for the channels.

The Force Off Controller (FOC) can be configured to force off all of the channels supported by the SII_IQ via **IQ_IDC_CFG.FRC_OFF_ALL**. For AIL applications, the FOC also can be triggered to close all of the channels when the PHY looses sync for the entire link. The FOC can be configured to allow this condition to force off all of the channels via **IQ_IDC_CFG.RM_FAIL_FRC_OFF_EN**, which is only defined for AIL applications.

The FOC can be configured to individually force off a channel via **IQ_IDC_CHAN_CFG[N].CHAN_FRC_OFF**. The FOC waits until the channel is in the CHAN_OFF state and then inserts an EOP into the PSI Staging FIFO for the channel. All packets closed in this manner are marked as having an error and may also be dropped by the PKTDMA if **IQ_IDC_CFG.FAIL_MARK_ONLY** is set to zero.

7.4.1.2.3 Rate Controller

Based on the MMR value programmed into the Rate Controller (RC), the PSI Controller throttles the master thread ready signals to control the BW of the data sent to the IQNB. This function is required because data from the ICC may burst into the SI, suddenly requiring a large amount of bandwidth and potentially overwhelming the IQNB.

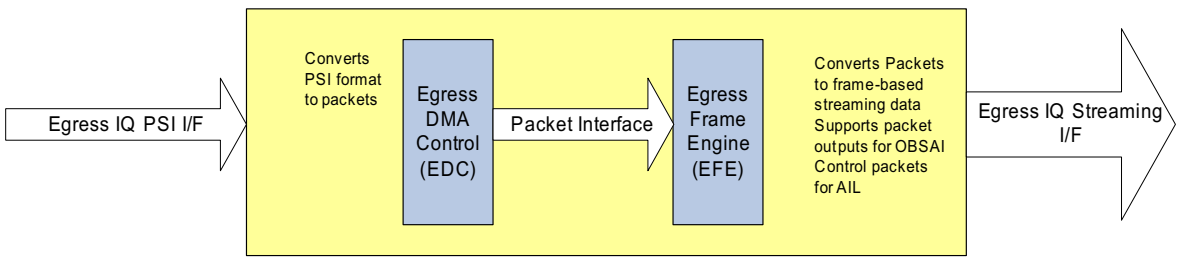
The rate-control algorithm is based on bus utilization within a 16-clock cycle window. The RC sums the number of active cycles (i.e., request cycles from IQNB) within this 16-clock cycle window and compares it to the value programmed in **IQ_IDC_RATE_CTL_CFG.RATE**[3:0] + 1. If the number of active cycles is greater than or equal to this value, the RC drives thread enable low, otherwise thread enable will be driven high.

Example: **IQ_IDC_RATE_CTL_CFG.RATE** = 0; This MMR is programmed to the number of active cycles allowed in the 16-clock window minus 1. A value of 0 means that the PSI Controller can only send one transaction to the IQNB within the window. A value of 15 means that the PSI Controller can use all 16 clock cycles of the window (100% BW)

7.4.2 Egress IQ

Egress IQ module consists of an Egress DMA Controller (EDC) and an Egress Framing Engine (EFE). Figure 7-27 shows a block diagram of the SI Egress IQ block.

Figure 7-27. SI Egress IQ Block Diagram



7.4.2.1 Egress DMA Controller (EDC)

The EDC requests packet data from the IQNB, and it is delivered on a 128-bit slave Tx PSI interface (Scheduler). The EFE reads this data approximately every 4-samples/chips of time for AxC channels. Since the IQNB is operating in the VBUS clock domain (*vbus_clk*) and the EFE is operating in the system clock domain (*sys_clk*), a clock domain crossing FIFO (CDC FIFO) is provided.

7.4.2.1.1 PSI Error Checks

The Scheduler checks the PSI *data_type* and the number of PS data phases and creates an EE event (*si_ee_egr_iq_psi_data_type_err*) if it detects errors. PSI *data_type* errors include unsupported data types for both AxC and OBSAI Control channels, packets with no PS data for AxC channels, and packets with extra PS data for both AxC and OBSAI Control channels.

If **IQ_EDC_CFG.PSI_ERR_CHK_DISABLE** is 0, the EDC scheme for handling *data_type* errors is to convert the data phase with the *data_type* error and all subsequent data phases for the remainder of the packet to all zeros, which is a safe value. When **IQ_EDC_CFG.PSI_ERR_CHK_DISABLE** is one, the Scheduler still detects missing PS data and extracts the symbol number, which will cause the EFE to detect a symbol error and flush the channel.

7.4.2.1.2 Data Swapper

The Data Swapper performs programmable endian independent data and IQ swapping logic on a per-channel basis. This logic is controlled by **EDC_CH_CFG[N].DAT_SWAP** and **EDC_CH_CFG[N].IQ_ORDER**. The EDC swapper works in exactly the reverse order of IDC swapper. See Section 7.4.1.2.1 for more detail.

7.4.2.1.3 Debug Support

The EDC debug support includes the following:

- 24-bit SOP counter (**IQ_EDC_SOP_CNTR_STS**) that increments each time the Scheduler receives an SOP over the PSI. This counter wraps when it reaches its max. count.
- 24-bit EOP counter (**IQ_EDC_EOP_CNTR_STS**) that increments each time the Scheduler receives an EOP over the PSI. This counter wraps when it reaches its max. count.

If the user can see only SOP increase without increments of EOP, it indicates there is a non-proper configuration in the SI or ICC.

7.4.2.2 Egress Framing Engine (EFE)

The EFE converts loosely-timed DMA data into strictly-timed data to the ICC using radio time. Micro AT timing strobes are used as the exact timing reference. As part of the operation, the EFE exactly predicts the DMA data packetization via the Radio Framing FSM. If packetization errors or starvation are detected, EFE inserts zero traffic, and re-synchronizes DMA traffic to the next radio frame boundary. In a sense, the Radio Framing FSM is the synchronization master and the DMA traffic is the slave.

The EFE can be thought of as having an input stage and an output stage. The output timing is dictated by Micro AT timing signals, while the input stage operations are driven by the availability of buffer. The LTE3MHz and LTE1.4MHz radio standards have packet lengths which are not always quad-word aligned (i.e., last QWD of packet is not fully populated). The EFE concatenates these types of DMA packets to form whole quad-words for ICC consumption.

EFE can handle both AxC and OBSAI Control packets, and channels are configured for AxC traffic when **IQ_EFE_CHAN_CFG[N].CHAN_OBSAI_CTL** is 0. OBSAI Control channels that carry Ethernet frames are configured when **IQ_EFE_CHAN_CFG[N].CHAN_ENET_CTL** and **IQ_EFE_CHAN_CFG[N].CHAN_OBSAI_CTL** are both 1.

AxC channels that carry GSM compressed mode traffic for AIL applications are treated in the same manner as OBSAI Control channels. GSM compressed mode channels are configured on a radio standard variant basis via **IQ_EFE_RAD_STD_CFG[8].GSM_CMP_MODE**.

7.4.2.2.1 Scheduler for AID and DIO Applications

The Scheduler for AID and DIO applications consists of a Visitation Engine and a TDM LUT. The Micro AT. The Visitation Engine can support up to eight radio standard variants simultaneously. It receives the 4-sample strobes and frame boundary strobes for each of the radio standard variants from the Micro AT and starts the visitation process (i.e., wakes up) when one of the 4-sample strobes fire.

The TDM LUT is a 256x8-bit RAM where each entry consists of a 7-bit channel number (**IQ_EFE_CHAN_TDM_LUT_CFG[256].CHAN_INDEX[7])** and an enable bit (**IQ_EFE_CHAN_TDM_LUT_CFG[256].CHAN_INDEX_EN[1])**. The entries are allocated to each radio standard variant via MMR values with the starting address in the TDM LUT for the radio standard variant (**IQ_EFE_RAD_STD_SCH_CFG[8].TDM_START**) and its length (**IQ_EFE_RAD_STD_SCH_CFG[8].TDM_LEN**).

The TDM LUT is configured via the VBUSP interface to the SI. The Scheduler supports dynamic changes to the TDM LUT, but certain rules which are outlined below must be followed.

- Adding a channel on the fly to the end of the radio standard variant LUT table:
  - New channel must be in the CHAN_OFF state
  - Set **CHAN_INDEX_EN** bit in entry that will be added
  - Enable channel via **IQ_EFE_CHAN_CFG[N].CHAN_EN**
  - Increment LUT length via **IQ_EFE_RAD_STD_CFG[8].TDM_LEN**
  - Channel is not “in service” until it is in the CHAN_ON state. This synchronizes the addition of a new channel to a frame boundary with an adjustment for the AxC Offset. Any visitations before CHAN_ON state results in 0 data sent to the ICC.
- Deleting a channel on the fly:
  - Disable channel via **IQ_EFE_CHAN_CFG[N].CHAN_EN**
  - Channel is not “out of service” until it is in the CHAN_OFF state. This synchronizes the deletion of a channel to the end of a Symbol/Time slot.
  - Clear **CHAN_INDEX_EN** bit in LUT
- Enabling and disabling a radio standard variant
  - A radio standard variant is enabled via **IQ_EFE_RAD_STD_CFG.EN**. Once enabled, the visitations start at the next SOF.
  - Once a radio standard variant is disabled, the visitations will stop immediately. Therefore, it is the responsibility of the user to ensure that all of the AxC channels associated with a radio standard variant are in the CHAN_OFF state before it is disabled. This is accomplished by disabling each AxC channel associated with the radio standard variant via **IQ_EFE_CHAN_CFG[N].CHAN_EN** and waiting for all of the associated channels to reach the CHAN_OFF state. This can be detected via **IQ_EFE_CHAN_ON[N/32].CHAN_ON_STS**.
- The position on any channel in the CHAN_ON state cannot be changed in the LUT. The channel has to be deleted and then added. Fragmentation of the LUT table can occur when channels are deleted. This shows up as wasted reads of the LUT table that do not result in any visitations.

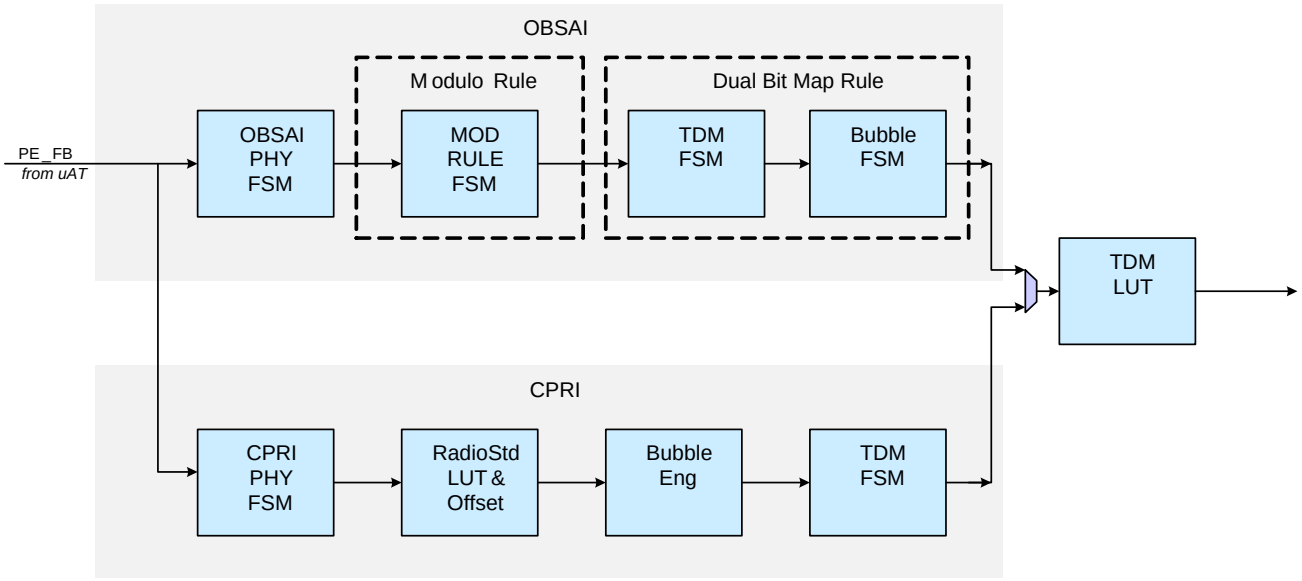
7.4.2.2.2 Scheduler for AIL Applications

Largely, the SI_E AIL_PE scheduler is comprised of two independent circuits, one each for CPRI/OBSAI. In general, there are several similar concepts in both schedules:

- PHY FSM
- Channel visitation FSM/Rule
- Bubble FSM (rate matcher)

In OBSAI operation, the OBSAI scheduler samples and holds the uAT RadT for the entire duration of the TDM. In CPRI operation, the uAT RadT values are unused. Both OBSAI and CPRI are able to share the TDM LUT which lists channel numbers in order of visitation. The LUT is partitioned by the user to be shared between multiple flows within the PHY. CPRI flows are radio standards while OBSAI flows are more generic transmission rules.

Figure 7-28. SI_E AIL_PE Scheduler



7.4.2.2.3 AIL_PE CPRI SI_E Scheduler

There are three different offset concepts in CPRI:

- PHY Offset: The PHY turns on when the uAT pe-fb fires. This is effectively an advanced “delta” compare value against the BCN counter.
- Radio Standard Offset: CPRI5.0 introduces the concept of groups of AxC. AIL refers to these groups as radio standards. The TDM & Bubble FSM of group is permitted to start at an offset relative to the PHY frame boundary. This offset may only be whole basic frames.
- AxC Offset: This is an extension of OBSAI which is not really specified in CPRI. AIL allows every AxC within a group to be offset relative to the Radio Standard Offset. Simplistic programming of AIL can zero the radio and AxC offsets

Each CPRI AxC container (repeating each basic frame) is progammably mapped to a radio standard. For rate matching radio standards such as GSM into the CPRI PHY (which is WCDMA/LTE orientated) some stuffing samples are required. This operation is more generically called “bubble insertion.” After other operations, CPRI visitations of AxC are simply in a TDM repeating pattern.

The TDM is implemented via a lookup table, but other circuit implementation limitations restrict the use of this LUT to be either one entry per AxC, or bursts of consecutive entries per AxC. It is illegal to program the LUT with multiple entries for any given AxC with other AxC interleaved between the entries. (AIF2 supported this flexible interleaving but it is illegal for IQN2.)

PE_TDM_LUT_CFG[256]: For CPRI: Used to map streams of CPRI containers to appropriate AxC. AxCs are listed in TDM order within each group (radio standard). Different portions of LUT allocated to different groups (radio standards). The number of TDM LUT used should be matched with the real container number used in the AxC container group (could be multiple basic frames).

For OBSAI: AxCs are listed in TDM order per OBSAI DBMR. Different portions of LUT are allocated to different DBMR. The number of TDM LUT used will be matched with the number of AxCs within DBMR.

PE_TDM_LUT_CFG[256].AXC: List of AxC indexes giving TDM AxC order.

PE_TDM_LUT_CFG[256].EN: Enables each entry. Disabled entries will result in OBSAI Empty Message or CPRI empty container. LTE1.4MHz for CPRI requires disabling of certain containers and it allows only limited BW to be used.

7.4.2.2.4 AIL_PE OBSAI SI_E Scheduler

OBASI supports transmission rules in three parts:

- Modulo
- Dual Bit Map
- TDM Look Up Table (shared between CPRI/OBSAI)

The implementation of the Modulo Rule Circuit is a straightforward counter-based approach. 32 different versions of the same circuit are concurrently operating. The counter is programmed with:

- Modulo (12 bits): Modulo-1 is the terminal count.
- Index (12 bits): Indicates at which count, the circuit will enable transmission.
- En (1bit): Enables the counter (if off, output will never fire).
- DBMR_EN (1bit): Enables Dual Bit Map as 2 nd Rule stage, otherwise output will bypass the DBMR circuit simply using the first entry from the AxC LUT.
- DatCtrl (1bit): 1'b1: only responds to AxC data msgs.; 1;b0: only responds to control msgs.

The counter simply resets to zero at each Frame boundary and increments by +1 whenever the appropriate link and data vs. control message is active. When the counter reaches a terminal count of (Modulo – 1) the counter wraps back to 0.

For a given link, only one Modulo rule may fire in a given cycle. It is considered a programming error for multiple Modulo rules to fire and will yield unpredictable results. If two rules fire simultaneously both rules may be unrecoverably corrupted until the rules are disabled, then restarted.

The Dual Bit Map Rules (DBMR) circuit is basically a counter that circularly TDM X channels. Every time the Modulo Rule Fires, the next channel is serviced. Note that at the end of round robin TDM servicing of X channels, a gap of xbubble messages is added. The gap is controlled by the "Bit Maps."

The Bubble FSM consists of a state machine following the Dual Bit Map algorithm. In every state, a single bit of either of the two "Bit Maps" indicates:

- 1'b1: after the "X" count, one additional xbubble count prior to rewinding X count
- 1'b0: after the "X" count, simple start over again

The concept of a bubble is wasted BW where an OBSAI Empty Message is sent out over the PHY in place of productive traffic.

Table 7-6. OBSAI Dual Bit Map FSM Fields

Parameter	Definition	OBSAI Width (bits)	AIL Width (bits)
X	Maximum number of AxC that will fit into a given virtual link. Zero indicates one AxC	-	6
Bit_Map_1_Mult	Number of times the first bit map is repeated. Zero represents one use of bit map1	-	8
Bit_Map_1	Value of the first Bit Map. The Bit Map is read starting from the right most (LSB) bit. The 32bit word in the lowest address is read first.	80	128
Bit_Map_1_Size	Size of the first Bit Map (number of bits). Zero represents length of one.	7	7
Bit_Map_2	Value of the second Bit Map. The Bit Map is read starting from the right most (LSB) bit. The 32bit word in the lowest address is read first.	48	96
Bit_Map_2_Size	Size of the second Bit Map (number of bits). Zero indicates **zero** length.	6	7

The algorithm is pretty simple. After every X or X+1 count, the use of the bit map is advanced by one position. Bit_Map_1 is used Bit_Map_1_Mult times then Bit_Map_2 is used once. Then the operation is repeated. When "using" a bit map, only a portion of the bit map is used, indicated by Bit_Map_1_Size and Bit_Map_2_Size.

7.4.2.2.5 AxC Offset

The SI Egress supports per-channel AxC offsets. These are used to effectively shift the frame boundary of the AxC relative to the frame boundary of the radio standard variant.

- **AIL OBSAI:** AXC_OFFSET is programmed in *sys_clk* cycles and used to compare against the RADT provided by the Micro AT. The offset within a QWD, for each AxC channel is provided by **IQ_EFE_CHAN_CFG[N].AXC_FINE_OFFSET[2].**

NOTE: **AXC_FINE_OFFSET** is not specified in the OBSAI standard. Configure as 0 for pure OBSAI compliance. The **AXC_FINE_OFFSET** field is only defined for AIL applications.

- **AIL CPRI:** AXC_OFFSET is programmed in number of samples. The offset within a QWD for each AxC channel is provided by **AXC_OFFSET[**1:0 **].**
- **AID/DIO:** Same as AIL CPRI.

7.4.2.2.6 Channel ON/OFF

A channel may turn ON only at a radio frame boundary. A channel may turn OFF on any SYM/SLOT boundary (SYM is an LTE/WiMax concept and SLOT is a similar GSM/WCDMA concept). For OBSAI, the radio frame boundary for each radio standard variant is implied when the RADT_CNT for the assigned radio standard variant from the Scheduler crosses the AxC offset value.

The CHAN_ON concept is basically **IQ_EFE_CHAN_CFG[N].CHAN_EN** re-timed to the frame boundary for the radio standard variant that the channel is assigned to. **IQ_EFE_CHAN_ON[N/32].CHAN_ON_STS** gives SW visibility to the CHAN_ON status. When **CHAN_ON_STS** is active for a channel, the EFE will feed a constant stream of zeros to the ICC until DMA data is available.

7.4.2.2.7 DMA SYNC

The DMA SYNC concept is based on a channel being in the CHAN_ON state and synchronized to DMA data. It only applies to AxC channels and will not be driven for OBSAI Control channels. The DMA SYNC state is entered once a DMA SOF is detected. Once disabled via **IQ_EFE_CHAN_CFG[N].CHAN_EN** or during shutdown via *global_en*, the channel exits the DMA SYNC state on the next SYM/SLOT boundary. **IQ_EFE_DMA_SYNC[N/32].DMA_SYNC_STS** gives SW visibility to the DMA SYNC status.

Additionally, the channel exits the DMA SYNC state immediately for any flush condition. A flushed channel will naturally go back into the DMA SYNC state on the next DMA SOF boundary. The DMA SOF occurs on the SOP for a SYM/SLOT with the SYM/SLOT number of 0 for non-TDD channels or the SYM/SLOT number matches the value in **IQ_EFE_RAD_STD_CFG[8].TDD_FIRST_SYM** for TDD channels.

7.4.2.2.8 Radio Framing FSM

The primary function of the Radio Framing FSM is to sequence through AxC channels at precise radio sample instances (i.e., visitations from the Scheduler) while predicting framing conditions for each AxC channel's data stream (i.e., SOF, SOP, EOP, and SYMBOL #).

The Radio Framing FSM configuration is radio standard specific and used for {LTE, WCDMA, WiMax, TD-SCDMA, GSM} and their variants. The Controller has eight sets of framing counter configurations to support up to eight radio standard variants. The high degree of programmability is to satisfy all the special requirements of all the different radio standards. The Radio Framing FSM diagram is exactly the same as the SI_IFE Radio Framing FSM diagram in Section 7.4.1.1.1.

The Radio Framing FSM is used for AxC channels only. A separate FSM is maintained per AxC channel and configured via per-radio standard variant MMRs as explained below. An FSM starts on a frame boundary when the FSM detects that the channel has gone into the CHAN_ON state.

The Radio Framing FSM has three major fields or counters:

- **SAMP_CNT**: A per-channel, count down, sample counter that loads a terminal count value from the Sample Terminal Count LUT (**IQ_EFE_FRM_SAMP_TC_CFG[256].FRM_SAMP_TC)** at the start of every symbol **.** Since the Radio Framing FSM stores the value of **IQ_EFE_FRM_SAMP_TC_CFG[256].FRM_SAMP_TC** at the start of each symbol, SW can dynamically change the MMR value.

- **SYM_CNT**: A per-channel, count up symbol counter that increments by one each time the SAMP_CNT under flows. When it reaches the terminal count indicated by **IQ_EFE_FRM_TC_CFG[8].FRM_SYM_TC** and SAMP_CNT under flows, it sends a frame boundary strobe to external circuits and wraps back to zero (also resets the INDEX_CNT).
- The Radio Framing FSM stores the value of **IQ_EFE_FRM_TC_CFG[8].FRM_SYM_TC** when it reaches the terminal count indicated by **IQ_EFE_FRM_TC_CFG[8].FRM_INDEX_TC** and SAMP_CNT under flows. This provides SW with a window where it can dynamically change **FRM_SYM_TC**.
- **INDEX_CNT**: A per-channel, count up index counter that increments by one each time the SAMP_CNT under flows. When it reaches the terminal count indicated by **IQ_EFE_FRM_TC_CFG[8].FRM_INDEX_TC** and SAMP_CNT under flows, it wraps back to **IQ_EFE_FRM_TC_CFG[8].FRM_INDEX_SC**. The intent is that INDEX_CNT should be either identical to SYM_CNT or wrap an even number of times within the total SYM_CNT. The INDEX_CNT is used to index the Sample Terminal Count LUT that supplies the length of each symbol to SAMP_CNT. This allows a set of different SYM/SLOT lengths to be supported.
- The Radio Framing FSM stores the value of **IQ_EFE_FRM_TC_CFG[8].FRM_INDEX_TC** and **IQ_EFE_FRM_TC_CFG[8].FRM_INDEX_TC** when it reaches the terminal count indicated by **FRM_INDEX_TC** and SAMP_CNT under flows. This provides SW a window where it can dynamically change **FRM_INDEX_SC** and **FRM_INDEX_TC**.

7.4.2.2.9 TDD Handling

Two modes of TDD are supported by the Radio Framing FSM. The first is called the TDD LUT mode, and it is controlled on a per-radio standard variant basis with a separate enable/disable control and TDD LUT for each variant. When it is enabled via **IQ_EFE_RAD_STD_CFG[8].TDD_LUT_EN**, the associated 160 entry TDD LUT (**IQ_ EFE_TDD_EN_CFG[8][5].TDD_EN[32])** indicates which symbols are enabled/disabled (i.e., TDD-ON/TDD-OFF) for DMA. **SYM_CNT** is used as an index into the TDD LUT. The symbol number of the first enabled symbol of a radio frame for each radio standard variant when it is in TDD mode is provided in **IQ_EFE_RAD_STD_CFG[8].TDD_FIRST_SYM**.

The Radio Framing FSM makes use of the TDD configuration MMRs by storing the **TDD_EN** for the next symbol, the value of **TDD_LUT_EN**, and the value of **TDD_FIRST_SYM** when the SAMP_CNT under flows. This provides SW a window where it can dynamically change these values.

The second TDD mode is controlled on a per-channel basis via the **IQ_EFE_CHAN_CFG[N].CHAN_TDD_FRC_OFF** bit. This bit forces the channel into TDD OFF regardless of the TDD configuration (i.e., **TDD_EN**, **TDD_LUT_EN**, and **TDD_FIRST_SYM**) of the radio standard variant the channel is assigned to. The channel enters TDD OFF on the next symbol (i.e., SAMP_CNT under flows) after **CHAN_TDD_FRC_OFF** is set to a 1. The channel will exit TDD OFF on the next symbol (i.e., SAMP_CNT under flows) after **CHAN_TDD_FRC_OFF** is set to a 0.

NOTE: Use cases for **CHAN_TDD_FRC_OFF** would most likely require an AT system event that wakes up a CPU on a particular symbol to put a channel in TDD OFF on the next symbol for a period of time. One intended use is GSM BB Hopping.

7.4.2.2.10 GSM Support (AIL Applications Only)

The SI Egress supports GSM compressed mode on a per-radio standard variant basis via **IQ_EFE_RAD_STD_CFG[8].GSM_CMP_MODE**. In this mode, the actual length of the packet received from the SOC or IQN2 peer is less than the programmed slot length in **IQ_EFE_FRM_SAMP_TC_CFG[256].FRM_SAMP_TC**. For OBSAI, the unpopulated portion of the GSM slot is legal and replaced with OBSAI Empty Messages in the ICC. For CPRI, it is replaced with 0 data.

Base band hopping for AxC channel:

The SI Egress supports GSM BB Hopping for AxC channels. In this mode, AxC traffic hops between a group of channels on a symbol-by-symbol basis. This behavior is supported in the Radio Framing FSM in a manner similar to how it supports TDD mode. A radio standard variant can be configured to support GSM BB Hopping for AxC channels via **IQ_EFE_RAD_STD_CFG[8].GSM_AXC_BBHOP_MODE**. The Controller sends OBSAI empty messages to the ICC for visitations to TDD-OFF symbols due to either

CHAN_TDD_FRC_OFF or TDD_LUT_EN for both OBSAI and CPRI. Although, zero data is also sent to the ICC for visitations to TDD-OFF symbols for AxC channels not configured for GSM BB Hopping, OBSAI empty messages (internal signal for CPRI) are not sent. For OBSAI, this means the channel is not valid for any AxC during the symbol time. For CPRI, the OBSAI empty message signal is delivered to ICC, which means the zero data does not indicate the channel is valid during the symbol time.

Base band hopping for OBSAI Control channel: (OBSAI only)

The SI Egress also supports the power control messages for GSM BB Hopping which are sent to the PE as OBSAI Control packets. A full or partial (address only) OBSAI header is sent to the PE via protocol specific field in descriptor header.

7.4.3 Ingress Control (ICTL)

The ICTL module provides a common interface between the components of an IQN2 (i.e., AID and AIL) and the IQN2 buffer for control information for the Ingress path. The ICTL receives packets from the ICC and converts them to a Rx PSI format that drives the common IQNB which is in the VBUS_CLK domain. The destination of these PSI packets is the PKTDMA in IQN2.

Channels are enabled or disabled by SW. The actual Channel ON/OFF activity is controlled by ICC packet status. Once enabled, via writing, **ICTL_CHAN_EN_CFG[N].CHAN_EN**, a channel turns on when the next SOP is received from the ICC for that channel. Once disabled, the channel turns OFF on the next EOP for that channel. SW may read the ON/OFF status of each channel via **ICTL_CHAN_ON_STS.CHAN_ON[N]**.The Force Off Controller (FOC) can be configured to force off all of the channels supported by the SI ICTL via **ICTL_CFG.FRC_OFF_ALL**.

In addition to tracking channel ON/OFF status, “in packet” status also is tracked. Every SOP written to the ICTL places a channel “in packet.” Every EOP written to the ICTL places a channel “out of packet.” **ICTL_IN_PKT_STS.IN_PKT[N]** provides this packet status.

For AIL applications, the FOC also can be triggered to close all of the channels when the PHY looses sync for the entire link. The FOC can be configured to allow this condition to force off all of the channels via **IQ_IDC_CFG.RM_FAIL_FRC_OFF_EN**, which is only defined for AIL applications.

Global enable/disable for all ICTL channels. Disable causes all “On” channels to gracefully shutdown on next packet EOP. This can be controlled by writing to **ICTL_GLOBAL_EN_SET** and **ICTL_GLOBAL_EN_CLR** and read via **ICTL_GLOBAL_EN_STS**.

7.4.3.1 Rate Controller (RC)

Based on the MMR value programmed into the ICTL Rate Controller, the PSI Controller will remove/delay master thread ready to give CTL data more or less BW. This function is required because control data from the ICC may burst data into the ICTL thus, suddenly requiring a large amount of bandwidth and potentially overwhelming the IQNB.

The rate control algorithm is based on bus utilization within a 16-clock cycle window. The RC sums the number of active cycles (i.e., request cycles from IQNB) within this 16-clock cycle window and compares it to the value programmed in **ICTL_RATE_CTL_CFG.RATE**[3:0] + 1. If the number of active cycles is greater than or equal to this value, the RC will drive enable low, otherwise enable will be driven high.

Example: **ICTL_RATE_CTL_CFG.RATE** = 0; The percentage of BW requested would be 1/16 = 6%.

The IQN2 should not request data from the system at a rate greater than 25% to 33% (i.e., 1 out of 4 clocks to 1 out of 3 clocks) of the maximum rate supported by the VBUSM connected to IQN2. As such, the IQ data rate plus CTL data rate plus the rate of the normal traffic should not exceed 25% to 33% of the maximum VBUSM rate.

7.4.3.2 Debug Support

The ICTL debug support includes the following:

- 24-bit SOP counter (**ICTL_SOP_CNTR_STS**) that increments each time the PSI Controller sends an SOP over the PSI. This counter wraps when it reaches its max count.
- 24-bit EOP counter (**ICTL_EOP_CNTR_STS**) that increments each time the PSI Controller sends an EOP over the PSI. This counter wraps when it reaches its max count.

7.4.4 Egress Control (ECTL)

The ECTL module provides a common interface between the components of an IQN2 (i.e., AID and AIL) and the IQN2 buffer (IQNB) for control information for the Egress path. The ECTL requests Control Data via the IQNB and it is delivered on a 128-bit slave Tx PSI interface (Scheduler). The packet data and associated sideband information (e.g., SOP, EOP) are stored in the Data Buffer.

Channels are enabled or disabled by SW. The actual Channel ON/OFF activity is controlled by ICC packet status. Once enabled, via writing **ECTL_CHAN_CFG[N].CHAN_EN**, a channel turns on immediately. Once disabled, the channel turns OFF on the next EOP sent to the ICC for that channel or immediately if the channel is not in packet.

In addition to tracking channel ON/OFF status, “in packet” status also is tracked. Every valid SOP to the ECTL places a channel “in packet.” Every EOP to the ECTL places a channel “out of packet.” **ECTL_IN_PKT_STS.IN_PKT[N]** provides this packet status.

Global enable/disable for all ECTL channels. Disable causes all “On” channels to gracefully shutdown on next packet EOP. This is an internal register whose state can be changed by writes to **ECTL _GLOBAL_EN_SET** and **ECTL _GLOBAL_EN_CLR** and read via **ECTL _GLOBAL_EN_STS**.

7.4.4.1 Rate Controller

Based on the MMR value programmed into the ECTL Rate Controller via **ECTL_RATE_CTL_CFG**, the Scheduler will remove/delay slave thread ready to give the ECTL data more or less BW.

7.4.4.2 DB Threshold Setup

The per-channel data available indication is based on either an EOP present in the Data Buffer or the threshold value programmed in the per-channel **ECTL_DB_THOLD_CFG[N]** register. (N = 0~ 15 for AID and 0 ~ 3 for AIL)

Example1: **ECTL_DB_THOLD_CFG[0]** = 0 (default) The Data Buffer indicates data available for channel “0” if there is any data in the buffer.

Example2: **ECTL_DB_THOLD_CFG[2]** = 1 The Data Buffer indicates data available for channel “2” once the threshold of “2” Quad Words of data in the buffer is reached and the buffer does not go empty or there is an EOP in the buffer for channel 2.

Example3: **ECTL_DB_THOLD_CFG[2]** = 3 The Data Buffer indicates data available for channel “2” once the threshold of “4” Quad Words of data in the buffer is reached and the buffer does not go empty or there is an EOP in the buffer for channel 2.

7.4.4.3 Debug Support

The EDC debug support includes the following:

- 24-bit SOP counter (**ECTL_SOP_CNTR_STS**) that increments each time the Scheduler receives an SOP over the PSI. This counter wraps when it reaches its max. count.
- 24-bit EOP counter (**ECTL_EOP_CNTR_STS**) that increments each time the Scheduler receives an EOP over the PSI. This counter wraps when it reaches its max. count.

7.4.5 Micro AT (uAT)

The Micro AT (uAT) generates local timing information in radio time in the form of programmable strobes, typically frame strobes or four sample strobes. The uAT has a base timer (BCN) and radio timers. Strobes are generated based on these timers. The uAT BCN is synchronized to a master AT by capturing the uAT BCN upon receiving MstSlvSync from the AT master. This value is used by software to determine what offset should be applied to the free-running BCN so adjusted BCN_CNT value can be provided, which will be used in Delta by the TM as well as having an accurate time reference for generating strobes. The RADTs operate in the same fashion as BCN and have offsets programmed by SW to get true reference time for generating strobes.

The programmer will understand that the timing of the MstSlvSync is based on AT BCN time and program all offsets to BCN or RADTs according to the sync capture value which is captured offset BCN value.

PI Capture and Rp3-01 Capture are also captured offset BCN values upon their respective capture strobes. Also, frame boundary signal is used to qualify the captured offset BCN for PI checking.

A Pi window is set by software in two registers, one for Pi max. and one for Pi min. An error interrupt will be generated when the captured Pi BCN is outside of that window. The **uat_pi_bcn_capture_sts** MMR also has a field, **kchar_position** that captures if the k-character was received on the upper or lower received byte.

Rp3-01 capture happens when the uAT is strobed by the AIL PD. The PD has an interrupt pd_ee_rp3_01_capture_info. When this interrupt occurs, the rp3-01 capture register may be read by SW.

There are 22 RADT events which are enabled by the uAT to handle up to eight different radio standards simultaneously and drive the SI ingress, SI egress, DIO ingress, and DIO egress.

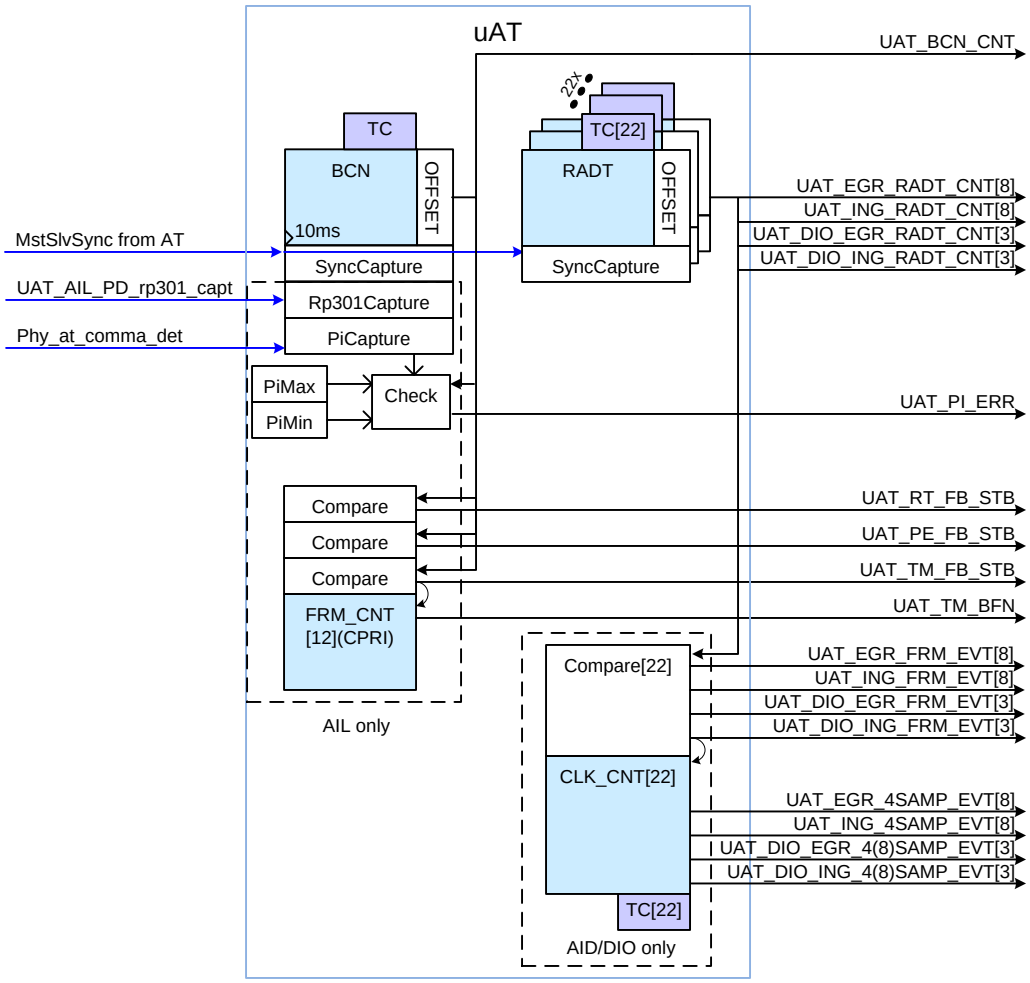
Different strobes based on BCN or RADTs are generated for different applications. The two applications described here are for AIL and for AID/DIO. AIL will be BCN-based for CPRI and both BCN and RADTs will be used for OBSAI. AID/DIO will be radio time based.

Procedure for uAT startup:

- SW sets up the IQN2 AT.
- SW writes all uAT RADT, BCN and event timer terminal counts.
- AT is started.
- The uAT run bit is set by SW in the uat_cfg MMR to start up the uAT.
- When a sync is received from the AT after a frame boundary, SW may be alerted by an AT frame boundary event.
- The timer values for RADTs and BCN will be captured by hardware and read by SW.
- SW will then adjust the RADTs and BCN offsets to adjust these timers based on the captured values.
- The targets of uAT may then enable the use of uAT outputs, like the frame boundary and four sample strobes as well as BCN and RADT values.

For the AIL application, SW may write a new value to the BCN frame counter at any time depending on system frame BFN information received outside of uAT, because the original frame counter might not be matched with BFN number from outside when the BCN counter updated by offset register setup.

Figure 7-29. uAT Block Diagram



Micro AT event is generated by setting a compare register to compare with the RADT or BCN offset-adjusted count. The compare value is used for frame boundary strobes. That means users can add frame level offset by using this register. This also can be done by updating BCN or RADT offset registers. It is the user's responsibility to match master AT RADT offset with uAT RADT offset.

AID/DIO also have 4-sample strobes which will be triggered on its associated frame strobe (FRM_STB) and use a counter to generate a 4-sample strobe. Each radio time strobe event generator FRM/4SAMP will be associated with one RADT. The event generator 0 to 7 drive UAT_EGR_FRM_EVT/UAT_EGR_4SAMP_EVT. Event generators 8 to 15 drive UAT_ING_FRM_EVT/UAT_ING_4SAMP_EVT (AID only).

Event generator 16 to 18 drive UAT_DIO_EGR_FRM_EVT/UAT_DIO_EGR_4SAMP_EVT. Event generator 19 to 21 drive UAT_DIO_ING_FRM_EVT/UAT_DIO_ING_4SAMP_EVT. These events only used for DIO (DIO engine control) and it could be 4, 8, 16 sample event depending on CLK_CNT setup.

AIL has three frame level internal strobe like UAT_RT_FB_STB, UAT_PE_FB_STB, UAT_TM_FB_STB and these strobes are matched with pe1, pe2, and delta strobe in AIF2.

AIL CPRI: Use BCN timer only. No RADT event is required.

AIL OBSAI: Use BCN and 8RADT timers. No RADT event is required.

AID: Use BCN and 8RADT timers. The first 16 RADT events are used.

DIO: Use BCN, 8RADT(for SI egress only) and three DIO RADT timers. Eight RADT events and six DIO RADT events are used.

7.5 AID

7.5.1 Overview

The IQN2 AID interfaces to a DFE module via the AID/DFE interface. The Ingress block accepts UL data from the DFE and partitions the frames it receives into packets (e.g., symbols for LTE or eight quad-word packets for DIO). It sends the symbol based traffic to the IQN2 PKTDMA or DIO traffic to IQN2 DIO via a master PKTDMA PSI interface. The Egress block usually reads DL data from system memory or IQN2 DIO via a slave PKTDMA PSI interface and paces the data delivery to the DFE to a 4-sample (chip) strobe from AID uAT RADT.

7.5.2 SI

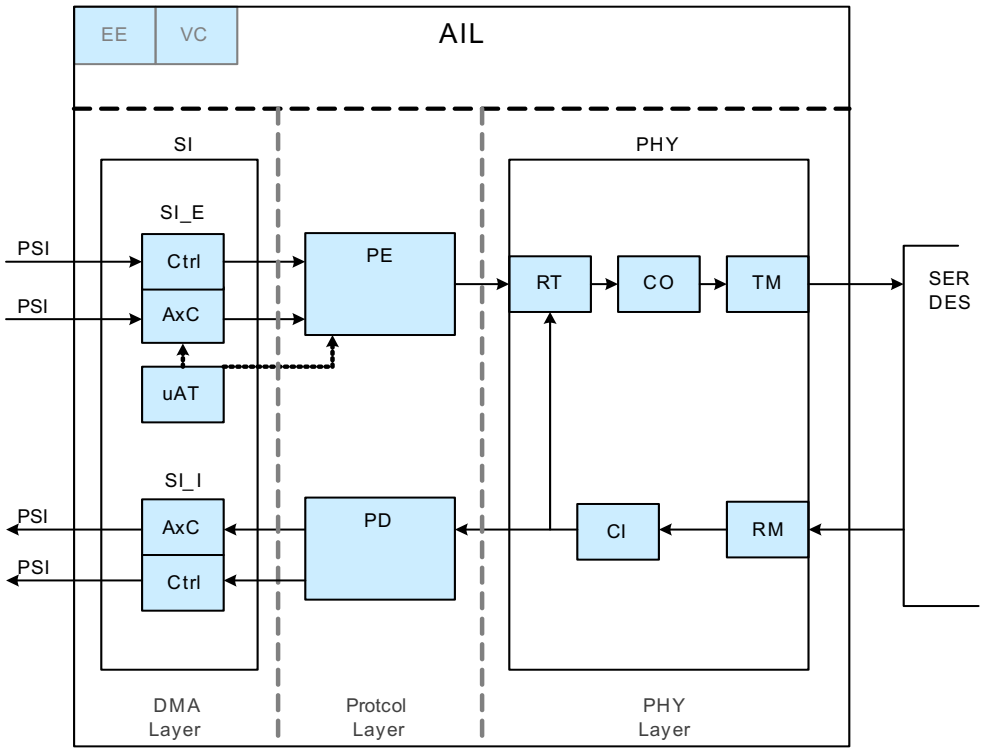
The AID function is a pre-processor or post-processor plus DMA interface for the DFE module. Essentially all other major sub-system of IQN2 {AIL, AID, DIO} also require nearly the identical function. As an implementation and user simplification this common functionality is define as SI (system interface) and implemented as a reusable module. The re-use module overlays all the functionality between all the use scenarios and is implemented with parameterized number of channels. In effect, the SI and AID are one-and-the-same. all HW detail about SI are already described in Section 7.4.

See the DFE User Guide for more details about DFE functionality and see the DFE LLD example code for AID ingress micro AT event compare value setup.

7.6 AIL (Antenna Interface CPRI/OBSAI Link)

The IQN2 AIL interfaces to a Radio module via either of CPRI or OBSAI protocol.The interface to the overall IQN2 subsystem is done via a reuse module, SI. All major IQN2 building block components use SI as the interface into the IQN2 switching infrastructure, IQS. Figure 7-30 shows important submodules within AIL.

Figure 7-30. AIL Block Diagram



7.6.1 Re-synchronization

Through programming errors, bad input timing, or startup conditions, failed timing between IQN2 submodules can exist. In these cases, error handling mechanisms activate to flush and reset submodules allowing them to attempt re-synchronization at the next available time.

7.6.1.1 TM Re-synchronization

The TM Fail mechanism provides a means for the IQN2 AIL IP Block to initialize traffic flow transmitted on each of the AIL links. The Tx Mac block determines the synchronization status for the antenna interface and either initiates or does not initiate a TM Fail condition for the link. The TM Fail condition is used by other blocks within AIL to re-synchronize the data path. Re-synchronization occurs on the next 10 ms frame boundary.

Even if the frame is failed in mid-frame, the rest of the current frame is transmitted as an empty frame. An empty frame contains:

- OBSAI
  - Correctly placed K28.5 & K28.7 framing characters
  - Empty messages (defined as all 1s in address and 0s elsewhere)
- CPRI
  - Correctly placed K28.5 framing characters
  - Correctly Sync & Timing CPRI Control Words
  - Correctly L1 Inband Protocol control word
  - Zero for antenna carrier data and other control words

7.6.1.2 RT Re-synchronization

The RT is an aggregation point between the PHY received data path and the PE output path. Ultimately, the RT is feeding the TM. There are basically three static modes for RT:

- PE only (no RM)
- RM only (no PE)
- PE & RM aggregation

On each PHY frame boundary, the RT attempts to merge the timing of the two possible sources of data. This is accomplished by stalling both RM/CI and PE data streams until a JIT (Just In Time) moment indicated by the uAT RT_FB strobe. Once RT_FB fires, the RT performs its aggregation operation and transfers data to the CO/TM.

The RT FIFO (buffers data from the CI/RM) operation is affected by sync. In sync/re-sync operations, the FIFO is always primed with SOF. A circuit feeding the FIFO will drop-on-the-floor entries until an SOF is received. RT FIFO overflow or TM_RESYNC initiate this FIFO re-sync operation.

7.6.1.3 PE/SI_EGR Re-synchronization

The PE SIE_Scheduler is the master FSM for PE operation. The FSM is PHY frame orientated where the link rate is taken from the global MMR so that incorrect programming is not possible. The FSM starts and stops on PHY frame boundaries, so only full PHY framing is possible. The uAT PE_FB strobe starts the construction of PE PHY frames.

Internally, PE operations continue regardless of consumption by RT from the PE/RT FIFO. Internal PE operations are exactly controlled by the PHY FSM. Sync to the PHY is achieved through the PE/RT FIFO where RT control the read timing of the FIFO, in particular it controls the timed use of SOF.

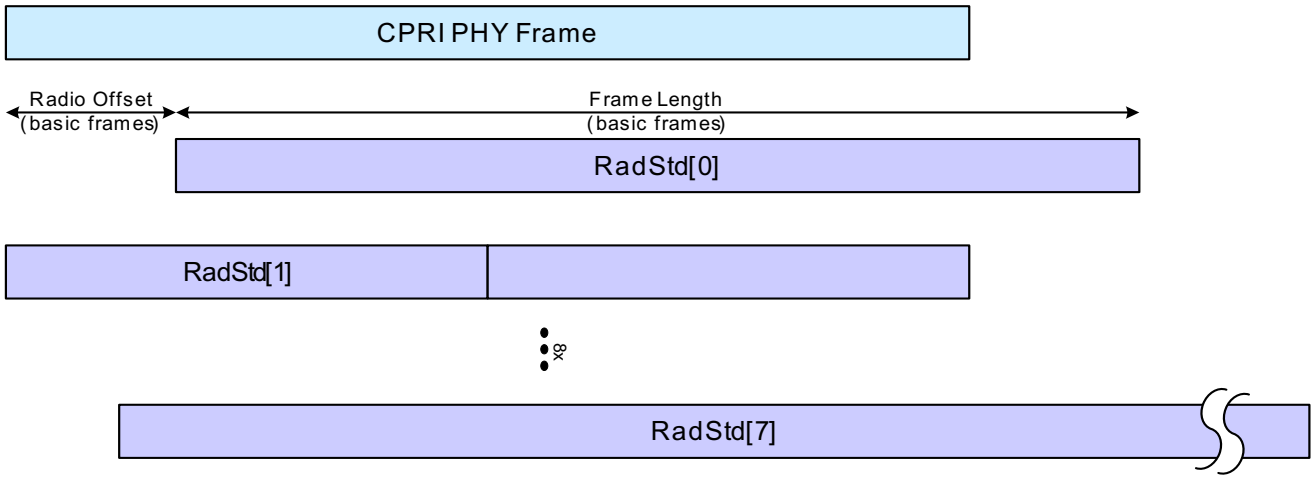
When PE receives a RT_PE_RESYNC, PE flushes the PE/RT FIFO and drops-on-the-floor, all FIFO writes until the next SOF.

7.6.2 AIL Protocol Layer, PD, PE CPRI AxC

CPRI packing method 3 specifies the formula of inserting valid AxC samples and zeros (bubbles or stuffing samples) for purpose of rate matching. The following sections describes how PD, PE controls each step for this operation.

7.6.2.1 CPRI Radio Standard Offset

Figure 7-31. CPRI Radio Standard Offset



CPRI specifies the concept of a Radio Standard being offset relative to the PHY frame boundary. Particularly for GSM “networking” cases, the Radio Frame is not aligned to the CPRI PHY frame. With this requirement, AIL generalizes the Radio Frame offset concept.

The AIL implementation of radio frame offsets is an enable, offset, and length. The **CPRI_RADSTD_CFG[8].EN** will trigger the radio standard to turn ON for the beginning of basic frame when **CPRI_RADSTD1_CFG[8].HFRM_OFFSET, CPRI_RADSTD1_CFG[8].BFRM_OFFSET** is reached. In cases such as GSM when the radio standard is longer than 10 ms, the SW must take care to enable the radio standard at the appropriate time. In order to do that, the correct 10 ms PHY frame boundary is used as a reference. (The HW does a simple comparison to the concatenated HF_CNT, BF_CNT without first waiting for a PHY frame boundary.)

A Radio Standard turns OFF immediately when **CPRI_RADSTD_CFG[8].EN** is disabled. In the case of AIL_PD usage, the radio standard turns OFF immediately when the RM indicates that the PHY has gone down. When in the OFF state, the PD halts all traffic for the effected channels while the PE processes zero traffic.

AIL supports both a Radio Standard Offset defined by HFRM_OFFSET & BFRM_OFFSET and an offset for each individual AIL channel defined by AxC_offset. The concept of an individual AxC offset is not contained within the CPRI standard, and as such it is expected that most users will program AxC_offset to zero. When used, the AxC offset is relative to the Radio Frame Boundary and not the PHY frame boundary.

7.6.2.2 PD, PE CPRI AxC: Map to AxC Group

The first stage is a simple LUT which maps the AxC Container index to an AxC group. The AxC group should be considered to be one of the eight supported radio standards.

For PD, the AIL_PHY_CI is providing a Basic Frame index of 0-63. This LUT operation is simply a 1-of-64 select from MMR parameters.

For PE, **pE_cpri_cfg.AXC_CONT_TC** is a configuration register indicating how many CPRI AxC containers are supported within each basic frame and it depends on the link rate used for the Phy. Programmed values 0-to-63 correspond to length 1-to-64.

pd_cpri_axc0_cfg[64](PE_CPRI_CONT_CFG[64]) is a configuration register with one entry per possible CPRI PHY container. Only CPRI 16x link rate can use all 64 entries.

pd_cpri_axc0_cfg[64].cont_lut_en(PE_CPRI_CONT_CFG[64].LUT_EN) indicates whether or not the container is used.

pd_cpri_axc0_cfg[64].cont_lut_grp(PE_CPRI_CONT_CFG[64].LUT_GRP) indicates which group the container is allocated to. In practice, the groups should correspond one-to-one with the eight possible radio standard variants.

After the AxC is assigned to a radio standard, there is an enable function for each radio standard that is dependent on an MMR that enables the radio standard. The **CPRI_RADSTD_CFG[8].EN** register is used to enable each individual radio standard. The concatenation of the **CPRI_RADSTD1_CFG[8].BFRM_OFFSET[8]** register and the **CPRI_RADSTD1_CFG[8].HFRM_OFFSET[8]** defines the radio standard offset. The status of the ON/OFF state for each radio standard can be monitored by the **CPRI_RADSTD_STS[8].ON** register.

Once the radio standard is enabled, the radio standard boundary is marked so the control path logic can enable each AxC on a radio standard boundary. The radio standard boundary is continuously marked upon each wrap of a counter that counts the number of AxCs in a radio standard frame. The number of basic frames for each radio standard is defined by the **CPRI_RADSTD2_CFG[8].BFRM_NUM[18]** register.

7.6.2.3 PD, PE CPRI AxC: Bubble FSM

The next operation is the radio standard offset operation, necessary to align the Bubble FSM operation. The bubble FSM indicates which supplied containers are unused. The TDM FSM ignores these bubbled containers.

- CPRI Parameters
  - S: # Samples per AxC per K BasicFrames
  - K: # BasicFrames per ContainerBlock (container group)
  - N_{AxC} (N_A): # AxC per AxC Group
  - N_C: # of containers per BasicFrame allocated to the AxC Group
    - number of containers per basic frame allocated to this radio standard
  - N_V: # stuffing samples (bubbles) per container block
    - “bubble” is used in this document as a synonym to “stuffing sample”
- The basic approach of the CPRI rate matching is simply:
  - Whenever there is at least one bubble, then the first container of the container block always has the first bubble.
  - All other bubbles are as even spaced as possible.

Effectively, the equation floor ($i \times K \times N_C / N_V$) is implemented by having an adder which starts at zero on each container block and adds ($K \times N_C / N_V$) to the accumulated value every time a bubble is inserted by the circuit. In parallel, the simple counter increments every container of the container group, starting at zero on each container block boundary. The choice to insert a bubble is simple: if the container count is greater than or equal to the ($K \times N_C / N_V$) accumulator count, then a bubble is inserted.

($K \times N_C / N_V$) is a real number which is programmed by the user. The value is approximated with 12 fractional bits of precision. Analysis of all parameters in the CPRI spec. indicates that 12 bits of fractional precision is sufficient. The approximated value for ($K \times N_C / N_V$) is programmed in two different parts: GAP_INT and GAP_FRAC represent the integer and fraction portions of approximated value.

When the link is OFF or a Radio Standard is OFF, all counters are reset to their zero. This bubble FSM starts operation with the first container group boundary which is the same as the radio standard offset defined by HFRM_OFFSET and BFRM_OFFSET.

The container group length is KNC (in units of containers). If the circuit detects no wrap back to zero on the radio frame boundary, it forces the wrap and activates cpri_bub_fsm_err which logs the error in the EE mechanism.

Here is a pseudo code of bubble FSM operation as an example:

```
endlessLoop:

 if (LinkOff | CONT_CNT==(KNC_CFG - 1) | RAD_SOF)

 { BUB_GAP_CNT = 0; CONT_CNT = 0; }

 if ((CONT_CNT >= INT(BUB_GAP_CNT)) & (KNC_CFG >= BUB_GAP_INT_CFG))

 {  InsertBubbleNow;

   BUB_GAP_CNT += (BUB_GAP_INT_CFG + BUB_GAP_FRAC_CFG); }

 CONT_CNT++;
```

7.6.2.3.1 CPRI AxC: Bubble FSM MMR

This circuit implements the CPRI 5.0 Mapping Method #3 bubble insertion mechanism. Bubbles waste CPRI containers, the purpose is for rate matching of radio standards which do not have similar sampling rates to the CPRI PHY container rates.

PE_CPRI_BUB_FSM_CFG[8].KNC[18]: (K x N_C) fsm-by-fsm, total number of containers per AxC Container Group. Max. value for K is 4608 and 32 for N_c. set N-1

PE_CPRI_BUB_FSM2_CFG[8].GAP_INT[18]: Floor(KxN_c/N_V)fsm-by-fsm, number of containers between bubbles (Integer portion). Zero is an illegal value. This should be set to equal or greater than KNC, if bubble is not required for the FSM.

PE_CPRI_BUB_FSM2_CFG[8].GAP_FRAC[12]: KxN_c/N_V - Floor(KxN_c/N_V) fsm-by-fsm, number of containers between bubbles (Fractional portion).

PD_CPRI_BUB_FSM_CFG[8].KNC[18]: (K x N_C) fsm-by-fsm, total number of containers per AxC Container Group. Max. value for K is 4608 and 32 for N_c. set N-1

PD_CPRI_BUB_FSM2_CFG[8].GAP_INT[18]: Floor(KxN_c/N_V)fsm-by-fsm, number of containers between bubbles (Integer portion). Zero means no bubble.

PD_CPRI_BUB_FSM2_CFG[8].GAP_FRAC[12]: KxN_c/N_V - Floor(KxN_c/N_V) fsm-by-fsm, number of containers between bubbles (Fractional portion).

7.6.2.4 PD, PE CPRI AxC: TDM FSM

Last stage, the TDM FSM simply counts from zero until NCONT. The count value is used to index the TDM LUT giving AXC and EN. If the TDM position is not enabled, the contents is thrown-on-the-floor. If the container were indicated to be a bubble, the container will be skipped from data insertion.

While there are eight different TDM FSMs, there is only one LUT to support them all. The user partitions the LUT. The START_LUT value indicates the starting position for each of the eight FSMs. The NCONT field indicates the max. number of supported AxC containers which is also the LUT length per FSM.

CPRI_TDM_FSM_CFG[8].EN: Enable the FSM. Containers targeting a disabled TDM_FSM are discarded.

CPRI_TDM_FSM_CFG[8].NCONT[8]: Number of TDM_LUT entries for this FSM (For LTE20, 8 sequential entries within TDM_LUT).

CPRI_TDM_FSM_CFG[8].STRT_LUT[8]: First TDM_LUT entry for this FSM.

CPRI_TDM_LUT_CFG[256].AxC[6]: Shared LUT, list of AxC indexes giving TDM AxC order over CPRI link, different parts of LUT allocated to different FSM.

CPRI_TDM_LUT_CFG[256].EN: Shared LUT, enables each entry. Disabled entries will result in dropped CPRI containers. Main use of this enable is the SW would maintain unique AxC value for unused containers.

The TDM FSM is a simple counter per group. It is a simple up counter which counts 0-to-**CPRI_TDM_FSM_CFG[8].NCONT[8],** wrapping back to zero.

It is illegal for a user to modify the **CPRI_TDM_LUT_CFG** for any active AxC. The user may only change regions which are not currently being accessed by an active AxC. Turning channels ON/OFF should be done with the **chan_en** in SI rather than dynamic modification of this.

7.6.2.5 PD, PE CPRI AxC: Programming Example

Example 1: LTE20 MHz two AxCs on 8x link rate AIL. (Assume only one FSM is used and no bubble inserted.)

8x link AIL supports total 32 containers per basic frame but only 16 containers are used for two LTE20MHz AxCs (15 bit I,Q). The first eight sequential containers are used for AxC0 and the next eight containers are used for AxC1. If the FSM does not include any bubble, KNC should be set equal to NCONT.

CONT_LUT_EN[0] ~ [15] = 1, CONT_LUT_EN[16] ~ [31] = 0 (enable the first 16 containers in basic frame), AXC_CONT_TC (for PE)= 31

KNC = 15, GAP_INT(PE) = 16 (set equal or bigger value than KNC not to insert any bubble) GAP_INT(PD) = 0 (in case of PD bubble FSM, zero means no bubble), GAP_FRAC = 0

NCONT = 15, STRT_LUT = 0

TDM_LUT_CFG.AXC[0] ~[7] = 0 (AxC0), TDM_LUT_CFG.AXC[8] ~[15] = 1 (AxC1), TDM_LUT_CFG.EN[0] ~[15] = 1 (enabled 16 containers for this TDM FSM)

Example 2: LTE15 MHz two AxCs on 4x link rate AIL. (Assume only one FSM is used.)

4x link AIL supports total 16 containers per basic frame and all 16 containers are used for two LTE15MHz AxCs (15 bit I,Q) with bubble insertion. The first eight sequential containers are used for AxC0 and the next eight containers are used for AxC1. There are two ways to support LTE15MHz. One way is inserting bubbles for unused BW by bubble FSM and the other way is controlling BW by TDM LUT itself without inserting bubbles.

Case I: bubble insertion

CONT_LUT_EN[0] ~ [15] = 1 (enable all 16 containers in basic frame and it includes BW for bubbles), AXC_CONT_TC (for PE)= 15

KNC = 15, GAP_INT(PE) = 4 (insert stuffing sample every four containers. B,A0,A0,A0,B,A0,A0,A0,B,A1,A1,A1,B,A1,A1,A1,B,A0,.....) GAP_INT(PD) = 4, GAP_FRAC = 0

NCONT = 11, STRT_LUT = 0

TDM_LUT_CFG.AXC[0] ~[5] = 0 (AxC0), TDM_LUT_CFG.AXC[6] ~[11] = 1 (AxC1), TDM_LUT_CFG.EN[0] ~[11] = 1 (enabled 12 containers for this TDM FSM)

Case II: TDM_LUT control without bubble

CONT_LUT_EN[0] ~ [15] = 1 (enable all 16 containers in basic frame), AXC_CONT_TC (for PE)= 15

KNC = 15, GAP_INT(PE) = 16, GAP_INT(PD) = 0, GAP_FRAC = 0

NCONT = 15, STRT_LUT = 0

TDM_LUT_CFG.AXC[0] ~[5] = 0 (AxC0), TDM_LUT_CFG.AXC[8] ~[13] = 1 (AxC1), TDM_LUT_CFG.EN[0] ~[5] = 1 (enabled 6 TDM containers for AxC0 data), TDM_LUT_CFG.EN[6] ~[7] = 0 (disabled TDM for 2 containers), TDM_LUT_CFG.EN[8] ~[13] = 1 (enabled 6 TDM containers for AxC1 data), TDM_LUT_CFG.EN[14] ~[15] = 0 (disabled TDM for 2 containers)

7.6.3 AIL Protocol Layer, PD, Ingress

7.6.3.1 AIL PD OBSAI

The PD and SI ingress work in conjunction with each other creating the protocol layer of AIL. PD is the pre-processing engine for the SI performing only the OBSAI-specific portions of the overall protocol layer processing.

7.6.3.1.1 PD OBSAI Header Route

OBSAI is a header-based protocol. For each of 64 possible DMA Channels, the OBSAI Route circuit is a set of 64 parallel compare circuits. When a compare circuit fires, the particular channel associated with that compare circuit yields an OBSAI message. Each of the compare circuits has a one-to-one mapping to the SI_ingress DMA channel number.

The 13-bit address field and the 5-bit type field are simple compare circuits which trigger on an exact match. The Time Stamp field has programmable usages where it can either be used to extend the addressing scheme or it can be used for the original intended purpose of time stamping AxC samples or indicating SOP/EOP for in packet use cases. When using as an address extension, the entire field can be used, or only the 4 LSBs.

7.6.3.1.2 PD OBSAI RP3-01 Virtual HW Reset

The RP3-01 Virtual HW Reset is a mechanism by which a remote device can cause the receiving SoC to execute a device level HW reset without the need of SW intervention. The basic rationale is for a remote device to only have an OBSAI interface to a centralized BTS. The remote device may have a SW bug which has hung the entire SoC. The only means by which to reset the remote device is via the OBSAI link.

OBSAI Virtual HW Reset Message

- Type = 5'b0_1101
- TS = 6'b00_0000
- Payload= {14byte zeros, 2 byte CRC calculated over header and payload}

The **AIL_PD_OBSAI_TYPE_LUT_CFG.RP3_01_RST** signal controls the EE and pin strobe.

7.6.3.1.3 PD OBSAI SOF Reception Window

The OBSAI timestamp codes are re-used, not deterministic, and as such it is necessary to qualify a potential SOF with a time window. The time window needs to be narrow enough that the correct timestamp is selected, and not a replay of the same value later in the radio frame, yet the window needs to be wide enough to span potential fiber drift.

For AxC traffic, the SOF OBSAI message is expected to arrive within a window of time, referred to as the reception window. On startup conditions, the enabled channel will not move to PD_CHAN_ON state unless a SOF is received within this window.

The window is defined with its center at **PD_CHAN_CFG[64].AXC_OFFSET[25]** and a plus/minus offset adder **PD_OBSAI_RADSTD_CFG[8].AXCOFFSET_WIN[12]**

The PD will determine that an OBSAI timestamp is SOF if:

- The AxC channel is enabled, but not yet PD_CHAN_ON
- The OBSAI message arrives within the reception window
- The OBSAI timestamp is a possible SOF

7.6.3.1.4 PD OBSAI Pkt Time Stamp

There are several forms of OBSAI packet, each requires a different handling.

- OBSAI Ethernet Time Stamp (multiple msg)
  - SOP: 6'b100000
  - MOP: 6'b000000

  - EOP: 6'b1 *nnnnn* : *nnnnn* is never equal to 0 and indicates the number of bytes from the start of RP3 payload (payload bytes in this message only) containing MAC frame data (counting started from the byte after the header). This *nnnnn* value is to calculate packet length. It effectively determines the CRC location.

Ethernet uses the MSB of TS to indicate SOP or EOP. In the case of EOP, the 5 LSB can never equal 5'b0_0000. Using this fact, PD can deterministically discriminate SOP from EOP. MOP TS is always equal to 6'b00_0000. Unlike other OBSAI Types, Ethernet has the unique characteristic that its length is not necessarily an even number of QWD. The 5 LSB are used to indicate the number of valid bytes in the last (EOP) OBSAI message.

- OBSAI Generic Packet Time Stamp (multiple msg)
  - SOP: 6'b10 *nnnn*
  - MOP: 6'b00 *nnnn*
  - EOP: 6'b11 *nnnn* (*nnnn*: is an extension of OBSAI address and is the same for all elements within the packet)
- OBSAI Control Message Time Stamp (single msg)
  - Generic Control Message:
    - Time Stamp = 6'b000000
  - Control Message for Air Interface Synchronized Operations:
    - Time Stamp = 6'b000001

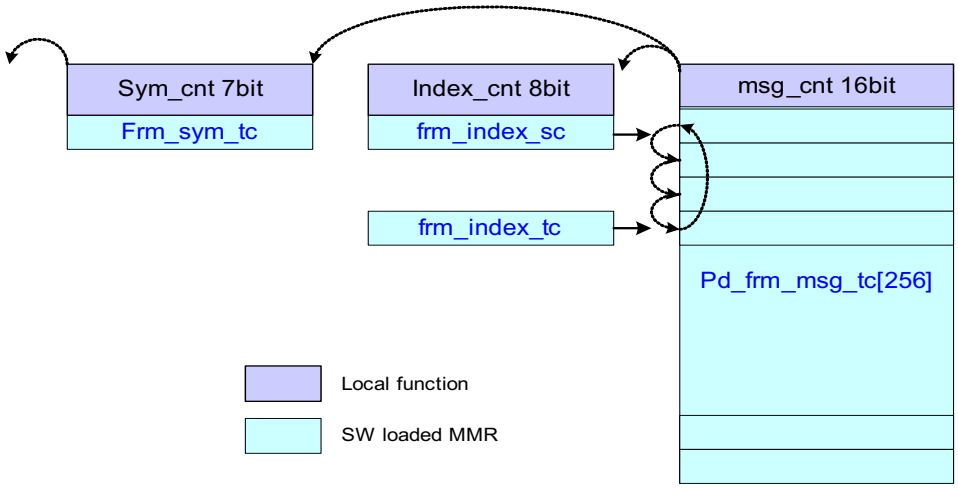
pd_obsai_type_lut_cfg[32].obsai_pkt_en: Determines if channel is packet type channel or AxC type channel. AxC types align to Radio Frame Boundary while packet alignment is a don't care. AxC channels are expected to stream, where packet channels are on-demand. AxC channels use OBSAI Time Stamp and AxC Offset while packet traffic does not. Intended to be programmed consistently with other TS format fields.

- OBSAI_AXC -value 0: OBSAI_AXC
- OBSAI_PKT -value 1: OBSAI_PKT

7.6.3.1.5 PD OBSAI Radio Framing FSM

The radio framing engine is used by PD to predict the OBSAI time stamp. The framing counter configuration is radio standard specific and used for {LTE, WiMax, TD-SCDMA, GSM}. It is complex in order to satisfy all the special requirements of all the different radio standards.

Figure 7-32. PD_Frame: Framing Counter Circuit



Both PD and SI have radio framing engines. In most applications, these are programmed identically and are completely redundant. In LTE3.0 and LTE1.4 symbol boundaries are not always on OBSAI message boundaries. In these special LTE cases, the PD is programmed with whole messages whereas the SI is programmed with the exact number of samples. For these special LTE cases, the user approximates the SYM boundaries. The precise symbol boundaries in PD are unimportant so long as the sum of all SYM lengths exactly equal the LTE frame length.

LTE typically uses the subframe concept where the subframe consumes only 12 or 14 entries in the **pd_frm_msg_tc**, replaying 10 times per LTE frame.

GSM is programmed as a 60 ms frame. GSM requires 104 entries in the **pd_frm_msg_tc**. In the GSM case, the index count and symbol count are the same.

The **pd_frm_msg_tc** is partitioned by the user into eight different radio standards. The user defines a different **frm_index_sc** for each of the radio standards. The **frm_index_tc** indicates the end of the used region per AxC.

The FRM_INDEX is a counter which parallels the FRM_SYM count, but programmed to wrap one or several times prior to the FRM_SYM wrap. Used specifically in LTE as a 6 or 7 count (instead of the 120 or 140 count of the FRM_SYM). This FRM_INDEX concept is useful in limiting the supported range of **PD_FRM_MSG_TC[256]**.

7.6.3.1.6 PD OBSAI GSM Base Band Hop

From a system-level perspective, channels are multiplexing rapidly between different frequencies. From the perspective of a single AIL, it is possible that some GSM time slots will have no OBSAI traffic, instead OBSAI empty_msg is sent/received.

The **pd_OBSAI_gsm_bbhop_cfg[2].off_stb[32]** is basically a strobe per channel which is controlled via MMR access. The processor maintains these bits on a GSM slot-by-slot basis. This bit alerts PD that the next Sym/Slot will be BBHOP OFF.

For GSM BB Hopping, the PD mostly behaves normally, incrementing through its radio framing FSM for every received OBSAI message received. When the PD is in the middle of an active time slot and it receives an off_stb for that channel, it will expect the next time slot the channel be OFF. Once the EOP is received, the Radio FSM is advanced for an entire time slot. In the event that the PD is already in an OFF time slot and it receives another off_stb, it will immediately advance the radio framing FSM by an additional time slot. In this way, whole time-slots are skipped via processor control.

The **pd_gsm_bbhop_cfg.off_stb** sets an internal sticky bit which is not readable via MMR. The sticky bit is cleared the first time it is used. It is also cleared if the channel is not active (a channel is active if it is chan_en or if it is chan_on). With this clearing mechanism, any erroneous MMR write to this register during boot or debug are cleared prior to normal operation.

NOTE: AIF2 and IQN2 AIL differ significantly in the handling of Base Band Hopping. AIF2 essentially does not use the radio framing engine for BBHOP. IQN2 relies on SW to write an MMR strobe bit for each HOP OFF Sym/Slot in order to advance the radio framing engine.

7.6.3.1.7 PD OBSAI Ethernet Header Strip

The Ethernet circuit simply strips the Ethernet preamble and start of frame. The Ethernet header is always eight bytes which is very convenient as AIL_PD has an internal data format of four bytes; stripping two data phases is simple. When enabled to strip, the stripping circuit blindly strips without checking that the bytes indeed are the correct Ethernet Preamble and start of frame.

The strip operation is to simply zero the first eight bytes. Additionally, the data path controls the CRC circuit to disregard the first two words when calculating the CRC. The CRC module passes these two words (eight bytes) without change.

7.6.3.2 AIL PD CPRI CW

The CPRI CW circuits are a dedicated data path which are a single byte in width. CPRI CW occur each Basic Frame which is every 260ns of time. CPRI uses a SYS_CLK of 245.7MHz for 2x, 4x, 8x, 16x yielding 64 clock cycles between each CPRI Basic Frame, and uses a SYS_CLK of 307.2Mhz for 5x,10x yielding 80 clock cycles between each CPRI Basic Frame. The number of control word bytes per CRPI basic frame are variable depending on link rate with a maximum of 16 bytes with the highest link rate.

At the output of the CPRI CW handling circuits, the data is separated in packets on a channel-by-channel basis. The interface to the SoC Teranet is 128 bits. The DMA subsystem is designed to handle only a maximum peak BW. Even a three byte length packet consumes a minimum of one QWD on the DMA interface.

Each CPRI CW channel is individually controlled as to which features are enabled such as CRC or the type of delineation {Null, hyperframe, HDLC, or Fast Ethernet}.

NOTE: It is the responsibly of the user to avoid “machine gun” firing in large numbers of very small packets. This operation may overwhelm the SI control buffers causing dropping of some traffic. Small packets use the buffer inefficiently allowing for less elasticity for stalls due to AxC traffic stalling CW traffic.

7.6.3.2.1 AIL_PD CPRI CW,CW LUT

There are 64 CPRI sub-channels in each CPRI hyperframe (256 CW per hyperframe). For example, sub-channel 0 occupies CW {0, 64, 128, 192}. This sub-channel count is used to index the CW_LUT. The CPRI CW LUT simply maps each CW to one of four CPRI control channels -OR- disables the CPRI CW so that it is discarded. The CW LUT is simply a 256 array of MMR. Sub-channel 52 which occupies CW {52, 116,180,244} is reserved for CPRI PORT ID transmission and reception, so it cannot be used as CW available bandwidth. (This is not in CPRI spec. but internally decided by TI.)

7.6.3.2.2 AIL_PD CPRI CW, HyperFrame LUT

This feature is usually disabled by setting **pd_cpri_cw_chan[4].hf_lut_en** = 0. When a given channel is enabled to use the hyperframe LUT, only the CW which are in the enabled hyperframes are used by the CPRI CW channels. The intended use of this feature is RTWP (Received Total Wideband Power) and there is only one hyperframe LUT for all four channels. RTWP is originally intended to only be transported on Hyperframe {0, 30, 60, 90, 120}. In the event of UL RE Chaining, it can shift to hyperframe {1, 31, 61, 91, 121}. The implementation of this feature does not permit the unused hyperframes to be used by another CPRI CW channel.

7.6.3.2.3 AIL_PD CPRI CW, Delineation

The CW delineation formats are 4B/5B, HDLC, Null and HyperFrame. To identify SOP and EOP the 4B/5B, HDLC, and Null all require more than one byte of data so storage is needed for these four functions. Also, 4B/5B and HDLC are not byte-aligned or multiples of eight bits so they need to be treated as bit-based interfaces.

HyperFrame Delineation

It is guaranteed that hyperframe packets on a channel start with the first byte for that channel after the hyperframe boundary signal. The first byte for a channel after this signal is asserted is sent with an SOP. One or more channels may start a packet before the next hyperframe boundary signal assertion.

The input FIFO marks that last byte of the hyperframe (indicated by bf_cnt=255 & byte_cnt= max for link rate). This may or may not be an active transfer for a channel. The Hyperframe Delineation mechanism only creates EOP of a packet on CW255. The effect is the application must wait until HyperFrame end prior to receiving the full packet information. In case of RTWP Power measurements, the extra latency is 3.12 M sec.

NOTE: Hyperframe delineation works like AxC mode, which means it consistently consumes Rx free descriptors even when there is no valid incoming packet. Descriptor starvation should be controlled by the user application.

Null Delineation

With this form of delineation, the user chooses a character which indicates no traffic is present. The character (indicated by **pd_cpri_null.null_char[9]**)may not be used in the packet as the circuit would interpret this as EOP. The most logical choice of Null character would be a non-comma K-character.

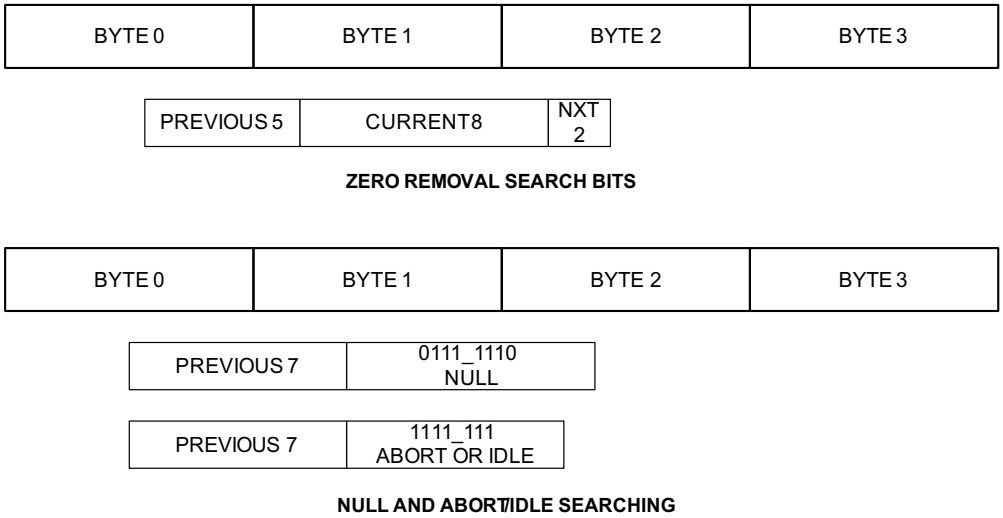
The 8B/10B encoding used over the PHY has a little extra BW to indicate characters other than ASCII characters. These are K-characters. Internal to AIL, the data path has a 9th bit per byte which represents the current byte is a K-character. 8B/10B indicates some special K-characters which are used by SERDES bit alignment and OBSAI/CPRI uses some of these for frame alignment. There are other K-characters available for users for purposes such as AIL Null delineation. Null delineation compares the bytes from the channel buffers with the programmable NULL value to determine if the byte is a null or k-char.

HDLC Delineation

- byte-wide operation for input and output
- 0111_1110 (null) character
  - Gives byte alignment to serial bit stream
  - A valid data character following a null character indicates an SOP
  - A null character following a valid data character indicates EOP
- 1111_1111_1111_1111(OFF) character, out of pkt and bit alignment. Needs more than 15 ones in a row.
- 1111_1111_0111_1110(ABORT) character, acts as EOP of current packet and sets EE error bit. Eight to 15 ones in a row indicates an ABORT rather than OFF.
- 011_1110 (escape) character, remove trailing zero. Removes zero inserted by transmit when there are more than 5 ones in a row other than IDLE, NULL, and ABORT characters.
- Supports CRC bit/byte swapping.

The HDLC logic monitors the four 4-byte-wide channel buffers (Figure 7-33) to determine the amount of bits available on cycles selecting it. Due to zero-bit removal the output of these registers have to be examined as a bit stream rather than as bytes. The HDLC needs to be able to examine the five MSB bits from the previous byte and two bits from the following byte to determine which zero bits need to be removed. Since these can have any bit alignment in the data these 15 bits need to be selected from 24 bits of data.

Figure 7-33. HDLC Bit Fields Monitoring



For SOP, EOP, and Abort detection the previous seven bits need to be examined with the current eight bits to find any NULL, IDLE, or Abort bit sequences when the bit alignment is not known. This requires 24 bits of valid data also due to not knowing the alignment of the bits within the bytes.

Due to supporting CRC bit/byte swapping the data going to the CRC needs to be delayed for two bytes of transfers to allow for the SOP detection. When the EOP is seen, the last two bytes have the bit/byte swapping applied to them before they are sent on to the CRC. Bit/byte swapping is controlled by **pd_cpri_cw_CHAN_CFG.hdlc_rvrs_crc[1:0]**

Fast Ethernet Delineation (4B5B)

The 4B5B delineation is similar to the HDLC since it is also not aligned to bytes. As it tracks how many bits are available it waits for 15 bits to be available before starting to process the data. While idle only 1s are coming in so the logic does not know the bit alignment. The state machine monitoring the data is in IDLE until it detects the SOP string at which point the read pointer gets re-positioned to align with the 5-bit boundaries and it goes to the SOP state. The following 5-bit value is decoded and an SOP sent along with this data when it is being sent out. It cannot be sent out until the following 10 bits are available so checking for EOP can be done.

If an EOP follows the SOP byte, the byte will be sent out with both SOP and EOP and the state machine will return to IDLE. Typically, it will be receiving more data so it will go to the MOP state sending out data as long as there is no EOP found. When the next 10 bits indicate an EOP the current byte is sent out with the EOP bit set and the state machine returns to IDLE. This is the same state transition as the Null Delimiter does, the only differences are the values and number of bits being checked.

If an SOP, HALT, or IDLE pattern is seen before the EOP is seen while in the MOP state, a byte with an EOP is sent out along with an error indication and the state machine will go to IDLE. The state machine will start looking for the next occurrence of an SOP before starting a packet.

To provide different bit ordering that may need to be supported, each of the four channels has a 2-bit swapping field for data before and after the 4b5b delimiter logic. The **pd_cpri_cw_CHAN_CFG.dlmt_imux[3:0][1:0]** swap bits in CPRI layer input byte (8-bit aligned data of encoded 5-bit nibble), before doing 4b5b decoding and it is normally used for backward compatibility of AIF2 PD pre-4b5b bit swap operation. **pd_cpri_cw_CHAN_CFG.dlmt_omux[3:0][1:0]** swaps 4-bit nibble after 4b5b decoding is done. **pd_cpri_cw_CHAN_CFG.QWD_omux[3:0][1:0]** swaps bits or 4-bit nibble after CRC logic operation is done. This field supports AIF2 backward compatibility for PD post-4b5b bit swap operation.

Table 7-7. PD CW Logic Bit Swap Option

Value	Name	Function
0	NO_SWAP	No swapping within a byte is done
1	SWAP_NIBBLES	Bits [7:4] and [3:0] are swapped within the byte.
2	SWAP_NIBBLE_BITS	Bits [7:4] are swapped to [4:7] and bits [3:0] are swapped to [0:3]
3	SWAP_BOTH	Bits [7:4] are swapped to [0:3] and bits [3;0] are swapped to [4:7]

This is very useful feature to accept any type of control word packet format from any kinds of radio devices.

To allow for different radio equipment vendor interpretations of the spec. as far as bit ordering, the **pd_cpri_cw_4b5b_CFG.bit_order[1]** reverses the order of the 5-bit (encoded nibble) translation. This reversal includes header and SSD, ESD data attached by HW. The **pd_cpri_cw_4b5b_CFG.ssd_order[1]** reverses the order of the SSD1 or ESD1 and SSD2 or ESD2 comparison. Normally, this option is not used.

The **pd_cpri_cw_4b5b_CFG.hdr[1:0]** MMR selects what to do when there is a preamble attached to the head of the packet (Table 7-8). The preamble is either seven or eight bytes so the two-bit field selects the following:

Table 7-8. PD 4B5B Preamble Stripping

Value	Name	Description
0	NO_STRIP	No bytes are stripped off and the entire packet is passed on to the CRC. This is used when there is no preamble.
1	STRIP_7	Strips off 7 bytes of preamble (Typical use case).
2	STRIP_8	Strips off 8 bytes of preamble (AIF2 backward compatibility).
3	NO_CRC	Passes the preamble in without stripping, but ignores the CRC check. This is used if the user application is to deal with the preamble and CRC.

7.6.3.2.4 AIL_PD CPRI CW, CRC

The CRC circuit can be programmed to generically apply CRC to any of the delineation flows. In practice, the user will always use CRC16 for HDLC and CRC32 for Fast Ethernet. This flexibility allows the user to create a custom flow with CRC, such as adding CRC to Hyperframe Delineated, which is not formally specified in the CPRI standard.

The CRC type is indicated on a channel-by-channel basis with **pd_cpri_cw_chan_CFG[4].crc_sel[2]** which indicates {no_crc, CRC32, CRC16, CRC8}. The CRC8 has a programmable polynomial indicated by **pd_cpri_crc_CFG.crc8_poly[8]**. There is only one CRC8 polynomial for use with all four CPRI CW channels.

The CRC circuit can either be initialized with zeros or ones, indicated by **pd_cpri_cw_chan_cfg[4].crc_init.** When ones are chosen as the CRC init value, the success/failure of the CRC check is determined by comparing the result with a constant value “Magic Number” which is different for every polynomial. The CRC circuit hard codes these “Magic Numbers” for CRC32 & CRC16. For CRC8, the “Magic Number” is supplied by **pd_cpri_crc_cfg.crc8_comp[8].**

7.6.3.2.5 AIL_PD CPRI CW, QWD Output Interface

The output stage has the same nibble and bit swapping logic that was in the delimiter circuit. It is replicated here to re-order the bits if the CRC section needs them in a different order than the SI. **Pd_cpri_cw_CHAN_CFG.qwd_omux[2]** provides the selection for the multiplexing.

7.6.4 AIL Protocol Layer, PE, Egress

7.6.4.1 AIL_PE_CPRI_CW

7.6.4.1.1 PE CPRI CW CRC

The CRC circuit supports the same 8, 16, and 32-bit CRC as the PD. The main difference in the logic is that rather than checking the CRC, the result is inserted over the last bytes of the packet. The input FIFO indicates which bytes are to hold the CRC. The CRC residual registers are loaded for all bytes other than the ones to be loaded with the CRC. The data output is either the input data passed through or it is the multiplexed result of previous CRC calculations. The result is held in one byte register per channel until a read is requested by the CW FSM.

7.6.4.1.2 PE CPRI CW Delineation

The 4b5b, Null, HyperFrame, and HDLC delineation circuits all perform a similar function to the corresponding circuits in the PD, except these do encoding instead of decoding. All circuits other than HyperFrame increase the amount of data being transmitted due to adding SOP, EOP, or NULL bytes or adding filler bits in HDLC. Due to this, data may be output from a delineation module without it having read data from the input FIFO.

As in the PD and in the PE CW Input FIFO, each byte can have its nibbles and bits swapped before and after encoding to be able to match any interpretation of the standards. These are all controlled per channel by MMRs.

PE CPRI CW Delineation - HyperFrame

At the start of each HyperFrame, all HyperFrame channel FSM are put into an IDLE state. When the first enabled HyperFrame cycle occurs with an SOP byte in the input FIFO for the channel, the FSM becomes PKT_ACTIVE and the SOP and any other bytes following it are sent on all the following HyperFrame enabled cycles until an EOP is seen. When an EOP is seen, that byte is sent out and the state goes to PKT_DONE and no other packet data is transferred until after the start of the next HyperFrame. If the first enabled HyperFrame cycle occurs and there is not an SOP word available, the FSM goes directly to the PKT_DONE state. At most, one packet per channel can be transmitted in any HyperFrame.

There are two error conditions to handle in the transmit of HyperFrame packets. The first condition to handle is if there is no data available while transferring a packet. This generates a starvation condition which is flagged with an EE (pe_ee_cpri_cw_hypfm_starve_err) which also triggers a flush for this channel in the input FIFO. The other case is if the packet does not complete before the start of the next HyperFrame. Any transition from PKT_ACTIVE directly to IDLE generates an EE (pe_ee_cpri_cw_hypfm_oflow_err) and triggers a flush of the remainder of the packet.

PE CPRI CW Delineation - Null

When Null data is requested to be transferred, if there is no data available or the last transfer was an EOP the Null logic responds with a NULL character. The NULL character is programmed by an MMR and is typically a K-Char. If there was no data available but the interface was still in the middle of the packet, the NULL is sent and an error is indicated for starvation of the data. Nulls continue to be sent for data until a valid SOP is seen. The **pe_ee_cpri_cw_null_starve_err** signal indicates this error condition which also causes a flush to occur in the Input FIFO.

When an SOP is seen, the output data transits from NULL to the incoming data. All data is sent unmodified until after the EOP. Assuming no starvation condition, when the byte with the EOP is seen it is sent and a flag is set indicating a NULL needs to be sent. On the following data request cycle it is responded to with a NULL rather than data from the Input FIFO. A single NULL between non-NULL data indicates EOF of the previous packet and the SOF of the next packet.

PE CPRI CW Delineation - HDLC

When HDLC data is requested to be transferred, if there is no data available or the last transfer was an EOP, the HDLC logic responds with a NULL character. The Null character is a 0111_1110. If there was no data available, but the interface was still in the middle of the packet, the Abort character (1111_1111_0111_1110) is sent and an error (pe_ee_cpri_cw_hdlc_starve_err) is indicated for the starvation of the data. Nulls will continue to be sent for data until a valid SOP is seen and the error signal triggers a flush for the channel in the Input FIFO.

Data is sent unmodified except for doing an escape if there are 5 ones in a row. To avoid more than five ones in a row in the data when this occurs, a zero bit is added after the fifth one. This causes the output stream to lose byte alignment since more than eight bits may be produced for each 8-bit input. Up to two extra bits may be created for any byte that comes in due to the data in the incoming byte and the value that was sent out previously. The last data sent and any residual data from the previous byte is held per channel. The residual buffer holds the previous byte sent and up to seven bits of the next byte to send.

PE CPRI CW Delineation - 4B5B

When 4b5b data is used every eight bits into the module results in 10 bits being generated. Since only eight bits are removed from the 4b5b module on any cycle, there will always be residual data to be held for each channel. The 10-bit value is either the encoded value based on the available data or the IDLE pattern. If the incoming data is being used and it is an SOP or an EOP, an extra 10-bit field is added to the buffer. SOPs have the 10 SOP bits added before adding the new data and for EOPs the 10-bit EOP is added after the 10 bits for the data are added.

If no data are available during a packet when data is requested, an EOP is generated and an error indication (**pe_ee-cpri_cw_4b5b_starve_err**) sent to the EE block. All data until an SOP is seen will be dropped and replaced with IDLE.

To provide different bit ordering that may need to be supported, each of the four channels has a 2-bit swapping field for data before and after the 4b5b delimiter logic. The **pE_cpri_cw_CHAN_CFG.dlmt_Omux[3:0][1:0]** swap bits in CPRI layer output byte (8-bit aligned data of encoded 5-bit nibble), after doing 4b5b encoding and it is normally used for backward compatibility of AIF2 PE post-4b5b bit swap operation. **pE_cpri_cw_CHAN_CFG.dlmt_Imux[3:0][1:0]** swaps 4-bit nibble before 4b5b decoding is done. This MMR is normally used with the BIT_ORDER field in 4B5B CFG MMR. **pE_cpri_cw_CHAN_CFG.Imux[3:0][1:0]** swaps bits or 4-bit nibble before CRC logic operation is done. This field supports AIF2 backward compatibility for PE pre-4b5b bit swap operation.

Table 7-9. PE CW Logic Bit Swap Option

Value	Name	Function
0	NO_SWAP	No swapping within a byte is done
1	SWAP_NIBBLES	Bits [7:4] and [3:0] are swapped within the byte.
2	SWAP_NIBBLE_BITS	Bits [7:4] are swapped to [4:7] and bits [3:0] are swapped to [0:3]
3	SWAP_BOTH	Bits [7:4] are swapped to [0:3] and bits [3;0] are swapped to [4:7]

This is a very useful feature to create any type of control word packet format for any kinds of radio devices.

To allow for different radio equipment vendor interpretations of the spec. as far as bit ordering, the **pE_cpri_cw_4b5b_CFG.bit_order[1]** reverses the order of the 5-bit (encoded nibble) translation. This reversal includes header and SSD, ESD data attached by 4b5b logic. The **pE_cpri_cw_4b5b_CFG.ssd_order[1]** reverses the order of the SSD1 or ESD1 and SSD2 or ESD2 comparison. Normally, this option is not used.

The **pE_cpri_cw_4b5b_CFG.hdr[1:0]** MMR selects the number of bytes of the preamble added between the SSD and the first byte of data. The value to use for the first six or seven bytes and the one to use for the last byte of preamble (start of frame data) are set in **pE_cpri_cw_4b5b_CFG.hdr_PREAMBLE[1:0]** and **pE_cpri_cw_4b5b_CFG.hdr_SOP[1:0]**. Preamble bytes are not part of the CRC so they can be added after the CRC module. The preamble is either seven or eight bytes so the two-bit field selects the following:

Table 7-10. PD 4B5B Preamble Adding

Value	Name	Description
0	NO_PREAMBLE	No preamble. This is used when user application generates Ethernet header information.
1	PREAMBLE_7	Add 7 bytes of preamble (Typical use case).
2	PREAMBLE_8	Add 8 bytes of preamble (AIF2 backward compatibility).

Table 7-11 shows the 4b5b logic implementation as a 4B5B encoder. Seven bytes preamble was used with 0xD5 as a start of frame data. The 5B column shows the SSD1 and SSD2 attached by HW.

Table 7-11. 4B5B Encoding Example

EtherFrame		4B before DLMT_IMUX (MSB nibble first)	4B after DLMT_IMUX (LSB nibble first)	5B before BIT_ORDER (MSB bit first)	5B after BIT_ORDER (LSB bit first)
SSD1				11000	00011
SSD2				10001	10001

Table 7-11. 4B5B Encoding Example (continued)

EtherFrame		4B before DLMT_IMUX (MSB nibble first)	4B after DLMT_IMUX (LSB nibble first)	5B before BIT_ORDER (MSB bit first)	5B after BIT_ORDER (LSB bit first)
Preamble	55h	5	5	01011	11010
		5	5	01011	11010
	55h	5	5	01011	11010
		5	5	01011	11010
	55h	5	5	01011	11010
		5	5	01011	11010
	55h	5	5	01011	11010
		5	5	01011	11010
	55h	5	5	01011	11010
		5	5	01011	11010
	55h	5	5	01011	11010
		5	5	01011	11010
	55h	5	5	01011	11010
		5	5	01011	11010
SFD	D5h	D	5	01011	11010
		5	D	11011	11011
DATA	24h	2	4	01010	01010
		4	2	10100	00101

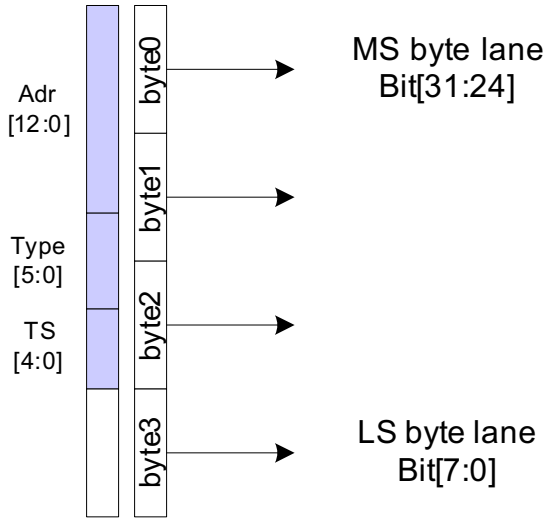
Natively, IQN2 HW supports big endian bit order, but many radio devices require little endian bit order for Ethernet packets and additional swap operations need to be done to create little endian bit order packets. 4B5B logic cannot swap 10-bit level data (only do 5-bit level swap) and that is the main reason why 4-bit nibble swap should be done by the DLMT_IMUX. (Same operation is done by DLMT_OMUX on ingress.)

7.6.4.2 AIL_PE_OBSAI

7.6.4.2.1 AIL_PE_OBSAI Header and TimeStamp

In OBSAI mode, The four words (16 bytes) of payload are pretty much a simple pass through and the most significant function of this block is OBSAI header construction (Figure 7-34). The OBSAI header is always the first word of the five words (only the three MSB of the header phase are populated in big endian format where the first OBSAI byte transmitted is in the MSByte lane).

Figure 7-34. OBSAI Header



The OBSAI Address and Type fields are simply inserted from either MMR or PacketDMA Protocol Specific info. The TS (Time Stamp) field is normally calculated, but can alternatively be inserted, or even partially inserted.

OBSAI Address & Type

Address and Type fields are always inserted. The **pe_obsai_hdr_cfg[64]** MMR controls the operation, and there is a register for each of 64 possible channels. The ps_insert field of this MMR controls the source of the insertion to either come from **pe_obsai_hdr_cfg** fields or from the DMA packet (protocol specific). ps_insert has three options, all insertion comes from **pe_obsai_hdr_cfg**, all insertion comes from PS, or only the address comes from PS.

NOTE: PS_INSERT is not possible with AxC traffic, but only for control traffic. In cases of AxC traffic, the protocol-specific information fields are needed to pass SYMBOL index and therefore cannot be used to pass Adr or Type information. For AxC traffic, PS_INSERT programmed to zero (unused).

OBSAI TS

The **pe_obsai_hdr_cfg[64].TS_mask** controls whether the TS is to be inserted or generated. When inserted, the ps_insert field controls the source. There is a partially inserted option which has the intended use case of extending the OBSAI address while still retaining two MSb for some packet demarcation. The HW implementation is generic and simply generates all six bits, only using the top two MSb and inserting the remaining four LSb from either **pe_obsai_hdr_cfg[64].ts_adr** or PS as indicted by ps_insert.

Time stamp generation is controlled by **pe_obsai_hdr_cfg[64].tx_frmt**

- NO_TS (AxC): The generated TS is forced to zero.
- NORM_TS (AxC): Used for WCDMA and LTE. The 6-bit TS starts with zero at SOF and increments ++1 every subsequent visit. The value wraps back to zero every 64 qwd.
- GSM_DL (AxC): MSB of TS is 1’b1 for each SOP (SOP starts each Time Slot). The remainder of the TS bits start at zero on SOP and increment ++1 each OBSAI message, wrapping back to zero every 32 OBSAI messages.
- GSM_UL (AxC): MSB of TS is 1’b1 for first four OBSAI messages of each GSM Time Slot (SOP starts each Time Slot). The remainder of the TS bits start at zero on SOP and increment ++1 each OBSAI message, wrapping back to zero every 32 OBSAI messages.
- CTL_PKT(Pkt): TS is 6’00_0000 (same as NO_TS)
- GEN_PKT (Pkt): Generic packet is comprised of two or more OBSAI messages where SOP: 6’b10_XXXX EOP:6’11_XXXX MOP:00_XXXX

- ETHERNET (Pkt): SOP: 6'h10_0000 MOP: 6'h00_0000 EOP: 6'h1n_nnnn where n_nnnn is the number of valid bytes in last transfer.

7.6.4.2.2 AIL_PE_OBSAI Ethernet

- Ethernet Preamble
  - SI_IQ_EGR already provides eight bytes of zeros appended
  - PE overwrites first eight bytes with Preamble and SOF
    - bit order is reversible
- Ethernet Header
  - Dst_Adr, Src_Adr, Length fields are provided in PacketDMA packet already loaded in proper location
- Ethernet CRC
  - PacketDMA packet already has 4-byte gap in end of packet for overwriting by AIL_PE_OBSAI_CRC circuit. PE CRC circuit overwrites this field with calculated CRC. CRC is not calculated over Ethernet Preamble and SOF.

The CRC generation feature of PE can be turned OFF and rather the CRC may be provided by either NetCP or SW controlled processors. This is a reasonable option, since packets forwarded from NetCP will have the CRC field supplied anyway. It is envisioned that packets sourced from the SoC processors are simpler, private LAN communications which are easily padded to full nx16 byte size.

7.6.4.2.3 AIL_PE_OBSAI_CRC

The AIL_PE_OBSAI_CRC performs CRC calculation for up to 64 channels. It serially processes each channel and processes 4, 3, or 2 bytes in each data phase. CRC is programmable as CRC32 or CRC16.

When performing CRC, the CRC circuit overwrites the last bytes received. These bytes are not used in the CRC calculation and simply discarded. Other than the actual two or four bytes of CRC, the CRC circuit passes all bytes without alteration.

In cases where the CRC operation is disabled, the CRC circuit simply passes all bytes for that packet.

The 16-bit and 32-bit polynomials are fixed and use the Ethernet and OBSAI standard polynomials . The 32-bit Ethernet polynomial is $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^{8} + X^{7} + X^{5} + X^{4} + X^{2} + X + 1$ and has the CRC value complemented in the received packet. The 16-bit OBSAI polynomial is $X^{16} + X^{12} + X^{5} + 1$. Typically, the 32-bit polynomial uses an initialization value of 0xffffffff and the 16-bit uses 0x0.

7.6.5 AIL PHY

The Physical Interface of the Antenna Interface Link (AIL PHY) for IQN2 terminates the transmission and reception of digitized serial data defined by CPRI and OBSAI standard specifications into a frame-aligned system clock domain for protocol encoding and decoding of an external antenna interface signal.

7.6.5.1 Physical Interface Link Rates

The external signal data link rates for the various options of the physical interface are shown in the following tables.

Table 7-12. OBSAI Line Rates

OBSAI LINE RATES			
LINE RATE	**Multiplier**	**DATA RATE**	**Max # of WCDMA AxCs per Link**
1.536Gbps	2x	1.2288Gbps	8
3.072Gbps	4x	2.4576Gbps	16
6.144Gbs	8x	4.9152Gbps	32

Table 7-13. CPRI Line Rates

CPRI LINE RATES				
LINE RATE	**Multiplier**	**DATA RATE**	**Max # of WCDMA AxCs 7 bit UL 15 bit DL**	**Max # of WCDMA AxCs 8 bit UL 16 bit DL**
1.2288Gbps	2x	983.04Mbps	8	7
2.4576Gbps	4x	1.96608Gbps	16	15
3.072 Gbps	5x	2.45756Gbps	20	19
4.9152Gbps	8x	3.93216Gps	32	30
6.144 Gbps	10x	4.91512Gps	40	38
9.8304 Gbps	16x	7.86432Gps	64	60

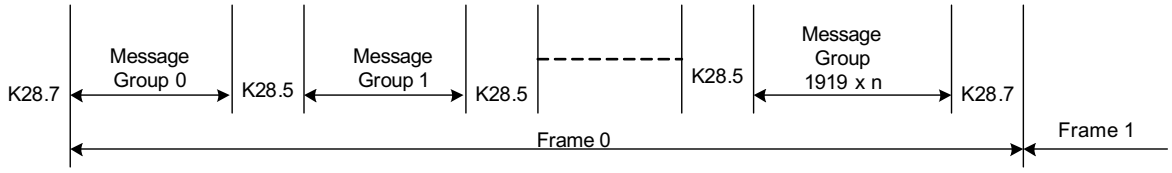
7.6.5.2 Frame Formatting

Both OBSAI RP3 and CPRI interfaces have defined, unique frame formats. These are described in the respective standards and summarized in another chapter of this document. The Physical Interface Frame Synchronization must follow either of these two formats. The selection of which format is used for each physical interface is defined by a configuration register for the module that is configured by software. Frame formats are controlled by Frame Control Logic within the Physical Interface blocks.

7.6.5.2.1 OBSAI Frame Format

An OBSAI RP3 master frame is preceded by a K28.7 character. A master frame is divided into message groups, which are separated by K28.5 characters. An OBSAI RP3 frame initialization is realized upon a duration of K28.5 characters occurring in the serial stream. These initialization characters are used to train a serial receiver with the framing byte boundary. Figure 7-35 illustrates a basic frame format supported by IQN2 assuming initialization has been achieved.

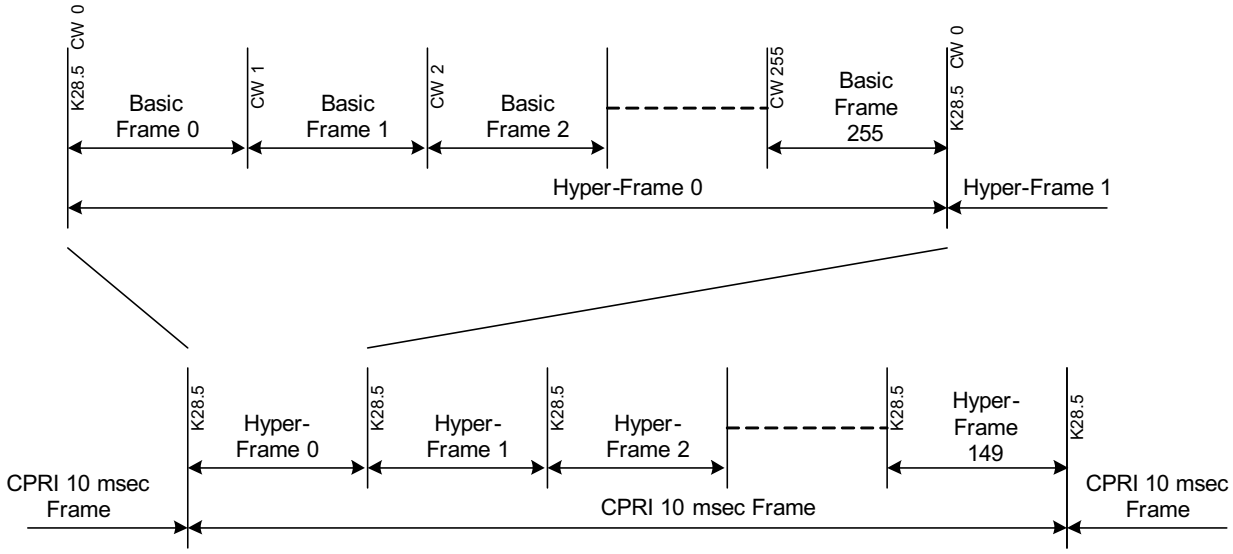
Figure 7-35. OBSAI Frame Format



7.6.5.2.2 CPRI Frame Format

CPRI frames (Figure 7-36) maintain a concept of a 10 msec frame that is used as a master frame reference. Within the CPRI 10 msec frame are 150 hyperframes. Each hyperframe is separated by K28.5 symbols. Within each hyperframe are 256 basic frames. Each basic frame contains 16 words, the first word being a control word. The first control word within a basic frame within a hyperframe contains the K28.5 character indicating the edge of the hyperframe. The hyperframe number 0 indicates the first hyperframe within the CPRI 10 msec frame.

Figure 7-36. CPRI Frame Format



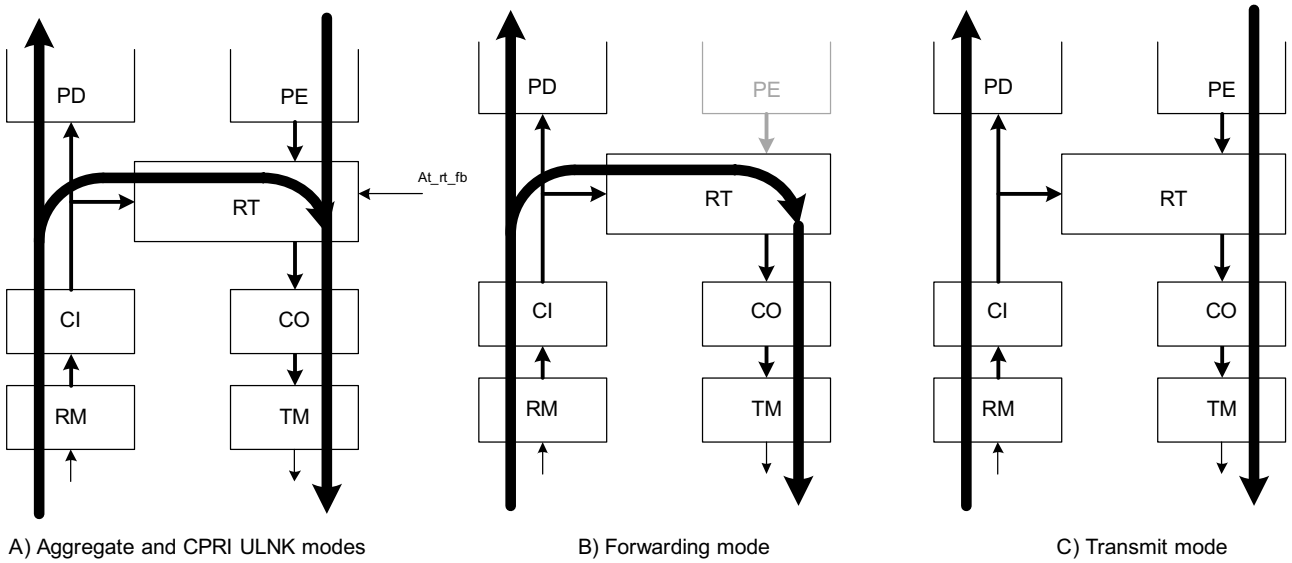
7.6.5.3 AIL Link Data Path Configuration Modes

Each AIL Link may be configured for a separate configuration mode. There are four possible configuration modes:

- Forwarding mode
- Transmit mode
- Aggregate mode
- CPRI ULNK mode

How these modes operate are detailed in the RT block section. The following figures (Figure 7-37) illustrate the data flow within the AIL Phy for each of these configurations.

Figure 7-37. AIL Data Path Configuration Modes



7.6.5.4 RM Module

The RM Module block supports the data path connection from a SerDes module receive link of AIL Phy. The RM converts a two-byte wide parallel stream in the two-byte clock domain of the received signal that is clocked directly from the SerDes module into an eight-byte-wide parallel stream transmitted to the system clock domain of AIL. The RM Module also recovers framing, provides serial link decoding, and performs clock synchronization of either an OBSAI or CPRI signal.

7.6.5.4.1 RM Serial Decoding

8b10b Serial De-coding

Serial De-coding for the received signal is performed within the serial link clock domain on two-byte clock boundaries. A 20-bit coded data word clocked at the two-byte SerDes module receiver clock rate is the interface used to transfer data between the antenna interface link and the SerDes module. The Receive Serial Decoding converts the 20 bits of serial data received from an external differential pair high-speed serial link into two-byte wide received data using 8b/10b decoding. The 8b10b coding manages a running disparity over the sequential bytes to determine coding selections to achieve optimal ones density. The 8b/10b decoder also provides K character indication to support comma character recognition, and code violation indications that indicate a code violation for each byte written to the receive FIFO.

Code Violation Indication

Code violations may be detected in the 8b/10b decoder logic within bytes received from the SerDes macro receiver. A code violation indication bit is associated with each byte in the 64-bit data path so that code violations can be recognized. The code violation indications are generated by the 8b/10b decoding logic and are passed through the clock synchronization FIFO. The number of line code violations are maintained in an MMR status register.

7.6.5.4.2 Clock Detection Function

The AIL Phy contains dedicated circuitry to detect the validity of a receiver clock signal from the SerDes module. The clock detection is useful to determine AIL Phy functionality during failures, and to help isolate causes of a failure in the data path.

The clock detection circuit provides the following features:

- Clock detection is dedicated to the RM Block SerDes link
- Watchdog feature
  - Monitors clock activity
  - Generates an event if clock is not active
  - Programmable wrap that determines detection window
- Clock Quality feature
  - Creates MMR register that describes clock quality
  - Programmable wrap register that determines accuracy

The clock detection function is divided into two components. One component provides a watchdog capability designed to indicate that a clock is not present. The second component determines the quality of the clock signal received from the SerDes module.

The watchdog circuit consists of a programmable counter with a wrap detection that generates an event. The value of the wrap is set through an **PHY_RM_CLK_DET_CFG.WD_WRAP[8].** If the counter does wrap, an event is triggered.

The clock quality circuit is designed to count the number of received clock edges with the known good quality system clock. Two counters are used, one that counts the number of system clock edges, and another that counts a number of receiver clock edges. Upon a programmable wrap of the receiver clock count in a **PHY_RM_CLK_DET_CFG.MON_WRAP[16]**, the system clock count is captured. The captured clock can be monitored in a **PHY_RM_CLK_QUAL_STS.VALUE[16]**.

7.6.5.4.3 Payload Descrambling

Descrambler Control consists of a configuration signal that enables the descrambling, and a mode signal that toggles the descrambler between operational and initialization modes. These signals are determined by configuration registers for the interface, and by the state of the Receive Frame Synchronization.

In OBSAI mode, the Descrambler FSM must perform the scrambling seed protocol to acquire seed. Once the seed is acquired, an indication must be made to the Rx FSM that it can continue with state transitions.

In CPRI mode, the scrambler seed is acquired by recognizing the Z.0.2-4 bytes of each hyperframe. These four bytes are decoded by dedicated hardware to determine the seed value for every hyperframe. An EE event is generated upon the capture of a different seed value from a previous hyperframe.

7.6.5.4.4 Serdes Comma Alignment Control

The Receive Frame Control logic can disable the receiver SerDes module from performing byte alignment on the received serial interface with a dedicated output. Once the Rx FSM transitions from determining that line codes are valid, the RM sends signal to SerDes, so that it disables the symbol alignment. This capability can be configured via **PHY_RM_DP_CFG.SD_AUTO_ALIGN_EN[1]**.

7.6.5.4.5 Receive Frame Synchronization Rx FSM

The Receive Frame Synchronizer State Machine manages the operation of the receive data path. The state machine performs different transitions for OBSAI vs. CPRI modes. The basic operation in both modes provides a status of frame reception on the received signal that is used to manage the control signals of the data path.

In general, the state machine resets to an ‘Unsync’(ST0) state that indicates the data path is not yet operational. Upon reception of valid codes from the receiver, the state machine attempts to identify K characters. For certain rate links above 4.5Ghz, the state machine must satisfy the scrambler seed initialization algorithm performed on the received signal. Once K characters are recognized (after the scrambling seed protocol is satisfied), subframes of either message groups or hyperframes are identified. Once consistent frames are recognized, the state machine determines frame synchronization has been achieved by a transition to the ‘Frame Sync’(ST3) state and normal operation of the data path can begin. The state machine will exit the ‘Frame Sync’ state upon the following list of violations

1. Consecutive number of bytes with code violations
2. Consecutive number of blocks of bytes with code violations
3. Misalignment of message groups in OBSAI
4. Misalignment of hyperframes in CPRI
5. Misalignment of comma bytes in OBSAI of CPRI
6. Out of sequence HFN number in CPRI
7. Loss of Signal of the receiver
8. Disabling of the RM Enable MMR

Figure 7-38. RM Rx FSM State Transitions

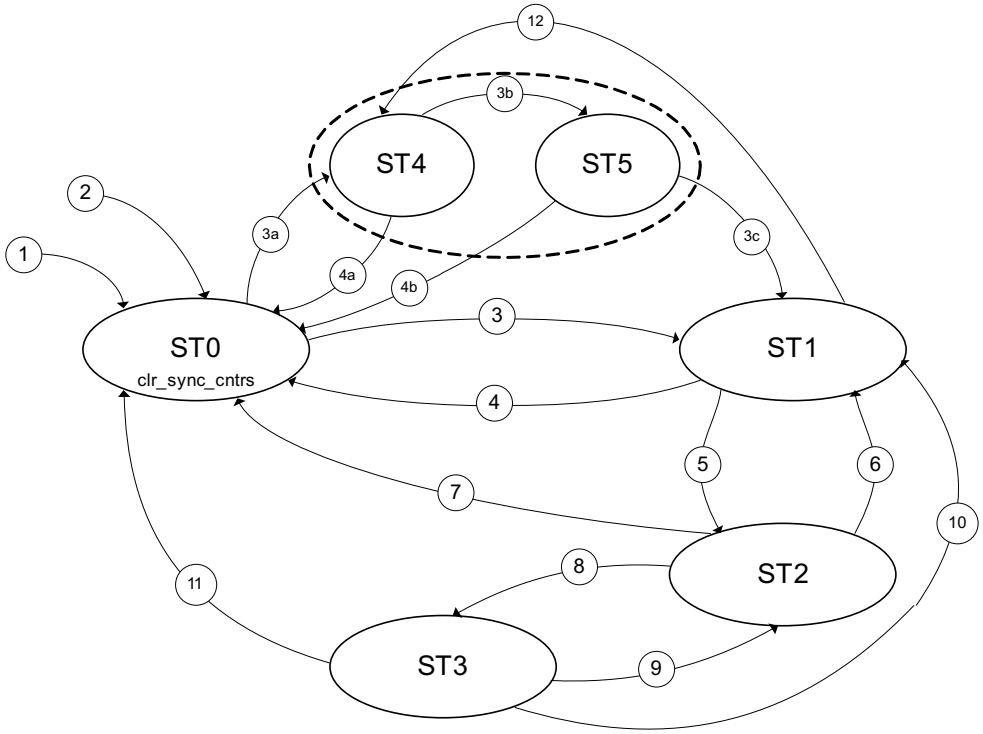


Table 7-14. Rx Sync FSM State Transition Table

Transition	OBSAI RP3 Description	CPRI Description
1	rst_n	rst_n
2	*!rx_en* | *sd_rm_los_dtct*	*!rx_en* | num_los_det (i.e. N * 8b10b errors in a Hyperframe) | *sd_rm_los_dtct*
3a	*scr_en* & *sync_t* consecutive valid blocks of bytes received	n/a
3b	*scr_en* & Scrambling seed captured and verified	n/a
3c	*scr_en* & Acknowledge training pattern received	n/a
3	*! scr_en* & *sync_t* consecutive valid blocks of bytes received	K28.5 byte received & !(num_los_det | *sd_rm_los_dtct*)
4a	*unsync_t* consecutive invalid blocks of bytes received	n/a
4b	*unsync_t* consecutive invalid blocks of bytes received	n/a
4	*unsync_t* consecutive invalid blocks of bytes received	K28.5 byte !received & (y_cntr = 0 & w_cntr = 0 & x_cntr = 0)
5	One K28.7 Idle byte received	(K28.5 byte received & (y_cntr = 0 & w_cntr = 0 & x_cntr = 0)) occurs *sync_t* consecutive times
6	*frame_unsync_t* consecutive invalid message groups received	n/a
7	*unsync_t* consecutive invalid blocks of bytes received	(K28.5 byte !received & (y_cntr = 0 & w_cntr = 0 & x_cntr = 0)) occurs *unsync_t* consecutive times
8	*frame_sync_t* consecutive valid message groups received	(K28.5 byte received & (y_cntr = 0 & w_cntr = 0 & x_cntr = 0)) *frame_sync_t* consecutive times
9	n/a	(K28.5 byte !received & (y_cntr = 0 & w_cntr = 0 & x_cntr = 0)) *frame_unsync_t* consecutive times
10	*frame_unsync_t* consecutive invalid message groups received (Idle order matters)	n/a
11	*unsync_t* consecutive invalid blocks of bytes received OR (lcv_unsync_en & num_los_det)	n/a

Table 7-14. Rx Sync FSM State Transition Table (continued)

Transition	OBSAI RP3 Description	CPRI Description
12	IDEL_REQ pattern detected	n/a

Table 7-15. Rx Sync FSM State Names

State	OBSAI RP3 Name	CPRI Name
ST0	UNSYNC	XACQ1
ST1	WAIT_FOR_K28.7_IDLES	XACQ *n*
ST2	WAIT_FOR_FRAME_SYNC_T	XSYNC *n*
ST3	FRAME_SYNC	HFNSYNC
ST4	WAIT_FOR_SEED	n/a
ST5	WAIT_FOR_ACK	n/a'

The following comprise the CPRI synchronization counters:

- y_cntr = Byte Number within a word (0 to 1, 0 to 3, 0 to 4 or 0 to 7 or 0 to 9 or 0 to 15 depending on link rates 2x, 4x, 5x, 8x 10, 16x respectively)
- w_cntr = Word counter in a Basic Frame (0 up to 32)
- b_cntr = Byte counter per word (0 to 63)
- x_cntr = Basic Frame counter (0 to 255)

7.6.5.4.6 CPRI L1-Inband Signals

The RM captures all of the CPRI L1 In-band registers and stores them in status registers. The L1 In-band registers within Xs=2 of the CPRI frame are used to drive the TM L1 In-band signals. The L1 In-band Reset signal is monitored for a remote SoC reset command. An SoC Reset command is determined if five consecutive L1 In-band Reset signals are received high. The command is cleared if the L1 In-band Reset signal is receive low for five consecutive frames. The SoC Reset command sets the SOC_RESET signal from the RM. This signal is masked from generating a reset if the **PHY_RM_CFG.RST_EN[1]** bit is not enabled high.

7.6.5.5 TM Module

The Tx Mac (TM) block supports the data path connection to a SerDes module transmit link of AIL Phy. The Tx Mac converts an eight-byte-wide parallel stream into a two-byte-wide parallel stream in the system clock domain of the transmitted signal that is clocked directly into the SerDes module. The Tx Mac also provides frame formatting and synchronization, and serial coding of either an OBSAI or CPRI signal.

7.6.5.5.1 8b10b Encoding

Serial Coding for the transmitted signal is performed within the system clock domain on two-byte clock boundaries. A 20-bit coded data word clocked at the system clock rate is the interface used to transfer data between the TM Module and the SerDes module. The Transmit Serial Coding converts two-byte-wide transmit data to 8b/10b encoded transmit symbols for input to the SerDes module that is then to be transmitted over an external differential pair high-speed serial link. The 8b10b coding manages a running disparity over the sequential bytes to determine coding selections to achieve optimal ones density. The 8b/10b coder acknowledges K character indication from the output of the transmit FIFO to support comma character insertion that are used for OBSAI and CPRI frame synchronization and byte alignment of the serial interface.

7.6.5.5.2 TM Frame Synchronization

The TM Synchronization Data Path provides the infrastructure that utilizes control signals from the Tx FSM to generate the frame formats for both OBSAI and CPRI on the transmitted signal. The transmit data is byte-aligned to the frame format on a two-byte lane data path. The frame is established by the insertion of K28.7 and K28.5 characters by Frame Control logic. The K28.7 and K28.5 characters indicate start of frame or idle conditions. The data that is transmitted is either from the Tx FIFO (when data is ready), or from a generated empty frame.

Data is optionally scrambled for OBSAI 8x rate, or CPRI 16x,10x, 8x only, but K characters are never scrambled. In OBSAI mode, the scrambler is placed into an initialization phase with an initial seed value in **PHY_TM_SCR_CTRL_CFG.SEED_VALUE[6:0]** and need to be enabled by **PHY_TM_SCR_CTRL_CFG.SCR_EN.** In CPRI mode, data is scrambled from the first hyperframe boundary when the scrambler is enabled by a valid non-zero seed is programmed. Data is scrambled with a seed that is programmed within an **PHY_TM_CPRI_SCR_CTRL_CFG.SEED_VALUE[30:0]**.

The Tx FSM within the Transmit Control Logic manages the multiplexing within the data path.

In OBSAI mode, the Tx FSM determines to transmit:

1) Data from the CO_TM Interface

2) A K28.7 at master frame boundaries

3) AK28.5 character at message group boundaries that are not master frame

4) Data for the Scrambling Seed Protocol

5) Empty Messages (if Tx FIFO not ready or flushed)

In CPRI mode, the Tx FSM determines to transmit

1) Data from the CO_TM Interface

2) K28.5 Comma Byte

3) All other Synchronization words

4) All L1 In-band signaling control words, including HFN, BFN, PtrP

5) Empty IQ Data (if Tx FIFO not ready or flushed)

The Transmit Control Logic and the Tx FSM uses the delta signal from the Antenna Timer Subsystem to determine transmission of the K28.7 master frame value in OBSAI, and the K28.5 comma detect byte in CPRI, and then multiplexes all other data sources to the transmit data path by counting byte clocks. Once the delta pulse is detected and the TM Enable MMR bit is set, data is transmitted. The data transmitted is empty data of all zeros in the IQ data, and either empty messages in OBSAI or synchronization and L1inband control words with all other control words set to zero in CPRI. Once the Tx Fifo Ready signal is active, valid messages and data from the Tx Fifo fill the transmitted frames.

In OBSAI 8x mode, feedback from the Rx FSM in the associated RM link affects the use of the seed initialization sequence that is necessary to acquire the scrambling seed. This usually occurs before empty frames are transmitted from power up, but could be enabled at anytime the Rx FSM is in a state that requires the seed value. The feedback from the Rx FSM must be selected from up to eight sources and must be re-synchronization to the system clock boundary of the TM block.

7.6.5.5.3 Transmit Control Logic / Tx FSM

The Transmit Control logic contains the Tx FSM finite state machine that manages the operation of the transmit data path. The state machine performs similar transitions in both OBSAI and CPRI modes. The basic operation in both modes provides a status of frame transmission on the transmitted signal that is used to manage the control signals of the data path.

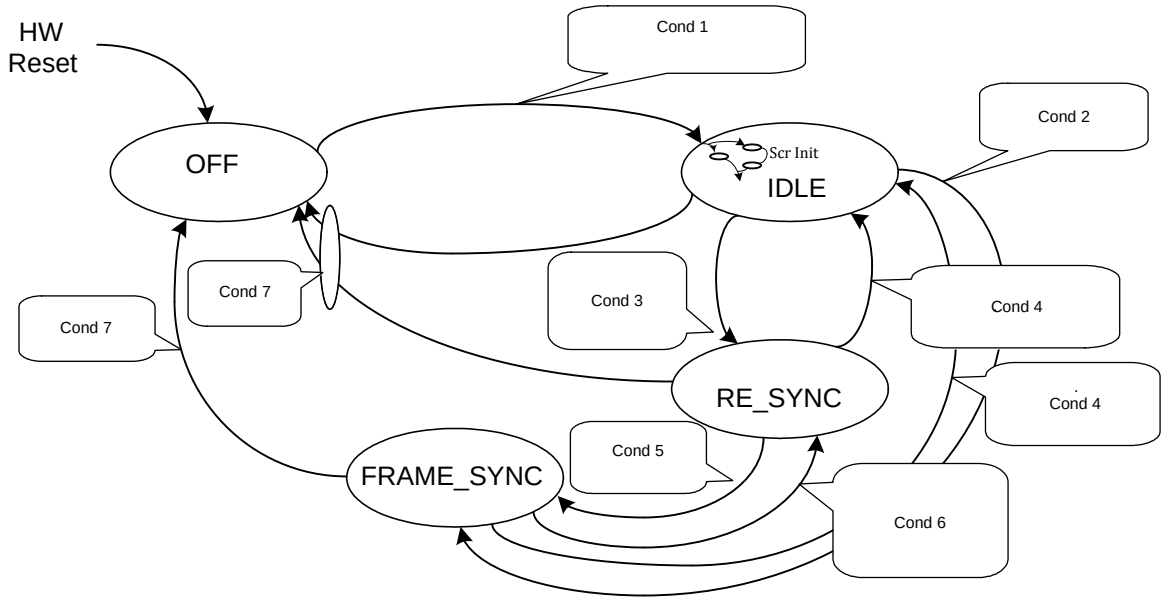
Table 7-16. Tx FSM Transition Conditions

Transition	Condition
Cond 1	TM Enable and not (RM Loss of Signal and LOS_EN)
Cond 2	Delta Pulse and FIFO Ready and (not Scr_En or (Scr_En & RM_Seed_Acq and RM_IDLE_ACK))

Table 7-16. Tx FSM Transition Conditions (continued)

Transition	Condition
Cond 3	Delta Pulse and FIFO Not Ready and (not Scr_En or (Scr_En & RM_Seed_Acq and RM_IDLE_ACK))
Cond 4	Scr_En and not (RM_Seed_Acq and RM_IDLE_ACK)
Cond 5	FIFO Ready and Delta Pulse
Cond 6	Transmit Data Frame Mismatch or FIFO Starve or Delta Pulse Inactive/Modified or TM_FLUSH
Cond 7	TM Disable or (RM Loss of Signal and LOS_En)

Figure 7-39. TM Tx FSM State Transitions



In general, the state machine resets to an ‘Off’ state that indicates the data path is not yet operational. Upon enabling of the TM block, the state machine transitions to the ‘IDLE’ state in which it forces the Tx Mac to generate K characters. Upon reception of the ‘Delta’ pulse (TM_FB signal), the state machine transitions to the ‘Re-Sync’ state that initiates the construction of empty frames and messages that are transmitted. The state machine waits for the FIFO to be ready so that it can transit to the ‘Frame Sync’ state for normal transmit operation. The ‘Frame Sync’ state is exited upon FIFO starvation, a missing or changed ‘Delta’ pulsed, or upon a disabling of the TM block.

7.6.5.5.4 Tx FSM Payload Scrambling Control

Scrambler Control for OBSAI consists of a configuration **PHY_TM_SCR_CTRL_CFG.SCR_EN** and **PHY_TM_SCR_CTRL_CFG.SEED_VALUE** that enables the scrambling, a mode signal that toggles the scrambler between operational and initialization modes, and state transitions of a separate Scrambler FSM dedicated to the scrambler initialization process. In OBSAI mode, the Scrambler FSM is enabled to control a scrambler seed initialization process while the Tx FSM is in the IDLE state.

In CPRI mode, the **PHY_TM_CPRI_SCR_CTRL_CFG.SEED_VALUE[30:0]** is all that is needed to enable and perform scrambling on payload. The Tx FSM provides control signals to the data path to allow scrambling on all payload except for the comma byte and the synchronization byte following the comma byte. The scrambling sequence is initialized at the beginning of every hyperframe with a 31-bit scrambler seed. During changes in the scrambling seed register, the changes are allowed to take effect on the next hyperframe boundary of the transmitted data.

7.6.5.5.5 K Character Indication

The K characters are inserted and checked from the data path by the frame synchronization logic within the system clock domain. A K character indication bit is associated with each byte in the transmit path so that the 8b/10b coding blocks can recognize the characters. A K character signal is derived from the 8b/10b decoding blocks so that byte alignment can be achieved in the SerDes module, and the receiver frame synchronization can be informed of K character reception.

7.6.5.5.6 Empty Message and Empty Frame Insertion – TM Fail

The Transmit Frame Control block begins transmitting frames once the block is enabled and the frame sync pulse is received from the Antenna Timer Subsystem. If data is not available, the Transmit Control Logic and Tx FSM initializes a TM Fail condition on the link. Upon the TM Fail condition, the TM Flush signal becomes active and effectively signals the preceding blocks in the data path that data was not available while the TM block was ready to transmit. During the TM Fail condition, the TM Block transmits empty messages while in OBSAI mode, and empty Basic Frames while in CPRI mode until the next master frame boundary for which data is available from the Tx FIFO.

7.6.5.6 CI/CO Module

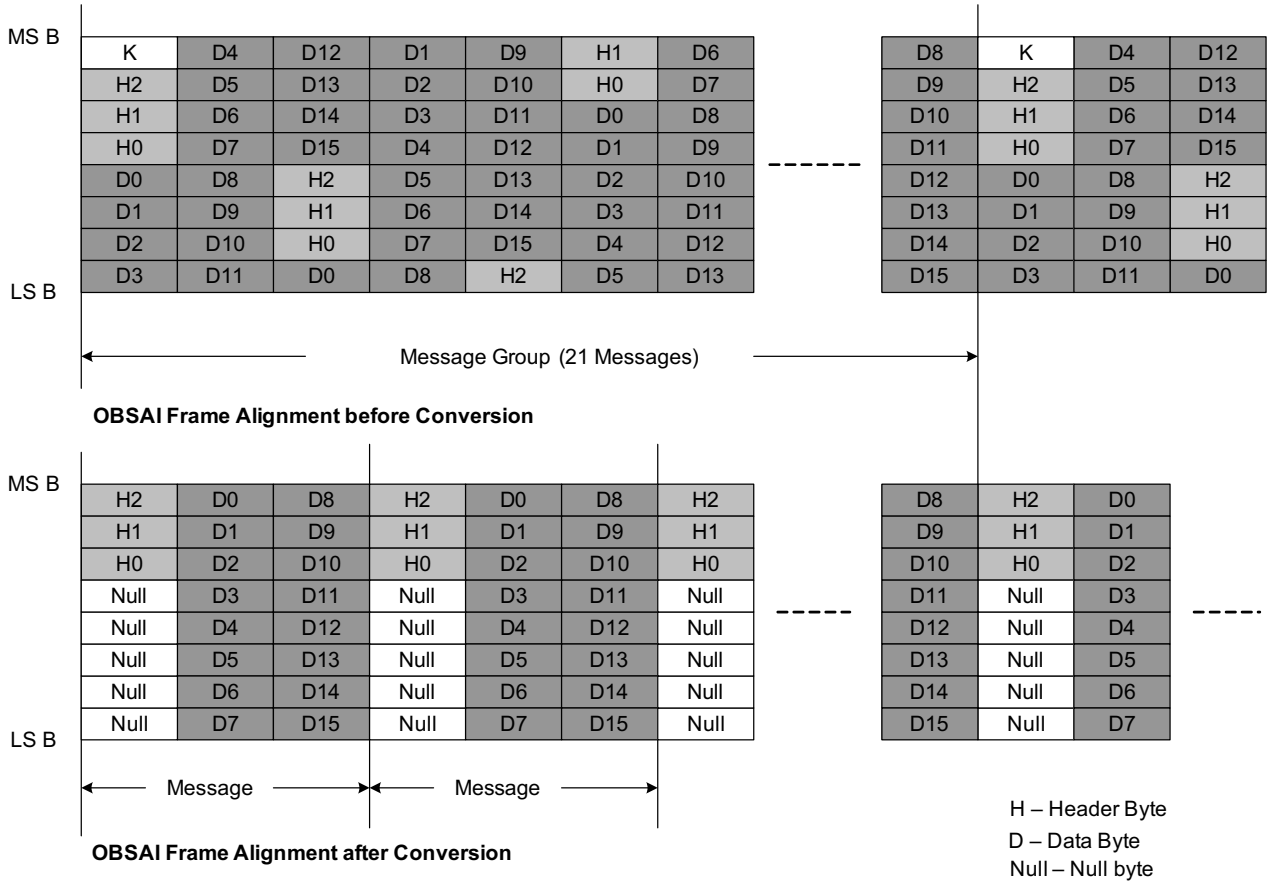
7.6.5.6.1 CI functionality

The CPRI Input Conversion of the AIL Phy aligns CPRI and OBSAI samples to 4-byte boundaries with the AIL Phy Physical Interface data path. For OBSAI, messages are aligned to an eight-byte-wide block. Since an OBSAI message is 19 bytes, each block requires and address phase that aligns the three address bytes to the least significant three bytes of the data path, and two data phases that each transfers eight bytes of data.

For CPRI, basic frames are terminated to create a control word phase, and a data phase. The control word phase consists of one bus cycle for CPRI 8x, 5x, 4x, 2x, and consists of two bus cycles for CPRI 16x, 10x. The data phase consists of multiple bus cycles carrying two data samples, each sample aligned to a four-byte boundary of the bus. The data phase utilizes as many bus cycles as required to terminate all of the antenna carrier containers within the basic frame.

For OBSAI formats, the conversion process is shown in Figure 7-40. It is expected that OBSAI message groups are aligned to the eight-byte boundary of the input data bus. The conversion process modifies the input so that OBSAI messages are isolated on the resultant 8-byte bus.

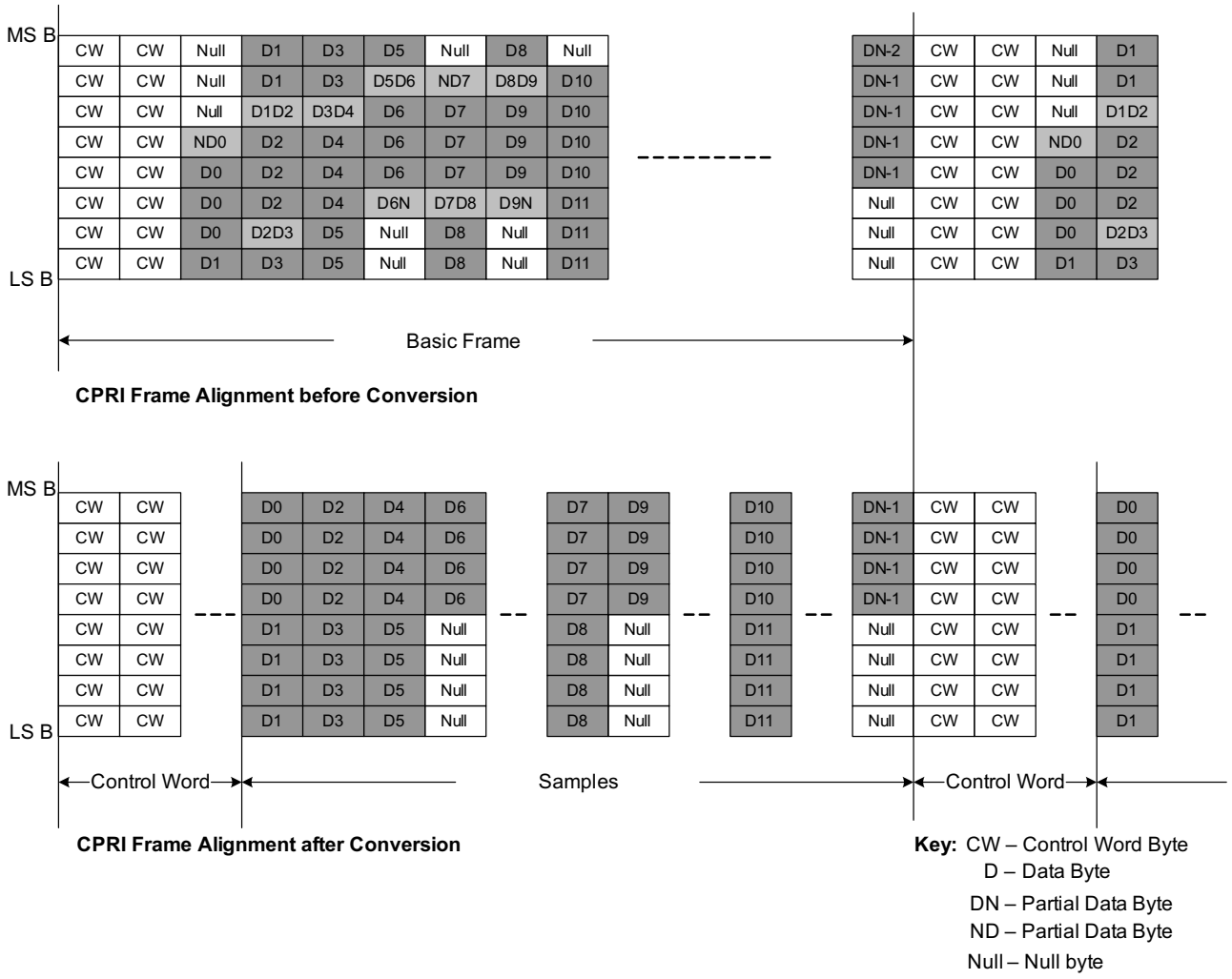
Figure 7-40. CI OBSAI Frame Alignments



In CPRI format, an antenna container group boundary can be placed on any even bit within the basic frame and any offsets between groups must be an even number of bits. All of the containers within a container group must be mapped back to back without offsets or gaps. Each container can be thirty bits of 15-bit IQ data or the case of two 7-bit IQ data with an over-sampling ratio of two and two additional reserved bits, or 32 bits of 16-bit IQ data or the case of two 8-bit IQ data with an over-sampling ratio of two, but all of the samples within an antenna carrier container group must have the same sample size. For 30-bit samples, the resultant bus aligns each 15-bit sample over 16 bits of the bus with the most significant bit replicated, and it aligns each 7-bit sample over 8 bits of the bus with the most significant bit replicated.

The following CPRI example (Figure 7-41) shows a possible configuration for a basic frame for a CPRI 16x link that contains three antenna carrier container groups, the first container group with 30-bit samples and the second and third container groups with 32-bit samples. For CPRI 16x links, the input bus is eight bytes wide and it is expected that the CPRI basic frame is aligned to the 8-byte data path.

Figure 7-41. CI CPRI 16x Frame Alignments



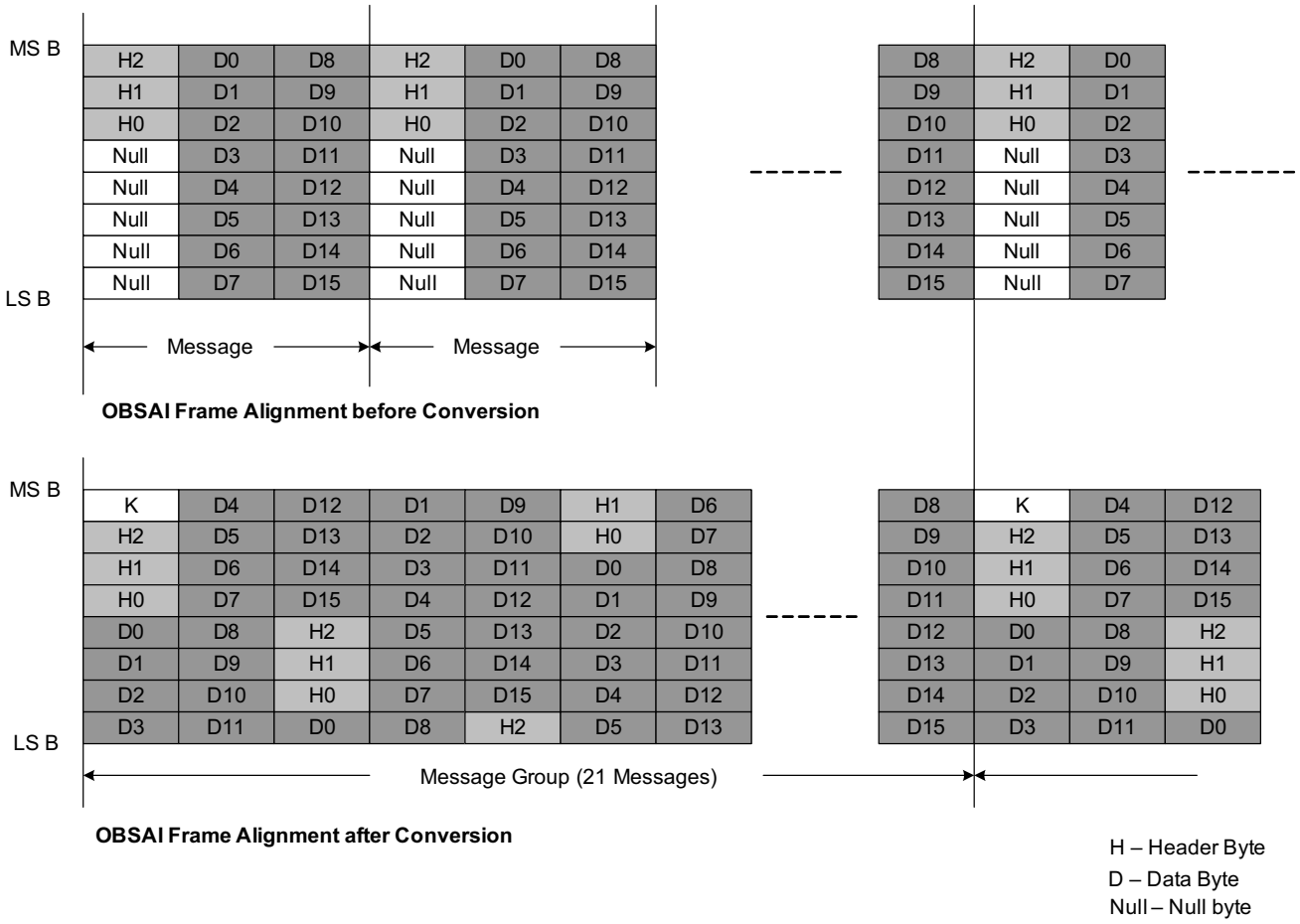
7.6.5.6.2 CO functionality

The CPRI Output Conversion of the AIL Phy modifies CPRI and OBSAI samples to a streamed parallel interface that emulates the external frame format to be transmitted from the TM.

For OBSAI, messages blocks contained on an 8-byte data path with header cycles separated from data cycles are re-configured into message groups that are aligned to an eight-byte data path in which the data is a parallel stream of the actual external OBSAI frame format. For CPRI, basic frames are regenerated from data samples so the antenna carriers are aligned within antenna carrier boundaries and I and Q data bits are interleaved.

For OBSAI formats, the conversion process is shown in Figure 7-42. It is expected that OBSAI messages are aligned to the eight-byte input data bus such that the OBSAI 3-byte address is received over the three least significant bits of the bus first, followed by two 8-byte wide data fields. The conversion process modifies the input so that OBSAI message groups are contiguous on the resultant 8-byte bus.

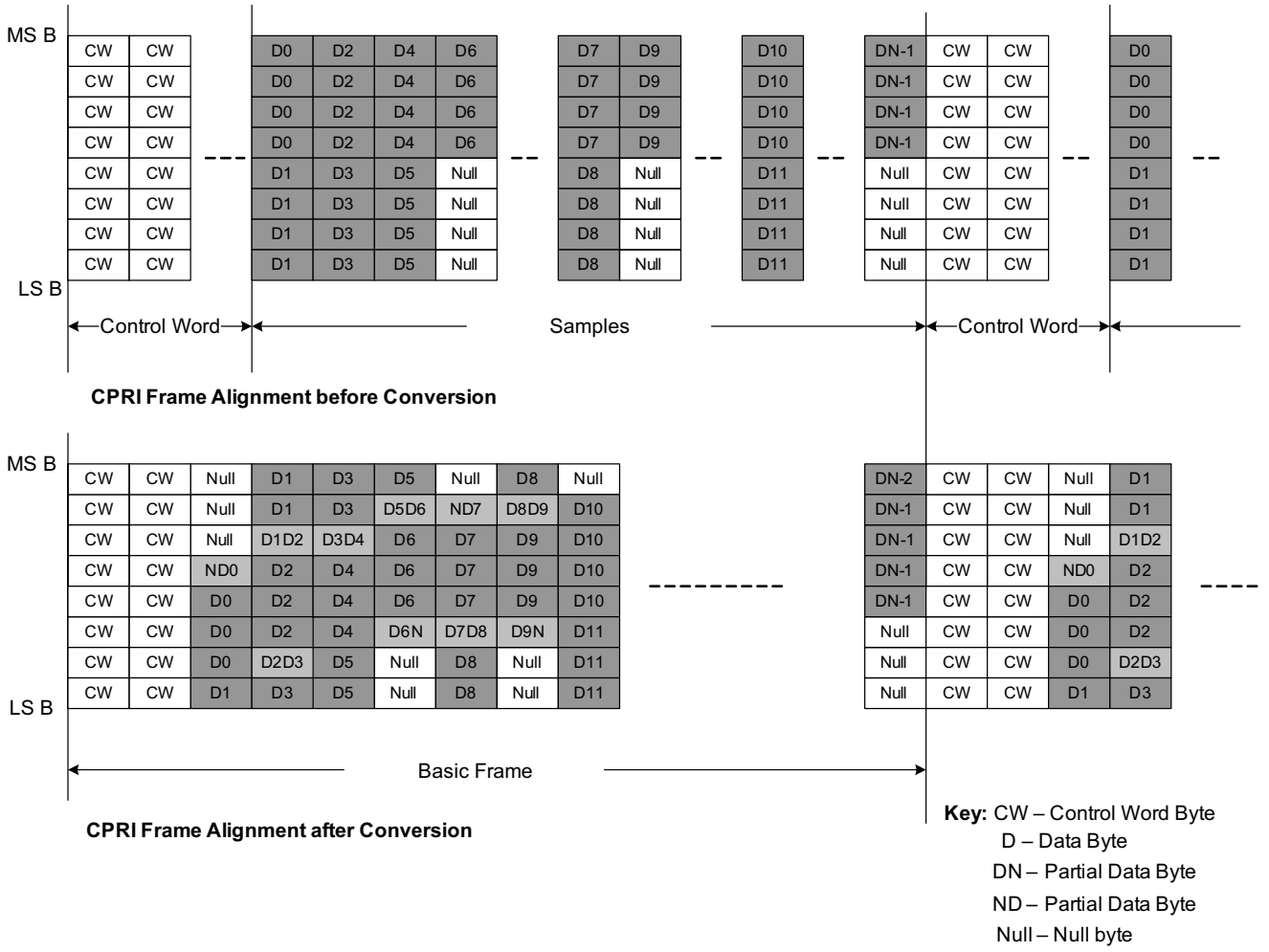
Figure 7-42. CO OBSAI Frame Alignments



For CPRI formats, an antenna container group boundary can be placed on any even bit within the basic frame and any offsets between groups must be an even number of bits. Each container can be thirty bits of 15-bit IQ data or the case of two 7-bit IQ data with an over-sampling ratio of two and two additional reserved bits, or 32 bits for the case of one 16-bit IQ data or the case of two 8-bit IQ data with an over-sampling ratio of two, but all of the samples within an antenna carrier container group must have the same sample size. For 30-bit samples, it is expected that the input bus aligns each 15-bit sample over 16 bits of the bus with the most significant bit replicated, and it aligns each 7-bit sample over eight bits of the bus with the most significant bit replicated.

Figure 7-43 shows a possible configuration for a basic frame for a CPRI 16x link that contains three antenna carrier container groups, the first container group with 30-bit samples and the second and third container groups with 32-bit samples. For CPRI 16x links, the output bus is eight bytes wide and it is expected that the CPRI basic frame is aligned to the 8-byte data path.

Figure 7-43. CO CPRI 16x Frame Alignments



For 7 or 15-bit data, the incoming values need to be saturated and shifted.The saturation logic determines saturation on individual I and Q samples based on the sample value exceeding the maximum allowable positive or negative value. The maximum allowable values and the saturation values are shown in Table 7-17.

Table 7-17. CO Block Saturation Values

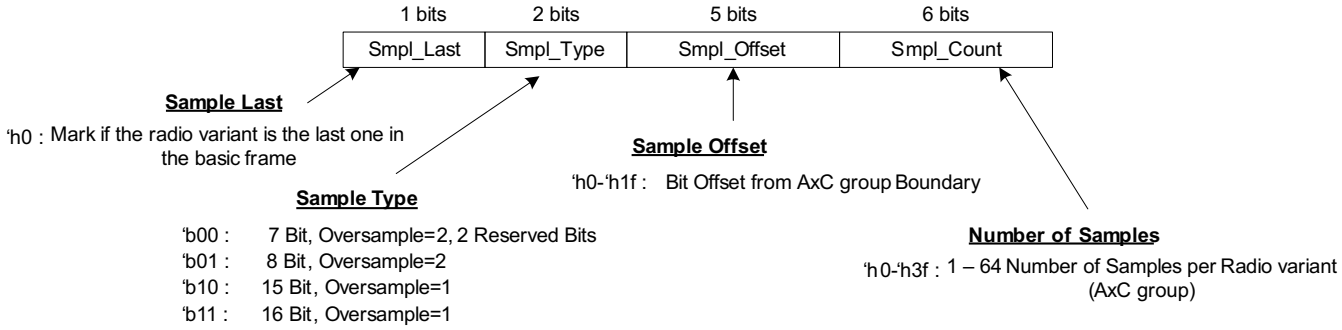
Number of bits	Sample Size	Input Range	Output Result
8	7	8'h40 – 8'h7f (Positive)	8'h3f
8	7	8'hc0 – 8'h81 (Negative)	8'h40
16	15	16'h4000-16'h7fff (Positive)	16'h3fff
16	15	16'hc000 – 16'h8001 (Negative)	16'h4000

7.6.5.6.3 CI/CO AxC Container Configuration LUT Description

The CPRI Input and Output Conversion block utilizes entries from a look-up table (LUT) in a RAM block to define the conversion process. There are up to eight LUT entries. The LUT entries identify the number of samples, the size of the samples, and the offset of the antenna carrier container group boundary. The format of the LUT entries is shown below. The offset is a 5-bit value that must always indicate an even number of bits with a maximum of 30. This value indicates the offset of the next antenna carrier container group from the end of the last container group, or from the beginning of the I/Q data of the basic frame.

The number of antenna carriers in any one antenna carrier container group can be up to a maximum of 64. This is determined by a six-bit value from 0 to ‘x3f. The first two bits indicate the sample characteristics, either 7-bit samples with over-sampling ratio of two plus two reserved bits, 8-bit samples with over-sampling ratio of two, 15-bit samples with over-sampling ratio of one, or 16-bit samples with over-sampling ratio of one.

Figure 7-44. CI/CO CPRI Input/Output Conversion AxC Container Configuration LUT Entry



The CPRI Input/Output Converter state machine retrieves and decodes the AxC Container Configuration LUT entries in order to perform the CPRI conversion. Each antenna carrier container group boundary must begin within 32 bits of the end of the previous container group boundary. The containers within each container group are packed with samples as either 30-bit or 32-bit entries without gaps. The converter logic decodes the data within each container as valid samples until the number of the samples in the LUT entry is fulfilled, then the state machine retrieves the next LUT entry and decodes the next container. The state machine will wrap back to the first LUT entry once the basic frame is exhausted with possible containers or the LUT is exhausted.

The LUT entry table is implemented with an A table and a B table. The table is selected by a the **PHY_CI(CO)_LUT_CFG** configuration register. The table selection is made active upon a valid SOF indication. The dual table approach makes it possible to update the table while affecting some radio standards but not affecting others.

7.6.5.6.4 CI/CO programming

The AIL supports the utilization of up to eight radio variants within a CPRI signal. These eight radio variants are mapped into programmed partitioned segments in a fixed and equivalent manner within each basic frame of the CPRI protocol. The AIL PHY CI and CO blocks provide programmable MMRs that manage the decoding of individual AxC positions in the radio variant mapping of the CPRI basic frame.

The MMR space of the CI and CO blocks consists of eight entries, each of which specify the characteristics of the fixed AxC mapping for each radio variant mapped into the CPRI basic frame. These MMRs, numbered 0 - 7, define the use of the CPRI PHY interface of the AIL only.

Each MMR register of the CI and CO blocks contains the following fields:

Smpl_Count - a 6-bit value defining the number of consecutive AxC containers in the radio variant.

Smpl_Type - a 2-bit value indicating the type of container, of which there are four types:

- ‘h0: 7 bit samples within 30 bit containers
- ‘h1: 8 bit samples within 32 bit containers
- ‘h2: 15 bit samples within 30 bit containers
- ‘h3: 16 bit samples within 32 bit containers

Smpl_Offset - a-5 bit value indicating the amount of gap bits filling before the current radio variant.

Smpl_Last - Indicates the current radio variant is the last used to define the CPRI AxC mapping within the basic frame.

The AIL supports CPRI link rates that contain the following fixed number of bits in the AxC field of the Basic Frame:

- 2x Rate: 240 bits

- 4x Rate: 480 bits
- 5x Rate: 600 bits
- 8x Rate: 960 bits
- 10x Rate: 1200 bits
- 16x Rate: 1920 bits

The CI and CO state machines utilize the MMRs in consecutive order, from 0 to 7, to account for all of the fixed numbers of bits, determined by the link rate, in the AxC field of each basic frame. In order to characterize the data in the AxC field for each radio variant, the MMR fields for each entry are used as follows:

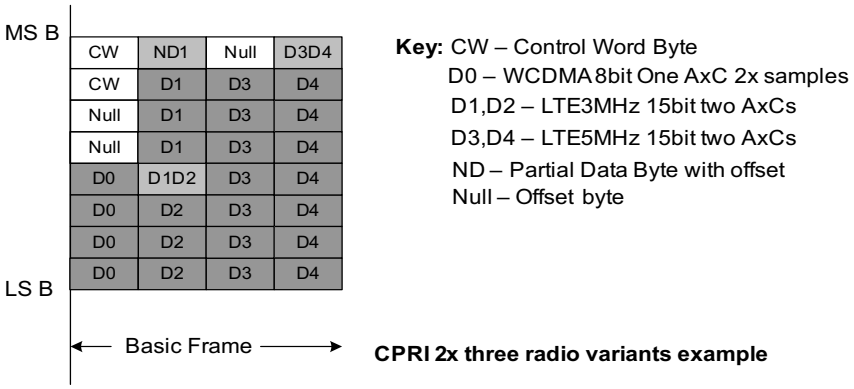
The Smpl_Offset is used first to determine the number of gap filler bits that must be bypassed before the current radio variant begins, then the Smpl_Type field is used to determine the size of each consecutive containers within the radio variant, and finally the Smpl_Count determines the number of consecutive samples that are mapped within the current radio variant.

The Smpl_Last bit, when set, indicates that the current radio variant is defining the last radio variant mapped into the basic frame, and must only be set when the total number of accumulated bits programmed into the MMRs equal the total number of fixed bits within the basic frame for the given link rate. If the last radio variant size is not long enough to be reached at the end of the basic frame, the Smpl_Count can be set larger than its original length as an extension or a dummy radio variant can be created to fill the Smpl_Count gap to the end of the basic frame. This dummy radio variant does nothing except hold a certain amount of container BW for correct CI/CO operation.

The Smpl_Offset field must be an even number, so even though there are 32 possible values for a 5-bit field, only the 16 even values are valid. The Smpl_Offset field is only five bits, allowing a maximum of 30 bit offsets between radio variants. Smpl_Offset is mainly used to fill the radio variant gap which caused by using a different sample type between radio variants (7-bit, 8-bit, 15-bit, 16-bit).

Example1: Consider a 2x link rate that contains three radio variants. The first radio variant supports a single WCDMA AxC channel of eight-bit samples (2x over sampled) and begins at a 16-bit offset from the very beginning of the AxC field of the basic frame. The second radio variant supports two LTE3MHz AxC channels of 15-bit samples and begins four bits after the end of the first radio variant. The third radio variant supports two LTE5 AxC channels of 15-bit samples and begins eight bits after the end of the second radio variant.

Figure 7-45. CPRI 2x Link Rate Three Radio Variants Example



WCDMA: Smpl_Count = 1 (set 0), Smpl_offset = 16, Smpl_type = 1, Smpl_Last = 0

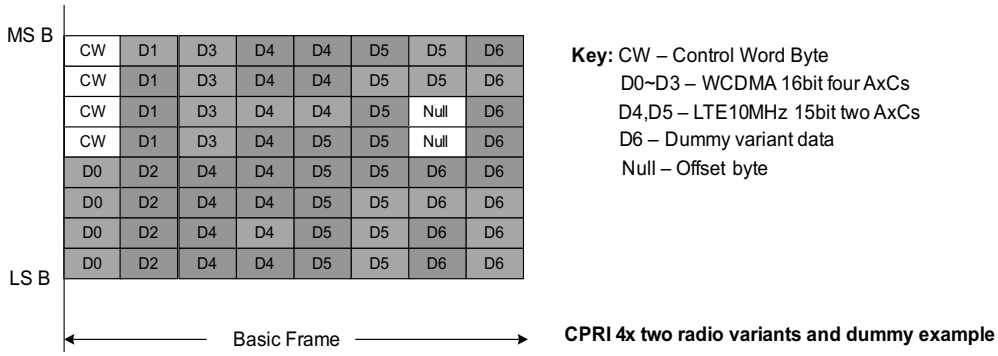
LTE3: Smpl_Count = 2 (set 1), Smpl_offset = 4, Smpl_type = 2, Smpl_Last = 0

LTE5: Smpl_Count = 4 (set 3), Smpl_offset = 8, Smpl_type = 2, Smpl_Last = 1

The total number of bits is 16 + (1*32) + 4 + (2*30) + 8+ (4*30) = 240 bits. This programming accounts for all of the 240 bits within the AxC field of a basic frame for a 2x link rate.

Example2: Consider a 4x link rate that contains two radio variants and a dummy variant. The first radio variant supports four WCDMA AxC channel of 16-bit samples and begins from the very beginning of the AxC field of the basic frame. The second radio variant supports one LTE20MHz AxC channel of 15-bit samples and begins without offset after the end of the first radio variant. The third radio variant is dummy and begins right after the end of the second radio variant and fill dummy data to the end of the basic frame.

Figure 7-46. CPRI 4x Link Rate Two Radio Variants and Dummy Example



WCDMA: Smpl_Count = 4 (set 3), Smpl_offset = 0, Smpl_type = 3, Smpl_Last = 0

LTE10: Smpl_Count = 8 (set 7), Smpl_offset = 0, Smpl_type = 2, Smpl_Last = 0

Dummy: Smpl_Count = 3(set 2), Smpl_offset = 16, Smpl_type = 3, Smpl_Last = 1

The total number of bits is (4*32) + (8*30) + 16 + (3*32) = 480 bits. This programming accounts for all of the 480 bits within the AxC field of a basic frame for a 4x link rate.

7.6.5.7 RT Module

The Re-transmitter block connects the Protocol Encoders and the re-transmit path from the CPRI Input Converters to the transmit path of the AIL IP block. The re-transmitter supports selection of re-transmit path from available receive link to transmit link. The re-transmitter block has the ability to perform aggregation, transmit, or re-transmit functions on a message-per-message basis in OBSAI mode, or as fixed configuration in CPRI mode.

The block contains a 4K byte buffer designated the Rx Link FIFO and is designed to accommodate fiber drift of the received link. This buffer also is used to accommodate a window for the alignment of Pi and Delta. Upon initialization, the master frame boundary of the input data bus is first decoded, whereupon data is then written into the buffer. Depending on whether the configuration mode is for aggregate or re-transmit, the data in the buffer is either aligned with the frame boundary of the input bus from the PE module, or is forwarded to the TM until a flow control indication from the TM/CO indicates wait cycles needed by the TM logic to align with delta transmit timing.

The RT block can be configured to support CPRI uplink re-chaining. In this mode, the CPRI control words are stored in the Rx Link FIFO in unique address slots, and up to four basic frames of IQ data are stored in a Basic Frame Buffer. In order to buffer the hyperframe control words, the address of the Rx Link FIFO is indexed to store the hyperframe control words from address location zero starting with the synchronization byte 0.0.0 to the last control word in the hyperframe. The control words then are read on the transmit side of the Rx Link FIFO at the address slots that align with the position in the transmitted hyperframe.

7.6.5.7.1 Addition Block

The Addition Block is a mathematical unit that performs addition and saturation functions on individual I and Q samples within the transmitted payload. The addition function is configured for either 8-bit operation, or 16-bit operation. Each operation is performed on a single I or Q sample. The adder inputs are multiplexed for the different sample sizes.

Both the A and B inputs are sent to a comparator. The comparator generates an active signal to the RT Controller in the event that A and B do not match. The comparator is used to check consistency of the headers between OBSAI messages. The result of the comparator is aligned with the message boundaries in the RT Controller to determine a header mismatch on aggregated streams. The RT Controller has the ability to initiate an event of the occurrence of the mismatched header.

Saturation is performed on each adder output. Saturation logic detects addition overflow and replaces the overflowed value with a value based on the selected width. The saturation values are 8-bit data: +/- 127 and 16-bit data: +/- 32,767. Seven-bit or 15-bit saturation for CPRI output data is controlled by CO block.

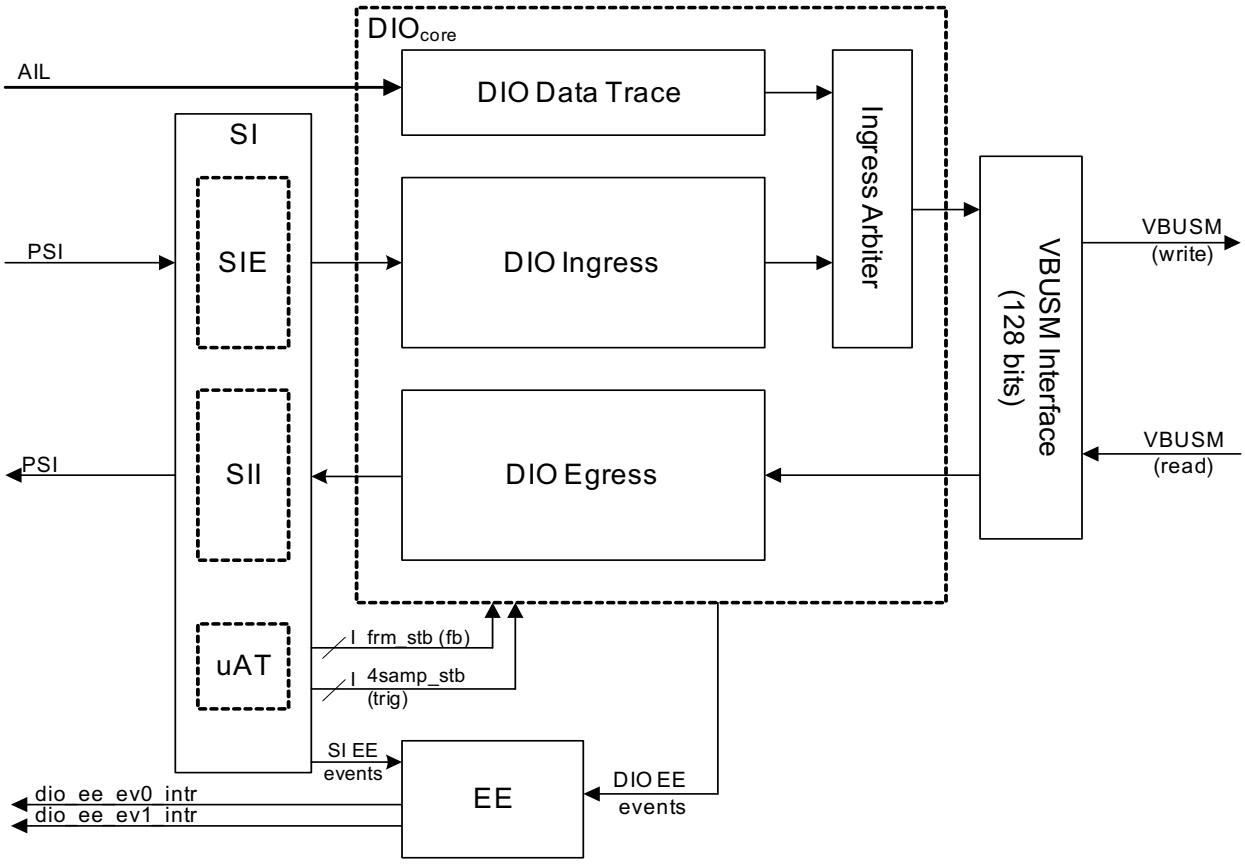
Table 7-18. RT Block Saturation Values

Number of Bits	Sample sSize	Input Range	Output Results
8	8	8'h80-8'hff(Positive) + CO	8'h7f
8	8	8'hc0-8'h81(Negative) + CO	8'h80
16	16	16'h8000-16'hffff(Positive) + CO	16'h7fff
16	16	16'hc000-16'h8001(Negative) + CO	16'h8000

7.7 DIO

The DIO allows for Direct I/O, non-packet-based DMA for WCDMA applications. It uses a common DMA engine design that is constructed specifically for WCDMA-based transfers. The DIO module controls the WCDMA IQ data coming from and going to the PSI bus with minimum latency. The DIO also implements RSA (RAC WCDMA UL format) Data Format Conversion for both the Ingress and Egress directions.

Figure 7-47. DIO Block Diagram



The DIO Ingress is comprised of a Data Buffer (RAM), three DMA engines and a Scheduler that ties the Data Buffer, DMA engines and VBUSM Interface together. The DIO Data Trace is comprised of a single, specialized DMA engine, a data trace buffer and data trace data format logic.

7.7.1 DMA Engine (DIO Core)

Both Ingress and Egress use the same DMA engine design. Three DMA engines are provided for each the Ingress and Egress. Since multiple DMA engines may be triggered at the same time, a priority scheme must be used. A round-robin algorithm is used where each DMA engine operates in sequence and runs to completion where engine zero has the highest priority. It may be beneficial to the user to place either the most latency sensitive target (e.g., TAC) or slowest target (e.g., DDR3) on the lower/lowest DMA channel.

DMA requests come from the uAT in the form of periodic events or triggers. Before a DMA engine will respond to a trigger event, two actions must occur; the DMA engine must be enabled and a Frame Boundary event must have been received from the uAT.

Each DMA engine has a Data Buffer Channel Number Table (DBCNT) LUT that the user programs with the Data Buffer Channel Number/ID, whether the channel is enabled or not and its corresponding AxC VBUS base address.

This table is double-buffered (i.e., ping/pong) so that channels may be added or deleted. The user indicates to the DMA engine (**dio_tabel_sel_cfg.bcn_table_sel[3]**), which table is to be active during the next frame. When **bcn_table_sel[3]=0**, Table A is selected and when **bcn_table_sel[3]=1**, Table B is selected. The non-selected table may be written any time between frame boundary strobes from the uAT. Switching tables, using **dio_tabel_sel_cfg.bcn_table_sel[I]**, must be done in the middle, between frame boundary strobes in order to assure that the new table takes effect in the next frame.

With the exception of **dio_tabel_sel_cfg.dma_num_axc[3], dio_tabel_sel_cfg.bcn_table_sel[3]** and the DBCNT tables themselves, the rest of the DMA configuration MMRs should not be changed while the DMA engine is operational or unexpected results may occur.

NOTE: When a DMA engine is enabled (e.g., **dio_dma_cfg0.dma_eng_en[3]** = 1), it will not start accepting uAT triggers until the next Frame Boundary strobe for that DMA engine is received. This is a very important aspect of synchronization which controls the DIO alignment of its data with the other radio components of the system.

NOTE: When a DMA engine is disabled (e.g., **dio_dma_cfg0.dma_eng_en[3]** = 0), it will continue to operate until the next Frame Boundary Strobe. At that point, the engine will shut down only when there are no pending triggers and any current transfers have completed, i.e., the engine has returned to the Idle state. In this way, Start of Frame can be defined as the first DMA block processed and End of Frame being the last DMA block processed in a BCNT loop.

It is important to note the following restrictions when programming the Data Buffer Channel Tables (DBCNT):

1. When **dio_dma_cfg0.dma_num_qw[3]** is programmed for one quad word per AxC, the next three entries in the table after the first must be sequential, e.g., 0, 1, 2, 3 or 4, 5, 6, 7 etc.
2. When **dio_dma_cfg0.dma_num_qw[3]** is programmed for two quad words per AxC, pairs of table entries must be sequential, e.g., 0, 1 or 5, 6 etc.
3. When **dio_dma_cfg0.dma_num_qw[3]** is programmed for four quad words per AxC, there are no restrictions.

7.7.2 DIO SI Sub-Module

The SI (IQN2 System Interface) submodule provides a common interface between the components of an IQN2 (i.e., AID, AIL, and DIO) and the IQN2 buffer or IQNB (switch) via the PSI bus for both the DIO Ingress and DIO Egress paths. The SI also provides the micro-AT (uAT) timer including up to eight SI ingress events and six DIO engine events generators.

NOTE: The SI allows for Endian swapping. However, this feature is not to be used with the DIO.

CAUTION

DIO, as a special case, has a reversed connection between the SI submodule and Core block. For downlink (SoC level Egress), the Egress DIO core is internally connected with ingress SI (SII) and the Ingress DIO core is connected with egress SI (SIE) for uplink (SoC level Ingress). This reversed internal block connection is only applied to DIO and not for the AIL and AID. This switched direction is also applied to uAT radio timers and events. Egress RAD timers are used for Egress SI frame strobe and four-sample strobe generation that must be used for SoC level Ingress (Uplink) operation. The user's special care needs to be taken for the programming of DIO MMRs.

The DIO uAT provides eight local Radio Timing along with Frame Strobes (FB) and four sample strobes (SB) for SI operation and also provides three DIO RAD timing on each direction along with 4, 8, 16 sample strobes for DIO engine operation.

DIO2_UAT_EGR_RADT[8]: Frame strobe and four-sample strobe used for Uplink (SIE) operation.

DIO2_UAT_ING_RADT[8]: Not used. DIO Downlink (SII) does not require Radio timer event.

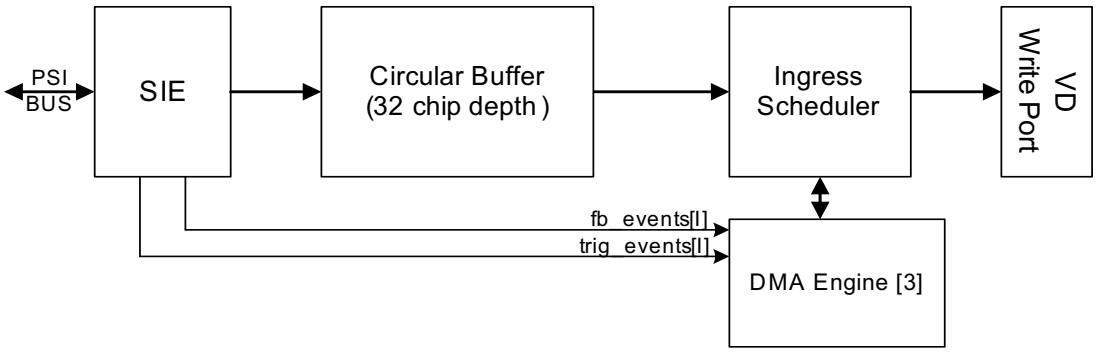
DIO2_UAT_DIO_EGR_RADT[3]: 4,8,16-sample strobes are used for Downlink (egress DIO engine) operation.

DIO2_UAT_DIO_ING_RADT[3]: 4,8,16-sample strobes are used for Uplink (ingress DIO engine) operation.

7.7.3 Uplink (Ingress)

The Ingress DIO provides multiple DMA engines to control the transfer of data from the DB buffers to each of multiple destinations: RAC, L2, MSMC, FFTC, or DDR3. Precise timing of transfers occurs based on uAT signaling.

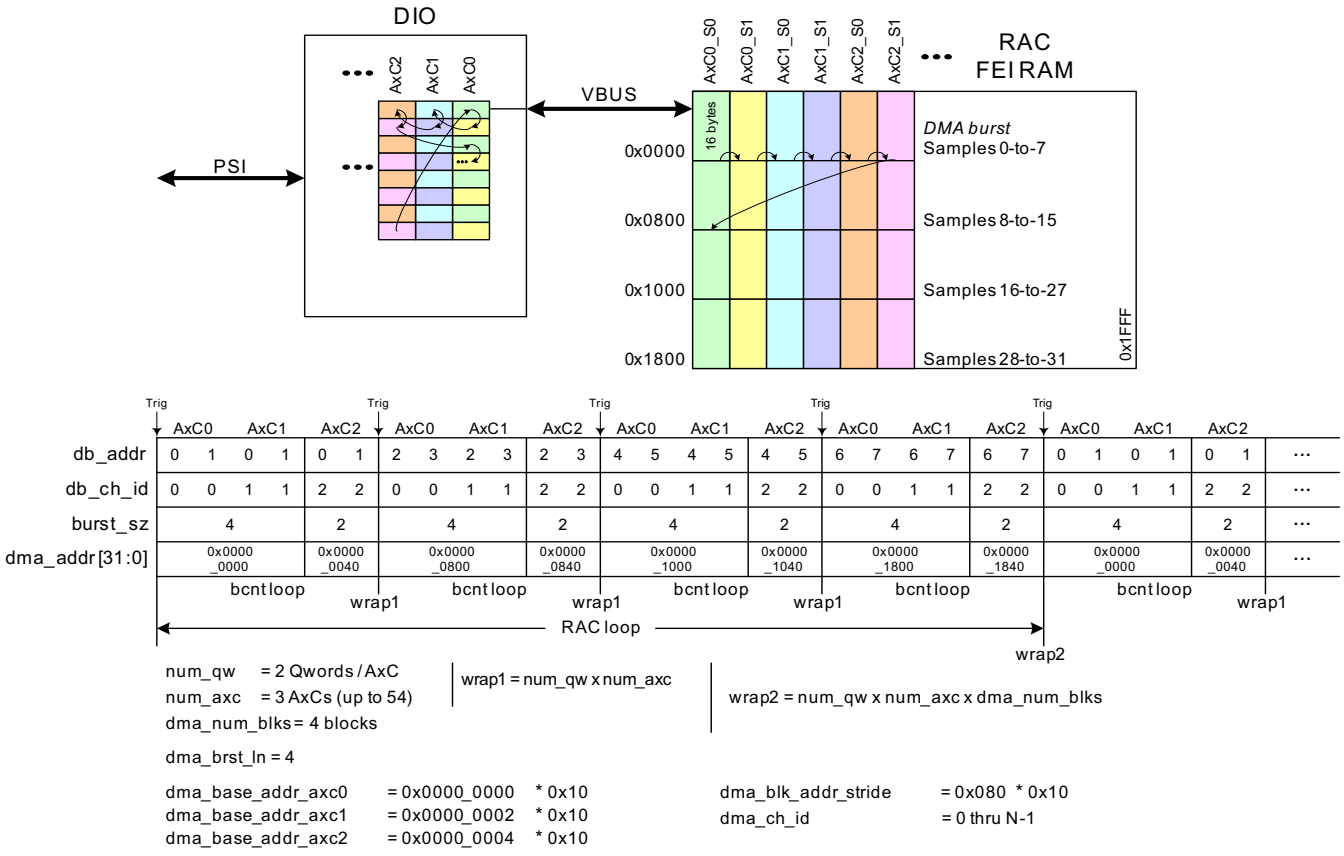
Figure 7-48. DIO Ingress Block Diagram



7.7.3.1 RAC Example

Figure 7-49 provides an example of how the DIO is programmed for RAC DMA. Trigger period is eight chips of time.

Figure 7-49. RAC Example

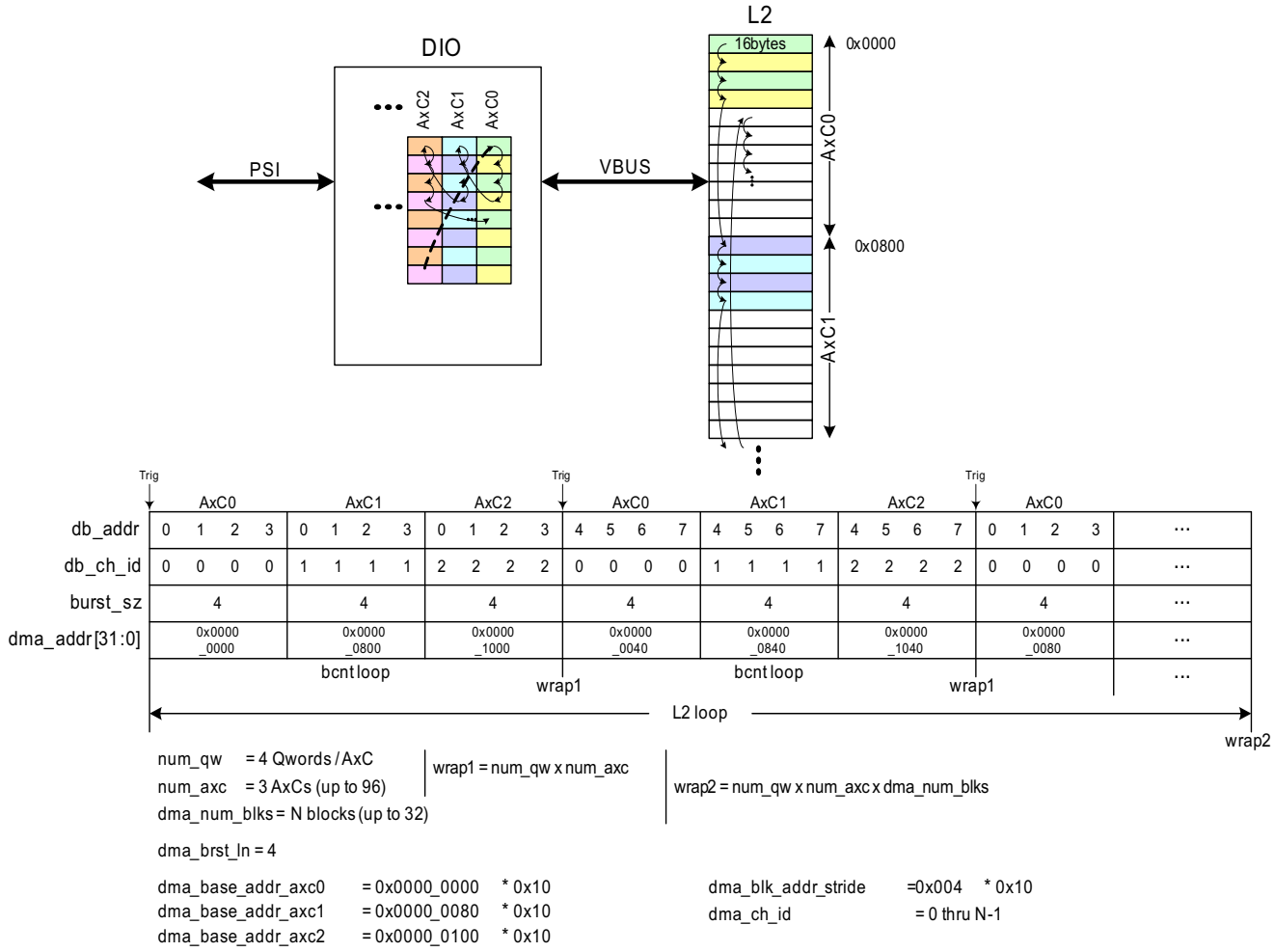


NOTE: The total number of quad samples in frame for the radio standard should be dividable by the dma_num_blks. i.e., WCDMA has 9600 quad samples per frame and it is not dividable by 256, so 256 cannot be used as dma_num_blks.

7.7.3.2 L2 / MSMC Example:

Figure 7-50 provides an example of how the DIO is programmed for L2 / MSMC DMA. Trigger period is 16 chips of time.

Figure 7-50. L2 / MSMC Example

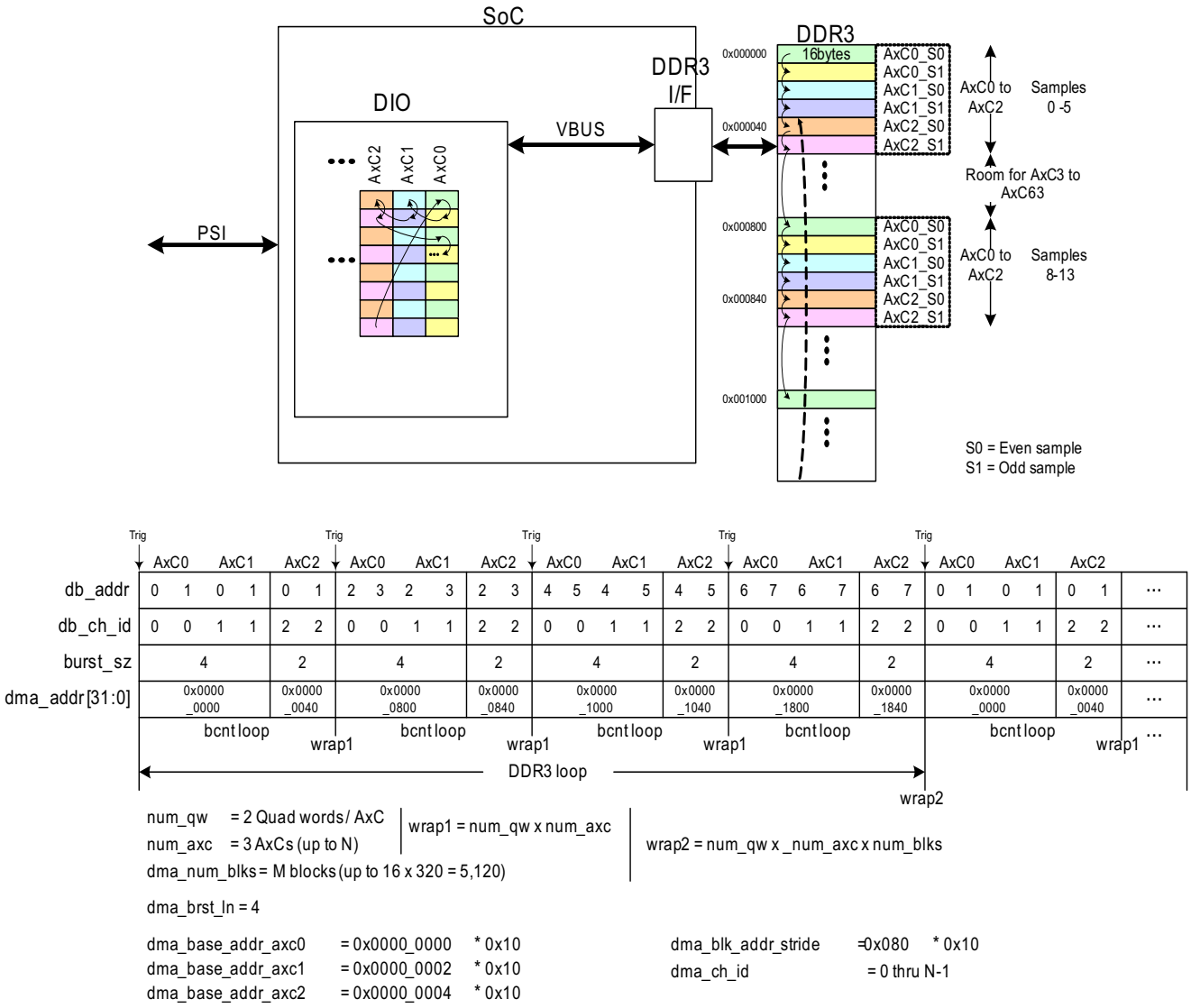


7.7.3.3 DDR3 Example:

DDR3 is used to store and later retrieve delayed data streams. Up to one frame plus one slot for “N” AxCs can be stored in this memory. There are 15 slots in a Frame, so the memory must be capable of storing up to 16 slots x 320 chips/slot = 40,960 chips of data for up to “N” AxCs.

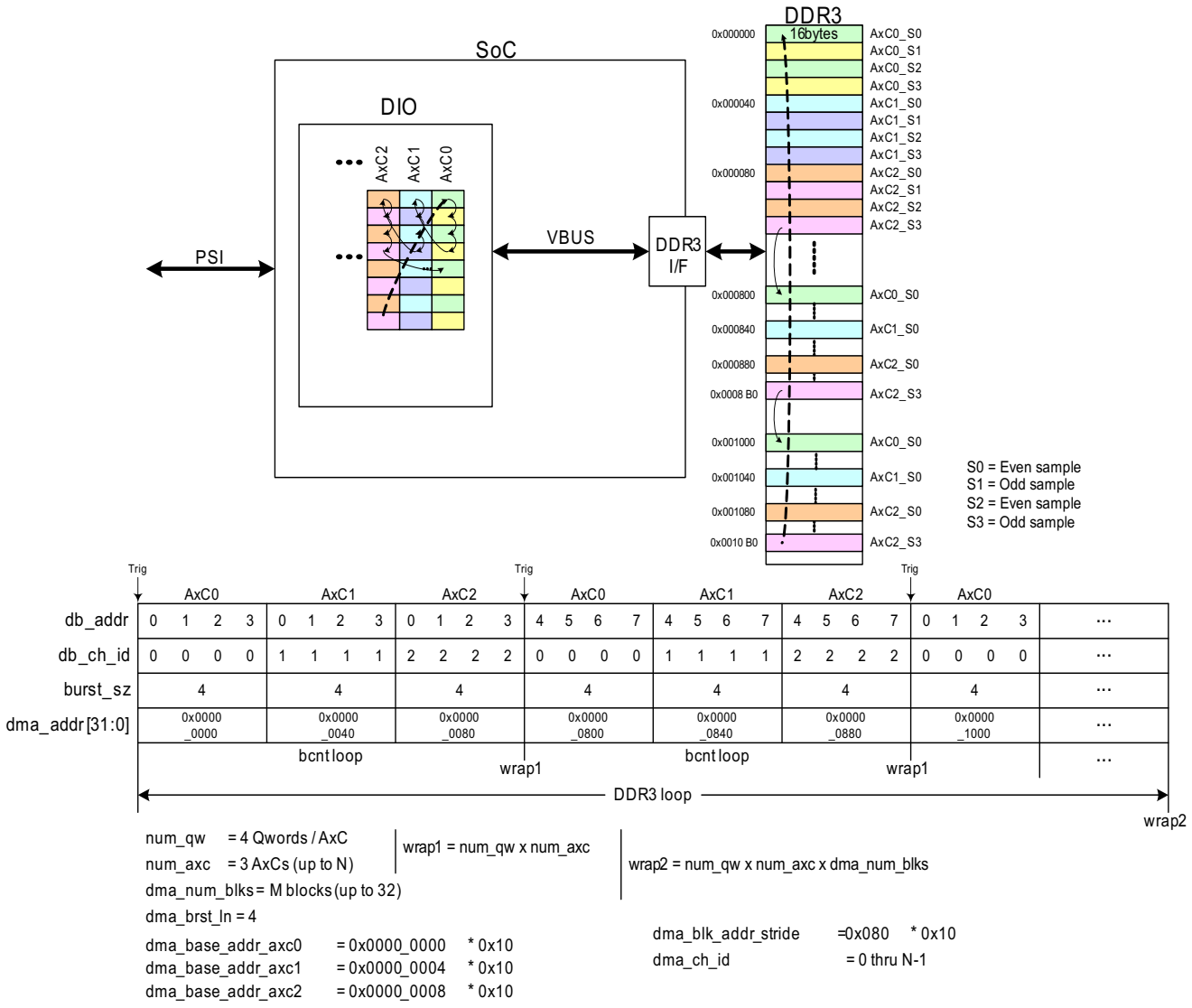
Figure 7-51 shows an example of how the DIO is programmed for DDR3 DMA. Trigger period is 8 or 16 chips of time. In this example, a pair of even and odd samples are written per AxC.

Figure 7-51. DDR3 Example 1



In Figure 7-52, two pair of even and odd samples are written per AxC. This is a much more efficient use of the VBUS and DDR controller.

Figure 7-52. DDR3 Example 2



7.7.3.4 Circular Data Buffer

The Ingress Circular Data Buffer consists of a 2-port RAM capable of handling “N” channels, each with a maximum depth of 128 bytes (32 chips). It also has logic to convert data into RSA WCDMA UL format. Based on control information from the DMA engine, data is pulled from the circular buffer and sent along with a VBUS address to the VBUSM Interface (VD) via the scheduler.

The Ingress AxC offset feature is a per-channel, Modulo 8 AxC offset in four sample (1 QW) increments that determine the starting address within a circular data buffer e.g., a value of 0 would cause zero offset and SOF data to be written to location 0 in a circular data buffer. A value of 1 would cause the SOF data to be written to a circular data buffer starting at location 1. A value of 0 would also represent an offset of 8, 16, etc. since the circular data buffer is modulo 8 in nature.

The RSA data format conversion logic separates the even and odd samples. The RSA data format conversion occurs on the output of data from the circular data buffer. The **DMA_CFG0[3].RSA_CNVRT_EN** field enables or disables the format conversion logic and little, big endian option can be selected from **GLOBAL_CFG.RSA_BIG_ENDIAN** MMR instead of using byte swap option in DIO SI.

Figure 7-53. RSA UL Data Format Conversion (Big Endian)

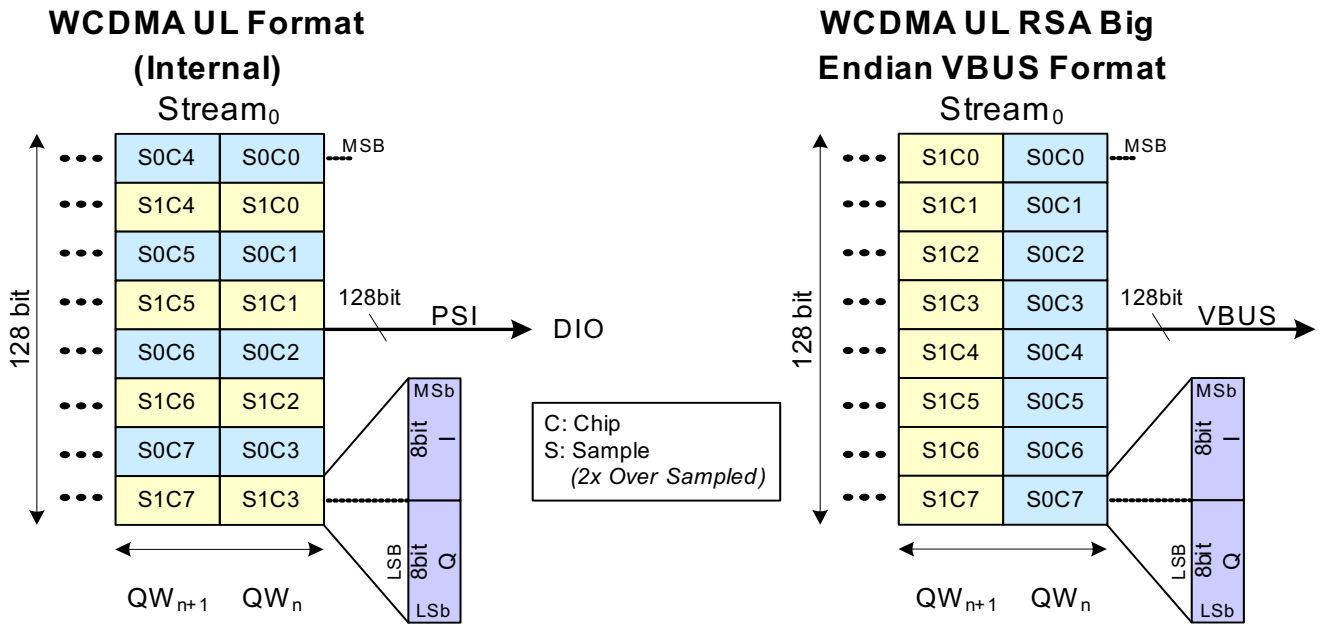
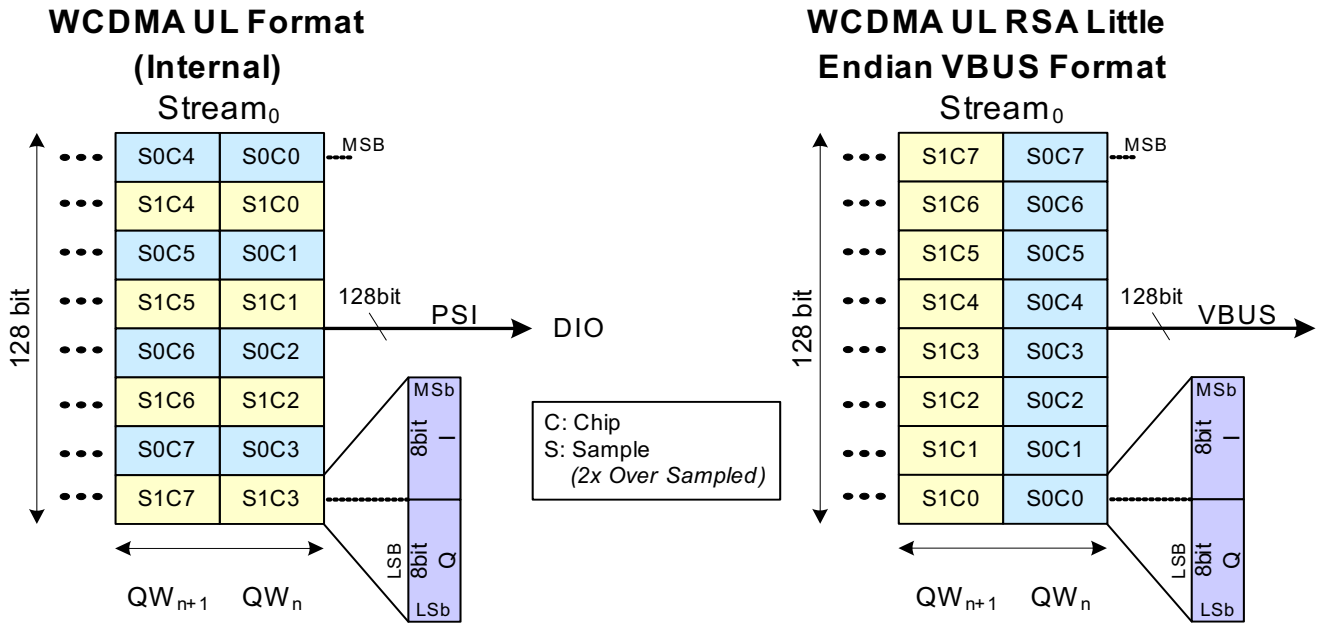


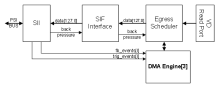
Figure 7-54. RSA UL Data Format Conversion (Little Endian)



7.7.4 Downlink (Egress)

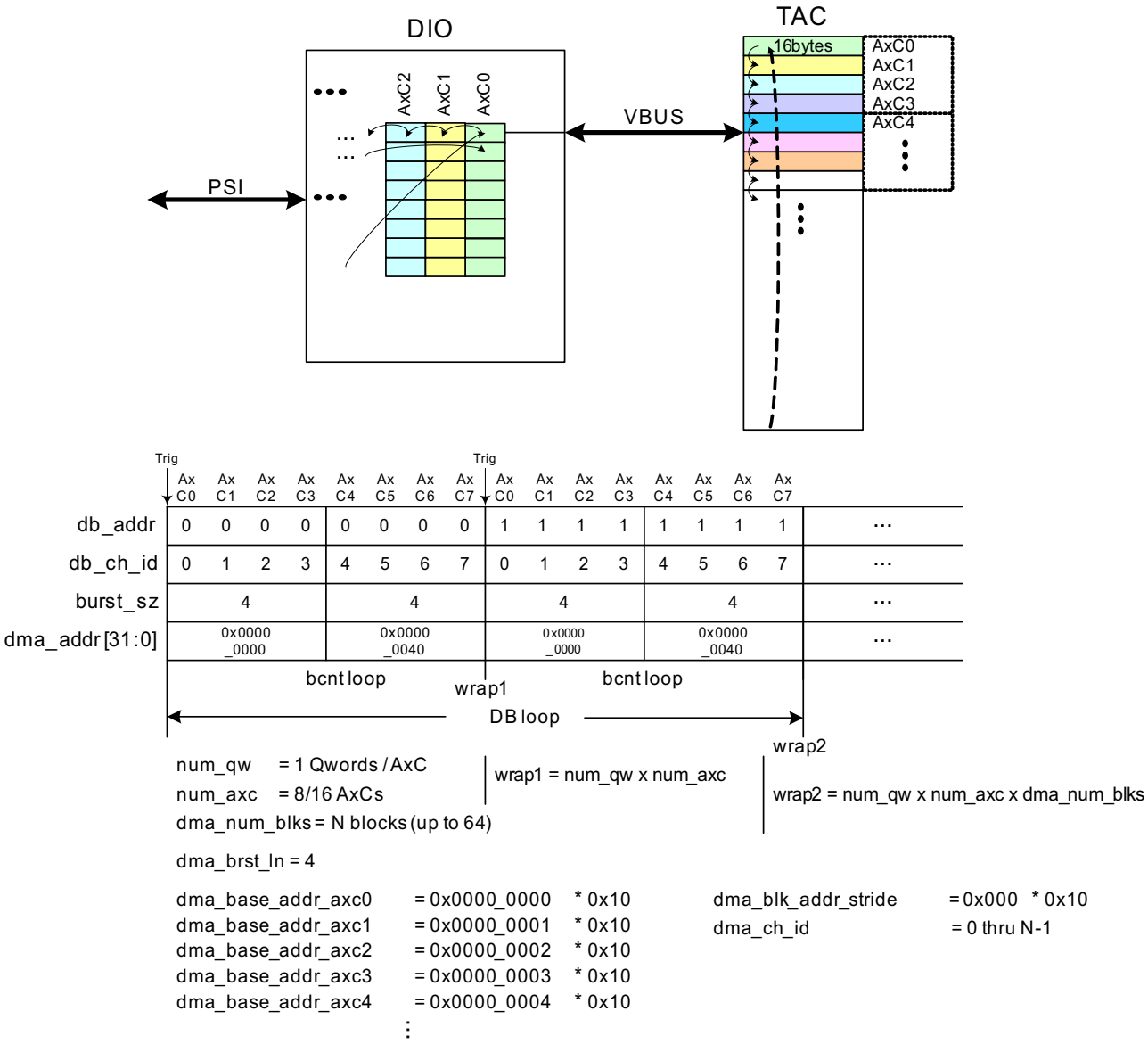
The Egress DIO provides multiple DMA engines to control the transfer of data from each of multiple source like TAC, L2, MSMC or DDR3 to DIO SI FIFO. Precise timing of DMA transfers occurs based on uAT DIO RAD events.

Figure 7-55. DIO Egress Block Diagram



7.7.4.1 TAC Example

Figure 7-56. TAC Example



For L2/MSMC/DDR3 example, see examples in Uplink chapter.

7.7.4.2 Egress Scheduler

The Egress Scheduler receives a request from one of its DMA engines for a block transfer. After giving the DMA engine a grant, the scheduler writes the starting VBUS address to the VBUSM interface's read block and the DMA engine proceeds to the next phase, i.e., next block transfer.

The SI is the interface to the IQS (switch) via the PSI bus from the DIO core. It provides FIFO buffering, framing, exception handling and the interface to the PSI bus. When its FIFO becomes partly full, it will put back pressure on the Egress Scheduler. The scheduler will, in turn, halt all data in the pipeline and stop requesting data from the VD (VBUSM Data Interface).

The SI Interface (SIF) contains the egress RSA Data Format Converter and the AxC Offset Generator (AOG).

The AxC offset generator delays the start of frame (SOF) to the SI, on a per-channel basis and by a programmable value of whole number of quad words (four samples). The AxC offset from Frame Boundary is in 4-sample (1 QW) increments. For Example, a value of 0 would cause zero offset from frame boundary. A value of 1 would cause a 4-sample offset from frame boundary.The maximum delay supported is 2^{17} = 131,072 quad words (524,288 samples).

Downlink RSA data format converter for big and little endian is shown in the following figures. The **DMA_CFG0[3].RSA_CNVRT_EN** field enables or disables the format conversion logic and little, big endian option can be selected from **GLOBAL_CFG.RSA_BIG_ENDIAN** MMR instead of using byte swap option in DIO SI.

Figure 7-57. RSA DL Data Format Conversion (Big Endian)

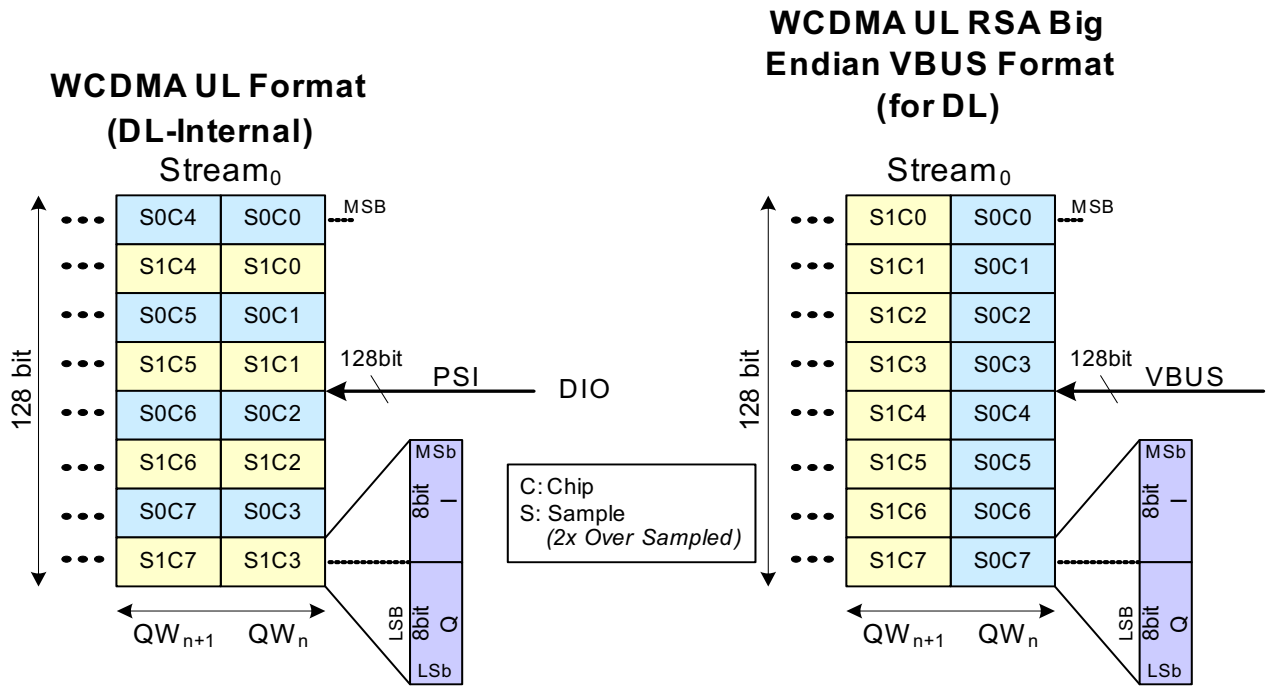
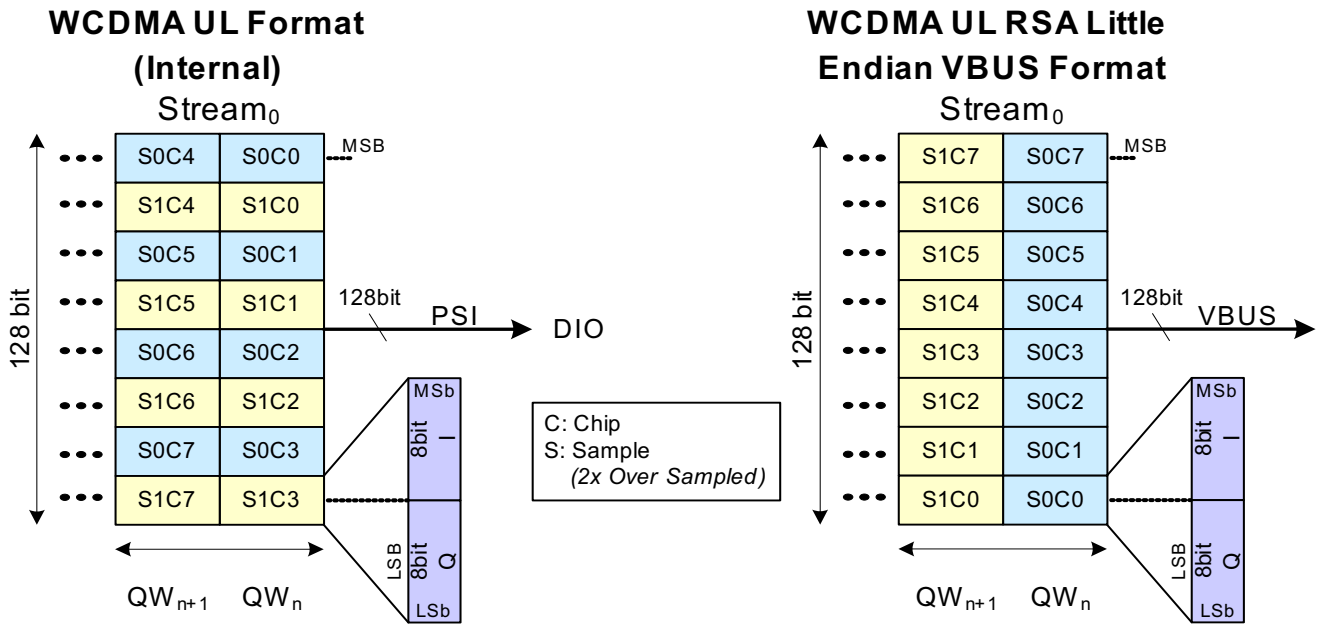


Figure 7-58. RSA DL Data Format Conversion (Little Endian)



7.7.5 Data Trace

The Data Trace feature allows data from the AIL RM, via an external multiplexer, to be stored in either L2, MSMC, or DDR3 for analysis. This is a debug feature for the AIL only and cannot be used for the DFE/AID.

A link in the AIL is selected via the external multiplexer for its raw or framed data to be sent to the DIO Data Trace. Data Trace data is in the VBUS clock domain. **VC_DTMUX_CFG.DT_LINK_SEL[2]** MMR is used to select from which AIL data trace is to use.

The bullets below describe the Data Trace functional operation:

- Normal Operation: **dt_global_en_set -> dt_en -> dt_start_stb**

  (a) Raw Start / Continuous Capture:
  - DMA data starting on **dt_start_stb**
  - Stop data DMA when **dt_en** = 0 AND end of circular buffer is reached

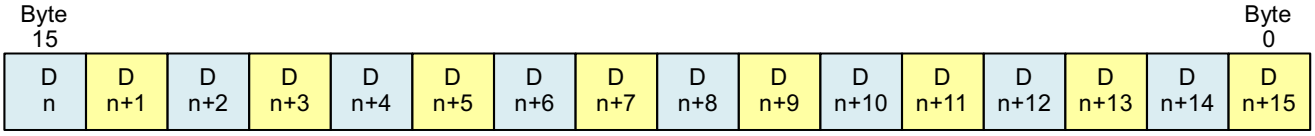
  (b) Raw Start / One Shot Capture:
  - DMA data starting on **dt_start_stb**
  - Stop data DMA when end of circular buffer is reached

  (c) Sync to SOF Start / Continuous Capture:
  - DMA data starting after **dt_start_stb** then from SOF
  - Stop data DMA when **dt_en** = 0 AND end of circular buffer is reached

  (d) Sync to SOF Start / One Shot Capture:
  - DMA data starting after **dt_start_stb** then from SOF
  - Stop data DMA when end of circular buffer is reached

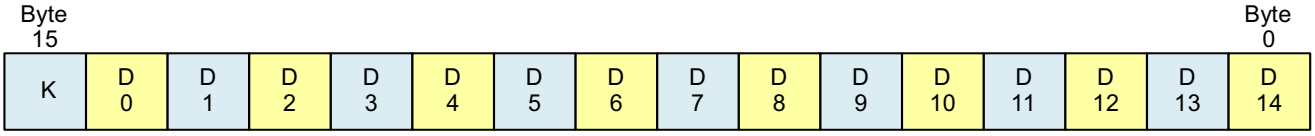
Data is packed into 16-byte Quad Words for storage into the DT Buffer. In continuous, raw mode (**dio_dt_cfg0.dt_start_mode** = 0), two transfers of 8-byte data are packed in big endian format (**dio_dt_cfg0.dt_endian_sel** = 0) as shown in Figure 7-59. Byte 15 is first in time.

Figure 7-59. Raw Data Quad Word Format - Big Endian



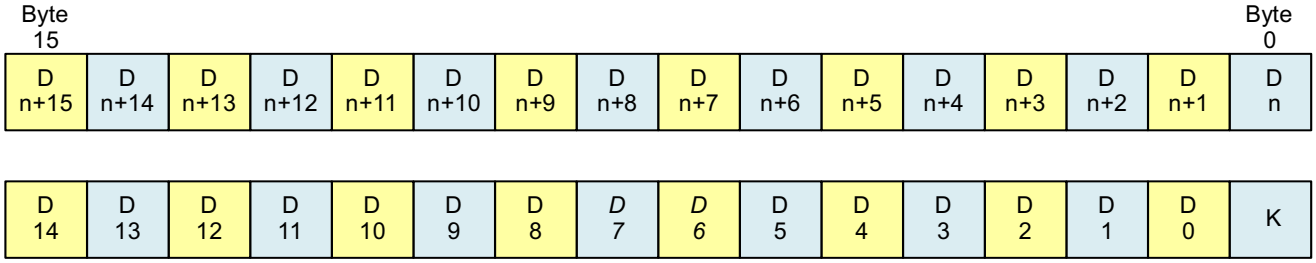
In Sync-to-SOF mode (**dio_dt_cfg0.dt_start_mode** = 1), data is packed into 16-byte Quad Words, in big endian format (**dio_dt_cfg0.dt_endian_sel** = 0), starting with the K-character that is coincident with SOF as shown in Figure 7-60. Byte 15 is first in time.

Figure 7-60. Frame Synced Quad Word Format - Big Endian



Data may also be stored in little endian format (**dio_dt_cfg0.dt_endian_sel** = 1) as shown in Figure 7-61.

Figure 7-61. Quad Word Format - Little Endian



The Data Trace DMA engine receives requests for transfers from the DT Buffer read/write logic for as many as four quad word bursts of data that are in the DT Buffer. Trace data received will be transferred to L2, MSMC, or DDR3 starting at **dio_dt_cfg1.dt_dma_base_address** and up to **dio_dt_cfg2.dt_dma_wrap** * 0x40 - 1 where data will begin overwriting old data starting at **dio_dt_cfg1.dt_dma_base_address** again.

For **dt_dma_base_address,** only quad-word (128 bit) granularity is supported. Non-quad-word aligned base addresses are NOT supported.

Registers

The beginning of this chapter should include a brief description of the peripheral registers and a table listing each of the registers with a pointer to the information for each one.

Topic **Page**

8.1 Address Map

Table 8-1. Memory Map of IQN2 Register Region Addresses

Module	Sub-module	IP Level Address	Sub-Module Level Address	Section
Top				Section 8.2
	VC	0x00_0000	0x00_0000	
	EE	0x00_4000	0x00_4000	
	PSR	0x00_8000	0x00_8000	
IQS		0x02_0000	0x02_0000	Section 8.3
AT				Section 8.4
	AT	0x01_0000	0x00_0000	
	AT EE	0x01_8000	0x00_8000	
AID				Section 8.5
	SI sysclk	0x04_0000	0x00_0000	
	SI vbusclk	0x04_8000	0x00_8000	
	EE sysclk	0x05_0000	0x01_0000	
	EE DFE	0x05_1000	0x01_1000	
	EE vbusclk	0x05_2000	0x01_2000	
DIO				Section 8.7
	SI sysclk	0x06_0000	0x00_0000	
	SI vbusclk	0x06_8000	0x00_8000	
	DIO Core	0x07_0000	0x01_0000	
	DIO EE	0x07_8000	0x01_8000	
AIL_0				Section 8.6
	SI sysclk	0x20_0000	0x00_0000	
	SI vbusclk	0x20_8000	0x00_8000	
	PE	0x22_0000	0x02_0000	
	PD	0x22_8000	0x02_8000	
	PHY	0x23_0000	0x03_0000	
	EE vbusclk	0x23_2000	0x03_2000	
	EE sysclk	0x23_4000	0x03_4000	
AIL_1				Section 8.6
	SI sysclk	0x24_0000	0x00_0000	
	SI vbusclk	0x24_8000	0x00_8000	
	PE	0x26_0000	0x02_0000	
	PD	0x26_8000	0x02_8000	
	PHY	0x27_0000	0x03_0000	
	EE vbusclk	0x27_2000	0x03_2000	
	EE sysclk	0x27_4000	0x03_4000	

8.2 TOP Registers

Table 8-2. TOP Register Groups

Offset	Acronym	Description	Section
0x0000	vc_sys_sts_cfg	VC System Status and Control registers	Section 8.2.1
0x0020	vc_cdma_status	VC PKTDMA Status registers	Section 8.2.2
0x0080	vc_subchip_pid_sts	VC subchip PID Status registers	Section 8.2.3
0x0100	vc_sd_lk	VC SERDES link status registers	Section 8.2.4
0x4000	IQN2 Top level EE registers	IQN2 Top level EE registers	Section 8.2.5
0x8000	PSR_CONFIG_REGS	PSR Configuration MMRs	Section 8.2.6
0x8800	PSR_EE	IQN_PSR_EE EE register group	Section 8.2.7
0x8C00	PKTDMA_EE	IQN_PSR_PKTDMA_EE EE register group	Section 8.2.8

8.2.1 vc_sys_sts_cfg [Address = 0x0000]

Table 8-3. vc_sys_sts_cfg

Offset	Acronym	Register Description	Section
0x0000	IQN2 PERIPERAL ID REGISTER	IQN2 Periperal ID Register	Section 8.2.1.1
0x0004	IQN2 SCRATCH REGISTER	VC Scratch Register	Section 8.2.1.2
0x0008	IQN2 SW RESET REGISTER	VC Software Reset Register	Section 8.2.1.3
0x000C	IQN2 EMULATION CONTROL REGISTER	IQN2 Emulation Control Register	Section 8.2.1.4
0x0014	IQN2 DATA TRACE MUX SELECT REGISTER	Iqn2 data trace mux select Register	Section 8.2.1.5
0x0018	SD SYSTEM CLOCK CONTROL REGISTER	VC clkctl system clock control Register	Section 8.2.1.6

8.2.1.1 IQN2 PERIPERAL ID REGISTER [Address = 0x0000]

IQN2 Peripheral ID Register

Figure 8-1. IQN2 PERIPERAL ID REGISTER

31 30	29 28	27 16	15 11	10 8	7 6	5 0
SCHEME	Reserved	FUNC	RTL	MAJOR	CUSTOM	MINOR
R-0x0001	NA-0	R-0x0841	R-0x000A	R-0x0001	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-4. IQN2 PERIPERAL ID REGISTER Field Descriptions

Bits	Name	Description
31-30	SCHEME	Current scheme
29-28	Reserved	RESERVED
27-16	FUNC	Function code assigned to IQN2
15-11	RTL	RTL Version R code
10-8	MAJOR	Major revision X code
7-6	CUSTOM	Custom version code
5-0	MINOR	Minor revision Y code

8.2.1.2 IQN2 SCRATCH REGISTER [Address = 0x0004]

VC Scratch Register

Figure 8-2. IQN2 SCRATCH REGISTER

31	0
SCRATCH	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-5. IQN2 SCRATCH REGISTER Field Descriptions

Bits	Name	Description
31-0	SCRATCH	This is the VC Scratch Field used for debug testing basic read and write to mmrs.

8.2.1.3 IQN2 SW RESET REGISTER [Address = 0x0008]

VC Software Reset Register

Figure 8-3. IQN2 SW RESET REGISTER

31	8	7	6	5
Reserved		SW_RESET_AIL3	SW_RESET_AIL2	SW_RESET_AIL1
NA-0		W-0	W-0	W-0

4	3	2	1	0
SW_RESET_AIL0	SW_RESET_PKTDMA	SW_RESET_DIO	SW_RESET_AID	SW_RESET
W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-6. IQN2 SW RESET REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7	SW_RESET_AIL3	AIL3 are software resets which reset various sections of IQN2. (AIL3 not populated)
6	SW_RESET_AIL2	AIL2 are software resets which reset various sections of IQN2. (AIL2 not populated)
5	SW_RESET_AIL1	AIL1 software resets which reset various sections of IQN2.
4	SW_RESET_AIL0	AIL0 software resets which reset various sections of IQN2.
3	SW_RESET_PKTDMA	PktDMA software resets which reset various sections of IQN2.
2	SW_RESET_DIO	DIO software resets which reset various sections of IQN2.
1	SW_RESET_AID	AID software resets which reset various sections of IQN2.
0	SW_RESET	Global IQN2 Reset. Preferably use LPSC to reset IQN2

8.2.1.4 IQN2 EMULATION CONTROL REGISTER [Address = 0x000C]

IQN2 Emulation Control Register

Figure 8-4. IQN2 EMULATION CONTROL REGISTER

31	10	9	8
RSVD_10		SHUTDOWN_STATUS	SHUTDOWN_ON
NA-0		R-0	R-0

7	4	3	2	1	0
RSVD_4		FRC_SHUTDOWN	RT_SEL	SOFT	FREERUN
NA-0		R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-7. IQN2 EMULATION CONTROL REGISTER Field Descriptions

Bits	Name	Description
31-10	RSVD_10	RESERVED
9	SHUTDOWN_STATUS	Indicates the shutdown controller has finished shutting down and is holding the IQN2 in shutdown when set.
8	SHUTDOWN_ON	Indicates the shutdown controller is processing a shutdown.
7-4	RSVD_4	RESERVED
3	FRC_SHUTDOWN	Forces the shutdown controller to shut down the entire IQN cleanly. • RUN (0) = IQN2 allowed to run. • SHUTDOWN (1) = IQN2 shuts down.
2	RT_SEL	RT_SEL bit • emu_dbgsusp (0) = IQN2 emulation mode is controlled only by the aif2_emu_dbgsusp CBA signal. The aif2_emu_dbgsusp_rt signal is ignored. • emu_dbgsusp_rt (1) = IQN2 emulation mode is controlled only by the aif2_emu_dbgsusp_rt CBA signal. The aif2_emu_dbgsusp signal is ignored.
1	SOFT	SOFT bit. This bit is ignored by the IQN2. IQN2 always performs a graceful SOFT stop • HARD_STOP (0) = Value ignored by IQN2 • SOFT_STOP (1) = Value ignored by IQN2
0	FREERUN	FREERUN bit • RESPOND (0) = IQN2 responds to the emulation suspend signal • IGNORE (1) = IQN2 ignores emulation suspend signals and runs to completion

8.2.1.5 IQN2 DATA TRACE MUX SELECT REGISTER [Address = 0x0014]

Iqn2 data trace mux select Register

Figure 8-5. IQN2 DATA TRACE MUX SELECT REGISTER

31	2	1	0
Reserved		VC_DTMUX	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-8. IQN2 DATA TRACE MUX SELECT REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	RESERVED
1-0	VC_DTMUX	Iqn2 data trace mux select Register selects which ail data trace to use • AIL0 (0) = ail0 is selected • AIL1 (1) = ail1 is selected

8.2.1.6 SD SYSTEM CLOCK CONTROL REGISTER [Address = 0x0018]

VC clkctl system clock control Register

Figure 8-6. SD SYSTEM CLOCK CONTROL REGISTER

31	4	3	2	0
Reserved		AT_DFE_CLK_SEL	SYSCLK_SEL	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-9. SD SYSTEM CLOCK CONTROL REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3	AT_DFE_CLK_SEL	Selects dfe_pll_clk for the AT and uAT clock if = 1. The selected sysclk derived from the SERDES txbclk is used when = 0. This should only be set when using DFE and not used for AIL
2-0	SYSCLK_SEL	SD system clock control Register selects which SERDES txbclk to use for sys_clk. bits 0 and 1 select which serdes lane to use. bit 2 selects 1/2 the txbclk speed when set (always set CPRI 16x). 0x0: Full byte clock rate lane0 0x1: Full byte clock rate lane1 0x4: Half byte clock rate lane0 0x5: Half byte clock rate lane1 (others codes unused) • AIL0 (0) = ail0 SD txbclk used • AIL1 (1) = ail0 SD txbclk used • AIL0_CPRI16x (4) = ail0 SD txbclk/2 used for CPRI 16x • AIL1_CPRI16x (5) = ail1 SD txbclk/2 used for CPRI 16x

8.2.2 vc_cdma_status [Address = 0x0020]

Table 8-10. vc_cdma_status

Offset	Acronym	Register Description	Section
0x0020	PKTDMA TX TAKEDOWN STATUS LSB REGISTER	PKTDMA TX takedown status lsb Register	Section 8.2.2.1
0x0024	PKTDMA TX TAKEDOWN STATUS MSB REGISTER	PKTDMA TX takedown status msb Register	Section 8.2.2.2
0x0028	PKTDMA TX ENABLE STATUS LSB REGISTER	PKTDMA TX enable status lsb Register	Section 8.2.2.3
0x002C	PKTDMA TX ENABLE STATUS MSB REGISTER	PKTDMA TX enable status msb Register	Section 8.2.2.4
0x0030	PKTDMA TX PACKET STATUS LSB REGISTER	PKTDMA TX packet status lsb Register	Section 8.2.2.5
0x0034	PKTDMA TX PACKET STATUS MSB REGISTER	PKTDMA TX packet status msb Register	Section 8.2.2.6
0x0038	PKTDMA RX TAKEDOWN STATUS LSB REGISTER	PKTDMA RX takedown status lsb Register	Section 8.2.2.7
0x003C	PKTDMA RX TAKEDOWN STATUS MSB REGISTER	PKTDMA RX takedown status msb Register	Section 8.2.2.8
0x0040	PKTDMA RX ENABLE STATUS LSB REGISTER	PKTDMA RX enable status lsb Register	Section 8.2.2.9
0x0044	PKTDMA RX ENABLE STATUS MSB REGISTER	PKTDMA RX enable status msb Register	Section 8.2.2.10
0x0048	PKTDMA RX PACKET STATUS LSB REGISTER	PKTDMA RX packet status lsb Register	Section 8.2.2.11
0x004C	PKTDMA RX PACKET STATUS MSB REGISTER	PKTDMA RX packet status msb Register	Section 8.2.2.12

8.2.2.1 PKTDMA TX TAKEDOWN STATUS LSB REGISTER [Address = 0x0020]

PKTDMA TX takedown status lsb Register

Figure 8-7. PKTDMA TX TAKEDOWN STATUS LSB REGISTER

31	0
TDOWN_STATUS_L	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-11. PKTDMA TX TAKEDOWN STATUS LSB REGISTER Field Descriptions

Bits	Name	Description
31-0	TDOWN_STATUS_L	PKTDMA TX takedown status lsb. each bit corresponds to each channel

8.2.2.2 PKTDMA TX TAKEDOWN STATUS MSB REGISTER [Address = 0x0024]

PKTDMA TX takedown status msb Register

Figure 8-8. PKTDMA TX TAKEDOWN STATUS MSB REGISTER

31 16	15 0
Reserved	TDOWN_STATUS_H
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-12. PKTDMA TX TAKEDOWN STATUS MSB REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	TDOWN_STATUS_H	PKTDMA TX takedown status msb. each bit corresponds to each channel

8.2.2.3 PKTDMA TX ENABLE STATUS LSB REGISTER [Address = 0x0028]

PKTDMA TX enable status lsb Register

Figure 8-9. PKTDMA TX ENABLE STATUS LSB REGISTER

31	0
ENABLE_STATUS_L	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-13. PKTDMA TX ENABLE STATUS LSB REGISTER Field Descriptions

Bits	Name	Description
31-0	ENABLE_STATUS_L	PKTDMA TX enable status lsb. each bit corresponds to each channel

8.2.2.4 PKTDMA TX ENABLE STATUS MSB REGISTER [Address = 0x002C]

PKTDMA TX enable status msb Register

Figure 8-10. PKTDMA TX ENABLE STATUS MSB REGISTER

31	16	15	0
Reserved		ENABLE_STATUS_H	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-14. PKTDMA TX ENABLE STATUS MSB REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	ENABLE_STATUS_H	PKTDMA TX enable status msb. each bit corresponds to each channel

8.2.2.5 PKTDMA TX PACKET STATUS LSB REGISTER [Address = 0x0030]

PKTDMA TX packet status lsb Register

Figure 8-11. PKTDMA TX PACKET STATUS LSB REGISTER

31	0
PKT_STATUS_L	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-15. PKTDMA TX PACKET STATUS LSB REGISTER Field Descriptions

Bits	Name	Description
31-0	PKT_STATUS_L	PKTDMA TX packet status lsb. each bit corresponds to each channel

8.2.2.6 PKTDMA TX PACKET STATUS MSB REGISTER [Address = 0x0034]

PKTDMA TX packet status msb Register

Figure 8-12. PKTDMA TX PACKET STATUS MSB REGISTER

31	16	15	0
Reserved		PKT_STATUS_H	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-16. PKTDMA TX PACKET STATUS MSB REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	PKT_STATUS_H	PKTDMA TX packet status msb. each bit corresponds to each channel

8.2.2.7 PKTDMA RX TAKEDOWN STATUS LSB REGISTER [Address = 0x0038]

PKTDMA RX takedown status lsb Register

Figure 8-13. PKTDMA RX TAKEDOWN STATUS LSB REGISTER

31	0
TDOWN_STATUS_L	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-17. PKTDMA RX TAKEDOWN STATUS LSB REGISTER Field Descriptions

Bits	Name	Description
31-0	TDOWN_STATUS_L	PKTDMA RX takedown status lsb. each bit corresponds to each channel

8.2.2.8 PKTDMA RX TAKEDOWN STATUS MSB REGISTER [Address = 0x003C]

PKTDMA RX takedown status msb Register

Figure 8-14. PKTDMA RX TAKEDOWN STATUS MSB REGISTER

31 16	15 0
Reserved	TDOWN_STATUS_H
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-18. PKTDMA RX TAKEDOWN STATUS MSB REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	TDOWN_STATUS_H	PKTDMA RX takedown status msb. each bit corresponds to each channel

8.2.2.9 PKTDMA RX ENABLE STATUS LSB REGISTER [Address = 0x0040]

PKTDMA RX enable status lsb Register

Figure 8-15. PKTDMA RX ENABLE STATUS LSB REGISTER

31	0
ENABLE_STATUS_L	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-19. PKTDMA RX ENABLE STATUS LSB REGISTER Field Descriptions

Bits	Name	Description
31-0	ENABLE_STATUS_L	PKTDMA RX enable status lsb. each bit corresponds to each channel

8.2.2.10 PKTDMA RX ENABLE STATUS MSB REGISTER [Address = 0x0044]

PKTDMA RX enable status msb Register

Figure 8-16. PKTDMA RX ENABLE STATUS MSB REGISTER

31	16	15	0
Reserved		ENABLE_STATUS_H	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-20. PKTDMA RX ENABLE STATUS MSB REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	ENABLE_STATUS_H	PKTDMA RX enable status msb. each bit corresponds to each channel

8.2.2.11 PKTDMA RX PACKET STATUS LSB REGISTER [Address = 0x0048]

PKTDMA RX packet status lsb Register

Figure 8-17. PKTDMA RX PACKET STATUS LSB REGISTER

31	0
PKT_STATUS_L	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-21. PKTDMA RX PACKET STATUS LSB REGISTER Field Descriptions

Bits	Name	Description
31-0	PKT_STATUS_L	PKTDMA RX packet status lsb. each bit corresponds to each channel

8.2.2.12 PKTDMA RX PACKET STATUS MSB REGISTER [Address = 0x004C]

PKTDMA RX packet status msb Register

Figure 8-18. PKTDMA RX PACKET STATUS MSB REGISTER

31	16	15	0
Reserved		PKT_STATUS_H	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-22. PKTDMA RX PACKET STATUS MSB REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	PKT_STATUS_H	PKTDMA RX packet status msb. each bit corresponds to each channel

8.2.3 vc_subchip_pid_sts [Address = 0x0080]

Table 8-23. vc_subchip_pid_sts

Offset	Acronym	Register Description	Section
0x0080	IQN2SC_CLKCTL PERIPERAL ID REGISTER	iqn2 clock control subchip Periperal ID Register	Section 8.2.3.1
0x0084	IQN2SC_AIL PERIPERAL ID REGISTER	iqn2 ail subchip Periperal ID Register	Section 8.2.3.2

8.2.3.1 IQN2SC_CLKCTL PERIPERAL ID REGISTER [Address = 0x0080]

iqn2 clock control subchip Periperal ID Register

Figure 8-19. IQN2SC_CLKCTL PERIPERAL ID REGISTER

31 16	15 11	10 8	7 6	5 0
Reserved	RTL	MAJOR	CUSTOM	MINOR
NA-0	R-0x0001	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-24. IQN2SC_CLKCTL PERIPERAL ID REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-11	RTL	RTL Version R code
10-8	MAJOR	Major revision X code
7-6	CUSTOM	Custom version code
5-0	MINOR	Minor revision Y code

8.2.3.2 IQN2SC_AIL PERIPERAL ID REGISTER [Address = 0x0084]

iqn2 ail subchip Periperal ID Register

Figure 8-20. IQN2SC_AIL PERIPERAL ID REGISTER

31 16	15 11	10 8	7 6	5 0
Reserved	RTL	MAJOR	CUSTOM	MINOR
NA-0	R-0x0009	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-25. IQN2SC_AIL PERIPERAL ID REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-11	RTL	RTL Version R code
10-8	MAJOR	Major revision X code
7-6	CUSTOM	Custom version code
5-0	MINOR	Minor revision Y code

8.2.4 vc_sd_lk [Address = 0x0100 + (R × 0x0010)]

Table 8-26. vc_sd_lk

Offset	Acronym	Register Description	Section
0x0100 + (*R* × 0x0010)	SERDES TRANSMIT STATUS REGISTER	SERDES transmit status Register	Section 8.2.4.1
0x010C + (*R* × 0x0010)	SERDES RECEIVE STATUS REGISTER	(TI Diag Use Only) SERDES receive status Register. User should read SERDES registers directly	Section 8.2.4.2

8.2.4.1 SERDES TRANSMIT STATUS REGISTER [Address = 0x0100 + (*R* × 0x0010)]

Range (*R*) = 0:3

SERDES transmit status Register

Figure 8-21. SERDES TRANSMIT STATUS REGISTER

31	1	0
Reserved		LN_OK
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-27. SERDES TRANSMIT STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	LN_OK	(TI Use Only) link clocks are stable. OK to send and receive data. (PLL is locked). User can check SERDES register directly

8.2.4.2 SERDES RECEIVE STATUS REGISTER [Address = 0x010C + (*R* × 0x0010)]

Range (*R*) = 0:3

(TI Diag Use Only) SERDES receive status Register. User should read SERDES registers directly

Figure 8-22. SERDES RECEIVE STATUS REGISTER

31	2	1	0
Reserved		LOSDTCT	COMMA_DET
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-28. SERDES RECEIVE STATUS REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	LOSDTCT	(TI Use Only) The receiver frame synchronizer must have knowledge that each Ser-des port had detected a loss of signal condition so that the receiver can suppress events due to a loss of frame synchronization.
0	COMMA_DET	(TI Use Only) The receiver frame synchronizer must have knowledge that each Ser-des port had completed a requested byte alignment so that the byte alignment control logic can operate.

8.2.5 IQN2 Top level EE registers [Address = 0x4000]

Table 8-29. IQN2 Top level EE registers

Offset	Acronym	Register Description	Section
0x4000	EE EV0 ORGN RAW STATUS REGISTER	EE EV0 Origination Status Register	Section 8.2.5.1
0x4004	EE EV1 ORGN RAW STATUS REGISTER	EE EV1 Origination Status Register	Section 8.2.5.2
0x4010	EE EOI EV 0 REGISTER	EOI EV 0 Register	Section 8.2.5.3
0x4014	EE EOI EV 1 REGISTER	EOI EV 1 Register	Section 8.2.5.4
0x4018	EE EOI CPPI REGISTER	EOI EV Multicore Navigator Register	Section 8.2.5.5

8.2.5.1 EE EV0 ORGN RAW STATUS REGISTER [Address = 0x4000]

EE EV0 Origination Status Register

Figure 8-23. EE EV0 ORGN RAW STATUS REGISTER

31	10	9	8	7	6
Reserved		PSR_EE_STS	AIL3_EE_EV1	AIL2_EE_EV1	AIL1_EE_STS
NA-0		R-0	R-0	R-0	R-0

5	4	3	2	1	0
AIL0_EE_STS	IQS_EE_STS	DIO_EE_STS	DFE_EE_STS	AID_EE_STS	AT_EE_STS
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-30. EE EV0 ORGN RAW STATUS REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	Reserved.
9	PSR_EE_STS	PSR origination status.
8	AIL3_EE_EV1	AIL 3 origination status.
7	AIL2_EE_EV1	AIL 2 origination status.
6	AIL1_EE_STS	AIL 1 origination status.
5	AIL0_EE_STS	AIL 0 origination status.
4	IQS_EE_STS	IQS origination status.
3	DIO_EE_STS	DIO origination status.
2	DFE_EE_STS	DFE origination status.
1	AID_EE_STS	AID origination status.
0	AT_EE_STS	AT origination status.

8.2.5.2 EE EV1 ORGN RAW STATUS REGISTER [Address = 0x4004]

EE EV1 Origination Status Register

Figure 8-24. EE EV1 ORGN RAW STATUS REGISTER

31	10	9	8	7	6
Reserved		PSR_EE_STS	AIL3_EE_STS	AIL2_EE_STS	AIL1_EE_STS
NA-0		R-0	R-0	R-0	R-0

5	4	3	2	1	0
AIL0_EE_STS	IQS_EE_STS	DIO_EE_STS	DFE_EE_STS	AID_EE_STS	AT_EE_STS
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-31. EE EV1 ORGN RAW STATUS REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	Reserved.
9	PSR_EE_STS	PSR origination status.
8	AIL3_EE_STS	AIL 3 origination status.
7	AIL2_EE_STS	AIL 2 origination status.
6	AIL1_EE_STS	AIL 1 origination status.
5	AIL0_EE_STS	AIL 0 origination status.
4	IQS_EE_STS	IQS origination status.
3	DIO_EE_STS	DIO origination status.
2	DFE_EE_STS	DFE origination status.
1	AID_EE_STS	AID origination status.
0	AT_EE_STS	AT origination status.

8.2.5.3 EE EOI EV 0 REGISTER [Address = 0x4010]

EOI EV 0 Register

Figure 8-25. EE EOI EV 0 REGISTER

31	8	7	0
Reserved		EOI_0_VECTOR_REG	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-32. EE EOI EV 0 REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	EOI_0_VECTOR_REG	End Of Interrupt vector register for EV 0

8.2.5.4 EE EOI EV 1 REGISTER [Address = 0x4014]

EOI EV 1 Register

Figure 8-26. EE EOI EV 1 REGISTER

31	8	7	0
Reserved		EOI_1_VECTOR_REG	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-33. EE EOI EV 1 REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	EOI_1_VECTOR_REG	End Of Interrupt vector register for EV 1

8.2.5.5 EE EOI CPPI REGISTER [Address = 0x4018]

EOI EV Multicore Navigator Register

Figure 8-27. EE EOI CPPI REGISTER

31	8	7	0
Reserved		EOI_CPPI_VECTOR_REG	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-34. EE EOI CPPI REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	EOI_CPPI_VECTOR_REG	End Of Interrupt vector register for Multicore Navigator

8.2.6 PSR_CONFIG_REGS [Address = 0x8000]

Table 8-35. PSR_CONFIG_REGS

Offset	Acronym	Register Description	Section
0x8000	PSR EGRESS BW_LIMIT CONFIGURATION REGISTER	Selects the setting of the amount of bandwidth limit for flushing packets	Section 8.2.6.1
0x8004	PSR INGRESS CONFIGURATION REGISTER	Controls extraction of PS_DATA from the ingress path	Section 8.2.6.2
0x8200	PSR INGRESS CHANNEL DROP OR FLUSH PACKET ON ERROR CONFIGURATION REGISTER	Selects if forces the channel into continuous flush and if it drops packets on error.	Section 8.2.6.3
0x8400	PSR EGRESS CHANNEL REGISTER	Enables packing PS data for the channel. Sets the arbitration priority for the channel.	Section 8.2.6.4

8.2.6.1 PSR EGRESS BW_LIMIT CONFIGURATION REGISTER [Address = 0x8000]

Selects the setting of the amount of bandwidth limit for flushing packets

Figure 8-28. PSR EGRESS BW_LIMIT CONFIGURATION REGISTER

31	12	11	8	7	0
Reserved		BW_LIMIT		Reserved	
NA-0		R/W-0		NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-36. PSR EGRESS BW_LIMIT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-8	BW_LIMIT	Percent bandwidth limit setting for flushing a packet from a channel in the PKTDMA. 0 is 1/16 of VBUS bandwidth. Should be set to the maximum VBUS bandwidth expected to be used in normal operation rounded up to the next faster bandwidth setting. For example if the maximum VBUS bandwidth used by all channels is 11/16 of the maximum available, the value should be set to a 4 to use 5/16 of the bandwidth during flush.
7-0	Reserved	RESERVED

8.2.6.2 PSR INGRESS CONFIGURATION REGISTER [Address = 0x8004]

Controls extraction of PS_DATA from the ingress path

Figure 8-29. PSR INGRESS CONFIGURATION REGISTER

31	1	0
Reserved		PS_DATA_EXT
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-37. PSR INGRESS CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	PS_DATA_EXT	Selects if the SI generates a PS_DATA with the incomming data • enable (0) = PSR Expansion is controlled by SI. Typically AxC channels result in chan_num and sym_index written as PS_DATA and there is no PS_DATA transfer for control channels.(Currently always leave at 0.) • disable (1) = PSR Expansion is disabled, AxC chan_num and sym_index are not written to PS_DATA. This mode will use less BW on PktDMA engine bus. (For TI future use)

8.2.6.3 PSR INGRESS CHANNEL DROP OR FLUSH PACKET ON ERROR CONFIGURATION REGISTER [Address = 0x8200 + (*S* × 0x0004)]

Size (*S*) = 0:47

Selects if forces the channel into continuous flush and if it drops packets on error.

Figure 8-30. PSR INGRESS CHANNEL DROP OR FLUSH PACKET ON ERROR CONFIGURATION REGISTER

31	3	2	1	0
Reserved		FORCE_FLUSH	DROP_PKT	Reserved
NA-0		R/W-0	R/W-0	NA-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-38. PSR INGRESS CHANNEL DROP OR FLUSH PACKET ON ERROR CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	RESERVED
2	FORCE_FLUSH	(For TI use only) set to 0. Forces the channel into continuous FLUSH. FLUSH operation will EOP any mid-flight packet and discard all new traffic for a given channel. Only known use case of this field is to support partial resets of i.e. individual links (advanced operation which is not officially supported) • no_flush (0) = Does not flush, packets transfer normally (Always set to 0) • flush (1) = Force a flush of the channel.
1	DROP_PKT	Normally set to 1. Drops the corrupted packet when FLUSH during mid packet. FLUSH likely caused by PktDMA buffer overflow for a given channel. (FLUSH also caused by force_flush) • keep (0) = Keeps packet for SW to examine on errors. • drop (1) = Tells the PKTDMA to drop the packet and release all its buffers for the packet. (Normally set to 1 for all channels unless doing debug)
0	Reserved	RESERVED

8.2.6.4 PSR EGRESS CHANNEL REGISTER [Address = 0x8400 + (*S* × 0x0004)]

Size (*S*) = 0:47

Enables packing PS data for the channel. Sets the arbitration priority for the channel.

Figure 8-31. PSR EGRESS CHANNEL REGISTER

31	11	10	8	7	1	0
Reserved		ARB_PRIORITY		Reserved		PACK_PS_DATA
NA-0		R/W-0		NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-39. PSR EGRESS CHANNEL REGISTER Field Descriptions

Bits	Name	Description
31-11	Reserved	RESERVED
10-8	ARB_PRIORITY	Arbitration priority for the channel on the PKTDMA PSI bus. 0 is highest priority.
7-1	Reserved	RESERVED
0	PACK_PS_DATA	Packs the PS_DATA for IQ channels when set. When not set, PS_DATA will be passed for special purposes • do_not_pack (0) = Does not pack PS_DATA. Normally used on CTL channels or OBSAI channels needing more than 16 bits of PS_DATA. • pack (1) = Pack PS_DATA. Normally used on IQ channels

8.2.7 PSR_EE [Address = 0x8800]

Table 8-40. PSR_EE

Offset	Acronym	Register Description	Section
0x8800	ING_FLUSH_A RAW INTERRUPT STATUS	Ingress flush errors for register ing_flush_a with channels 0 through 31.	Section 8.2.7.1
0x8804	ING_FLUSH_A RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.2.7.2
0x8808	ING_FLUSH_A RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.2.7.3
0x880C	ING_FLUSH_A EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.4
0x8810	ING_FLUSH_A EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.5
0x8814	ING_FLUSH_A EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.6
0x8818	ING_FLUSH_A EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.7
0x881C	ING_FLUSH_A EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.8
0x8820	ING_FLUSH_A EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.9
0x8824	ING_FLUSH_A EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.10
0x8828	ING_FLUSH_A EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.11
0x882C	ING_FLUSH_B RAW INTERRUPT STATUS	Ingress flush errors for reguster ing_flush_b with channels 32 through 47.	Section 8.2.7.12
0x8830	ING_FLUSH_B RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.2.7.13
0x8834	ING_FLUSH_B RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.2.7.14
0x8838	ING_FLUSH_B EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.15
0x883C	ING_FLUSH_B EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.16
0x8840	ING_FLUSH_B EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.17
0x8844	ING_FLUSH_B EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.18
0x8848	ING_FLUSH_B EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.19
0x884C	ING_FLUSH_B EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.20
0x8850	ING_FLUSH_B EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.21
0x8854	ING_FLUSH_B EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.22
0x88B0	EGR_PROTOCOL_ERR_A RAW INTERRUPT STATUS	Egress protocol errors for register egr_protocol_err_a with channels 0 through 31.	Section 8.2.7.23
0x88B4	EGR_PROTOCOL_ERR_A RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.2.7.24
0x88B8	EGR_PROTOCOL_ERR_A RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.2.7.25

Table 8-40. PSR_EE (continued)

Offset	Acronym	Register Description	Section
0x88BC	EGR_PROTOCOL_ERR_A EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.26
0x88C0	EGR_PROTOCOL_ERR_A EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.27
0x88C4	EGR_PROTOCOL_ERR_A EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.28
0x88C8	EGR_PROTOCOL_ERR_A EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.29
0x88CC	EGR_PROTOCOL_ERR_A EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.30
0x88D0	EGR_PROTOCOL_ERR_A EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.31
0x88D4	EGR_PROTOCOL_ERR_A EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.32
0x88D8	EGR_PROTOCOL_ERR_A EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.33
0x88DC	EGR_PROTOCOL_ERR_B RAW INTERRUPT STATUS	Egress protocol errors for register egr_protocol_err_b with channels 32 through 47.	Section 8.2.7.34
0x88E0	EGR_PROTOCOL_ERR_B RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.2.7.35
0x88E4	EGR_PROTOCOL_ERR_B RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.2.7.36
0x88E8	EGR_PROTOCOL_ERR_B EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.37
0x88EC	EGR_PROTOCOL_ERR_B EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.38
0x88F0	EGR_PROTOCOL_ERR_B EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.39
0x88F4	EGR_PROTOCOL_ERR_B EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.2.7.40
0x88F8	EGR_PROTOCOL_ERR_B EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.2.7.41
0x88FC	EGR_PROTOCOL_ERR_B EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.2.7.42
0x8900	EGR_PROTOCOL_ERR_B EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.43
0x8904	EGR_PROTOCOL_ERR_B EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.2.7.44
0x8960	PSR_ORIG_REG	This is the origination register indicating which PSR interrupt register group caused the interrupt.	Section 8.2.7.45

8.2.7.1 ING_FLUSH_A RAW INTERRUPT STATUS [Address = 0x8800]

Ingress flush errors for register ing_flush_a with channels 0 through 31.

Figure 8-32. ING_FLUSH_A RAW INTERRUPT STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-41. ING_FLUSH_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	Channel flush indication for ingress channels 0 through 31. An ingress flush error indicates a transfer to this PKTDMA channel was attempted when the channel was full which triggers a flush of the rest of the packet.

8.2.7.2 ING_FLUSH_A RAW SET [Address = 0x8804]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-33. ING_FLUSH_A RAW SET

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-42. ING_FLUSH_A RAW SET Field Descriptions

Bits	Name	Description
31-0	ERR	Sets the corresponding bit in the raw_status register when written with a 1.

8.2.7.3 ING_FLUSH_A RAW CLEAR [Address = 0x8808]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-34. ING_FLUSH_A RAW CLEAR

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-43. ING_FLUSH_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	ERR	Clears the corresponding bit in the raw_status register when written with a 1.

8.2.7.4 ING_FLUSH_A EV0 ENABLE STATUS [Address = 0x880C]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-35. ING_FLUSH_A EV0 ENABLE STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-44. ING_FLUSH_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.5 ING_FLUSH_A EV0 ENABLE SET [Address = 0x8810]

Allows software to force any bit in the correesponding enable register high.

Figure 8-36. ING_FLUSH_A EV0 ENABLE SET

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-45. ING_FLUSH_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.6 ING_FLUSH_A EV0 ENABLE CLEAR [Address = 0x8814]

Allows software to clear any bit in the correesponding enable register.

Figure 8-37. ING_FLUSH_A EV0 ENABLE CLEAR

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-46. ING_FLUSH_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.7 ING_FLUSH_A EV1 ENABLE STATUS [Address = 0x8818]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-38. ING_FLUSH_A EV1 ENABLE STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-47. ING_FLUSH_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.8 ING_FLUSH_A EV1 ENABLE SET [Address = 0x881C]

Allows software to force any bit in the correesponding enable register high.

Figure 8-39. ING_FLUSH_A EV1 ENABLE SET

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-48. ING_FLUSH_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.9 ING_FLUSH_A EV1 ENABLE CLEAR [Address = 0x8820]

Allows software to clear any bit in the correesponding enable register.

Figure 8-40. ING_FLUSH_A EV1 ENABLE CLEAR

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-49. ING_FLUSH_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.10 ING_FLUSH_A EV0 ENABLED STATUS [Address = 0x8824]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-41. ING_FLUSH_A EV0 ENABLED STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-50. ING_FLUSH_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.11 ING_FLUSH_A EV1 ENABLED STATUS [Address = 0x8828]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-42. ING_FLUSH_A EV1 ENABLED STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-51. ING_FLUSH_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.12 ING_FLUSH_B RAW INTERRUPT STATUS [Address = 0x882C]

Ingress flush errors for reguster ing_flush_b with channels 32 through 47.

Figure 8-43. ING_FLUSH_B RAW INTERRUPT STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-52. ING_FLUSH_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Channel flush indication for ingress channels 32 through 47. An ingress flush error indicates a transfer to this PKTDMA channel was attempted when the channel was full which triggers a flush of the rest of the packet.

8.2.7.13 ING_FLUSH_B RAW SET [Address = 0x8830]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-44. ING_FLUSH_B RAW SET

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-53. ING_FLUSH_B RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Sets the corresponding bit in the raw_status register when written with a 1.

8.2.7.14 ING_FLUSH_B RAW CLEAR [Address = 0x8834]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-45. ING_FLUSH_B RAW CLEAR

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-54. ING_FLUSH_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Clears the corresponding bit in the raw_status register when written with a 1.

8.2.7.15 ING_FLUSH_B EV0 ENABLE STATUS [Address = 0x8838]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-46. ING_FLUSH_B EV0 ENABLE STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-55. ING_FLUSH_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.16 ING_FLUSH_B EV0 ENABLE SET [Address = 0x883C]

Allows software to force any bit in the correesponding enable register high.

Figure 8-47. ING_FLUSH_B EV0 ENABLE SET

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-56. ING_FLUSH_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.17 ING_FLUSH_B EV0 ENABLE CLEAR [Address = 0x8840]

Allows software to clear any bit in the correesponding enable register.

Figure 8-48. ING_FLUSH_B EV0 ENABLE CLEAR

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-57. ING_FLUSH_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.18 ING_FLUSH_B EV1 ENABLE STATUS [Address = 0x8844]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-49. ING_FLUSH_B EV1 ENABLE STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-58. ING_FLUSH_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.19 ING_FLUSH_B EV1 ENABLE SET [Address = 0x8848]

Allows software to force any bit in the correesponding enable register high.

Figure 8-50. ING_FLUSH_B EV1 ENABLE SET

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-59. ING_FLUSH_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.20 ING_FLUSH_B EV1 ENABLE CLEAR [Address = 0x884C]

Allows software to clear any bit in the correesponding enable register.

Figure 8-51. ING_FLUSH_B EV1 ENABLE CLEAR

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-60. ING_FLUSH_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.21 ING_FLUSH_B EV0 ENABLED STATUS [Address = 0x8850]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-52. ING_FLUSH_B EV0 ENABLED STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-61. ING_FLUSH_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.22 ING_FLUSH_B EV1 ENABLED STATUS [Address = 0x8854]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-53. ING_FLUSH_B EV1 ENABLED STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-62. ING_FLUSH_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.23 EGR_PROTOCOL_ERR_A RAW INTERRUPT STATUS [Address = 0x88B0]

Egress protocol errors for register egr_protocol_err_a with channels 0 through 31.

Figure 8-54. EGR_PROTOCOL_ERR_A RAW INTERRUPT STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-63. EGR_PROTOCOL_ERR_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	Protocol error indication of an unsupported data type or a missing PS_DATA transfer when one was expected for egress channels 0 through 31

8.2.7.24 EGR_PROTOCOL_ERR_A RAW SET [Address = 0x88B4]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-55. EGR_PROTOCOL_ERR_A RAW SET

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-64. EGR_PROTOCOL_ERR_A RAW SET Field Descriptions

Bits	Name	Description
31-0	ERR	Sets the corresponding bit in the raw_status register when written with a 1.

8.2.7.25 EGR_PROTOCOL_ERR_A RAW CLEAR [Address = 0x88B8]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-56. EGR_PROTOCOL_ERR_A RAW CLEAR

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-65. EGR_PROTOCOL_ERR_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	ERR	Clears the corresponding bit in the raw_status register when written with a 1.

8.2.7.26 EGR_PROTOCOL_ERR_A EV0 ENABLE STATUS [Address = 0x88BC]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-57. EGR_PROTOCOL_ERR_A EV0 ENABLE STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

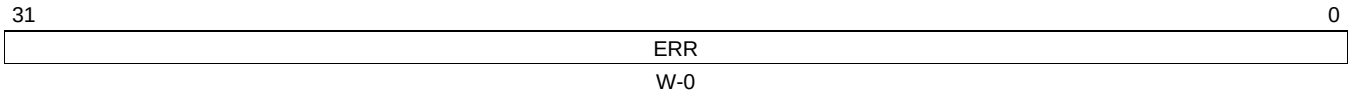
Table 8-66. EGR_PROTOCOL_ERR_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.27 EGR_PROTOCOL_ERR_A EV0 ENABLE SET [Address = 0x88C0]

Allows software to force any bit in the correesponding enable register high.

Figure 8-58. EGR_PROTOCOL_ERR_A EV0 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-67. EGR_PROTOCOL_ERR_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.28 EGR_PROTOCOL_ERR_A EV0 ENABLE CLEAR [Address = 0x88C4]

Allows software to clear any bit in the correesponding enable register.

Figure 8-59. EGR_PROTOCOL_ERR_A EV0 ENABLE CLEAR

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-68. EGR_PROTOCOL_ERR_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.29 EGR_PROTOCOL_ERR_A EV1 ENABLE STATUS [Address = 0x88C8]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-60. EGR_PROTOCOL_ERR_A EV1 ENABLE STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-69. EGR_PROTOCOL_ERR_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.30 EGR_PROTOCOL_ERR_A EV1 ENABLE SET [Address = 0x88CC]

Allows software to force any bit in the correesponding enable register high.

Figure 8-61. EGR_PROTOCOL_ERR_A EV1 ENABLE SET

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-70. EGR_PROTOCOL_ERR_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.31 EGR_PROTOCOL_ERR_A EV1 ENABLE CLEAR [Address = 0x88D0]

Allows software to clear any bit in the correesponding enable register.

Figure 8-62. EGR_PROTOCOL_ERR_A EV1 ENABLE CLEAR

31	0
ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-71. EGR_PROTOCOL_ERR_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.32 EGR_PROTOCOL_ERR_A EV0 ENABLED STATUS [Address = 0x88D4]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-63. EGR_PROTOCOL_ERR_A EV0 ENABLED STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-72. EGR_PROTOCOL_ERR_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.33 EGR_PROTOCOL_ERR_A EV1 ENABLED STATUS [Address = 0x88D8]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-64. EGR_PROTOCOL_ERR_A EV1 ENABLED STATUS

31	0
ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-73. EGR_PROTOCOL_ERR_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.34 EGR_PROTOCOL_ERR_B RAW INTERRUPT STATUS [Address = 0x88DC]

Egress protocol errors for register egr_protocol_err_b with channels 32 through 47.

Figure 8-65. EGR_PROTOCOL_ERR_B RAW INTERRUPT STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-74. EGR_PROTOCOL_ERR_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Protocol error indication of an unsupported data type or a missing PS_DATA transfer when one was expected for egress channels 32 through 47

8.2.7.35 EGR_PROTOCOL_ERR_B RAW SET [Address = 0x88E0]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-66. EGR_PROTOCOL_ERR_B RAW SET

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-75. EGR_PROTOCOL_ERR_B RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Sets the corresponding bit in the raw_status register when written with a 1.

8.2.7.36 EGR_PROTOCOL_ERR_B RAW CLEAR [Address = 0x88E4]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-67. EGR_PROTOCOL_ERR_B RAW CLEAR

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-76. EGR_PROTOCOL_ERR_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Clears the corresponding bit in the raw_status register when written with a 1.

8.2.7.37 EGR_PROTOCOL_ERR_B EV0 ENABLE STATUS [Address = 0x88E8]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-68. EGR_PROTOCOL_ERR_B EV0 ENABLE STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-77. EGR_PROTOCOL_ERR_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.38 EGR_PROTOCOL_ERR_B EV0 ENABLE SET [Address = 0x88EC]

Allows software to force any bit in the correesponding enable register high.

Figure 8-69. EGR_PROTOCOL_ERR_B EV0 ENABLE SET

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-78. EGR_PROTOCOL_ERR_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.39 EGR_PROTOCOL_ERR_B EV0 ENABLE CLEAR [Address = 0x88F0]

Allows software to clear any bit in the correesponding enable register.

Figure 8-70. EGR_PROTOCOL_ERR_B EV0 ENABLE CLEAR

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-79. EGR_PROTOCOL_ERR_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.40 EGR_PROTOCOL_ERR_B EV1 ENABLE STATUS [Address = 0x88F4]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-71. EGR_PROTOCOL_ERR_B EV1 ENABLE STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-80. EGR_PROTOCOL_ERR_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.2.7.41 EGR_PROTOCOL_ERR_B EV1 ENABLE SET [Address = 0x88F8]

Allows software to force any bit in the correesponding enable register high.

Figure 8-72. EGR_PROTOCOL_ERR_B EV1 ENABLE SET

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-81. EGR_PROTOCOL_ERR_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Sets the corresponding bit in the enable register when written with a 1.

8.2.7.42 EGR_PROTOCOL_ERR_B EV1 ENABLE CLEAR [Address = 0x88FC]

Allows software to clear any bit in the correesponding enable register.

Figure 8-73. EGR_PROTOCOL_ERR_B EV1 ENABLE CLEAR

31	16	15	0
Reserved		ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-82. EGR_PROTOCOL_ERR_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	Clears the corresponding bit in the enable register when written with a 1.

8.2.7.43 EGR_PROTOCOL_ERR_B EV0 ENABLED STATUS [Address = 0x8900]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-74. EGR_PROTOCOL_ERR_B EV0 ENABLED STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-83. EGR_PROTOCOL_ERR_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.44 EGR_PROTOCOL_ERR_B EV1 ENABLED STATUS [Address = 0x8904]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-75. EGR_PROTOCOL_ERR_B EV1 ENABLED STATUS

31	16	15	0
Reserved		ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-84. EGR_PROTOCOL_ERR_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.2.7.45 PSR_ORIG_REG [Address = 0x8960]

This is the origination register indicating which PSR interrupt register group caused the interrupt.

Figure 8-76. PSR_ORIG_REG

31	6	5	4
Reserved		EE_EGR_PROTOCOL_ERR_B	EE_EGR_PROTOCOL_ERR_A
NA-0		R-0	R-0
3	2	1	0
Reserved		EE_ING_FLUSH_B	EE_ING_FLUSH_A
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-85. PSR_ORIG_REG Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved
5	EE_EGR_PROTOCOL_ERR_B	If set a bit is set in the PSR ee_egr_protocol_err_b register.
4	EE_EGR_PROTOCOL_ERR_A	If set a bit is set in the PSR ee_egr_protocol_err_a register.
3-2	Reserved	Reserved
1	EE_ING_FLUSH_B	If set a bit is set in the PSR ee_ing_flush_b register.
0	EE_ING_FLUSH_A	If set a bit is set in the PSR ee_ing_flush_a register.

8.2.8 PKTDMA_EE [Address = 0x8C00]

Table 8-86. PKTDMA_EE

Offset	Acronym	Register Description	Section
0x8C00	PKTDMA_DESC_STARVE RAW INTERRUPT STATUS	PKTDMA SOP and MOP descriptor starvation errors.	Section 8.2.8.1
0x8C04	PKTDMA_DESC_STARVE RAW SET	Raw Set	Section 8.2.8.2
0x8C08	PKTDMA_DESC_STARVE RAW CLEAR	Raw Clear	Section 8.2.8.3
0x8C0C	PKTDMA_DESC_STARVE EV0 ENABLE STATUS	EV0 Enable Status	Section 8.2.8.4
0x8C10	PKTDMA_DESC_STARVE EV0 ENABLE SET	EV0 Enable Set	Section 8.2.8.5
0x8C14	PKTDMA_DESC_STARVE EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.2.8.6
0x8C18	PKTDMA_DESC_STARVE EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.2.8.7

8.2.8.1 PKTDMA_DESC_STARVE RAW INTERRUPT STATUS [Address = 0x8C00]

PKTDMA SOP and MOP descriptor starvation errors.

Figure 8-77. PKTDMA_DESC_STARVE RAW INTERRUPT STATUS

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-87. PKTDMA_DESC_STARVE RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	PKTDMA MOP Descriptor starvation error There were not enough descriptors available for the PKTDMA to complete the transfer of a packet it already started.
0	SOP_ERR	PKTDMA SOP Descriptor starvation error. There were not enough descriptors available for the PKTDMA to start the transfer of a packet.

8.2.8.2 PKTDMA_DESC_STARVE RAW SET [Address = 0x8C04]

Raw Set

Figure 8-78. PKTDMA_DESC_STARVE RAW SET

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-88. PKTDMA_DESC_STARVE RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SOP_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.2.8.3 PKTDMA_DESC_STARVE RAW CLEAR [Address = 0x8C08]

Raw Clear

Figure 8-79. PKTDMA_DESC_STARVE RAW CLEAR

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-89. PKTDMA_DESC_STARVE RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SOP_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.2.8.4 PKTDMA_DESC_STARVE EV0 ENABLE STATUS [Address = 0x8C0C]

EV0 Enable Status

Figure 8-80. PKTDMA_DESC_STARVE EV0 ENABLE STATUS

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-90. PKTDMA_DESC_STARVE EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SOP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.2.8.5 PKTDMA_DESC_STARVE EV0 ENABLE SET [Address = 0x8C10]

EV0 Enable Set

Figure 8-81. PKTDMA_DESC_STARVE EV0 ENABLE SET

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-91. PKTDMA_DESC_STARVE EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SOP_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.2.8.6 PKTDMA_DESC_STARVE EV0 ENABLE CLEAR [Address = 0x8C14]

EV0 Enable Clear

Figure 8-82. PKTDMA_DESC_STARVE EV0 ENABLE CLEAR

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-92. PKTDMA_DESC_STARVE EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SOP_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.2.8.7 PKTDMA_DESC_STARVE EV0 ENABLED STATUS [Address = 0x8C18]

EV0 Enabled Status

Figure 8-83. PKTDMA_DESC_STARVE EV0 ENABLED STATUS

31	2	1	0
Reserved		MOP_ERR	SOP_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-93. PKTDMA_DESC_STARVE EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	MOP_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SOP_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.3 IQS2 Registers

Table 8-94. IQS2 Register Groups

Offset	Acronym	Description	Section
0x0000	IQS_INGRESS_CONFIG	Ingress Configuration MMRs	Section 8.3.1
0x0200	IQS_INGRESS_CHAN_CONFIG	Ingress Channel Configuration MMRs	Section 8.3.2
0x2000	IQS_EGRESS_CHAN_CONFIG	IQS Egress Channel Configuration MMRs	Section 8.3.3
0x4000	IQS_EE	IQN_IQS2_EE EE register group	Section 8.3.4

8.3.1 IQS_INGRESS_CONFIG [Address = 0x0000]

Table 8-95. IQS_INGRESS_CONFIG

Offset	Acronym	Register Description	Section
0x0000	IQS INGRESS PKTDMA CONFIGURATION REGISTER	Ingress PKTDMA pushback control.	Section 8.3.1.1
0x0008	IQS INGRESS AID2 AXC CONFIGURATION REGISTER	Ingress AID2 AXC priority and pushback control	Section 8.3.1.2
0x000C	IQS INGRESS AID2 CTL CONFIGURATION REGISTER	Ingress AID2 CTL priority and pushback control	Section 8.3.1.3
0x0010	IQS INGRESS AIL0 AXC CONFIGURATION REGISTER	Ingress AIL0 and pushback AXC priority control	Section 8.3.1.4
0x0014	IQS INGRESS AIL0 CTL CONFIGURATION REGISTER	Ingress AIL0 CTL priority and pushback control	Section 8.3.1.5
0x0018	IQS INGRESS AIL1 AXC CONFIGURATION REGISTER	Ingress AIL1 AXC priority and pushback control	Section 8.3.1.6
0x001C	IQS INGRESS AIL1 CTL CONFIGURATION REGISTER	Ingress AIL1 CTL priority and pushback control	Section 8.3.1.7
0x0020	IQS INGRESS AIL2 AXC CONFIGURATION REGISTER	Ingress AIL2 AXC priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.1.8
0x0024	IQS INGRESS AIL2 CTL CONFIGURATION REGISTER	Ingress AIL2 CTL priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.1.9
0x0028	IQS INGRESS AIL3 AXC CONFIGURATION REGISTER	Ingress AIL3 AXC priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.1.10
0x002C	IQS INGRESS AIL3 CTL CONFIGURATION REGISTER	Ingress AIL3 CTL priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.1.11

8.3.1.1 IQS INGRESS PKTDMA CONFIGURATION REGISTER [Address = 0x0000]

Ingress PKTDMA pushback control.

Figure 8-84. IQS INGRESS PKTDMA CONFIGURATION REGISTER

31	1	0
Reserved		PB_SEL
NA-0		R/W-0x0001

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-96. IQS INGRESS PKTDMA CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	PB_SEL	Sets level where the PKTDMA FIFO pushback occurs on ingress ports that can be pushed back on. • pb_at_half_full (0) = Pushes back on ingress channels when the PKTDMA FIFO is over 1/2 full. At most 1/2 of the FIFO is available for traffic that can be pushed back on leaving atleast 1/2 of the FIFO for data that cannot be pushed back on. • pb_at_3qtr_full (1) = Pushes back on ingress channels when the PKTDMA FIFO is over 3/4 full. At most 3/4 of the FIFO is available for traffic that can be pushed back on leaving atleast 1/4 of the FIFO for data that cannot be pushed back on. (Set as Default)

8.3.1.2 IQS INGRESS AID2 AXC CONFIGURATION REGISTER [Address = 0x0008]

Ingress AID2 AXC priority and pushback control

Figure 8-85. IQS INGRESS AID2 AXC CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-97. IQS INGRESS AID2 AXC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.3 IQS INGRESS AID2 CTL CONFIGURATION REGISTER [Address = 0x000C]

Ingress AID2 CTL priority and pushback control

Figure 8-86. IQS INGRESS AID2 CTL CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-98. IQS INGRESS AID2 CTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.4 IQS INGRESS AIL0 AXC CONFIGURATION REGISTER [Address = 0x0010]

Ingress AIL0 and pushback AXC priority control

Figure 8-87. IQS INGRESS AIL0 AXC CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-99. IQS INGRESS AIL0 AXC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.5 IQS INGRESS AIL0 CTL CONFIGURATION REGISTER [Address = 0x0014]

Ingress AIL0 CTL priority and pushback control

Figure 8-88. IQS INGRESS AIL0 CTL CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-100. IQS INGRESS AIL0 CTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.6 IQS INGRESS AIL1 AXC CONFIGURATION REGISTER [Address = 0x0018]

Ingress AIL1 AXC priority and pushback control

Figure 8-89. IQS INGRESS AIL1 AXC CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-101. IQS INGRESS AIL1 AXC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.7 IQS INGRESS AIL1 CTL CONFIGURATION REGISTER [Address = 0x001C]

Ingress AIL1 CTL priority and pushback control

Figure 8-90. IQS INGRESS AIL1 CTL CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-102. IQS INGRESS AIL1 CTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.8 IQS INGRESS AIL2 AXC CONFIGURATION REGISTER [Address = 0x0020]

Ingress AIL2 AXC priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-91. IQS INGRESS AIL2 AXC CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-103. IQS INGRESS AIL2 AXC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.9 IQS INGRESS AIL2 CTL CONFIGURATION REGISTER [Address = 0x0024]

Ingress AIL2 CTL priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-92. IQS INGRESS AIL2 CTL CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-104. IQS INGRESS AIL2 CTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.10 IQS INGRESS AIL3 AXC CONFIGURATION REGISTER [Address = 0x0028]

Ingress AIL3 AXC priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-93. IQS INGRESS AIL3 AXC CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-105. IQS INGRESS AIL3 AXC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.1.11 IQS INGRESS AIL3 CTL CONFIGURATION REGISTER [Address = 0x002C]

Ingress AIL3 CTL priority and pushback control. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-94. IQS INGRESS AIL3 CTL CONFIGURATION REGISTER

31	9	8	7	2	1	0
Reserved		ALLOW_PUSHBACK	Reserved		PRI	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-106. IQS INGRESS AIL3 CTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ALLOW_PUSHBACK	When set allows the IQS to push back on the ingress PSI bus of this port due to the PKTDMA FIFO being too full. This allows reserving atleast 1/2 or 1/4 of the PKTDMA FIFO for the non-pushback ports. • no_pushback (0) = Do not enable pushback. Normally used for IQ data ports going to the PKTDMA and all ports going to the DIO. • en_pushback (1) = Enable pushback. Normally used only for CTL data ports going to the PKTDMA.
7-2	Reserved	RESERVED
1-0	PRI	Sets ingress port arbitration priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.2 IQS_INGRESS_CHAN_CONFIG [Address = 0x0200]

Table 8-107. IQS_INGRESS_CHAN_CONFIG

Offset	Acronym	Register Description	Section
0x0200	IQS INGRESS DIO2 PSI CONFIGURATION REGISTER	Sets the priority of the ingress DIO2 PSI channel.	Section 8.3.2.1
0x0400	IQS INGRESS AID2 AXC LUT CONFIGURATION REGISTER	Sets ingress AID2 AxC LUT for destination port and channel	Section 8.3.2.2
0x0600	IQS INGRESS AID2 CTL LUT CONFIGURATION REGISTER	Sets ingress AID2 CTL LUT for destination port and channel	Section 8.3.2.3
0x0800	IQS INGRESS AIL0 AXC LUT CONFIGURATION REGISTER	Sets ingress AIL0 AxC LUT for destination port and channel	Section 8.3.2.4
0x0A00	IQS INGRESS AIL0 CTL LUT CONFIGURATION REGISTER	Sets ingress AIL0 CTL LUT for destination port and channel	Section 8.3.2.5
0x0C00	IQS INGRESS AIL1 AXC LUT CONFIGURATION REGISTER	Sets ingress AIL1 AxC LUT for destination port and channel	Section 8.3.2.6
0x0E00	IQS INGRESS AIL1 CTL LUT CONFIGURATION REGISTER	Sets ingress AIL1 CTL LUT for destination port and channel	Section 8.3.2.7
0x1000	IQS INGRESS AIL2 AXC LUT CONFIGURATION REGISTER	Sets ingress AIL2 AxC LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.2.8
0x1200	IQS INGRESS AIL2 CTL LUT CONFIGURATION REGISTER	Sets ingress AIL2 CTL LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.2.9
0x1400	IQS INGRESS AIL3 AXC LUT CONFIGURATION REGISTER	Sets ingress AIL3 AxC LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.2.10
0x1600	IQS INGRESS AIL3 CTL LUT CONFIGURATION REGISTER	Sets ingress AIL3 CTL LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.	Section 8.3.2.11

8.3.2.1 IQS INGRESS DIO2 PSI CONFIGURATION REGISTER [Address = 0x0200 + (*S* × 0x0004)]

Size (*S*) = 0:15

Sets the priority of the ingress DIO2 PSI channel.

Figure 8-95. IQS INGRESS DIO2 PSI CONFIGURATION REGISTER

31	4	3	2	1	0
Reserved		Reserved		PRI	
NA-0		NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-108. IQS INGRESS DIO2 PSI CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	RESERVED
1-0	PRI	Sets ingress DIO2 PSI channel priority. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.

8.3.2.2 IQS INGRESS AID2 AXC LUT CONFIGURATION REGISTER [Address = 0x0400 + (*S* × 0x0004)]

Size (*S*) = 0:31

Sets ingress AID2 AxC LUT for destination port and channel

Figure 8-96. IQS INGRESS AID2 AXC LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-109. IQS INGRESS AID2 AXC LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.3 IQS INGRESS AID2 CTL LUT CONFIGURATION REGISTER [Address = 0x0600 + (*S* × 0x0004)]

Size (*S*) = 0:15

Sets ingress AID2 CTL LUT for destination port and channel

Figure 8-97. IQS INGRESS AID2 CTL LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-110. IQS INGRESS AID2 CTL LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.4 IQS INGRESS AIL0 AXC LUT CONFIGURATION REGISTER [Address = 0x0800 + (*S* × 0x0004)]

Size (*S*) = 0:63

Sets ingress AIL0 AxC LUT for destination port and channel

Figure 8-98. IQS INGRESS AIL0 AXC LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-111. IQS INGRESS AIL0 AXC LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.5 IQS INGRESS AIL0 CTL LUT CONFIGURATION REGISTER [Address = 0x0A00 + (*S* × 0x0004)]

Size (*S*) = 0:3

Sets ingress AIL0 CTL LUT for destination port and channel

Figure 8-99. IQS INGRESS AIL0 CTL LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-112. IQS INGRESS AIL0 CTL LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.6 IQS INGRESS AIL1 AXC LUT CONFIGURATION REGISTER [Address = 0x0C00 + (*S* × 0x0004)]

Size (*S*) = 0:63

Sets ingress AIL1 AxC LUT for destination port and channel

Figure 8-100. IQS INGRESS AIL1 AXC LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-113. IQS INGRESS AIL1 AXC LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.7 IQS INGRESS AIL1 CTL LUT CONFIGURATION REGISTER [Address = 0x0E00 + (*S* × 0x0004)]

Size (*S*) = 0:3

Sets ingress AIL1 CTL LUT for destination port and channel

Figure 8-101. IQS INGRESS AIL1 CTL LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-114. IQS INGRESS AIL1 CTL LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.8 IQS INGRESS AIL2 AXC LUT CONFIGURATION REGISTER [Address = 0x1000 + (*S* × 0x0004)]

Size (*S*) = 0:63

Sets ingress AIL2 AxC LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-102. IQS INGRESS AIL2 AXC LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-115. IQS INGRESS AIL2 AXC LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.9 IQS INGRESS AIL2 CTL LUT CONFIGURATION REGISTER [Address = 0x1200 + (*S* × 0x0004)]

Size (*S*) = 0:3

Sets ingress AIL2 CTL LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-103. IQS INGRESS AIL2 CTL LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-116. IQS INGRESS AIL2 CTL LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.10 IQS INGRESS AIL3 AXC LUT CONFIGURATION REGISTER [Address = 0x1400 + (*S* × 0x0004)]

Size (*S*) = 0:63

Sets ingress AIL3 AxC LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-104. IQS INGRESS AIL3 AXC LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-117. IQS INGRESS AIL3 AXC LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.2.11 IQS INGRESS AIL3 CTL LUT CONFIGURATION REGISTER [Address = 0x1600 + (*S* × 0x0004)]

Size (*S*) = 0:3

Sets ingress AIL3 CTL LUT for destination port and channel. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.

Figure 8-105. IQS INGRESS AIL3 CTL LUT CONFIGURATION REGISTER

31	10	9	8	7	6	0
Reserved		DEST		Reserved	CHAN	
NA-0		R/W-0		NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-118. IQS INGRESS AIL3 CTL LUT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9-8	DEST	Selects destination port. • PKTDMA (0) = Selects PKTDMA as the destination • DIO2 (1) = Selects DIO2 as the destination • RESERVED_2 (2) = Selects a reserved destination, do not use. • RESERVED_3 (3) = Selects a reserved destination, do not use.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.3 IQS_EGRESS_CHAN_CONFIG [Address = 0x2000]

Table 8-119. IQS_EGRESS_CHAN_CONFIG

Offset	Acronym	Register Description	Section
0x2000	IQS EGRESS PKTDMA CHANNEL CONFIGURATION REGISTER	Sets egress PKTDMA destination port and channel. Also sets internal arbitration and port PSI priority	Section 8.3.3.1
0x2200	IQS EGRESS DIO2 CHANNEL CONFIGURATION REGISTER	Sets egress DIO2 destination port and channel. Also sets internal arbitration and port PSI priority. A 0 is highest priority.	Section 8.3.3.2

8.3.3.1 IQS EGRESS PKTDMA CHANNEL CONFIGURATION REGISTER [Address = 0x2000 + (*S* × 0x0004)]

Size (*S*) = 0:47

Sets egress PKTDMA destination port and channel. Also sets internal arbitration and port PSI priority

Figure 8-106. IQS EGRESS PKTDMA CHANNEL CONFIGURATION REGISTER

31 19	18 16	15	14 12	11 8	7	6 0
Reserved	PSI_PRI	Reserved	ARB_PRI	DEST	Reserved	CHAN
NA-0	R/W-0	NA-0	R/W-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-120. IQS EGRESS PKTDMA CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-19	Reserved	RESERVED
18-16	PSI_PRI	PSI priority from the IQS output FIFOs to the destination module. Typically set the same as the ARB_PRI setting. A 0 is highest priority.
15	Reserved	RESERVED
14-12	ARB_PRI	Arbitration priority of each channel for transfers between the PKTDMA and the output FIFOs. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.
11-8	DEST	Selects destination port. • AID2_AXC (0) = Selects AID AXC as the destination • AID2_CTl (1) = Selects AID CTL as the destination • AIL0_AXC (2) = Selects AIL0 AXC as the destination • AIL0_CTL (3) = Selects AIL0 CTL as the destination • AIL1_AXC (4) = Selects AIL1 AXC as the destination • AIL1_CTL (5) = Selects AIL1_CTL as the destination • AIL2_AXC (6) = Selects AIL2 AXC as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations. • AIL2_CTL (7) = Selects AIL2 CTL as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations. • AIL3_AXC (8) = Selects AIL3 AXC as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations. • AIL3_CTL (9) = Selects AIL3_CTL as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.3.2 IQS EGRESS DIO2 CHANNEL CONFIGURATION REGISTER [Address = 0x2200 + (*S* × 0x0004)]

Size (*S*) = 0:15

Sets egress DIO2 destination port and channel. Also sets internal arbitration and port PSI priority. A 0 is highest priority.

Figure 8-107. IQS EGRESS DIO2 CHANNEL CONFIGURATION REGISTER

31 19	18 16	15	14 12	11 8	7	6 0
Reserved	PSI_PRI	Reserved	ARB_PRI	DEST	Reserved	CHAN
NA-0	R/W-0	NA-0	R/W-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-121. IQS EGRESS DIO2 CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-19	Reserved	RESERVED
18-16	PSI_PRI	PSI priority from the IQS output FIFOs to the destination module. Typically set the same as the arb_pri setting.A 0 is highest priority.
15	Reserved	RESERVED
14-12	ARB_PRI	Arbitration priority of each channel for tranfers between the DIO and the output FIFO. Typically higher speed standards require higher priorities and control ports can use lower priorities. A 0 is highest priority.
11-8	DEST	Selects destination port. • AID2_AXC (0) = Selects AID AXC as the destination • AID2_CTl (1) = Selects AID CTL as the destination • AIL0_AXC (2) = Selects AIL0 AXC as the destination • AIL0_CTL (3) = Selects AIL0 CTL as the destination • AIL1_AXC (4) = Selects AIL1 AXC as the destination • AIL1_CTL (5) = Selects AIL1_CTL as the destination • AIL2_AXC (6) = Selects AIL2 AXC as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations. • AIL2_CTL (7) = Selects AIL2 CTL as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations. • AIL3_AXC (8) = Selects AIL3 AXC as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations. • AIL3_CTL (9) = Selects AIL3_CTL as the destination. NOTE: AIL 2 and 3 not currently supported. These are to be treated as reserved locations.
7	Reserved	RESERVED
6-0	CHAN	Channel to use in the destination port.

8.3.4 IQS_EE [Address = 0x4000]

Table 8-122. IQS_EE

Offset	Acronym	Register Description	Section
0x4000	IQS EE_CHAN_ERR RAW INTERRUPT STATUS	Channel error register. When set indicates a transfer occurred for a non-existent destination port or channel.	Section 8.3.4.1
0x4004	IQS EE_CHAN_ERR RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.3.4.2
0x4008	IQS EE_CHAN_ERR RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.3.4.3
0x400C	IQS EE_CHAN_ERR EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.3.4.4
0x4010	IQS EE_CHAN_ERR EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.3.4.5
0x4014	IQS EE_CHAN_ERR EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.3.4.6
0x4018	IQS EE_CHAN_ERR EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.3.4.7
0x401C	IQS EE_CHAN_ERR EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.3.4.8
0x4020	IQS EE_CHAN_ERR EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.3.4.9
0x4024	IQS EE_CHAN_ERR EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.3.4.10
0x4028	IQS EE_CHAN_ERR EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.3.4.11
0x402C	IQS EE_ING_FLUSH_ERR RAW INTERRUPT STATUS	Ingress Flush error register. When set indicates the DIO detected the need to flush or the transfer was to an IQS DIO channel that was full.	Section 8.3.4.12
0x4030	IQS EE_ING_FLUSH_ERR RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.3.4.13
0x4034	IQS EE_ING_FLUSH_ERR RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.3.4.14
0x4038	IQS EE_ING_FLUSH_ERR EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.3.4.15
0x403C	IQS EE_ING_FLUSH_ERR EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.3.4.16
0x4040	IQS EE_ING_FLUSH_ERR EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.3.4.17
0x4044	IQS EE_ING_FLUSH_ERR EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.3.4.18
0x4048	IQS EE_ING_FLUSH_ERR EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.3.4.19
0x404C	IQS EE_ING_FLUSH_ERR EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.3.4.20
0x4050	IQS EE_ING_FLUSH_ERR EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.3.4.21
0x4054	IQS EE_ING_FLUSH_ERR EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.3.4.22
0x4058	IQS EE_EGR_FLUSH_ERR RAW INTERRUPT STATUS	Egress Flush error register. When set indicates that the destination module for the channel had requesed a flush.	Section 8.3.4.23
0x405C	IQS EE_EGR_FLUSH_ERR RAW SET	Allows software to force any bit in the correesponding raw status register high.	Section 8.3.4.24
0x4060	IQS EE_EGR_FLUSH_ERR RAW CLEAR	Allows software to clear any bit in the corresponding raw status register.	Section 8.3.4.25
0x4064	IQS EE_EGR_FLUSH_ERR EV0 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.3.4.26

Table 8-122. IQS_EE (continued)

Offset	Acronym	Register Description	Section
0x4068	IQS EE_EGR_FLUSH_ERR EV0 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.3.4.27
0x406C	IQS EE_EGR_FLUSH_ERR EV0 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.3.4.28
0x4070	IQS EE_EGR_FLUSH_ERR EV1 ENABLE STATUS	This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.	Section 8.3.4.29
0x4074	IQS EE_EGR_FLUSH_ERR EV1 ENABLE SET	Allows software to force any bit in the correesponding enable register high.	Section 8.3.4.30
0x4078	IQS EE_EGR_FLUSH_ERR EV1 ENABLE CLEAR	Allows software to clear any bit in the correesponding enable register.	Section 8.3.4.31
0x407C	IQS EE_EGR_FLUSH_ERR EV0 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.3.4.32
0x4080	IQS EE_EGR_FLUSH_ERR EV1 ENABLED STATUS	This is the result of masking the corresponding raw status register with the enable status register.	Section 8.3.4.33
0x4084	IQS ORIG_REG	This is the origination register indicating which interrupt register group caused the interrupt.	Section 8.3.4.34

8.3.4.1 IQS EE_CHAN_ERR RAW INTERRUPT STATUS [Address = 0x4000]

Channel error register. When set indicates a transfer occurred for a non-existent destination port or channel.

Figure 8-108. IQS EE_CHAN_ERR RAW INTERRUPT STATUS

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		R-0	NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-123. IQS EE_CHAN_ERR RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Egress Mux detected a port or channel error. This occurs when the destination port number in the egress PKTDMA or DIO LUT configuration register is higher than the number of output ports available or higher than the maximum number of channels in the largest port. This always indicates a programming error.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Ingress DIO2 detected a channel error. This occurs when the destination port number in the ingress port LUT configuration register is higher than the number of channels available in the DIO. This always indicates a programming error.
0	ING_PKTDMA_ERR	Ingress PKTDMA detected a channel error. This occurs when the destination port number in the ingress port LUT configuration register is higher than the number of channels available in the pktdma. This always indicates a programming error.

8.3.4.2 IQS EE_CHAN_ERR RAW SET [Address = 0x4004]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-109. IQS EE_CHAN_ERR RAW SET

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		W-0	NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-124. IQS EE_CHAN_ERR RAW SET Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Sets the corresponding bit in the raw_status register when written with a 1.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Sets the corresponding bit in the raw_status register when written with a 1.
0	ING_PKTDMA_ERR	Sets the corresponding bit in the raw_status register when written with a 1.

8.3.4.3 IQS EE_CHAN_ERR RAW CLEAR [Address = 0x4008]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-110. IQS EE_CHAN_ERR RAW CLEAR

31 17	16	15 2	1	0
Reserved	EGR_MUX_ERR	Reserved	ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0	W-0	NA-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-125. IQS EE_CHAN_ERR RAW CLEAR Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Clears the corresponding bit in the raw_status register when written with a 1.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Clears the corresponding bit in the raw_status register when written with a 1.
0	ING_PKTDMA_ERR	Clears the corresponding bit in the raw_status register when written with a 1.

8.3.4.4 IQS EE_CHAN_ERR EV0 ENABLE STATUS [Address = 0x400C]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-111. IQS EE_CHAN_ERR EV0 ENABLE STATUS

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		R-0	NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-126. IQS EE_CHAN_ERR EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	When high enables the corresponding raw status bit to generate an interrupt.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	When high enables the corresponding raw status bit to generate an interrupt.
0	ING_PKTDMA_ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.3.4.5 IQS EE_CHAN_ERR EV0 ENABLE SET [Address = 0x4010]

Allows software to force any bit in the correesponding enable register high.

Figure 8-112. IQS EE_CHAN_ERR EV0 ENABLE SET

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		W-0	NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-127. IQS EE_CHAN_ERR EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Sets the corresponding bit in the enable register when written with a 1.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Sets the corresponding bit in the enable register when written with a 1.
0	ING_PKTDMA_ERR	Sets the corresponding bit in the enable register when written with a 1.

8.3.4.6 IQS EE_CHAN_ERR EV0 ENABLE CLEAR [Address = 0x4014]

Allows software to clear any bit in the correesponding enable register.

Figure 8-113. IQS EE_CHAN_ERR EV0 ENABLE CLEAR

31 17	16	15 2	1	0
Reserved	EGR_MUX_ERR	Reserved	ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0	W-0	NA-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-128. IQS EE_CHAN_ERR EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Clears the corresponding bit in the enable register when written with a 1.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Clears the corresponding bit in the enable register when written with a 1.
0	ING_PKTDMA_ERR	Clears the corresponding bit in the enable register when written with a 1.

8.3.4.7 IQS EE_CHAN_ERR EV1 ENABLE STATUS [Address = 0x4018]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-114. IQS EE_CHAN_ERR EV1 ENABLE STATUS

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		R-0	NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-129. IQS EE_CHAN_ERR EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	When high enables the corresponding raw status bit to generate an interrupt.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	When high enables the corresponding raw status bit to generate an interrupt.
0	ING_PKTDMA_ERR	When high enables the corresponding raw status bit to generate an interrupt.

8.3.4.8 IQS EE_CHAN_ERR EV1 ENABLE SET [Address = 0x401C]

Allows software to force any bit in the correesponding enable register high.

Figure 8-115. IQS EE_CHAN_ERR EV1 ENABLE SET

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		W-0	NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-130. IQS EE_CHAN_ERR EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Sets the corresponding bit in the enable register when written with a 1.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Sets the corresponding bit in the enable register when written with a 1.
0	ING_PKTDMA_ERR	Sets the corresponding bit in the enable register when written with a 1.

8.3.4.9 IQS EE_CHAN_ERR EV1 ENABLE CLEAR [Address = 0x4020]

Allows software to clear any bit in the correesponding enable register.

Figure 8-116. IQS EE_CHAN_ERR EV1 ENABLE CLEAR

31 17	16	15 2	1	0
Reserved	EGR_MUX_ERR	Reserved	ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0	W-0	NA-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-131. IQS EE_CHAN_ERR EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	Clears the corresponding bit in the enable register when written with a 1.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	Clears the corresponding bit in the enable register when written with a 1.
0	ING_PKTDMA_ERR	Clears the corresponding bit in the enable register when written with a 1.

8.3.4.10 IQS EE_CHAN_ERR EV0 ENABLED STATUS [Address = 0x4024]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-117. IQS EE_CHAN_ERR EV0 ENABLED STATUS

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		R-0	NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-132. IQS EE_CHAN_ERR EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.
0	ING_PKTDMA_ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.3.4.11 IQS EE_CHAN_ERR EV1 ENABLED STATUS [Address = 0x4028]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-118. IQS EE_CHAN_ERR EV1 ENABLED STATUS

31	17	16	15	2	1	0
Reserved		EGR_MUX_ERR	Reserved		ING_DIO2_ERR	ING_PKTDMA_ERR
NA-0		R-0	NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-133. IQS EE_CHAN_ERR EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved.
16	EGR_MUX_ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.
15-2	Reserved	Reserved.
1	ING_DIO2_ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.
0	ING_PKTDMA_ERR	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.3.4.12 IQS EE_ING_FLUSH_ERR RAW INTERRUPT STATUS [Address = 0x402C]

Ingress Flush error register. When set indicates the DIO detected the need to flush or the transfer was to an IQS DIO channel that was full.

Figure 8-119. IQS EE_ING_FLUSH_ERR RAW INTERRUPT STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-134. IQS EE_ING_FLUSH_ERR RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	DIO2 Ingress path detected a flush condition. Either the DIO2 detected a flush or there was a write to the DIO2 Ingress FIFO when the FIFO for that channel was full.

8.3.4.13 IQS EE_ING_FLUSH_ERR RAW SET [Address = 0x4030]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-120. IQS EE_ING_FLUSH_ERR RAW SET

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-135. IQS EE_ING_FLUSH_ERR RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Sets the corresponding bit in the raw_status register when written with a 1.

8.3.4.14 IQS EE_ING_FLUSH_ERR RAW CLEAR [Address = 0x4034]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-121. IQS EE_ING_FLUSH_ERR RAW CLEAR

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-136. IQS EE_ING_FLUSH_ERR RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Clears the corresponding bit in the raw_status register when written with a 1.

8.3.4.15 IQS EE_ING_FLUSH_ERR EV0 ENABLE STATUS [Address = 0x4038]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-122. IQS EE_ING_FLUSH_ERR EV0 ENABLE STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-137. IQS EE_ING_FLUSH_ERR EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high enables the corresponding raw status bit to generate an interrupt.

8.3.4.16 IQS EE_ING_FLUSH_ERR EV0 ENABLE SET [Address = 0x403C]

Allows software to force any bit in the correesponding enable register high.

Figure 8-123. IQS EE_ING_FLUSH_ERR EV0 ENABLE SET

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-138. IQS EE_ING_FLUSH_ERR EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Sets the corresponding bit in the enable register when written with a 1.

8.3.4.17 IQS EE_ING_FLUSH_ERR EV0 ENABLE CLEAR [Address = 0x4040]

Allows software to clear any bit in the correesponding enable register.

Figure 8-124. IQS EE_ING_FLUSH_ERR EV0 ENABLE CLEAR

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-139. IQS EE_ING_FLUSH_ERR EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Clears the corresponding bit in the enable register when written with a 1.

8.3.4.18 IQS EE_ING_FLUSH_ERR EV1 ENABLE STATUS [Address = 0x4044]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-125. IQS EE_ING_FLUSH_ERR EV1 ENABLE STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-140. IQS EE_ING_FLUSH_ERR EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high enables the corresponding raw status bit to generate an interrupt.

8.3.4.19 IQS EE_ING_FLUSH_ERR EV1 ENABLE SET [Address = 0x4048]

Allows software to force any bit in the correesponding enable register high.

Figure 8-126. IQS EE_ING_FLUSH_ERR EV1 ENABLE SET

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-141. IQS EE_ING_FLUSH_ERR EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Sets the corresponding bit in the enable register when written with a 1.

8.3.4.20 IQS EE_ING_FLUSH_ERR EV1 ENABLE CLEAR [Address = 0x404C]

Allows software to clear any bit in the correesponding enable register.

Figure 8-127. IQS EE_ING_FLUSH_ERR EV1 ENABLE CLEAR

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-142. IQS EE_ING_FLUSH_ERR EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Clears the corresponding bit in the enable register when written with a 1.

8.3.4.21 IQS EE_ING_FLUSH_ERR EV0 ENABLED STATUS [Address = 0x4050]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-128. IQS EE_ING_FLUSH_ERR EV0 ENABLED STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-143. IQS EE_ING_FLUSH_ERR EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.3.4.22 IQS EE_ING_FLUSH_ERR EV1 ENABLED STATUS [Address = 0x4054]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-129. IQS EE_ING_FLUSH_ERR EV1 ENABLED STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-144. IQS EE_ING_FLUSH_ERR EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.3.4.23 IQS EE_EGR_FLUSH_ERR RAW INTERRUPT STATUS [Address = 0x4058]

Egress Flush error register. When set indicates that the destination module for the channel had requesed a flush.

Figure 8-130. IQS EE_EGR_FLUSH_ERR RAW INTERRUPT STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-145. IQS EE_EGR_FLUSH_ERR RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	DIO2 Egress path detected a flush condition. Either the Destination port generated a flush or there was a write to the DIO2 Egress FIFO when the FIFO for that channel was full.

8.3.4.24 IQS EE_EGR_FLUSH_ERR RAW SET [Address = 0x405C]

Allows software to force any bit in the correesponding raw status register high.

Figure 8-131. IQS EE_EGR_FLUSH_ERR RAW SET

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-146. IQS EE_EGR_FLUSH_ERR RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Sets the corresponding bit in the raw_status register when written with a 1.

8.3.4.25 IQS EE_EGR_FLUSH_ERR RAW CLEAR [Address = 0x4060]

Allows software to clear any bit in the corresponding raw status register.

Figure 8-132. IQS EE_EGR_FLUSH_ERR RAW CLEAR

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-147. IQS EE_EGR_FLUSH_ERR RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Clears the corresponding bit in the raw_status register when written with a 1.

8.3.4.26 IQS EE_EGR_FLUSH_ERR EV0 ENABLE STATUS [Address = 0x4064]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-133. IQS EE_EGR_FLUSH_ERR EV0 ENABLE STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-148. IQS EE_EGR_FLUSH_ERR EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high enables the corresponding raw status bit to generate an interrupt.

8.3.4.27 IQS EE_EGR_FLUSH_ERR EV0 ENABLE SET [Address = 0x4068]

Allows software to force any bit in the correesponding enable register high.

Figure 8-134. IQS EE_EGR_FLUSH_ERR EV0 ENABLE SET

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-149. IQS EE_EGR_FLUSH_ERR EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Sets the corresponding bit in the enable register when written with a 1.

8.3.4.28 IQS EE_EGR_FLUSH_ERR EV0 ENABLE CLEAR [Address = 0x406C]

Allows software to clear any bit in the correesponding enable register.

Figure 8-135. IQS EE_EGR_FLUSH_ERR EV0 ENABLE CLEAR

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-150. IQS EE_EGR_FLUSH_ERR EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Clears the corresponding bit in the enable register when written with a 1.

8.3.4.29 IQS EE_EGR_FLUSH_ERR EV1 ENABLE STATUS [Address = 0x4070]

This is the enable mask used to select which raw status bits generate an interrupt when both register bits are set.

Figure 8-136. IQS EE_EGR_FLUSH_ERR EV1 ENABLE STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-151. IQS EE_EGR_FLUSH_ERR EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high enables the corresponding raw status bit to generate an interrupt.

8.3.4.30 IQS EE_EGR_FLUSH_ERR EV1 ENABLE SET [Address = 0x4074]

Allows software to force any bit in the correesponding enable register high.

Figure 8-137. IQS EE_EGR_FLUSH_ERR EV1 ENABLE SET

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-152. IQS EE_EGR_FLUSH_ERR EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Sets the corresponding bit in the enable register when written with a 1.

8.3.4.31 IQS EE_EGR_FLUSH_ERR EV1 ENABLE CLEAR [Address = 0x4078]

Allows software to clear any bit in the correesponding enable register.

Figure 8-138. IQS EE_EGR_FLUSH_ERR EV1 ENABLE CLEAR

31	16	15	0
Reserved		FLUSH	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-153. IQS EE_EGR_FLUSH_ERR EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	Clears the corresponding bit in the enable register when written with a 1.

8.3.4.32 IQS EE_EGR_FLUSH_ERR EV0 ENABLED STATUS [Address = 0x407C]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-139. IQS EE_EGR_FLUSH_ERR EV0 ENABLED STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-154. IQS EE_EGR_FLUSH_ERR EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.3.4.33 IQS EE_EGR_FLUSH_ERR EV1 ENABLED STATUS [Address = 0x4080]

This is the result of masking the corresponding raw status register with the enable status register.

Figure 8-140. IQS EE_EGR_FLUSH_ERR EV1 ENABLED STATUS

31	16	15	0
Reserved		FLUSH	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-155. IQS EE_EGR_FLUSH_ERR EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	FLUSH	When high indicates the interrupt is active due to the corresponding bit in the raw status register.

8.3.4.34 IQS ORIG_REG [Address = 0x4084]

This is the origination register indicating which interrupt register group caused the interrupt.

Figure 8-141. IQS ORIG_REG

31	3	2	1	0
Reserved		EE_EGR_FLUSH_ERR	EE_ING_FLUSH_ERR	EE_CHAN_ERR
NA-0		R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-156. IQS ORIG_REG Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2	EE_EGR_FLUSH_ERR	If set a bit is set in the ee_egr_flush_err register.
1	EE_ING_FLUSH_ERR	If set a bit is set in the ee_ing_flush_err register.
0	EE_CHAN_ERR	If set a bit is set in the ee_chan_err register.

8.4 AT2 Registers

Table 8-157. AT2 Register Groups

Offset	Acronym	Description	Section
0x0000	AT2_START		Section 8.4.1
0x0010	AT2_RP1	Group of registers which relate to the OBSAI RP1 synchronization interface (Unused for CPRI and unsed for OBSAI when using other synch source such as IEEE1588)	Section 8.4.2
0x0020	AT2_BCN	Group of all registers relating to the BCN (BTS Chip Number) Timer. The BCN timer is the SOC central timer which synchronizes all timing applications. All uAT slave timers and System Event RADT timers are synchronized by this centralized AT2 BCN timer.	Section 8.4.3
0x0060	AT2_GSM	Special GSM T1, T1, T3 Timer Registers. The init values have the effect of over-writing the free running timers. The free running values are read from the sts register.	Section 8.4.4
0x0200	AT2_RADT	Group containing RADT configuration and status. A total of 8 RADT timers are available for purpose of supplying radio timer information to APP SW, RAC, and TAC. RADT timers are also available to system event circuits for purpose of radio timed system events.	Section 8.4.5
0x0400	AT2_EVENTS_24ARRAY	Array of system event control register. Each entry in Array is for each of 24 system events. System events are slaves of either RADT or BCN timers.	Section 8.4.6
0x0600	AT2_EVENTS	Group containing Non-Arrayed System Event control. Registers are 24 bits wide, one bit per system event.	Section 8.4.7
0x0800	AT2_RADT_SYM_LUT_RAM	RAM containing table of terminal count lengths of symbols or time slots. Programmed in units of AT2 clocks	Section 8.4.8
0x8000	AT2_EE	IQN_AT2_EE EE register group	Section 8.4.9

8.4.1 AT2_START [Address = 0x0000]

Table 8-158. AT2_START

Offset	Acronym	Register Description	Section
0x0000	AT2 AT2 TIMER ENABLES	Control for each of the RADT and the BCN timers	Section 8.4.1.1

8.4.1.1 AT2 AT2 TIMER ENABLES [Address = 0x0000]

Control for each of the RADT and the BCN timers

Figure 8-142. AT2 AT2 TIMER ENABLES

31	10	9	8	7	0
Reserved		RUN_BCN	Reserved	RADT_EN	
NA-0		R/W-0	NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-159. AT2 AT2 TIMER ENABLES Field Descriptions

Bits	Name	Description
31-10	Reserved	RESERVED
9	RUN_BCN	SW control which starts the BCN Timer running. SW starts cannot make correct timing, so it is expected the user will correct the timer value with an offset when it captures external sync
8	Reserved	RESERVED
7-0	RADT_EN	bit 0-7 enable RadT0-to-RadT7. RADT 7 will be used for driving the t1-t2-t3 GSM Timer. Once enabled, Timers will start running once the compare value equals the BCN timer value (which yeilds an exact sync)

8.4.2 AT2_RP1 [Address = 0x0010]

Table 8-160. AT2_RP1

Offset	Acronym	Register Description	Section
0x0010	AT2 AT2 OBSAI RP1 CONTROL	Configuration for OBSAI RP1 CRC circuit. (Unused for CPRI or non-RP1 OBSAI sync options)	Section 8.4.2.1
0x0014	AT2 AT2 RP1 TYPE CAPTURE	OBSAI RP1 Sync mechanism. Capture incoming RP1 FCB. (Ignore if not using RP1)	Section 8.4.2.2
0x0018	AT2 RP1 TOD CAPTURE LSBS	OBSAI RP1 Sync mechanism. Capture incoming RP1 FCB. (Ignore if not using RP1)	Section 8.4.2.3
0x001C	AT2 RP1 TOD CAPTURE MSBS	OBSAI RP1 Sync mechanism. Capture incoming RP1 FCB. (Ignore if not using RP1)	Section 8.4.2.4

8.4.2.1 AT2 AT2 OBSAI RP1 CONTROL [Address = 0x0010]

Configuration for OBSAI RP1 CRC circuit. (Unused for CPRI or non-RP1 OBSAI sync options)

Figure 8-143. AT2 AT2 OBSAI RP1 CONTROL

31 13	12	11	10	9	8 0
Reserved	CRC_INVERT	CRC_INIT_ONES	CRC_FLIP	CRC_USE	Reserved
NA-0	R/W-0	R/W-0	R/W-0	R/W-0	NA-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-161. AT2 AT2 OBSAI RP1 CONTROL Field Descriptions

Bits	Name	Description
31-13	Reserved	RESERVED
12	CRC_INVERT	Enables bit-by-bit inversion of calculated CRC value prior to comparison. • noinvert (0) = CRC bits are not inverted (Default, typical). • invert (1) = CRC bits are inverted.
11	CRC_INIT_ONES	Initialization value of the CRC engine. • init0 (0) = CRC is initialized to a 0 (Default, typical). • init1 (1) = CRC is initialized to an FFFF.
10	CRC_FLIP	CRC bit order select. • normal (0) = normal order is sending the CRC in big-endian with the MSB as the first bit out. (DEFAULT) • reverse (1) = reverse order is sending the CRC in little-endian with the LSB as the first bit out.
9	CRC_USE	When set to 1, a failed CRC check will result in the FCB being dropped. • dont_use (0) = CRC is not used • use (1) = CRC is used
8-0	Reserved	RESERVED

8.4.2.2 AT2 AT2 RP1 TYPE CAPTURE [Address = 0x0014]

OBSAI RP1 Sync mechanism. Capture incoming RP1 FCB. (Ignore if not using RP1)

Figure 8-144. AT2 AT2 RP1 TYPE CAPTURE

31	8	7	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

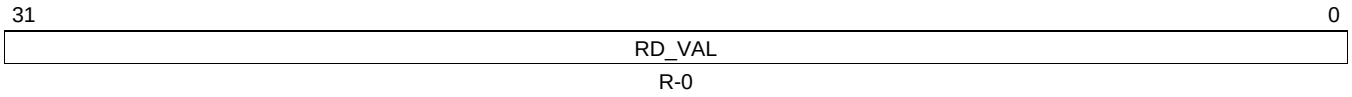
Table 8-162. AT2 AT2 RP1 TYPE CAPTURE Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	RD_VAL	RP1 Type field captured

8.4.2.3 AT2 RP1 TOD CAPTURE LSBS [Address = 0x0018]

OBSAI RP1 Sync mechanism. Capture incoming RP1 FCB. (Ignore if not using RP1)

Figure 8-145. AT2 RP1 TOD CAPTURE LSBS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-163. AT2 RP1 TOD CAPTURE LSBS Field Descriptions

Bits	Name	Description
31-0	RD_VAL	RP1 payload capture 32 LSBs

8.4.2.4 AT2 RP1 TOD CAPTURE MSBS [Address = 0x001C]

OBSAI RP1 Sync mechanism. Capture incoming RP1 FCB. (Ignore if not using RP1)

Figure 8-146. AT2 RP1 TOD CAPTURE MSBS

31	0
RD_VAL	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-164. AT2 RP1 TOD CAPTURE MSBS Field Descriptions

Bits	Name	Description
31-0	RD_VAL	RP1 payload capture 32 MSBs

8.4.3 AT2_BCN [Address = 0x0020]

Table 8-165. AT2_BCN

Offset	Acronym	Register Description	Section
0x0020	AT2 AT2 BCN OFFSET		Section 8.4.3.1
0x0024	AT2 BCN PA_TSCOMP CAPTURE	CPTS module in NETCP/PA provides a measurement pulse called pa_tscomp. When this pulse fires, the BCN Timer value is captured to this register. SW may then use this captured value to calculate a BCN timer error which is corrected by writing to the BCN Offset register.	Section 8.4.3.2
0x0028	AT2 BCN PHYSYNC CAPTURE	An external pin called PHYSYNC provides an optional sync measurement source. When a rising edge is detected on this pin, the BCN Timer value is captured to this register.	Section 8.4.3.3
0x002C	AT2 BCN RADSYNC CAPTURE	An external pin called RADSYNC provides an optional sync measurement source. When a rising edge is detected on this pin, the BCN Timer value is captured to this register. this RADSYNC is not used for RAD timer but only used for BCN timer	Section 8.4.3.4
0x0030	AT2 BCN RP1_SYNC CAPTURE	OBSAI RP1 optionally may be used as a sync measurement source. When a successful RP1 FCB is recieved, optionally a system event fires, the FCB message is captured to registers, and the BCN timer value is captured to this register.	Section 8.4.3.5
0x0034	AT2 BCN UAT SLAVE SYNC CAPTURE	The uAT will provide frame sync pulses back to the AT. When this pulse fires, the BCN Timer value is captured to this register. SW may then use this captured value to calculate a BCN timer error which is corrected by writing to the BCN Offset register.	Section 8.4.3.6
0x0038	AT2 BCN FRAME VALUE LSBS	BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows reading of the value	Section 8.4.3.7
0x003C	AT2 BCN FRAME VALUE MSBS	BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows reading of the value	Section 8.4.3.8
0x0040	AT2 BCN UAT SLAVE SELECT	BCN uat slave select for capturing the BCN when the uat slave sends back it's sync. This is for debug and small time adjustment in systems which have different AIL uAT clk vs sys_clk, not used if ail uAT is on the same sys_clk as AT	Section 8.4.3.9
0x0044	AT2 BCN FRAME INIT LSBS	BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows writing of the value. User may write to this register while BCN is running. Advisable to write in the middle of frame time to avoid wrap uncertaninty	Section 8.4.3.10
0x0048	AT2 BCN FRAME INIT MSBS	BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows writing of the value. User may write to this register while BCN is running.	Section 8.4.3.11
0x004C	AT2 BCN CLOCK COUNTER TC	Terminal count of BCN. User should chose value which vields 10ms. (245.76MHz) 2,457,599 (307.2MHz) 3,071,999	Section 8.4.3.12
0x0050	AT2 BCN FRAME TC LSBS	BCN Frame count value (BTS Frame Number). Terminal count for frame_count field. Frame count goes to 0 when it matches the concatenated MSB and LSB value of these two registers.	Section 8.4.3.13
0x0054	AT2 BCN FRAME TC MSBS	BCN Frame count value (BTS Frame Number). Terminal count for frame_count field	Section 8.4.3.14

8.4.3.1 AT2 AT2 BCN OFFSET [Address = 0x0020]

Figure 8-147. AT2 AT2 BCN OFFSET

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-166. AT2 AT2 BCN OFFSET Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	Offset for the free running raw BCN counter. The offset version of BCN is the value used for all measurement and sync purposes. (The offset mechanism gives a way to minimize clock domains crossing errors when syncing timers).SW uses the desired sync input capture status to calculate offset correction factor. This correction factor will be [Frame size - captured value].

8.4.3.2 AT2 BCN PA_TSCOMP CAPTURE [Address = 0x0024]

CPTS module in NETCP/PA provides a measurement pulse called pa_tscomp. When this pulse fires, the BCN Timer value is captured to this register. SW may then use this captured value to calculate a BCN timer error which is corrected by writing to the BCN Offset register.

Figure 8-148. AT2 BCN PA_TSCOMP CAPTURE

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-167. AT2 BCN PA_TSCOMP CAPTURE Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	BCN clock count pa_tscomp capture

8.4.3.3 AT2 BCN PHYSYNC CAPTURE [Address = 0x0028]

An external pin called PHYSYNC provides an optional sync measurement source. When a rising edge is detected on this pin, the BCN Timer value is captured to this register.

Figure 8-149. AT2 BCN PHYSYNC CAPTURE

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-168. AT2 BCN PHYSYNC CAPTURE Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	BCN clock count physync capture

8.4.3.4 AT2 BCN RADSYNC CAPTURE [Address = 0x002C]

An external pin called RADSYNC provides an optional sync measurement source. When a rising edge is detected on this pin, the BCN Timer value is captured to this register. this RADSYNC is not used for RAD timer but only used for BCN timer

Figure 8-150. AT2 BCN RADSYNC CAPTURE

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-169. AT2 BCN RADSYNC CAPTURE Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	BCN clock count radsync capture

8.4.3.5 AT2 BCN RP1_SYNC CAPTURE [Address = 0x0030]

OBSAI RP1 optionally may be used as a sync measurement source. When a successful RP1 FCB is recieved, optionally a system event fires, the FCB message is captured to registers, and the BCN timer value is captured to this register.

Figure 8-151. AT2 BCN RP1_SYNC CAPTURE

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

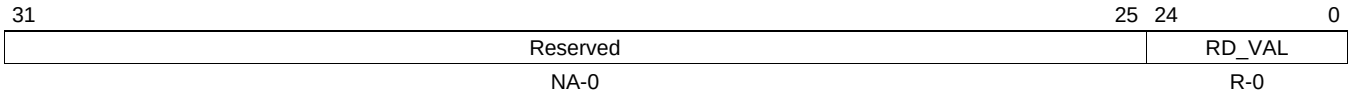
Table 8-170. AT2 BCN RP1_SYNC CAPTURE Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	BCN clock count rp1_sync capture

8.4.3.6 AT2 BCN UAT SLAVE SYNC CAPTURE [Address = 0x0034]

The uAT will provide frame sync pulses back to the AT. When this pulse fires, the BCN Timer value is captured to this register. SW may then use this captured value to calculate a BCN timer error which is corrected by writing to the BCN Offset register.

Figure 8-152. AT2 BCN UAT SLAVE SYNC CAPTURE



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-171. AT2 BCN UAT SLAVE SYNC CAPTURE Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	BCN clock count selected slave uAT sync capture. bcn_slvsel_cfg selects which uAT slave sync is used for capturing the BCN value in this register.

8.4.3.7 AT2 BCN FRAME VALUE LSBS [Address = 0x0038]

BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows reading of the value

Figure 8-153. AT2 BCN FRAME VALUE LSBS

31	12	11	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-172. AT2 BCN FRAME VALUE LSBS Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	RD_VAL	BCN Frame Value LSBs

8.4.3.8 AT2 BCN FRAME VALUE MSBS [Address = 0x003C]

BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows reading of the value

Figure 8-154. AT2 BCN FRAME VALUE MSBS

31	28	27	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-173. AT2 BCN FRAME VALUE MSBS Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-0	RD_VAL	BCN Frame Value MSBs

8.4.3.9 AT2 BCN UAT SLAVE SELECT [Address = 0x0040]

BCN uat slave select for capturing the BCN when the uat slave sends back it's sync. This is for debug and small time adjustment in systems which have different AIL uAT clk vs sys_clk, not used if ail uAT is on the same sys_clk as AT

Figure 8-155. AT2 BCN UAT SLAVE SELECT

31	4	3	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-174. AT2 BCN UAT SLAVE SELECT Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	VAL	BCN uat slave select for choosing which of up to 16 uats is used as the source of the sync signal.

8.4.3.10 AT2 BCN FRAME INIT LSBS [Address = 0x0044]

BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows writing of the value. User may write to this register while BCN is running. Advisable to write in the middle of frame time to avoid wrap uncertaninty

Figure 8-156. AT2 BCN FRAME INIT LSBS

31	12	11	0
Reserved		WR_VAL	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-175. AT2 BCN FRAME INIT LSBS Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	WR_VAL	BCN Frame Init LSBs

8.4.3.11 AT2 BCN FRAME INIT MSBS [Address = 0x0048]

BCN Frame count value (BTS Frame Number). Increments every time 10ms BCN timer wraps. This Register only allows writing of the value. User may write to this register while BCN is running.

Figure 8-157. AT2 BCN FRAME INIT MSBS

31	28	27	0
Reserved		WR_VAL	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-176. AT2 BCN FRAME INIT MSBS Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-0	WR_VAL	BCN Frame Init MSBs

8.4.3.12 AT2 BCN CLOCK COUNTER TC [Address = 0x004C]

Terminal count of BCN. User should chose value which yields 10ms. (245.76MHz) 2,457,599 (307.2MHz) 3,071,999

Figure 8-158. AT2 BCN CLOCK COUNTER TC

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-177. AT2 BCN CLOCK COUNTER TC Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	BCN Clock Counter TC. Set to one less than the number of clock cycles needed.

8.4.3.13 AT2 BCN FRAME TC LSBS [Address = 0x0050]

BCN Frame count value (BTS Frame Number). Terminal count for frame_count field. Frame count goes to 0 when it matches the concatenated MSB and LSB value of these two registers.

Figure 8-159. AT2 BCN FRAME TC LSBS

31	0
VAL	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-178. AT2 BCN FRAME TC LSBS Field Descriptions

Bits	Name	Description
31-0	VAL	BCN Frame TC LSBs

8.4.3.14 AT2 BCN FRAME TC MSBS [Address = 0x0054]

BCN Frame count value (BTS Frame Number). Terminal count for frame_count field

Figure 8-160. AT2 BCN FRAME TC MSBS

31	8	7	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-179. AT2 BCN FRAME TC MSBS Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	VAL	BCN Frame TC MSBs. Frame count goes to 0 when it matches the concatenated MSB and LSB value of these two registers.

8.4.4 AT2_GSM [Address = 0x0060]

Table 8-180. AT2_GSM

Offset	Acronym	Register Description	Section
0x0060	AT2 GSM T1 T2 T3 INITAL VALUE	Special GSM T1, T2, T3 count GSM frames in way which is useful to GSM only APP SW. This register is for writing only and can be written either before the timer starts counting or on-the-fly (Users should avoid modifiying value near wrap position to avoid uncertanty)	Section 8.4.4.1
0x0064	AT2 GSM T1 T2 T3 CURRENT VALUE	Special GSM T1, T2, T3 count GSM frames in way which is useful to GSM only APP SW. This register is for only for reading the current state (Users should avoid reading the value near the increment to avoid uncertainty)	Section 8.4.4.2

8.4.4.1 AT2 GSM T1 T2 T3 INITAL VALUE [Address = 0x0060]

Special GSM T1, T2, T3 count GSM frames in way which is useful to GSM only APP SW. This register is for writing only and can be written either before the timer starts counting or on-the-fly (Users should avoid modifiying value near wrap position to avoid uncertanty)

Figure 8-161. AT2 GSM T1 T2 T3 INITAL VALUE

31	22	21	16	15	11	10	0
Reserved		T3		T2		T1	
NA-0		W-0		W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-181. AT2 GSM T1 T2 T3 INITAL VALUE Field Descriptions

Bits	Name	Description
31-22	Reserved	RESERVED
21-16	T3	T3 w=init, affects at_gsm_tcount_value
15-11	T2	T2 w=init, affects at_gsm_tcount_value
10-0	T1	T1 w=init, affects at_gsm_tcount_value

8.4.4.2 AT2 GSM T1 T2 T3 CURRENT VALUE [Address = 0x0064]

Special GSM T1, T2, T3 count GSM frames in way which is useful to GSM only APP SW. This register is for only for reading the current state (Users should avoid reading the value near the increment to avoid uncertainty)

Figure 8-162. AT2 GSM T1 T2 T3 CURRENT VALUE

31 22	21 16	15 11	10 0
Reserved	T3	T2	T1
NA-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-182. AT2 GSM T1 T2 T3 CURRENT VALUE Field Descriptions

Bits	Name	Description
31-22	Reserved	RESERVED
21-16	T3	T3 r=value of T3 counter
15-11	T2	T2 r=value of T2 counter
10-0	T1	T1 r=value of T1 counter

8.4.5 AT2_RADT [Address = 0x0200 + (R × 0x0040)]

Table 8-183. AT2_RADT

Offset	Acronym	Register Description	Section
0x0200 + (*R* × 0x0040)	AT2 RADT STATUS, SAMPLE AND SYMBOL COUNT VALUE	Radio timer sample and symbol count value	Section 8.4.5.1
0x0204 + (*R* × 0x0040)	AT2 RADT STATUS, FRAME COUNT VALUE LSBS	RADT Frame Value 12 LSBs	Section 8.4.5.2
0x0208 + (*R* × 0x0040)	AT2 RADT STATUS, FRAME VALUE MSBS	RADT Frame Value MSBs	Section 8.4.5.3
0x020C + (*R* × 0x0040)	AT2 RADT STATUS, VALUE IN WCDMA RAC & TAC FORMAT	RADT has specific format which is expected by the RAC and TAC HW accelerator modules. EDMA performs a read of these values each RAC or TAC iteration cycle giving RAC and TAC a sense of real time.	Section 8.4.5.4
0x0210 + (*R* × 0x0040)	AT2 RADT FRAME INIT LSBS	RADT Frame Init LSBs	Section 8.4.5.5
0x0214 + (*R* × 0x0040)	AT2 RADT FRAME INIT MSBS	RADT Frame Init MSBs	Section 8.4.5.6
0x0218 + (*R* × 0x0040)	AT2 RADT COUNTER TERMINAL COUNT	AT RADT clock, LUT index and symbol counter terminal counts	Section 8.4.5.7
0x0220 + (*R* × 0x0040)	AT2 RADT FRAME TC LSBS	Radio frame terminal count LSBs. Frame counter resets to 0 when a frame boundary is met and the concatenated radt_frame_tc_msbs and radt_frame_tc_lsbs match the frame counter.	Section 8.4.5.8
0x0224 + (*R* × 0x0040)	AT2 RADT FRAME TC MSBS	Radio frame terminal count MSBs. Frame counter resets to 0 when a frame boundary is met and the concatenated radt_frame_tc_msbs and radt_frame_tc_lsbs match the frame counter.	Section 8.4.5.9
0x0228 + (*R* × 0x0040)	AT2 RADT BASE ADDRESS FOR INDEX	Radio timer LUT index start address pointer	Section 8.4.5.10
0x022C + (*R* × 0x0040)	AT2 BCN SYNC COMPARE VALUE	radt BCN sync compare	Section 8.4.5.11

8.4.5.1 AT2 RADT STATUS, SAMPLE AND SYMBOL COUNT VALUE [Address = 0x0200 + (*R* × 0x0040)]

Range (*R*) = 0:7

Radio timer sample and symbol count value

Figure 8-163. AT2 RADT STATUS, SAMPLE AND SYMBOL COUNT VALUE

31 27	26 19	18 0
Reserved	RADT_SYMCNT_VAL	RADT_SAMPCNT_VAL
NA-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-184. AT2 RADT STATUS, SAMPLE AND SYMBOL COUNT VALUE Field Descriptions

Bits	Name	Description
31-27	Reserved	RESERVED
26-19	RADT_SYMCNT_VAL	RADT symbol count Value
18-0	RADT_SAMPCNT_VAL	RADT sample count Value. Increments every radt_0_cfg clkcnt_tc +1 system clock cycles.

8.4.5.2 AT2 RADT STATUS, FRAME COUNT VALUE LSBS [Address = 0x0204 + (*R* × 0x0040)]

Range (*R*) = 0:7

RADT Frame Value 12 LSBs

Figure 8-164. AT2 RADT STATUS, FRAME COUNT VALUE LSBS

31 12	11 0
Reserved	RADT_FRM_VAL_LSB
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-185. AT2 RADT STATUS, FRAME COUNT VALUE LSBS Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	RADT_FRM_VAL_LSB	RADT Frame Value 12 LSBs

8.4.5.3 AT2 RADT STATUS, FRAME VALUE MSBS [Address = 0x0208 + (*R* × 0x0040)]

Range (*R*) = 0:7

RADT Frame Value MSBs

Figure 8-165. AT2 RADT STATUS, FRAME VALUE MSBS

31 28	27 0
Reserved	RADT_FRM_VAL_MSB
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-186. AT2 RADT STATUS, FRAME VALUE MSBS Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-0	RADT_FRM_VAL_MSB	RADT Frame Value MSBs

8.4.5.4 AT2 RADT STATUS, VALUE IN WCDMA RAC & TAC FORMAT [Address = 0x020C + (*R* × 0x0040)]

Range (*R*) = 0:7

RADT has specific format which is expected by the RAC and TAC HW accelerator modules. EDMA performs a read of these values each RAC or TAC iteration cycle giving RAC and TAC a sense of real time.

Figure 8-166. AT2 RADT STATUS, VALUE IN WCDMA RAC & TAC FORMAT

31 28	27 16	15 12	11 0
Reserved	RADT_FRM	RADT_SLOT	RADT_CHIP
NA-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-187. AT2 RADT STATUS, VALUE IN WCDMA RAC & TAC FORMAT Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-16	RADT_FRM	Frame Value
15-12	RADT_SLOT	Slot Value
11-0	RADT_CHIP	Chip Value

8.4.5.5 AT2 RADT FRAME INIT LSBS [Address = 0x0210 + (*R* × 0x0040)]

Range (*R*) = 0:7

RADT Frame Init LSBs

Figure 8-167. AT2 RADT FRAME INIT LSBS

31 12	11 0
Reserved	FRM_INIT_LSB
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-188. AT2 RADT FRAME INIT LSBS Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	FRM_INIT_LSB	RADT Frame Init LSBs loads a frame count directly to the counter LSB bits. This register and the MSB register should only be loaded when the RADT is off or if it is known it will not be incrementing during the time of the writes.

8.4.5.6 AT2 RADT FRAME INIT MSBS [Address = 0x0214 + (*R* × 0x0040)]

Range (*R*) = 0:7

RADT Frame Init MSBs

Figure 8-168. AT2 RADT FRAME INIT MSBS

31 28	27 0
Reserved	FRM_INIT_MSB
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-189. AT2 RADT FRAME INIT MSBS Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-0	FRM_INIT_MSB	RADT Frame Init MSBs loads a frame count directly to the counter MSB bits. This register and the LSB register should only be loaded when the RADT is off or if it is known it will not be incrementing during the time of the writes.

8.4.5.7 AT2 RADT COUNTER TERMINAL COUNT [Address = 0x0218 + (*R* × 0x0040)]

Range (*R*) = 0:7

AT RADT clock, LUT index and symbol counter terminal counts

Figure 8-169. AT2 RADT COUNTER TERMINAL COUNT

31 27	26 19	18 11	10 0
Reserved	SYMB_TC	LUTINDEX_TC	CLKCNT_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-190. AT2 RADT COUNTER TERMINAL COUNT Field Descriptions

Bits	Name	Description
31-27	Reserved	RESERVED
26-19	SYMB_TC	Symbol TC. This is the number of symbols in the frame minus 1.
18-11	LUTINDEX_TC	LUT Index TC. This is the number of sample entries in the table minus 1 plus the offset into the LUT for the start of the table for this RADT. It is typically either a 0 when all symbols are the same size or it is the number of symbols in the frame minus 1 plus the LUT starting address (radt_3_cfg lut_index_strt) so there is a separate LUT entry for each symbol.
10-0	CLKCNT_TC	Clock divider counter TC. The clock divider divides down the clock to a sample period before driving the sample counter. represents num clock ticks minus 1 per sample

8.4.5.8 AT2 RADT FRAME TC LSBS [Address = 0x0220 + (*R* × 0x0040)]

Range (*R*) = 0:7

Radio frame terminal count LSBs. Frame counter resets to 0 when a frame boundary is met and the concatenated radt_frame_tc_msbs and radt_frame_tc_lsbs match the frame counter.

Figure 8-170. AT2 RADT FRAME TC LSBS

31	0
FRM_TC_LSB	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-191. AT2 RADT FRAME TC LSBS Field Descriptions

Bits	Name	Description
31-0	FRM_TC_LSB	RADT Frame TC LSBs

8.4.5.9 AT2 RADT FRAME TC MSBS [Address = 0x0224 + (*R* × 0x0040)]

Range (*R*) = 0:7

Radio frame terminal count MSBs. Frame counter resets to 0 when a frame boundary is met and the concatenated radt_frame_tc_msbs and radt_frame_tc_lsbs match the frame counter.

Figure 8-171. AT2 RADT FRAME TC MSBS

31	8	7	0
Reserved		FRM_TC_MSB	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-192. AT2 RADT FRAME TC MSBS Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	FRM_TC_MSB	RADT Frame TC MSBs

8.4.5.10 AT2 RADT BASE ADDRESS FOR INDEX [Address = 0x0228 + (*R* × 0x0040)]

Range (*R*) = 0:7

Radio timer LUT index start address pointer

Figure 8-172. AT2 RADT BASE ADDRESS FOR INDEX

31	8	7	0
Reserved		LUT_INDEX_STRT	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-193. AT2 RADT BASE ADDRESS FOR INDEX Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	LUT_INDEX_STRT	LUT Index start address pointer to the symbol lut memory for this RADT.

8.4.5.11 AT2 BCN SYNC COMPARE VALUE [Address = 0x022C + (*R* × 0x0040)]

Range (*R*) = 0:7

radt BCN sync compare

Figure 8-173. AT2 BCN SYNC COMPARE VALUE

31 25	24 0
Reserved	BCN_SYNC_CMP
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-194. AT2 BCN SYNC COMPARE VALUE Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	BCN_SYNC_CMP	BCN compare value for synchronization to start the RADT. The RADT starts on the next occurance of the BCN counter matching this value after being enabled and is ignored after that as long as the RADT is enabled.

8.4.6 AT2_EVENTS_24ARRAY [Address = 0x0400 + (*R* × 0x0010)]

Table 8-195. AT2_EVENTS_24ARRAY

Offset	Acronym	Register Description	Section
0x0400 + (*R* × 0x0010)	AT2 SYSTEM EVENT OFFSET	event_offset after the start of frame and event strobe selection, the sys_event generator count out OFFSET clocks then fires once	Section 8.4.6.1
0x0404 + (*R* × 0x0010)	AT2 SYSTEM EVENT MODULO TERMINAL COUNT	Periodic system event rate. Programmed in sys_clks minus 1. after the event has fired once, the event will re-fire every MOD clocks	Section 8.4.6.2
0x0408 + (*R* × 0x0010)	AT2 SYSTEM EVENT MASK, LSBS	Programmably mask GSM system events. The system event generator maintains a count which indexes this mask LUT starting with the LSB. When zero, the bit suppresses the system event. This mechanism supports irregular patterns of system events. After the table is exausted, after 64 events, the pattern is repeated until the next strobe boundary slected by evt_strb_sel is detected.	Section 8.4.6.3
0x040C + (*R* × 0x0010)	AT2 SYSTEM EVENT MASK, MSBS	Programmably mask GSM system events.	Section 8.4.6.4

8.4.6.1 AT2 SYSTEM EVENT OFFSET [Address = 0x0400 + (*R* × 0x0010)]

Range (*R*) = 0:23

event_offset after the start of frame and event strobe selection, the sys_event generator count out OFFSET clocks then fires once

Figure 8-174. AT2 SYSTEM EVENT OFFSET

31 29	28 24	23 22	21 0
Reserved	EVT_STRB_SEL	Reserved	VAL
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-196. AT2 SYSTEM EVENT OFFSET Field Descriptions

Bits	Name	Description
31-29	Reserved	RESERVED
28-24	EVT_STRB_SEL	Selects which RADT counter and start-of-symbol vs. start-of-frame. Each the selected strobe fires, the given sys_event generator resets • RADT0_frame (0) = Use RADT Frame to trigger the event • RADT1_frame (1) = Use RADT Frame to trigger the event • RADT2_frame (2) = Use RADT Frame to trigger the event • RADT3_frame (3) = Use RADT Frame to trigger the event • RADT4_frame (4) = Use RADT Frame to trigger the event • RADT5_frame (5) = Use RADT Frame to trigger the event • RADT6_frame (6) = Use RADT Frame to trigger the event • RADT7_frame (7) = Use RADT Frame to trigger the event • RADT0_symb (8) = Use RADT Symbol to trigger the event • RADT1_symb (9) = Use RADT Symbol to trigger the event • RADT2_symb (10) = Use RADT Symbol to trigger the event • RADT3_symb (11) = Use RADT Symbol to trigger the event • RADT4_symb (12) = Use RADT Symbol to trigger the event • RADT5_symb (13) = Use RADT Symbol to trigger the event • RADT6_symb (14) = Use RADT Symbol to trigger the event • RADT7_symb (15) = Use RADT Symbol to trigger the event • BCN_frame (16) = Use BCN Frame to trigger the event • EVT_nrest (17) = Use Next higher event to trigger this event (i.e. event1 can trigger event0)
23-22	Reserved	RESERVED
21-0	VAL	Event Offset Index. This is the number of system clocks after the selected RADT event that the event is triggerred.

8.4.6.2 AT2 SYSTEM EVENT MODULO TERMINAL COUNT [Address = 0x0404 + (*R* × 0x0010)]

Range (*R*) = 0:23

Periodic system event rate. Programmed in sys_clks minus 1. after the event has fired once, the event will re-fire every MOD clocks

Figure 8-175. AT2 SYSTEM EVENT MODULO TERMINAL COUNT

31	22	21	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-197. AT2 SYSTEM EVENT MODULO TERMINAL COUNT Field Descriptions

Bits	Name	Description
31-22	Reserved	RESERVED
21-0	VAL	Event Modulo. Minimum programmed value should be 15. This corresponds to a minimum modulo of 16.

8.4.6.3 AT2 SYSTEM EVENT MASK, LSBS [Address = 0x0408 + (*R* × 0x0010)]

Range (*R*) = 0:23

Programmably mask GSM system events. The system event generator maintains a count which indexes this mask LUT starting with the LSB. When zero, the bit suppresses the system event. This mechanism supports irregular patterns of system events. After the table is exausted, after 64 events, the pattern is repeated until the next strobe boundary slected by evt_strb_sel is detected.

Figure 8-176. AT2 SYSTEM EVENT MASK, LSBS

31	0
VAL	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-198. AT2 SYSTEM EVENT MASK, LSBS Field Descriptions

Bits	Name	Description
31-0	VAL	Event Mask LSBs. all 0 will disable events, A 1 in a bit enables that event time. Typically set these to all ones when GSM masking is not desired.

8.4.6.4 AT2 SYSTEM EVENT MASK, MSBS [Address = 0x040C + (*R* × 0x0010)]

Range (*R*) = 0:23

Programmably mask GSM system events.

Figure 8-177. AT2 SYSTEM EVENT MASK, MSBS

31	0
VAL	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-199. AT2 SYSTEM EVENT MASK, MSBS Field Descriptions

Bits	Name	Description
31-0	VAL	Event Mask MSBs. all 0 will disable events, A 1 in a bit enables that event time. Typically set these to all ones when GSM masking is not desired.

8.4.7 AT2_EVENTS [Address = 0x0600]

Table 8-200. AT2_EVENTS

Offset	Acronym	Register Description	Section
0x0600	AT2 SYSTEM EVENT ENABLES	AT2 system events control APP SW timing. This MMR Enables each of 24 of these system events	Section 8.4.7.1
0x0604	AT2 SYSTEM EVENT FORCE REGISTER	For diagnostic purposes, this register allows the user to activate any of the 24 system events with a simple registers write. Useful for activating SW thread for testing purposes	Section 8.4.7.2

8.4.7.1 AT2 SYSTEM EVENT ENABLES [Address = 0x0600]

AT2 system events control APP SW timing. This MMR Enables each of 24 of these system events

Figure 8-178. AT2 SYSTEM EVENT ENABLES

31	24	23	0
Reserved		EN	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-201. AT2 SYSTEM EVENT ENABLES Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	EN	EVENT Enable when a bit is set to a 1. Must be enabled after event configuration.

8.4.7.2 AT2 SYSTEM EVENT FORCE REGISTER [Address = 0x0604]

For diagnostic purposes, this register allows the user to activate any of the 24 system events with a simple registers write. Useful for activating SW thread for testing purposes

Figure 8-179. AT2 SYSTEM EVENT FORCE REGISTER

31	24	23	0
Reserved		STRB	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-202. AT2 SYSTEM EVENT FORCE REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	STRB	EVENT Force causes an event when set to a 1 on the corresponding system event.

8.4.8 AT2_RADT_SYM_LUT_RAM [Address = 0x0800 + (R × 0x0004)]

Table 8-203. AT2_RADT_SYM_LUT_RAM

Offset	Acronym	Register Description	Section
0x0800 + (*R* × 0x0004)	AT2 AT2 SYMBOL LUT RAM	RAM based LUT which give a clock count length per sym/time_slot. This table approach gives a flexible approach to program framing timing for any random radio standard. For GSM, use 104 table entries, one each for 104 time_slots per 60 ms. For LTE norm_cyc_prefix use 7 or 14 table entries, one each for every symbol in a sub-frame. For WCDMA use a single entry to be replayed 15 (time slots) times per frame	Section 8.4.8.1

8.4.8.1 AT2 AT2 SYMBOL LUT RAM [Address = 0x0800 + (R × 0x0004)]

Range (*R*) = 0:255

RAM based LUT which give a clock count length per sym/time_slot. This table approach gives a flexible approach to program framing timing for any random radio standard. For GSM, use 104 table entries, one each for 104 time_slots per 60 ms. For LTE norm_cyc_prefix use 7 or 14 table entries, one each for every symbol in a sub-frame. For WCDMA use a single entry to be replayed 15 (time slots) times per frame

Figure 8-180. AT2 AT2 SYMBOL LUT RAM

31 19	18 0
Reserved	SYMBCNT_TC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-204. AT2 AT2 SYMBOL LUT RAM Field Descriptions

Bits	Name	Description
31-19	Reserved	RESERVED
18-0	SYMBCNT_TC	RadT symbol counter terminal count programmed in sys_clks (usually 245.76MHz or 307.2MHz) Set to the number of clock cycles needed minus 1. If all symbols are the same size only 1 location needs to be used, otherwise a separate location is needed for each symbol in the frame.

8.4.9 AT2_EE [Address = 0x8000]

Table 8-205. AT2_EE

Offset	Acronym	Register Description	Section
0x8000	AT2 AT_EE_0 RAW INTERRUPT STATUS	RP1 Errors and Synchronization input Info.	Section 8.4.9.1
0x8004	AT2 AT_EE_0 RAW SET	Raw Set	Section 8.4.9.2
0x8008	AT2 AT_EE_0 RAW CLEAR	Raw Clear	Section 8.4.9.3
0x800C	AT2 AT_EE_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.4.9.4
0x8010	AT2 AT_EE_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.4.9.5
0x8014	AT2 AT_EE_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.4.9.6
0x8018	AT2 AT_EE_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.4.9.7
0x801C	AT2 AT_EE_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.4.9.8
0x8020	AT2 AT_EE_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.4.9.9
0x8024	AT2 AT_EE_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.4.9.10
0x8028	AT2 AT_EE_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.4.9.11

8.4.9.1 AT2 AT_EE_0 RAW INTERRUPT STATUS [Address = 0x8000]

RP1 Errors and Synchronization input Info.

Figure 8-181. AT2 AT_EE_0 RAW INTERRUPT STATUS

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		R-0	R-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-206. AT2 AT_EE_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	A pa_tscomp sync input was received from NETCP PA (Valid when using IEEE1588 sync). BCN value was captured for use by APP SW to calc and correct BCN alignment
4	PHYSYNC_INFO	A strobe was recieved on the phyt (BCN) sync input pin (Only valid when using external sync pin) BCN value was captured for use by APP SW to calc and correct BCN alignment
3	RADSYNC_INFO	A strobe was recieved on the radt sync input pin (Only valid when using external sync pin). BCN value was captured for use by APP SW to calc and correct RADT alignment
2	RP1_SYNC_INFO	An RP1 FCB packet was received (Only valid with using OBSAI RP1 Sync Interface). BCN value was captured for use by APP SW to calc and correct BCN alignment
1	RP1_BIT_ERR	RP1 bit error (Only valid with using OBSAI RP1 Sync Interface). RP1 FCB recieved pattern is illegal. Data bits were not held for 8 consecutive RP1_clks
0	RP1_CRC_ERR	RP1 CRC error (Only valid with using OBSAI RP1 Sync Interface). RP1 FCB was recieved with bad CRC. APP SW should disregard FCB

8.4.9.2 AT2 AT_EE_0 RAW SET [Address = 0x8004]

Raw Set

Figure 8-182. AT2 AT_EE_0 RAW SET

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		W-0	W-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-207. AT2 AT_EE_0 RAW SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	PHYSYNC_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	RADSYNC_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	RP1_SYNC_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	RP1_BIT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	RP1_CRC_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.4.9.3 AT2 AT_EE_0 RAW CLEAR [Address = 0x8008]

Raw Clear

Figure 8-183. AT2 AT_EE_0 RAW CLEAR

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		W-0	W-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-208. AT2 AT_EE_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	PHYSYNC_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	RADSYNC_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	RP1_SYNC_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	RP1_BIT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	RP1_CRC_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.4.9.4 AT2 AT_EE_0 EV0 ENABLE STATUS [Address = 0x800C]

EV0 Enable Status

Figure 8-184. AT2 AT_EE_0 EV0 ENABLE STATUS

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		R-0	R-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-209. AT2 AT_EE_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	PHYSYNC_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	RADSYNC_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	RP1_SYNC_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	RP1_BIT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	RP1_CRC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.4.9.5 AT2 AT_EE_0 EV0 ENABLE SET [Address = 0x8010]

EV0 Enable Set

Figure 8-185. AT2 AT_EE_0 EV0 ENABLE SET

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		W-0	W-0
3		2	1	0
RADSYNC_INFO		RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
W-0		W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-210. AT2 AT_EE_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	PHYSYNC_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	RADSYNC_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	RP1_SYNC_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	RP1_BIT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	RP1_CRC_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.4.9.6 AT2 AT_EE_0 EV0 ENABLE CLEAR [Address = 0x8014]

EV0 Enable Clear

Figure 8-186. AT2 AT_EE_0 EV0 ENABLE CLEAR

31 6	5	4
Reserved	PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0	W-0	W-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-211. AT2 AT_EE_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	PHYSYNC_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	RADSYNC_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	RP1_SYNC_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	RP1_BIT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	RP1_CRC_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.4.9.7 AT2 AT_EE_0 EV1 ENABLE STATUS [Address = 0x8018]

EV1 Enable Status

Figure 8-187. AT2 AT_EE_0 EV1 ENABLE STATUS

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		R-0	R-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-212. AT2 AT_EE_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	PHYSYNC_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	RADSYNC_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	RP1_SYNC_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	RP1_BIT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	RP1_CRC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.4.9.8 AT2 AT_EE_0 EV1 ENABLE SET [Address = 0x801C]

EV1 Enable Set

Figure 8-188. AT2 AT_EE_0 EV1 ENABLE SET

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		W-0	W-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-213. AT2 AT_EE_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	PHYSYNC_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	RADSYNC_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	RP1_SYNC_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	RP1_BIT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	RP1_CRC_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.4.9.9 AT2 AT_EE_0 EV1 ENABLE CLEAR [Address = 0x8020]

EV1 Enable Clear

Figure 8-189. AT2 AT_EE_0 EV1 ENABLE CLEAR

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		W-0	W-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-214. AT2 AT_EE_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	PHYSYNC_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	RADSYNC_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	RP1_SYNC_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	RP1_BIT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	RP1_CRC_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.4.9.10 AT2 AT_EE_0 EV0 ENABLED STATUS [Address = 0x8024]

EV0 Enabled Status

Figure 8-190. AT2 AT_EE_0 EV0 ENABLED STATUS

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		R-0	R-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-215. AT2 AT_EE_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	PHYSYNC_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	RADSYNC_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	RP1_SYNC_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	RP1_BIT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	RP1_CRC_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.4.9.11 AT2 AT_EE_0 EV1 ENABLED STATUS [Address = 0x8028]

EV1 Enabled Status

Figure 8-191. AT2 AT_EE_0 EV1 ENABLED STATUS

31	6	5	4
Reserved		PA_TSCOMP_INFO	PHYSYNC_INFO
NA-0		R-0	R-0

3	2	1	0
RADSYNC_INFO	RP1_SYNC_INFO	RP1_BIT_ERR	RP1_CRC_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-216. AT2 AT_EE_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	PA_TSCOMP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	PHYSYNC_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	RADSYNC_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	RP1_SYNC_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	RP1_BIT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	RP1_CRC_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5 AID2 Registers

Table 8-217. AID2 Register Groups

Offset	Acronym	Description	Section
0x0000	AID2_SI_IQ_EFE_CONFIG_GROUP	Group containing EFE Channel Configuration registers	Section 8.5.1
0x0400	AID2_SI_IQ_EFE_RADIO _STANDARD_GROUP	Group of registers containing EFE configuration which is radio standard specific. Eight radio standards are supported, individual AxC channels are each assigned to one of these.	Section 8.5.2
0x0600	AID2_IQ_EFE_CHAN_AXC_OFFSET	Group containing IQ_EFE_CHAN_AXC_OFFSET RAM	Section 8.5.3
0x0800	AID2_IQ_EFE_FRM_SAMP_TC_MMR _RAM	Group containing Egress Sample Terminal Count Configuration registers	Section 8.5.4
0x0C00	AID2_IQ_EFE_CHAN_TDM_LUT	Group containing IQ_EFE_CHAN_TDM_LUT RAM	Section 8.5.5
0x1000	AID2_IQ_EFE_RADIO_STANDARD _SCHEDULER_GROUP	Group containing EFE Channel Scheduler Configuration registers	Section 8.5.6
0x2000	AID2_IQ_IFE_CHANNEL _CONFIGURATION_GROUP	Group containing IFE Radio Stanadard registers	Section 8.5.7
0x2200	AID2_IQ_IFE_RADIO_STANDARD _GROUP	Group containing IFE Radio Stanadard registers	Section 8.5.8
0x2340	AID2_IQ_IFE_CONFIG_GROUP	Group containing IFE Configuration registers	Section 8.5.9
0x2384	AID2_IQ_IDC_GENERAL_STATUS _GROUP	Group containing IDC Status registers	Section 8.5.10
0x23C0	AID2_IQ_IDC_CONFIGURATION _GROUP	Group containing IFE Radio Stanadard registers	Section 8.5.11
0x2400	AID2_IQ_IDC_CHANNEL_CONFIG _GROUP	Group containing IDC Channel Configuration registers	Section 8.5.12
0x2800	AID2_IFE_FRM_SAMP_TC_MMR _RAM	Group containing Sample Terminal Count Configuration registers	Section 8.5.13
0x3000	AID2_ECTL_PKT_IF	Group containing ECTL Configuration and Status Registers in the VBUS_CLK domain	Section 8.5.14
0x4000	AID2_ICTL_IDC_IF	Group containing ICTL IDC Configuration registers	Section 8.5.15
0x4280	AID2_ICTL_PKT_IF	Group containing ICTL Packet Interface Configuration registers	Section 8.5.16
0x5000	AID2_UAT_GEN_CTL	Run bit for all uAT timers and BCN registers	Section 8.5.17
0x5080	AID2_UAT_EGR_RADT	Egress RADT registers	Section 8.5.18
0x5100	AID2_UAT_ING_RADT	Ingress RADT registers	Section 8.5.19
0x5200	AID2_UAT_RADT_EVT	(Unused for AIL) RADT event compare registers for Frame strobe and iteration strobe counter config for 4sample Iteration strobe. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress	Section 8.5.20
0x8000	AID2_IQ_EDC_REGISTER_GROUP	Group containing EDC Configuration registers	Section 8.5.21
0xA000	AID2_IQ_INGRESS_VBUS_MMR _GROUP	Group containing VBUS Ingress IQ MMR registers	Section 8.5.22
0xB000	AID2_ECTL_REGISTER_GROUP	Group containing ECTL Configuration registers	Section 8.5.23
0xC000	AID2_CTL_INGRESS_VBUS_MMR _GROUP	Group containing VBUS Ingress CTL MMR registers	Section 8.5.24
0x1_0000	AID2_IQN_AID2_EE_SYSCLK_EE	IQN_AID2_EE_SYSCLK EE register group	Section 8.5.25

Table 8-217. AID2 Register Groups (continued)

Offset	Acronym	Description	Section
0x1_1000	AID2_EE_DFE	IQN_AID2_DFE_EE_SYSCLK EE register group	Section 8.5.26
0x1_2000	AID2_IQN_AID2_EE_VBUSCLK_EE	IQN_AID2_EE_VBUSCLK EE register group	Section 8.5.27

8.5.1 AID2_SI_IQ_EFE_CONFIG_GROUP [Address = 0x0000]

Table 8-218. AID2_SI_IQ_EFE_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x0000	AID2 IQ EFE CHANNEL CONFIGURATION REGISTER	IFE DMA Channel Configuration Register	Section 8.5.1.1
0x0200	AID2 IQ EFE CONFIGURATION REGISTER	EFE Rx to Tx Loopback Configuration Register	Section 8.5.1.2
0x0240	AID2 IQ EFE GLOBAL ENABLE SET REG	Set Global Enable for EFE	Section 8.5.1.3
0x0244	AID2 IQ EFE GLOBAL ENABLE CLEAR REG	Clear Global Enable for EFE	Section 8.5.1.4
0x0248	AID2 IQ EFE GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, EFE may still be closing out packets.	Section 8.5.1.5
0x0260	AID2 IQ EFE CHANNEL ON STATUS REG	Gives current On/Off Status of every available AxC stream. One bit per channel (bit0:ch0 ~ bit31:ch31). Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.5.1.6
0x0280	AID2 IQ EFE IN PACKET STATUS REGISTERS	Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP. Not used for DIO SI	Section 8.5.1.7
0x02A0	AID2 IQ EFE DMA SYNC STATUS REGISTERS	Gives current DMA SYNC state of AxC channels only. Bits are always zero for OBSAI control channels. Bit is activated when symbol 0 (non-TDD configuation) or first TDD-ON symbol (TDD configuration) of a frame is read from the Residual Buffer and the channel is in the CHAN_ON state. Bit is deactivated on the next SYM/SLOT boundary when channel is disabled or EFE is shutdown. Bit is deactivated immediately when the channel experiences starvation or a protocol error.	Section 8.5.1.8

8.5.1.1 AID2 IQ EFE CHANNEL CONFIGURATION REGISTER [Address = 0x0000 + (*S* × 0x0004)]

Size (*S*) = 0:31

IFE DMA Channel Configuration Register

Figure 8-192. AID2 IQ EFE CHANNEL CONFIGURATION REGISTER

31 15	14 12	11 9	8	7 1	0
Reserved	CHAN_RADIO_SEL	Reserved	CHAN_TDD_FRC_OFF	Reserved	CHAN_EN
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-219. AID2 IQ EFE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-15	Reserved	RESERVED
14-12	CHAN_RADIO_SEL	Assigns each channel to one of eight radio standard groups. i.e. radio standard 0 may be LTE 20MHz • RS0 (0) = Radio Standard 0 • RS1 (1) = Radio Standard 1 • RS2 (2) = Radio Standard 2 • RS3 (3) = Radio Standard 3 • RS4 (4) = Radio Standard 4 • RS5 (5) = Radio Standard 5 • RS6 (6) = Radio Standard 6 • RS7 (7) = Radio Standard 7
11-9	Reserved	RESERVED
8	CHAN_TDD_FRC_OFF	Alternate TDD mode for controlling TDD also used for GSM Base Band Hopping. APP SW controls updates this bit each symbol of time to control whether the next symbol will be TDD OFF. TDD OFF channels generate no Ingress DMA traffic and expect no Egress DMA traffic. Zeros are sent over the PHY. In BBHop mode, the same applies and in OBSAI, empty_msg is sent over the PHY instead of zeroed traffic • FRC_SYM_OFF (1) = Force symbols off • NO_FRC_OFF_SYM (0) = No forcing off of symbols
7-1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.5.1.2 AID2 IQ EFE CONFIGURATION REGISTER [Address = 0x0200]

EFE Rx to Tx Loopback Configuration Register

Figure 8-193. AID2 IQ EFE CONFIGURATION REGISTER

31	1	0
Reserved		LOOPBACK_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-220. AID2 IQ EFE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	LOOPBACK_EN	(TI use Only) 0x1: Ingress data from ICC is looped back to Egress data to ICC. DMA traffic is unused. (i.e. for purpose of DFE only testing)

8.5.1.3 AID2 IQ EFE GLOBAL ENABLE SET REG [Address = 0x0240]

Set Global Enable for EFE

Figure 8-194. AID2 IQ EFE GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-221. AID2 IQ EFE GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.5.1.4 AID2 IQ EFE GLOBAL ENABLE CLEAR REG [Address = 0x0244]

Clear Global Enable for EFE

Figure 8-195. AID2 IQ EFE GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-222. AID2 IQ EFE GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.5.1.5 AID2 IQ EFE GLOBAL ENABLE STATUS [Address = 0x0248]

Read Only status of global enable state. Even if this register is OFF, EFE may still be closing out packets.

Figure 8-196. AID2 IQ EFE GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-223. AID2 IQ EFE GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: efe_ON 0x0:efe_OFF

8.5.1.6 AID2 IQ EFE CHANNEL ON STATUS REG [Address = 0x0260]

Gives current On/Off Status of every available AxC stream. One bit per channel (bit0:ch0 ~ bit31:ch31). Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-197. AID2 IQ EFE CHANNEL ON STATUS REG

31	0
CHAN_ON	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-224. AID2 IQ EFE CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.5.1.7 AID2 IQ EFE IN PACKET STATUS REGISTERS [Address = 0x0280]

Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP. Not used for DIO SI

Figure 8-198. AID2 IQ EFE IN PACKET STATUS REGISTERS

31	0
IN_PKT	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-225. AID2 IQ EFE IN PACKET STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-0	IN_PKT	0x1: IN_PKT 0x0:OUT_PKT

8.5.1.8 AID2 IQ EFE DMA SYNC STATUS REGISTERS [Address = 0x02A0]

Gives current DMA SYNC state of AxC channels only. Bits are always zero for OBSAI control channels. Bit is activated when symbol 0 (non-TDD configuation) or first TDD-ON symbol (TDD configuration) of a frame is read from the Residual Buffer and the channel is in the CHAN_ON state. Bit is deactivated on the next SYM/SLOT boundary when channel is disabled or EFE is shutdown. Bit is deactivated immediately when the channel experiences starvation or a protocol error.

Figure 8-199. AID2 IQ EFE DMA SYNC STATUS REGISTERS

31	0
DMA_SYNC	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-226. AID2 IQ EFE DMA SYNC STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-0	DMA_SYNC	0x1: DMA synchronized to radio timing for this channel 0x0:DMA not synchronized to radio timing for this channel. Channel is in in re-sync mode.

8.5.2 AID2_SI_IQ_EFE_RADIO_STANDARD_GROUP [Address = 0x0400]

Table 8-227. AID2_SI_IQ_EFE_RADIO_STANDARD_GROUP

Offset	Acronym	Register Description	Section
0x0400	AID2 IQ EFE FRAME COUNT REGISTER	EFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants	Section 8.5.2.1
0x0420	AID2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER	EFE Radio Standard Configuration Register	Section 8.5.2.2
0x0440	AID2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.3
0x0460	AID2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.4
0x0480	AID2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.5
0x04A0	AID2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.6
0x04C0	AID2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.7
0x04E0	AID2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.8
0x0500	AID2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.9
0x0520	AID2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.2.10

8.5.2.1 AID2 IQ EFE FRAME COUNT REGISTER [Address = 0x0400 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants

Figure 8-200. AID2 IQ EFE FRAME COUNT REGISTER

31 24	23 16	15 8	7 0
Reserved	INDEX_TC	INDEX_SC	SYM_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-228. AID2 IQ EFE FRAME COUNT REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	INDEX_TC	Radio Framing Counter. Index Counter Terminal Count. Index counter terminal count which is the last value of the Index Counter before it wraps. For simple use case, program same as frm_sym_tc.
15-8	INDEX_SC	Radio Framing Counter. Index Counter Starting Location. Starting location of the Sample Terminal Count LUT loaded into the Index Counter when it first starts and each time it wraps. Depending on the radio standard, the index will wrap once per radio frame such as WCDMA or multiple times per frame as in LTE. Index is the address for XXX_IQ_EFE_FRM_SAMP_TC
7-0	SYM_TC	Radio Framing Counter. Symbol Count. Number of symbols per frame programmed as a terminal count.

8.5.2.2 AID2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER [Address = 0x0420 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Radio Standard Configuration Register

Figure 8-201. AID2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER

31	9	8	7	0
Reserved		TDD_LUT_EN	TDD_FIRST_SYM	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-229. AID2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	TDD_LUT_EN	Enable use of iq_efe_tdd_en_cfg and use of TDD_FIRST_SYM. Does not impact CHAN_TDD_FRC_OFF operation (which does not use TDD_FIRST_SYM) • ENABLED (1) = TDD enabled for this radio standard • DISABLED (0) = TDD disabled for this radio standard
7-0	TDD_FIRST_SYM	Selects first symbol to start TDD

8.5.2.3 AID2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT [Address = 0x0440 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-202. AID2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-230. AID2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.4 AID2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT [Address = 0x0460 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-203. AID2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-231. AID2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.5 AID2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT [Address = 0x0480 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-204. AID2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-232. AID2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.6 AID2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT [Address = 0x04A0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-205. AID2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-233. AID2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.7 AID2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT [Address = 0x04C0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-206. AID2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-234. AID2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.8 AID2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT [Address = 0x04E0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-207. AID2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-235. AID2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.9 AID2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT [Address = 0x0500 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-208. AID2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-236. AID2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.2.10 AID2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT [Address = 0x0520 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-209. AID2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-237. AID2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.3 AID2_IQ_EFE_CHAN_AXC_OFFSET [Address = 0x0600 + (*R* × 0x0004)]

Table 8-238. AID2_IQ_EFE_CHAN_AXC_OFFSET

Offset	Acronym	Register Description	Section
0x0600 + (*R* × 0x0004)	AID2 IQ EFE CHANNEL AXC OFFSET REG	Sets the AXC offset for each channel.	Section 8.5.3.1

8.5.3.1 AID2 IQ EFE CHANNEL AXC OFFSET REG [Address = 0x0600 + (*R* × 0x0004)]

Range (*R*) = 0:31

Sets the AXC offset for each channel.

Figure 8-210. AID2 IQ EFE CHANNEL AXC OFFSET REG

31	20	19	0
Reserved		AXC_OFFSET	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-239. AID2 IQ EFE CHANNEL AXC OFFSET REG Field Descriptions

Bits	Name	Description
31-20	Reserved	RESERVED
19-0	AXC_OFFSET	AxC-by-AxC delay control. Allows different timing alignments for each AxC. DIO & AID: this is a 4 sample offset relative to the group or TDM of AxC. AIL CPRI: this is a sample offset relative to the CPRI AxC Group. AIL OBSAI: this is a Radio Timer compare value (unit is sys_clk). Other than OBSAI, for most customer applications, these fields are programmed as zero.

8.5.4 AID2_IQ_EFE_FRM_SAMP_TC_MMR_RAM [Address = 0x0800 + (R × 0x0004)]

Table 8-240. AID2_IQ_EFE_FRM_SAMP_TC_MMR_RAM

Offset	Acronym	Register Description	Section
0x0800 + (*R* × 0x0004)	AID2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER	EFE AxC Radio Framing Sample Terminal Count Configuration Register	Section 8.5.4.1

8.5.4.1 AID2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER [Address = 0x0800 + (R × 0x0004)]

Range (*R*) = 0:255

EFE AxC Radio Framing Sample Terminal Count Configuration Register

Figure 8-211. AID2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER

31	18	17	0
Reserved		SAMP_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-241. AID2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-18	Reserved	Reserved
17-0	SAMP_TC	Radio Framing Counter. Number of samples (4 Bytes) per radio symbol programmed as a terminal count

8.5.5 AID2_IQ_EFE_CHAN_TDM_LUT [Address = 0x0C00 + (*R* × 0x0004)]

Table 8-242. AID2_IQ_EFE_CHAN_TDM_LUT

Offset	Acronym	Register Description	Section
0x0C00 + (*R* × 0x0004)	AID2 IQ EFE CHANNEL TDM LUT REG	EFE Channel TDM LUT configuration register	Section 8.5.5.1

8.5.5.1 AID2 IQ EFE CHANNEL TDM LUT REG [Address = 0x0C00 + (*R* × 0x0004)]

Range (*R*) = 0:255

EFE Channel TDM LUT configuration register

Figure 8-212. AID2 IQ EFE CHANNEL TDM LUT REG

31 9	8	7	6 0
Reserved	CHAN_INDEX_EN_CFG	Reserved	CHAN_INDEX_CFG
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-243. AID2 IQ EFE CHANNEL TDM LUT REG Field Descriptions

Bits	Name	Description
31-9	Reserved	Reserved
8	CHAN_INDEX_EN_CFG	TDM Channel Index LUT Enable
7	Reserved	Reserved
6-0	CHAN_INDEX_CFG	TDM Channel Index

8.5.6 AID2_IQ_EFE_RADIO_STANDARD_SCHEDULER_GROUP [Address = 0x1000]

Table 8-244. AID2_IQ_EFE_RADIO_STANDARD_SCHEDULER_GROUP

Offset	Acronym	Register Description	Section
0x1000	AID2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER	EFE Radio Standard Scheduler Configuration Register	Section 8.5.6.1

8.5.6.1 AID2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER [Address = 0x1000 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Radio Standard Scheduler Configuration Register

Figure 8-213. AID2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER

31	17	16	15	8	7	0
Reserved		TDM_EN	TDM_LEN		TDM_START	
NA-0		R/W-0	R/W-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-245. AID2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-17	Reserved	RESERVED
16	TDM_EN	EFE Scheduler Enable TDM • ENABLED (1) = TDM enabled for this radio standard • DISABLED (0) = TDM disabled for this radio standard
15-8	TDM_LEN	EFE Scheduler TDM Length
7-0	TDM_START	EFE Scheduler TDM Starting address in LUT

8.5.7 AID2_IQ_IFE_CHANNEL_CONFIGURATION_GROUP [Address = 0x2000]

Table 8-246. AID2_IQ_IFE_CHANNEL_CONFIGURATION_GROUP

Offset	Acronym	Register Description	Section
0x2000	AID2 IQ IFE CHANNEL CONFIGURATION REGISTER	IFE DMA Channel Configuration Register	Section 8.5.7.1

8.5.7.1 AID2 IQ IFE CHANNEL CONFIGURATION REGISTER [Address = 0x2000 + (*S* × 0x0004)]

Size (*S*) = 0:31

IFE DMA Channel Configuration Register

Figure 8-214. AID2 IQ IFE CHANNEL CONFIGURATION REGISTER

31 9	8	7	6 4	3 2	1	0
Reserved	CHAN_TDD_FRC_OFF	Reserved	CHAN_RADIO_SEL	CHAN_AXC_OFFSET	Reserved	CHAN_EN
NA-0	R/W-0	NA-0	R/W-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-247. AID2 IQ IFE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	CHAN_TDD_FRC_OFF	Forces a channel into the TDD OFF state on the next symbol after it is set to a 1 regardless of the TDD configuration of the radio standard variant the channel is assigned to. • FRC_SYM_OFF (1) = Force symbols off • NO_FRC_OFF_SYM (0) = No forcing off of symbols
7	Reserved	RESERVED
6-4	CHAN_RADIO_SEL	Radio Standard Select for channel • RS0 (0) = Radio Standard 0 • RS1 (1) = Radio Standard 1 • RS2 (2) = Radio Standard 2 • RS3 (3) = Radio Standard 3 • RS4 (4) = Radio Standard 4 • RS5 (5) = Radio Standard 5 • RS6 (6) = Radio Standard 6 • RS7 (7) = Radio Standard 7
3-2	CHAN_AXC_OFFSET	Fine AxC Offset within Quad Word • NONE (0) = No offset • ONE (1) = One sample offset • TWO (2) = Two sample offset • THREE (3) = Three sample offset
1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.5.8 AID2_IQ_IFE_RADIO_STANDARD_GROUP [Address = 0x2200]

Table 8-248. AID2_IQ_IFE_RADIO_STANDARD_GROUP

Offset	Acronym	Register Description	Section
0x2200	AID2 IQ IFE FRAME COUNT REGISTER	IFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants	Section 8.5.8.1
0x2220	AID2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER	IFE Radio Standard Configuration Register	Section 8.5.8.2
0x2240	AID2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.3
0x2260	AID2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.4
0x2280	AID2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.5
0x22A0	AID2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.6
0x22C0	AID2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.7
0x22E0	AID2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.8
0x2300	AID2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.9
0x2320	AID2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.5.8.10

8.5.8.1 AID2 IQ IFE FRAME COUNT REGISTER [Address = 0x2200 + (*S* × 0x0004)]

Size (*S*) = 0:7

IFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants

Figure 8-215. AID2 IQ IFE FRAME COUNT REGISTER

31 24	23 16	15 8	7 0
Reserved	INDEX_TC	INDEX_SC	SYM_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-249. AID2 IQ IFE FRAME COUNT REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	INDEX_TC	Radio Framing Counter. Index Counter Terminal Count. Index counter terminal count which is the last value of the Index Counter before it wraps. For simple use case, program same as frm_sym_tc.
15-8	INDEX_SC	Radio Framing Counter. Index Counter Starting Location. Starting location of the Sample Terminal Count LUT loaded into the Index Counter when it first starts and each time it wraps.
7-0	SYM_TC	Radio Framing Counter. Symbol Count. Number of symbols per frame programmed as a terminal count.

8.5.8.2 AID2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER [Address = 0x2220 + (*S* × 0x0004)]

Size (*S*) = 0:7

IFE Radio Standard Configuration Register

Figure 8-216. AID2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER

31	1	0
Reserved		TDD_LUT_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-250. AID2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	TDD_LUT_EN	Enable TDD • ENABLED (1) = TDD enabled for this radio standard • DISABLED (0) = TDD disabled for this radio standard

8.5.8.3 AID2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT [Address = 0x2240 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-217. AID2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-251. AID2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.4 AID2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT [Address = 0x2260 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-218. AID2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-252. AID2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.5 AID2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT [Address = 0x2280 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-219. AID2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-253. AID2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.6 AID2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT [Address = 0x22A0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-220. AID2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-254. AID2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.7 AID2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT [Address = 0x22C0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-221. AID2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-255. AID2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.8 AID2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT [Address = 0x22E0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-222. AID2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-256. AID2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.9 AID2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT [Address = 0x2300 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-223. AID2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-257. AID2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.8.10 AID2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT [Address = 0x2320 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-224. AID2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-258. AID2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.5.9 AID2_IQ_IFE_CONFIG_GROUP [Address = 0x2340]

Table 8-259. AID2_IQ_IFE_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x2340	AID2 IQ IFE GLOBAL ENABLE SET REG	Set Global Enable for IFE	Section 8.5.9.1
0x2344	AID2 IQ IFE GLOBAL ENABLE CLEAR REG	Clear Global Enable for IFE	Section 8.5.9.2
0x2348	AID2 IQ IFE GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, IFE may still be closing out packets.	Section 8.5.9.3
0x2350	AID2 IQ IFE CHANNEL ON STATUS REG	Gives current On/Off Status of every available AxC stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.5.9.4
0x2360	AID2 IQ IFE IN PACKET STATUS REGISTERS	Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP.	Section 8.5.9.5

8.5.9.1 AID2 IQ IFE GLOBAL ENABLE SET REG [Address = 0x2340]

Set Global Enable for IFE

Figure 8-225. AID2 IQ IFE GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-260. AID2 IQ IFE GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.5.9.2 AID2 IQ IFE GLOBAL ENABLE CLEAR REG [Address = 0x2344]

Clear Global Enable for IFE

Figure 8-226. AID2 IQ IFE GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-261. AID2 IQ IFE GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.5.9.3 AID2 IQ IFE GLOBAL ENABLE STATUS [Address = 0x2348]

Read Only status of global enable state. Even if this register is OFF, IFE may still be closing out packets.

Figure 8-227. AID2 IQ IFE GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-262. AID2 IQ IFE GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ife_ON 0x0:ife_OFF

8.5.9.4 AID2 IQ IFE CHANNEL ON STATUS REG [Address = 0x2350]

Gives current On/Off Status of every available AxC stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-228. AID2 IQ IFE CHANNEL ON STATUS REG

31	0
CHAN_ON	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-263. AID2 IQ IFE CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.5.9.5 AID2 IQ IFE IN PACKET STATUS REGISTERS [Address = 0x2360]

Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP.

Figure 8-229. AID2 IQ IFE IN PACKET STATUS REGISTERS

31	0
IN_PKT	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-264. AID2 IQ IFE IN PACKET STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-0	IN_PKT	0x1: IN_PKT 0x0:OUT_PKT

8.5.10 AID2_IQ_IDC_GENERAL_STATUS_GROUP [Address = 0x2384]

Table 8-265. AID2_IQ_IDC_GENERAL_STATUS_GROUP

Offset	Acronym	Register Description	Section
0x2384	AID2 IQ IDC STATUS REGISTER	IDC Status register.	Section 8.5.10.1
0x2390	AID2 IQ IDC IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the IFE	Section 8.5.10.2

8.5.10.1 AID2 IQ IDC STATUS REGISTER [Address = 0x2384]

IDC Status register.

Figure 8-230. AID2 IQ IDC STATUS REGISTER

31	1	0
Reserved		EMPTY
NA-0		R-0x0001

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-266. AID2 IQ IDC STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EMPTY	Empty indicator for IDC internal FIFOs • FIFO_NOT_EMPTY (0) = FIFOs are not empty • FIFO_EMPTY (1) = FIFOs are empty

8.5.10.2 AID2 IQ IDC IN PACKET STATUS REGISTER [Address = 0x2390]

Indicates when a channel is actively receiving a packet from the IFE

Figure 8-231. AID2 IQ IDC IN PACKET STATUS REGISTER

31	0
INPKT	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-267. AID2 IQ IDC IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-0	INPKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[15] is associated with channel 15

8.5.11 AID2_IQ_IDC_CONFIGURATION_GROUP [Address = 0x23C0]

Table 8-268. AID2_IQ_IDC_CONFIGURATION_GROUP

Offset	Acronym	Register Description	Section
0x23C0	AID2 IQ IDC CONFIGURATION REGISTER	IDC Configuration Register	Section 8.5.11.1

8.5.11.1 AID2 IQ IDC CONFIGURATION REGISTER [Address = 0x23C0]

IDC Configuration Register

Figure 8-232. AID2 IQ IDC CONFIGURATION REGISTER

31	2	1	0
Reserved		FRC_OFF_ALL	FAIL_MARK_ONLY
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-269. AID2 IQ IDC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved
1	FRC_OFF_ALL	Forces off all Ingress channels without waiting for an end of symbol or time slot. All open packets are automatically closed by creating an EOP for each open packet • FRC_OFF (1) = Force all channels off and close all open packets • NOP (0) = No effect
0	FAIL_MARK_ONLY	Controls how the IDC handles packet errors detected by IFE • DROP (0) = Drop Error packets • MARK (1) = Only Mark Packets With Errors

8.5.12 AID2_IQ_IDC_CHANNEL_CONFIG_GROUP [Address = 0x2400]

Table 8-270. AID2_IQ_IDC_CHANNEL_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x2400	AID2 IQ IDC CHANNEL CONFIGURATION REGISTERS	IDC Channel configuration registers.	Section 8.5.12.1

8.5.12.1 AID2 IQ IDC CHANNEL CONFIGURATION REGISTERS [Address = 0x2400 + (*S* × 0x0004)]

Size (*S*) = 0:31

IDC Channel configuration registers.

Figure 8-233. AID2 IQ IDC CHANNEL CONFIGURATION REGISTERS

31 25	24	23 21	20 16	15 6	5 4	3 2	1 0
Reserved	CHAN_FRC_OFF	Reserved	PKT_TYPE	Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-271. AID2 IQ IDC CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24	CHAN_FRC_OFF	Forces off all channel without waiting for an end of symbol or time slot. If channel has an open packet it is automatically closed by creating an EOP • FRC_OFF (0) = Force off channel and close an existing open packet • NOP (1) = No effect
23-21	Reserved	RESERVED
20-16	PKT_TYPE	Programmable packet type that is inserted into pkt_type field of PKTDMA Info Word 0.
15-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.5.13 AID2_IFE_FRM_SAMP_TC_MMR_RAM [Address = 0x2800 + (R × 0x0004)]

Table 8-272. AID2_IFE_FRM_SAMP_TC_MMR_RAM

Offset	Acronym	Register Description	Section
0x2800 + (*R* × 0x0004)	AID2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER	IFE AxC Framing Sample Terminal Count Configuration Register	Section 8.5.13.1

8.5.13.1 AID2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER [Address = 0x2800 + (*R* × 0x0004)]

Range (*R*) = 0:255

IFE AxC Framing Sample Terminal Count Configuration Register

Figure 8-234. AID2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER

31	18	17	0
Reserved		SAMP_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-273. AID2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-18	Reserved	Reserved
17-0	SAMP_TC	Radio Framing Counter. Number of samples (4 Bytes) per radio symbol programmed as a terminal count

8.5.14 AID2_ECTL_PKT_IF [Address = 0x3000]

Table 8-274. AID2_ECTL_PKT_IF

Offset	Acronym	Register Description	Section
0x3000	AID2 ECTL GLOBAL ENABLE SET REG	Set Global Enable for ECTL	Section 8.5.14.1
0x3004	AID2 ECTL GLOBAL ENABLE CLEAR REG	Clear Global Enable for ECTL	Section 8.5.14.2
0x3008	AID2 ECTL GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, ECTL may still be closing out packets.	Section 8.5.14.3
0x3100	AID2 ECTL CHANNEL ON STATUS REG	Gives current On/Off Status of every available CPRI control stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.5.14.4
0x3140	AID2 ECTL IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the ECTL	Section 8.5.14.5
0x3200	AID2 ECTL CHANNEL ENABLE CONFIGURATION REGISTER	ECTL Channel Configuration Enable Register	Section 8.5.14.6
0x3400	AID2 ECTL DB THRESHOLD REGISTER	ECTL Database Threshold Register	Section 8.5.14.7

8.5.14.1 AID2 ECTL GLOBAL ENABLE SET REG [Address = 0x3000]

Set Global Enable for ECTL

Figure 8-235. AID2 ECTL GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-275. AID2 ECTL GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.5.14.2 AID2 ECTL GLOBAL ENABLE CLEAR REG [Address = 0x3004]

Clear Global Enable for ECTL

Figure 8-236. AID2 ECTL GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-276. AID2 ECTL GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.5.14.3 AID2 ECTL GLOBAL ENABLE STATUS [Address = 0x3008]

Read Only status of global enable state. Even if this register is OFF, ECTL may still be closing out packets.

Figure 8-237. AID2 ECTL GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-277. AID2 ECTL GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ectl_ON 0x0:ectl_OFF

8.5.14.4 AID2 ECTL CHANNEL ON STATUS REG [Address = 0x3100]

Gives current On/Off Status of every available CPRI control stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-238. AID2 ECTL CHANNEL ON STATUS REG

31	16	15	0
Reserved		CHAN_ON	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-278. AID2 ECTL CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.5.14.5 AID2 ECTL IN PACKET STATUS REGISTER [Address = 0x3140]

Indicates when a channel is actively receiving a packet from the ECTL

Figure 8-239. AID2 ECTL IN PACKET STATUS REGISTER

31	16	15	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-279. AID2 ECTL IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	IN_PKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[3] is associated with channel 3

8.5.14.6 AID2 ECTL CHANNEL ENABLE CONFIGURATION REGISTER [Address = 0x3200 + (*S* × 0x0004)]

Size (*S*) = 0:15

ECTL Channel Configuration Enable Register

Figure 8-240. AID2 ECTL CHANNEL ENABLE CONFIGURATION REGISTER

31	1	0
Reserved		CHAN_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-280. AID2 ECTL CHANNEL ENABLE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.5.14.7 AID2 ECTL DB THRESHOLD REGISTER [Address = 0x3400 + (*S* × 0x0004)]

Size (*S*) = 0:15

ECTL Database Threshold Register

Figure 8-241. AID2 ECTL DB THRESHOLD REGISTER

31	2	1	0
Reserved		CHANNEL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-281. AID2 ECTL DB THRESHOLD REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved
1-0	CHANNEL	Data Buffer Threshold value before indicating data available per channel. Unit is QWD and normally set to zero

8.5.15 AID2_ICTL_IDC_IF [Address = 0x4000]

Table 8-282. AID2_ICTL_IDC_IF

Offset	Acronym	Register Description	Section
0x4000	AID2 ICTL CHANNEL CONFIGURATION REGISTERS	Per-channel configuration registers.	Section 8.5.15.1
0x4200	AID2 ICTL CONFIGURATION REGISTER	ICTL Configuration Register	Section 8.5.15.2
0x4204	AID2 ICTL STATUS REGISTER	ICTL Status register.	Section 8.5.15.3
0x4210	AID2 ICTL IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the ICTL	Section 8.5.15.4

8.5.15.1 AID2 ICTL CHANNEL CONFIGURATION REGISTERS [Address = 0x4000 + (*S* × 0x0004)]

Size (*S*) = 0:15

Per-channel configuration registers.

Figure 8-242. AID2 ICTL CHANNEL CONFIGURATION REGISTERS

31 25	24	23 21	20 16	15 6	5 4	3 2	1 0
Reserved	CHAN_FRC_OFF	Reserved	PKT_TYPE	Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-283. AID2 ICTL CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24	CHAN_FRC_OFF	Forces off all channel without waiting for an EOP. If channel has an open packet it is automatically closed by creating an EOP • FRC_OFF (0) = Force off channel and close an existing open packet • NOP (1) = No effect
23-21	Reserved	RESERVED
20-16	PKT_TYPE	Programmable packet type that is inserted into pkt_type field of PKTDMA Info Word 0.
15-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.5.15.2 AID2 ICTL CONFIGURATION REGISTER [Address = 0x4200]

ICTL Configuration Register

Figure 8-243. AID2 ICTL CONFIGURATION REGISTER

31	2	1	0
Reserved		FRC_OFF_ALL	FAIL_MARK_ONLY
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-284. AID2 ICTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved
1	FRC_OFF_ALL	Forces off all Ingress channels without waiting for an EOP. All open packets are automatically closed by creating an EOP for each open packet • FRC_OFF (1) = Force all channels off and close all open packets • NOP (0) = No effect
0	FAIL_MARK_ONLY	Controls how the ICTL handles packet errors detected by ICTL • DROP (0) = Drop Error Packets • MARK (1) = Only Mark Packets With Errors

8.5.15.3 AID2 ICTL STATUS REGISTER [Address = 0x4204]

ICTL Status register.

Figure 8-244. AID2 ICTL STATUS REGISTER

31	1	0
Reserved		EMPTY
NA-0		R-0x0001

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-285. AID2 ICTL STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EMPTY	Empty indicator for ICTL internal FIFOs • FIFO_NOT_EMPTY (0) = FIFOs are not empty • FIFO_EMPTY (1) = FIFOs are empty

8.5.15.4 AID2 ICTL IN PACKET STATUS REGISTER [Address = 0x4210]

Indicates when a channel is actively receiving a packet from the ICTL

Figure 8-245. AID2 ICTL IN PACKET STATUS REGISTER

31	16	15	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-286. AID2 ICTL IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	IN_PKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[3] is associated with channel 3

8.5.16 AID2_ICTL_PKT_IF [Address = 0x4280]

Table 8-287. AID2_ICTL_PKT_IF

Offset	Acronym	Register Description	Section
0x4280	AID2 ICTL GLOBAL ENABLE SET REG	Set Global Enable for ICTL	Section 8.5.16.1
0x4284	AID2 ICTL GLOBAL ENABLE CLEAR REG	Clear Global Enable for ICTL	Section 8.5.16.2
0x4288	AID2 ICTL GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, ICTL may still be closing out packets.	Section 8.5.16.3
0x42A0	AID2 ICTL CHANNEL ON STATUS REG	Gives current On/Off Status of every available stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.5.16.4
0x4400	AID2 ICTL CHANNEL ENABLE CONFIGURATION REGISTER	ICTL Channel Configuration Enable Register	Section 8.5.16.5

8.5.16.1 AID2 ICTL GLOBAL ENABLE SET REG [Address = 0x4280]

Set Global Enable for ICTL

Figure 8-246. AID2 ICTL GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-288. AID2 ICTL GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.5.16.2 AID2 ICTL GLOBAL ENABLE CLEAR REG [Address = 0x4284]

Clear Global Enable for ICTL

Figure 8-247. AID2 ICTL GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-289. AID2 ICTL GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.5.16.3 AID2 ICTL GLOBAL ENABLE STATUS [Address = 0x4288]

Read Only status of global enable state. Even if this register is OFF, ICTL may still be closing out packets.

Figure 8-248. AID2 ICTL GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-290. AID2 ICTL GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ictl_ON 0x0:ictl_OFF

8.5.16.4 AID2 ICTL CHANNEL ON STATUS REG [Address = 0x42A0]

Gives current On/Off Status of every available stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-249. AID2 ICTL CHANNEL ON STATUS REG

31	16	15	0
Reserved		CHAN_ON	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-291. AID2 ICTL CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.5.16.5 AID2 ICTL CHANNEL ENABLE CONFIGURATION REGISTER [Address = 0x4400 + (*S* × 0x0004)]

Size (*S*) = 0:15

ICTL Channel Configuration Enable Register

Figure 8-250. AID2 ICTL CHANNEL ENABLE CONFIGURATION REGISTER

31	1	0
Reserved		CHAN_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-292. AID2 ICTL CHANNEL ENABLE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.5.17 AID2_UAT_GEN_CTL [Address = 0x5000]

Table 8-293. AID2_UAT_GEN_CTL

Offset	Acronym	Register Description	Section
0x5000	AID2 UAT CONFIG REGISTER	This register simply starts the uAT timers running. It is implied that SW is unable to precisely time the start of timers. The intent is for the SW to correct the timers by later writting to the offset register of each timer.	Section 8.5.17.1
0x5004	AID2 UAT BCN TERMINAL COUNT REGISTER	UAT BCN terminal count Register	Section 8.5.17.2
0x5008	AID2 UAT BCN OFFSET REGISTER	UAT BCN offset Register	Section 8.5.17.3
0x500C	AID2 UAT SYNC BCN CAPTURE REGISTER	UAT SYNC BCN capture Register	Section 8.5.17.4

8.5.17.1 AID2 UAT CONFIG REGISTER [Address = 0x5000]

This register simply starts the uAT timers running. It is implied that SW is unable to precisely time the start of timers. The intent is for the SW to correct the timers by later writting to the offset register of each timer.

Figure 8-251. AID2 UAT CONFIG REGISTER

31	2	1	0
Reserved		DIAG_SYNC	UAT_RUN
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-294. AID2 UAT CONFIG REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	RESERVED
1	DIAG_SYNC	diag_sync = 1 starts the BCN and RAD counters if uat_run is set and an AT sync is received. This is only used in simulation and for diagnostics
0	UAT_RUN	UAT run starts the BCN and RAD counters free running

8.5.17.2 AID2 UAT BCN TERMINAL COUNT REGISTER [Address = 0x5004]

UAT BCN terminal count Register

Figure 8-252. AID2 UAT BCN TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-295. AID2 UAT BCN TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT BCN terminal count. BCN counts from zero to this limit and wraps to zero. Program as 2,457,599 for sys_clk=245.76MHz and 3,071,999 for sys_clk=307.2MHz

8.5.17.3 AID2 UAT BCN OFFSET REGISTER [Address = 0x5008]

UAT BCN offset Register

Figure 8-253. AID2 UAT BCN OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-296. AID2 UAT BCN OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	Offset correction to the raw uAT BCN counter. Used to correct the alignment of the local uAT BCN to the master AT2 BCN. BCN is initially randomly started. SW uses uat_sync_bcn_capture_sts rd_val to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.5.17.4 AID2 UAT SYNC BCN CAPTURE REGISTER [Address = 0x500C]

UAT SYNC BCN capture Register

Figure 8-254. AID2 UAT SYNC BCN CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-297. AID2 UAT SYNC BCN CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	uAT raw BCN value captured each frame boundary of AT2 master BCN. Used to calculate uAT BCN offset value for the purpose of aligning uAT to AT2 BCN.

8.5.18 AID2_UAT_EGR_RADT [Address = 0x5080 + (R × 0x0010)]

Table 8-298. AID2_UAT_EGR_RADT

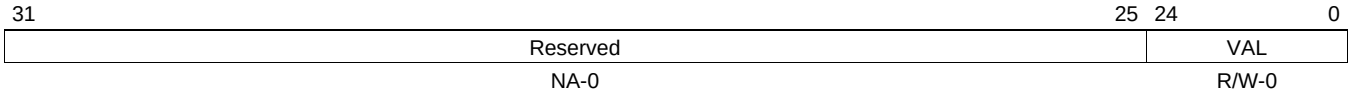
Offset	Acronym	Register Description	Section
0x5080 + (*R* × 0x0010)	AID2 UAT RADT TERMINAL COUNT REGISTER	UAT RADT terminal count Register	Section 8.5.18.1
0x5084 + (*R* × 0x0010)	AID2 UAT RADT OFFSET REGISTER	UAT RADT offset Register	Section 8.5.18.2
0x5088 + (*R* × 0x0010)	AID2 UAT SYNC RADT CAPTURE REGISTER	UAT SYNC RADT capture Register	Section 8.5.18.3

8.5.18.1 AID2 UAT RADT TERMINAL COUNT REGISTER [Address = 0x5080 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT terminal count Register

Figure 8-255. AID2 UAT RADT TERMINAL COUNT REGISTER



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-299. AID2 UAT RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.5.18.2 AID2 UAT RADT OFFSET REGISTER [Address = 0x5084 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT offset Register

Figure 8-256. AID2 UAT RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-300. AID2 UAT RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.5.18.3 AID2 UAT SYNC RADT CAPTURE REGISTER [Address = 0x5088 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT SYNC RADT capture Register

Figure 8-257. AID2 UAT SYNC RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-301. AID2 UAT SYNC RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	UAT RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.5.19 AID2_UAT_ING_RADT [Address = 0x5100 + (*R* × 0x0010)]

Table 8-302. AID2_UAT_ING_RADT

Offset	Acronym	Register Description	Section
0x5100 + (*R* × 0x0010)	AID2 UAT RADT TERMINAL COUNT REGISTER	UAT RADT terminal count Register	Section 8.5.19.1
0x5104 + (*R* × 0x0010)	AID2 UAT RADT OFFSET REGISTER	UAT RADT offset Register	Section 8.5.19.2
0x5108 + (*R* × 0x0010)	AID2 UAT SYNC RADT CAPTURE REGISTER	UAT SYNC RADT capture Register	Section 8.5.19.3

8.5.19.1 AID2 UAT RADT TERMINAL COUNT REGISTER [Address = 0x5100 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT terminal count Register

Figure 8-258. AID2 UAT RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-303. AID2 UAT RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.5.19.2 AID2 UAT RADT OFFSET REGISTER [Address = 0x5104 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT offset Register

Figure 8-259. AID2 UAT RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-304. AID2 UAT RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.5.19.3 AID2 UAT SYNC RADT CAPTURE REGISTER [Address = 0x5108 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT SYNC RADT capture Register

Figure 8-260. AID2 UAT SYNC RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-305. AID2 UAT SYNC RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	UAT RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.5.20 AID2_UAT_RADT_EVT [Address = 0x5200 + (R × 0x0008)]

Table 8-306. AID2_UAT_RADT_EVT

Offset	Acronym	Register Description	Section
0x5200 + (*R* × 0x0008)	AID2 UAT RADT EVENT COMPARE REGISTER	UAT RADT event compare Register per RADT. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress	Section 8.5.20.1
0x5204 + (*R* × 0x0008)	AID2 UAT RADT EVENT CLOCK COUNT TC REGISTER	UAT RADT event clock counter terminal count Register per RADT	Section 8.5.20.2

8.5.20.1 AID2 UAT RADT EVENT COMPARE REGISTER [Address = 0x5200 + (R × 0x0008)]

Range (*R*) = 0:21

UAT RADT event compare Register per RADT. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

Figure 8-261. AID2 UAT RADT EVENT COMPARE REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-307. AID2 UAT RADT EVENT COMPARE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT event compare per RADT. When compare value equals RADT count, frame rate event is generated. Also periodic event (i.e. 4SAMP) is started. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

8.5.20.2 AID2 UAT RADT EVENT CLOCK COUNT TC REGISTER [Address = 0x5204 + (*R* × 0x0008)]

Range (*R*) = 0:21

UAT RADT event clock counter terminal count Register per RADT

Figure 8-262. AID2 UAT RADT EVENT CLOCK COUNT TC REGISTER

31	16	15	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-308. AID2 UAT RADT EVENT CLOCK COUNT TC REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	VAL	UAT RADT event clock counter terminal count controls spacing of the periodic strobe (i.e. 4SAMP). Once the uat_evt_radt_cmp_cfg equals the RADT, the period strobe will fire and re-fire every time a clock counter reaches this terminal count. The The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

8.5.21 AID2_IQ_EDC_REGISTER_GROUP [Address = 0x8000]

Table 8-309. AID2_IQ_EDC_REGISTER_GROUP

Offset	Acronym	Register Description	Section
0x8000	AID2 IQ EDC CONFIGURATION REGISTER	EDC Configuration Register	Section 8.5.21.1
0x8004	AID2 IQ EDC SOP COUNTER STATUS REGISTER	Counts the number of SOPs seen by the IQ EDC	Section 8.5.21.2
0x8008	AID2 IQ EDC EOP COUNTER STATUS REGISTER	Counts the number of EOPs seen by the IQ EDC	Section 8.5.21.3
0x8080	AID2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER	EDC Status Occupancy counter for each channel register. User can ignore this (TI debug only)	Section 8.5.21.4
0x8200	AID2 IQ EDC CHANNEL CONFIGURATION REGISTERS	Per-channel configuration registers.	Section 8.5.21.5

8.5.21.1 AID2 IQ EDC CONFIGURATION REGISTER [Address = 0x8000]

EDC Configuration Register

Figure 8-263. AID2 IQ EDC CONFIGURATION REGISTER

31	1	0
Reserved		PSI_ERR_CHK_DISABLE
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-310. AID2 IQ EDC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	Reserved
0	PSI_ERR_CHK_DISABLE	Controls how the EDC handles packet errors detected by efe • DROP (0) = Drop the rest of the packet on errors • NO_DROP (1) = Do not drop packet on errors

8.5.21.2 AID2 IQ EDC SOP COUNTER STATUS REGISTER [Address = 0x8004]

Counts the number of SOPs seen by the IQ EDC

Figure 8-264. AID2 IQ EDC SOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-311. AID2 IQ EDC SOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	SOP_CNT	Count of the number of SOPs seen by the IQ EDC

8.5.21.3 AID2 IQ EDC EOP COUNTER STATUS REGISTER [Address = 0x8008]

Counts the number of EOPs seen by the IQ EDC

Figure 8-265. AID2 IQ EDC EOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-312. AID2 IQ EDC EOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	EOP_CNT	Count of the number of EOPs seen by the IQ EDC

8.5.21.4 AID2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER [Address = 0x8080 + (*S* × 0x0004)]

Size (*S*) = 0:7

EDC Status Occupancy counter for each channel register. User can ignore this (TI debug only)

Figure 8-266. AID2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER

31 24	23 16	15 8	7 0
OCC_CNTR_D	OCC_CNTR_C	OCC_CNTR_B	OCC_CNTR_A
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-313. AID2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	OCC_CNTR_D	Occupancy Counter for register D for this address
23-16	OCC_CNTR_C	Occupancy Counter for register C for this address
15-8	OCC_CNTR_B	Occupancy Counter for register B for this address
7-0	OCC_CNTR_A	Occupancy Counter for register A for this address

8.5.21.5 AID2 IQ EDC CHANNEL CONFIGURATION REGISTERS [Address = 0x8200 + (*S* × 0x0004)]

Size (*S*) = 0:31

Per-channel configuration registers.

Figure 8-267. AID2 IQ EDC CHANNEL CONFIGURATION REGISTERS

31 6	5 4	3 2	1 0
Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-314. AID2 IQ EDC CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.5.22 AID2_IQ_INGRESS_VBUS_MMR_GROUP [Address = 0xA000]

Table 8-315. AID2_IQ_INGRESS_VBUS_MMR_GROUP

Offset	Acronym	Register Description	Section
0xA000	AID2 IQ IDC RATE CONTROL CONFIGURATION REGISTER	IDC Rate Control Configuration register. Programmable rate control for OBSAI control word and generic packet mode	Section 8.5.22.1
0xA004	AID2 IQ IDC SOP COUNTER REGISTER	This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.5.22.2
0xA008	AID2 IQ IDC EOP COUNTER REGISTER	This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.5.22.3

8.5.22.1 AID2 IQ IDC RATE CONTROL CONFIGURATION REGISTER [Address = 0xA000]

IDC Rate Control Configuration register. Programmable rate control for OBSAI control word and generic packet mode

Figure 8-268. AID2 IQ IDC RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-316. AID2 IQ IDC RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the IDC to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the IDC to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.5.22.2 AID2 IQ IDC SOP COUNTER REGISTER [Address = 0xA004]

This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-269. AID2 IQ IDC SOP COUNTER REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-317. AID2 IQ IDC SOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	SOP_CNT	Wrapping count of SOPs sent on PSI.

8.5.22.3 AID2 IQ IDC EOP COUNTER REGISTER [Address = 0xA008]

This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-270. AID2 IQ IDC EOP COUNTER REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-318. AID2 IQ IDC EOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	EOP_CNT	Wrapping count of EOPs sent on PSI.

8.5.23 AID2_ECTL_REGISTER_GROUP [Address = 0xB000]

Table 8-319. AID2_ECTL_REGISTER_GROUP

Offset	Acronym	Register Description	Section
0xB000	AID2 ECTL RATE CONTROL CONFIGURATION REGISTER	ECTL Rate Control Configuration register. Programmable rate control for Rate Controller.	Section 8.5.23.1
0xB004	AID2 ECTL SOP COUNTER STATUS REGISTER	Counts the number of SOPs seen by the ECTL	Section 8.5.23.2
0xB008	AID2 ECTL EOP COUNTER STATUS REGISTER	Counts the number of EOPs seen by the ECTL	Section 8.5.23.3
0xB100	AID2 ECTL OCCUPANCY COUNTER STATUS REGISTER	ECTL Status Occupancy counter for each channel register. User can ignore this (TI debug only)	Section 8.5.23.4
0xB200	AID2 ECTL CHANNEL CONFIGURATION REGISTERS	ECTL Per-channel configuration registers.	Section 8.5.23.5

8.5.23.1 AID2 ECTL RATE CONTROL CONFIGURATION REGISTER [Address = 0xB000]

ECTL Rate Control Configuration register. Programmable rate control for Rate Controller.

Figure 8-271. AID2 ECTL RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-320. AID2 ECTL RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the ECTL to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the ICTL to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.5.23.2 AID2 ECTL SOP COUNTER STATUS REGISTER [Address = 0xB004]

Counts the number of SOPs seen by the ECTL

Figure 8-272. AID2 ECTL SOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-321. AID2 ECTL SOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	SOP_CNT	Count of the number of SOPs seen by the ECTL

8.5.23.3 AID2 ECTL EOP COUNTER STATUS REGISTER [Address = 0xB008]

Counts the number of EOPs seen by the ECTL

Figure 8-273. AID2 ECTL EOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-322. AID2 ECTL EOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	EOP_CNT	Count of the number of EOPs seen by the ECTL

8.5.23.4 AID2 ECTL OCCUPANCY COUNTER STATUS REGISTER [Address = 0xB100 + (*S* × 0x0004)]

Size (*S*) = 0:3

ECTL Status Occupancy counter for each channel register. User can ignore this (TI debug only)

Figure 8-274. AID2 ECTL OCCUPANCY COUNTER STATUS REGISTER

31 24	23 16	15 8	7 0
OCC_CNTR_D	OCC_CNTR_C	OCC_CNTR_B	OCC_CNTR_A
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-323. AID2 ECTL OCCUPANCY COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	OCC_CNTR_D	Occupancy Counter for register D for this address
23-16	OCC_CNTR_C	Occupancy Counter for register C for this address
15-8	OCC_CNTR_B	Occupancy Counter for register B for this address
7-0	OCC_CNTR_A	Occupancy Counter for register A for this address

8.5.23.5 AID2 ECTL CHANNEL CONFIGURATION REGISTERS [Address = 0xB200 + (*S* × 0x0004)]

Size (*S*) = 0:15

ECTL Per-channel configuration registers.

Figure 8-275. AID2 ECTL CHANNEL CONFIGURATION REGISTERS

31 6	5 4	3 2	1 0
Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-324. AID2 ECTL CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.5.24 AID2_CTL_INGRESS_VBUS_MMR_GROUP [Address = 0xC000]

Table 8-325. AID2_CTL_INGRESS_VBUS_MMR_GROUP

Offset	Acronym	Register Description	Section
0xC000	AID2 ICTL RATE CONTROL CONFIGURATION REGISTER	ICTL Rate Control Configuration register. Programmable rate control for Rate Controller.	Section 8.5.24.1
0xC004	AID2 ICTL SOP COUNTER REGISTER	This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.5.24.2
0xC008	AID2 ICTL EOP COUNTER REGISTER	This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.5.24.3

8.5.24.1 AID2 ICTL RATE CONTROL CONFIGURATION REGISTER [Address = 0xC000]

ICTL Rate Control Configuration register. Programmable rate control for Rate Controller.

Figure 8-276. AID2 ICTL RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-326. AID2 ICTL RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the ICTL to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the ICTL to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.5.24.2 AID2 ICTL SOP COUNTER REGISTER [Address = 0xC004]

This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-277. AID2 ICTL SOP COUNTER REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-327. AID2 ICTL SOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	SOP_CNT	Wrapping count of SOPs sent on PSI.

8.5.24.3 AID2 ICTL EOP COUNTER REGISTER [Address = 0xC008]

This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-278. AID2 ICTL EOP COUNTER REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-328. AID2 ICTL EOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	EOP_CNT	Wrapping count of EOPs sent on PSI.

8.5.25 AID2_IQN_AID2_EE_SYSCLK_EE [Address = 0x1_0000]

Table 8-329. AID2_IQN_AID2_EE_SYSCLK_EE

Offset	Acronym	Register Description	Section
0x1_0000	AID2 EE_SII_A RAW INTERRUPT STATUS	SI si_i IQ errors and info.	Section 8.5.25.1
0x1_0004	AID2 EE_SII_A RAW SET	Raw Set	Section 8.5.25.2
0x1_0008	AID2 EE_SII_A RAW CLEAR	Raw Clear	Section 8.5.25.3
0x1_000C	AID2 EE_SII_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.4
0x1_0010	AID2 EE_SII_A EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.5
0x1_0014	AID2 EE_SII_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.6
0x1_0018	AID2 EE_SII_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.7
0x1_001C	AID2 EE_SII_A EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.8
0x1_0020	AID2 EE_SII_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.9
0x1_0024	AID2 EE_SII_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.10
0x1_0028	AID2 EE_SII_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.11
0x1_002C	AID2 EE_SII_B RAW INTERRUPT STATUS	SI si_i CTL errors and info.	Section 8.5.25.12
0x1_0030	AID2 EE_SII_B RAW SET	Raw Set	Section 8.5.25.13
0x1_0034	AID2 EE_SII_B RAW CLEAR	Raw Clear	Section 8.5.25.14
0x1_0038	AID2 EE_SII_B EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.15
0x1_003C	AID2 EE_SII_B EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.16
0x1_0040	AID2 EE_SII_B EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.17
0x1_0044	AID2 EE_SII_B EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.18
0x1_0048	AID2 EE_SII_B EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.19
0x1_004C	AID2 EE_SII_B EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.20
0x1_0050	AID2 EE_SII_B EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.21
0x1_0054	AID2 EE_SII_B EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.22

Table 8-329. AID2_IQN_AID2_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_0058	AID2 EE_SII_C RAW INTERRUPT STATUS	SI si_i IQ per-channel start of frame errors	Section 8.5.25.23
0x1_005C	AID2 EE_SII_C RAW SET	Raw Set	Section 8.5.25.24
0x1_0060	AID2 EE_SII_C RAW CLEAR	Raw Clear	Section 8.5.25.25
0x1_0064	AID2 EE_SII_C EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.26
0x1_0068	AID2 EE_SII_C EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.27
0x1_006C	AID2 EE_SII_C EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.28
0x1_0070	AID2 EE_SII_C EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.29
0x1_0074	AID2 EE_SII_C EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.30
0x1_0078	AID2 EE_SII_C EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.31
0x1_007C	AID2 EE_SII_C EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.32
0x1_0080	AID2 EE_SII_C EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.33
0x1_0108	AID2 EE_SII_D RAW INTERRUPT STATUS	SI si_i CTL per-channel SOP received from ICC info	Section 8.5.25.34
0x1_010C	AID2 EE_SII_D RAW SET	Raw Set	Section 8.5.25.35
0x1_0110	AID2 EE_SII_D RAW CLEAR	Raw Clear	Section 8.5.25.36
0x1_0114	AID2 EE_SII_D EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.37
0x1_0118	AID2 EE_SII_D EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.38
0x1_011C	AID2 EE_SII_D EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.39
0x1_0120	AID2 EE_SII_D EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.40
0x1_0124	AID2 EE_SII_D EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.41
0x1_0128	AID2 EE_SII_D EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.42

Table 8-329. AID2_IQN_AID2_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_012C	AID2 EE_SII_D EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.43
0x1_0130	AID2 EE_SII_D EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.44
0x1_01B8	AID2 EE_SIE_A RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.5.25.45
0x1_01BC	AID2 EE_SIE_A RAW SET	Raw Set	Section 8.5.25.46
0x1_01C0	AID2 EE_SIE_A RAW CLEAR	Raw Clear	Section 8.5.25.47
0x1_01C4	AID2 EE_SIE_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.48
0x1_01C8	AID2 EE_SIE_A EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.49
0x1_01CC	AID2 EE_SIE_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.50
0x1_01D0	AID2 EE_SIE_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.51
0x1_01D4	AID2 EE_SIE_A EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.52
0x1_01D8	AID2 EE_SIE_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.53
0x1_01DC	AID2 EE_SIE_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.54
0x1_01E0	AID2 EE_SIE_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.55
0x1_01E4	AID2 EE_SIE_B RAW INTERRUPT STATUS	SI si_e CTL info.	Section 8.5.25.56
0x1_01E8	AID2 EE_SIE_B RAW SET	Raw Set	Section 8.5.25.57
0x1_01EC	AID2 EE_SIE_B RAW CLEAR	Raw Clear	Section 8.5.25.58
0x1_01F0	AID2 EE_SIE_B EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.59
0x1_01F4	AID2 EE_SIE_B EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.60
0x1_01F8	AID2 EE_SIE_B EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.61
0x1_01FC	AID2 EE_SIE_B EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.62

Table 8-329. AID2_IQN_AID2_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_0200	AID2 EE_SIE_B EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.63
0x1_0204	AID2 EE_SIE_B EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.64
0x1_0208	AID2 EE_SIE_B EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.65
0x1_020C	AID2 EE_SIE_B EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.66
0x1_0210	AID2 EE_SIE_C RAW INTERRUPT STATUS	SI si_e CTL per-channel SOP transmitted to ICC	Section 8.5.25.67
0x1_0214	AID2 EE_SIE_C RAW SET	Raw Set	Section 8.5.25.68
0x1_0218	AID2 EE_SIE_C RAW CLEAR	Raw Clear	Section 8.5.25.69
0x1_021C	AID2 EE_SIE_C EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.25.70
0x1_0220	AID2 EE_SIE_C EV0 ENABLE SET	EV0 Enable Set	Section 8.5.25.71
0x1_0224	AID2 EE_SIE_C EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.25.72
0x1_0228	AID2 EE_SIE_C EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.25.73
0x1_022C	AID2 EE_SIE_C EV1 ENABLE SET	EV1 Enable Set	Section 8.5.25.74
0x1_0230	AID2 EE_SIE_C EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.25.75
0x1_0234	AID2 EE_SIE_C EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.25.76
0x1_0238	AID2 EE_SIE_C EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.25.77
0x1_02C0	AID2 SYSCLK_ORIG_REG	This is the origination register indicating which interrupt register group caused the interrupt.	Section 8.5.25.78

8.5.25.1 AID2 EE_SII_A RAW INTERRUPT STATUS [Address = 0x1_0000]

SI si_i IQ errors and info.

Figure 8-279. AID2 EE_SII_A RAW INTERRUPT STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-330. AID2 EE_SII_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	SI Ingress IQ FIFO overflow error
4	SI_ING_IQ_IFE_DAT_INFO	SI Ingress IQ IFE transmitted valid data phase
3	SI_ING_IQ_IFE_EOP_INFO	SI Ingress IQ IFE transmitted EOP
2	SI_ING_IQ_IFE_SOP_INFO	SI Ingress IQ IFE transmitted SOP
1	SI_ING_IQ_ICC_DAT_INFO	SI Ingress IQ ICC data transfer received
0	SI_ING_IQ_ICC_SOF_INFO	SI Ingress IQ ICC Start of Frame received

8.5.25.2 AID2 EE_SII_A RAW SET [Address = 0x1_0004]

Raw Set

Figure 8-280. AID2 EE_SII_A RAW SET

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-331. AID2 EE_SII_A RAW SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.3 AID2 EE_SII_A RAW CLEAR [Address = 0x1_0008]

Raw Clear

Figure 8-281. AID2 EE_SII_A RAW CLEAR

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-332. AID2 EE_SII_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.4 AID2 EE_SII_A EV0 ENABLE STATUS [Address = 0x1_000C]

EV0 Enable Status

Figure 8-282. AID2 EE_SII_A EV0 ENABLE STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-333. AID2 EE_SII_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.5 AID2 EE_SII_A EV0 ENABLE SET [Address = 0x1_0010]

EV0 Enable Set

Figure 8-283. AID2 EE_SII_A EV0 ENABLE SET

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-334. AID2 EE_SII_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.6 AID2 EE_SII_A EV0 ENABLE CLEAR [Address = 0x1_0014]

EV0 Enable Clear

Figure 8-284. AID2 EE_SII_A EV0 ENABLE CLEAR

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-335. AID2 EE_SII_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.7 AID2 EE_SII_A EV1 ENABLE STATUS [Address = 0x1_0018]

EV1 Enable Status

Figure 8-285. AID2 EE_SII_A EV1 ENABLE STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
R-0	R-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-336. AID2 EE_SII_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.8 AID2 EE_SII_A EV1 ENABLE SET [Address = 0x1_001C]

EV1 Enable Set

Figure 8-286. AID2 EE_SII_A EV1 ENABLE SET

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-337. AID2 EE_SII_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.9 AID2 EE_SII_A EV1 ENABLE CLEAR [Address = 0x1_0020]

EV1 Enable Clear

Figure 8-287. AID2 EE_SII_A EV1 ENABLE CLEAR

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-338. AID2 EE_SII_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.10 AID2 EE_SII_A EV0 ENABLED STATUS [Address = 0x1_0024]

EV0 Enabled Status

Figure 8-288. AID2 EE_SII_A EV0 ENABLED STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
R-0	R-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-339. AID2 EE_SII_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.11 AID2 EE_SII_A EV1 ENABLED STATUS [Address = 0x1_0028]

EV1 Enabled Status

Figure 8-289. AID2 EE_SII_A EV1 ENABLED STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
R-0	R-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-340. AID2 EE_SII_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.12 AID2 EE_SII_B RAW INTERRUPT STATUS [Address = 0x1_002C]

SI si_i CTL errors and info.

Figure 8-290. AID2 EE_SII_B RAW INTERRUPT STATUS

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		R-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-341. AID2 EE_SII_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	SI Ingress CTL FIFO overflow error
2	SI_ING_CTL_ICC_DAT_INFO	SI Ingress CTL received valid data phase from ICC
1	SI_ING_CTL_ICC_EOP_INFO	SI Ingress CTL received EOP from ICC
0	SI_ING_CTL_PKT_ERR	SI Ingress CTL Packet error occurred

8.5.25.13 AID2 EE_SII_B RAW SET [Address = 0x1_0030]

Raw Set

Figure 8-291. AID2 EE_SII_B RAW SET

31	4	3		
Reserved		SI_ING_CTL_FIFO_OVFL_ERR		
NA-0		W-0		
	2	1		0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO		SI_ING_CTL_PKT_ERR
W-0		W-0		W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-342. AID2 EE_SII_B RAW SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.14 AID2 EE_SII_B RAW CLEAR [Address = 0x1_0034]

Raw Clear

Figure 8-292. AID2 EE_SII_B RAW CLEAR

31	4	3	
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	
NA-0		W-0	
2		1	0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-343. AID2 EE_SII_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.15 AID2 EE_SII_B EV0 ENABLE STATUS [Address = 0x1_0038]

EV0 Enable Status

Figure 8-293. AID2 EE_SII_B EV0 ENABLE STATUS

31	4	3	2	1	0
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
NA-0		R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-344. AID2 EE_SII_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_CTL_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.16 AID2 EE_SII_B EV0 ENABLE SET [Address = 0x1_003C]

EV0 Enable Set

Figure 8-294. AID2 EE_SII_B EV0 ENABLE SET

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		W-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

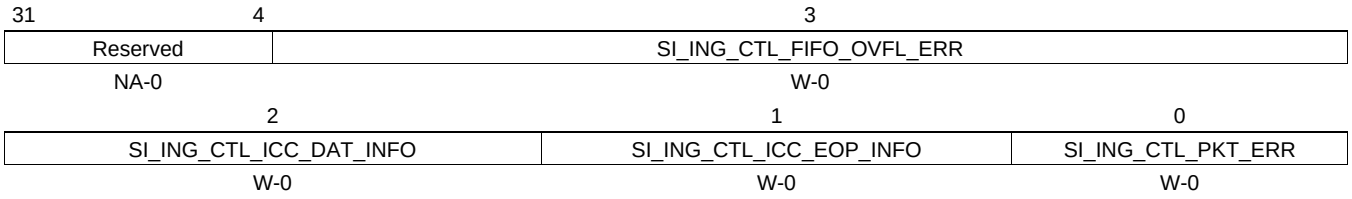
Table 8-345. AID2 EE_SII_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.17 AID2 EE_SII_B EV0 ENABLE CLEAR [Address = 0x1_0040]

EV0 Enable Clear

Figure 8-295. AID2 EE_SII_B EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-346. AID2 EE_SII_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.18 AID2 EE_SII_B EV1 ENABLE STATUS [Address = 0x1_0044]

EV1 Enable Status

Figure 8-296. AID2 EE_SII_B EV1 ENABLE STATUS

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		R-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-347. AID2 EE_SII_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_CTL_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.19 AID2 EE_SII_B EV1 ENABLE SET [Address = 0x1_0048]

EV1 Enable Set

Figure 8-297. AID2 EE_SII_B EV1 ENABLE SET

31	4	3		
Reserved		SI_ING_CTL_FIFO_OVFL_ERR		
NA-0		W-0		
	2	1		0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO		SI_ING_CTL_PKT_ERR
W-0		W-0		W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-348. AID2 EE_SII_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.20 AID2 EE_SII_B EV1 ENABLE CLEAR [Address = 0x1_004C]

EV1 Enable Clear

Figure 8-298. AID2 EE_SII_B EV1 ENABLE CLEAR

31	4	3	
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	
NA-0		W-0	
2		1	0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-349. AID2 EE_SII_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.21 AID2 EE_SII_B EV0 ENABLED STATUS [Address = 0x1_0050]

EV0 Enabled Status

Figure 8-299. AID2 EE_SII_B EV0 ENABLED STATUS

31	4	3	
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	
NA-0		R-0	
2		1	0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-350. AID2 EE_SII_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_CTL_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.22 AID2 EE_SII_B EV1 ENABLED STATUS [Address = 0x1_0054]

EV1 Enabled Status

Figure 8-300. AID2 EE_SII_B EV1 ENABLED STATUS

31	4	3	2	1	0
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
NA-0		R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

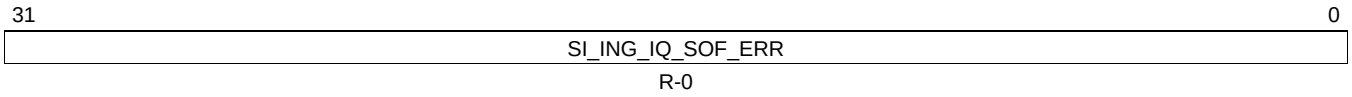
Table 8-351. AID2 EE_SII_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_CTL_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.23 AID2 EE_SII_C RAW INTERRUPT STATUS [Address = 0x1_0058]

SI si_i IQ per-channel start of frame errors

Figure 8-301. AID2 EE_SII_C RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-352. AID2 EE_SII_C RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	SI Ingress IQ per channel Start of Frame alignment error

8.5.25.24 AID2 EE_SII_C RAW SET [Address = 0x1_005C]

Raw Set

Figure 8-302. AID2 EE_SII_C RAW SET

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-353. AID2 EE_SII_C RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.25 AID2 EE_SII_C RAW CLEAR [Address = 0x1_0060]

Raw Clear

Figure 8-303. AID2 EE_SII_C RAW CLEAR

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-354. AID2 EE_SII_C RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.26 AID2 EE_SII_C EV0 ENABLE STATUS [Address = 0x1_0064]

EV0 Enable Status

Figure 8-304. AID2 EE_SII_C EV0 ENABLE STATUS

31	0
SI_ING_IQ_SOF_ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-355. AID2 EE_SII_C EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.27 AID2 EE_SII_C EV0 ENABLE SET [Address = 0x1_0068]

EV0 Enable Set

Figure 8-305. AID2 EE_SII_C EV0 ENABLE SET

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

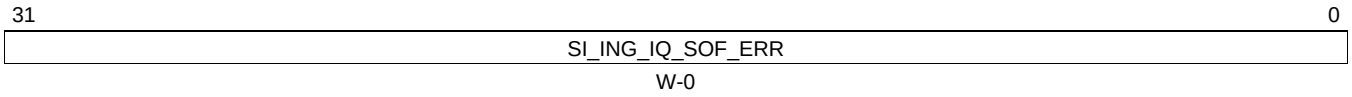
Table 8-356. AID2 EE_SII_C EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.28 AID2 EE_SII_C EV0 ENABLE CLEAR [Address = 0x1_006C]

EV0 Enable Clear

Figure 8-306. AID2 EE_SII_C EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

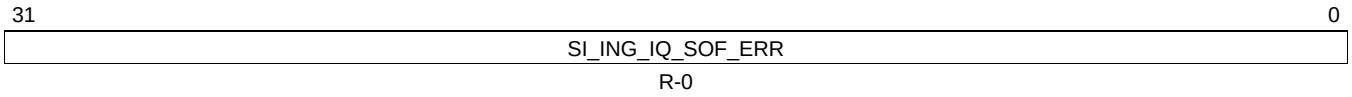
Table 8-357. AID2 EE_SII_C EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.29 AID2 EE_SII_C EV1 ENABLE STATUS [Address = 0x1_0070]

EV1 Enable Status

Figure 8-307. AID2 EE_SII_C EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-358. AID2 EE_SII_C EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.30 AID2 EE_SII_C EV1 ENABLE SET [Address = 0x1_0074]

EV1 Enable Set

Figure 8-308. AID2 EE_SII_C EV1 ENABLE SET

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

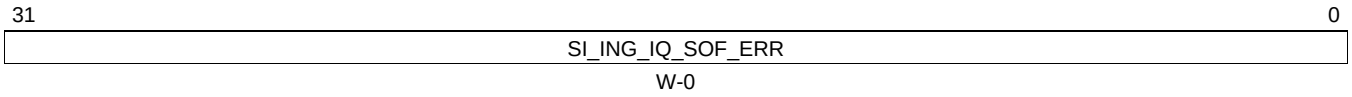
Table 8-359. AID2 EE_SII_C EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.31 AID2 EE_SII_C EV1 ENABLE CLEAR [Address = 0x1_0078]

EV1 Enable Clear

Figure 8-309. AID2 EE_SII_C EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-360. AID2 EE_SII_C EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.32 AID2 EE_SII_C EV0 ENABLED STATUS [Address = 0x1_007C]

EV0 Enabled Status

Figure 8-310. AID2 EE_SII_C EV0 ENABLED STATUS

31	0
SI_ING_IQ_SOF_ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-361. AID2 EE_SII_C EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.33 AID2 EE_SII_C EV1 ENABLED STATUS [Address = 0x1_0080]

EV1 Enabled Status

Figure 8-311. AID2 EE_SII_C EV1 ENABLED STATUS

31	0
SI_ING_IQ_SOF_ERR	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-362. AID2 EE_SII_C EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.34 AID2 EE_SII_D RAW INTERRUPT STATUS [Address = 0x1_0108]

SI si_i CTL per-channel SOP received from ICC info

Figure 8-312. AID2 EE_SII_D RAW INTERRUPT STATUS

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-363. AID2 EE_SII_D RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	SI Ingress CTL per channel SOP received from ICC

8.5.25.35 AID2 EE_SII_D RAW SET [Address = 0x1_010C]

Raw Set

Figure 8-313. AID2 EE_SII_D RAW SET

31 16	15 0
Reserved	SI_ING_CTL_ICC_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-364. AID2 EE_SII_D RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.36 AID2 EE_SII_D RAW CLEAR [Address = 0x1_0110]

Raw Clear

Figure 8-314. AID2 EE_SII_D RAW CLEAR

31 16	15 0
Reserved	SI_ING_CTL_ICC_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-365. AID2 EE_SII_D RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.37 AID2 EE_SII_D EV0 ENABLE STATUS [Address = 0x1_0114]

EV0 Enable Status

Figure 8-315. AID2 EE_SII_D EV0 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-366. AID2 EE_SII_D EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.38 AID2 EE_SII_D EV0 ENABLE SET [Address = 0x1_0118]

EV0 Enable Set

Figure 8-316. AID2 EE_SII_D EV0 ENABLE SET

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-367. AID2 EE_SII_D EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.39 AID2 EE_SII_D EV0 ENABLE CLEAR [Address = 0x1_011C]

EV0 Enable Clear

Figure 8-317. AID2 EE_SII_D EV0 ENABLE CLEAR

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-368. AID2 EE_SII_D EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.40 AID2 EE_SII_D EV1 ENABLE STATUS [Address = 0x1_0120]

EV1 Enable Status

Figure 8-318. AID2 EE_SII_D EV1 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-369. AID2 EE_SII_D EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.41 AID2 EE_SII_D EV1 ENABLE SET [Address = 0x1_0124]

EV1 Enable Set

Figure 8-319. AID2 EE_SII_D EV1 ENABLE SET

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-370. AID2 EE_SII_D EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.42 AID2 EE_SII_D EV1 ENABLE CLEAR [Address = 0x1_0128]

EV1 Enable Clear

Figure 8-320. AID2 EE_SII_D EV1 ENABLE CLEAR

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-371. AID2 EE_SII_D EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.43 AID2 EE_SII_D EV0 ENABLED STATUS [Address = 0x1_012C]

EV0 Enabled Status

Figure 8-321. AID2 EE_SII_D EV0 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-372. AID2 EE_SII_D EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.44 AID2 EE_SII_D EV1 ENABLED STATUS [Address = 0x1_0130]

EV1 Enabled Status

Figure 8-322. AID2 EE_SII_D EV1 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-373. AID2 EE_SII_D EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.45 AID2 EE_SIE_A RAW INTERRUPT STATUS [Address = 0x1_01B8]

SI si_e IQ errors and info.

Figure 8-323. AID2 EE_SIE_A RAW INTERRUPT STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-374. AID2 EE_SIE_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	SI Egress IQ transmitted data to ICC
3	SI_EGR_IQ_ICC_SOF_INFO	SI Egress IQ transmitted Start of Frame to ICC
2	SI_EGR_IQ_EFE_SYM_ERR	SI Egress IQ EFE symbol number error. (Packet boundary errors due to a missing, early, or late SOP disable the reporting of any symbol errors since the symbol number is only valid for SOPs)
1	SI_EGR_IQ_EFE_PKT_ERR	SI Egress IQ EFE packet boundary error
0	SI_EGR_IQ_EFE_STARVE_ERR	SI Egress IQ EFE data starvation error

8.5.25.46 AID2 EE_SIE_A RAW SET [Address = 0x1_01BC]

Raw Set

Figure 8-324. AID2 EE_SIE_A RAW SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-375. AID2 EE_SIE_A RAW SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.47 AID2 EE_SIE_A RAW CLEAR [Address = 0x1_01C0]

Raw Clear

Figure 8-325. AID2 EE_SIE_A RAW CLEAR

31 5	4	3
Reserved	SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0	W-0	W-0
2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

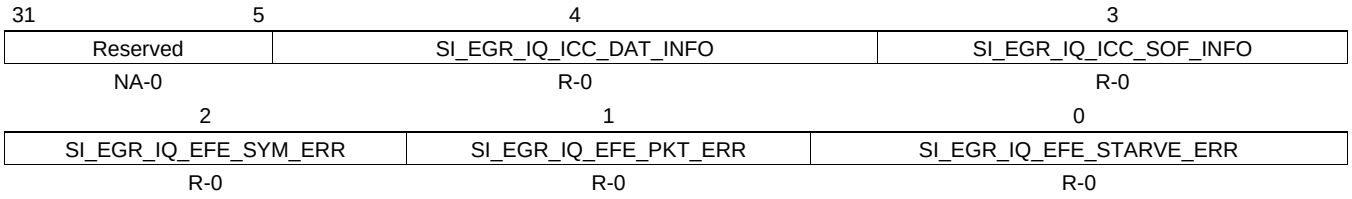
Table 8-376. AID2 EE_SIE_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.48 AID2 EE_SIE_A EV0 ENABLE STATUS [Address = 0x1_01C4]

EV0 Enable Status

Figure 8-326. AID2 EE_SIE_A EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-377. AID2 EE_SIE_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.49 AID2 EE_SIE_A EV0 ENABLE SET [Address = 0x1_01C8]

EV0 Enable Set

Figure 8-327. AID2 EE_SIE_A EV0 ENABLE SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-378. AID2 EE_SIE_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.50 AID2 EE_SIE_A EV0 ENABLE CLEAR [Address = 0x1_01CC]

EV0 Enable Clear

Figure 8-328. AID2 EE_SIE_A EV0 ENABLE CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-379. AID2 EE_SIE_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.51 AID2 EE_SIE_A EV1 ENABLE STATUS [Address = 0x1_01D0]

EV1 Enable Status

Figure 8-329. AID2 EE_SIE_A EV1 ENABLE STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-380. AID2 EE_SIE_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.52 AID2 EE_SIE_A EV1 ENABLE SET [Address = 0x1_01D4]

EV1 Enable Set

Figure 8-330. AID2 EE_SIE_A EV1 ENABLE SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-381. AID2 EE_SIE_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.53 AID2 EE_SIE_A EV1 ENABLE CLEAR [Address = 0x1_01D8]

EV1 Enable Clear

Figure 8-331. AID2 EE_SIE_A EV1 ENABLE CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-382. AID2 EE_SIE_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.54 AID2 EE_SIE_A EV0 ENABLED STATUS [Address = 0x1_01DC]

EV0 Enabled Status

Figure 8-332. AID2 EE_SIE_A EV0 ENABLED STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-383. AID2 EE_SIE_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.55 AID2 EE_SIE_A EV1 ENABLED STATUS [Address = 0x1_01E0]

EV1 Enabled Status

Figure 8-333. AID2 EE_SIE_A EV1 ENABLED STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-384. AID2 EE_SIE_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.56 AID2 EE_SIE_B RAW INTERRUPT STATUS [Address = 0x1_01E4]

SI si_e CTL info.

Figure 8-334. AID2 EE_SIE_B RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-385. AID2 EE_SIE_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	SI Egress CTL transmitted data to ICC
0	SI_EGR_CTL_ICC_EOP_INFO	SI Egress CTL transmitted EOP to ICC

8.5.25.57 AID2 EE_SIE_B RAW SET [Address = 0x1_01E8]

Raw Set

Figure 8-335. AID2 EE_SIE_B RAW SET

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-386. AID2 EE_SIE_B RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.58 AID2 EE_SIE_B RAW CLEAR [Address = 0x1_01EC]

Raw Clear

Figure 8-336. AID2 EE_SIE_B RAW CLEAR

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-387. AID2 EE_SIE_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.59 AID2 EE_SIE_B EV0 ENABLE STATUS [Address = 0x1_01F0]

EV0 Enable Status

Figure 8-337. AID2 EE_SIE_B EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-388. AID2 EE_SIE_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.60 AID2 EE_SIE_B EV0 ENABLE SET [Address = 0x1_01F4]

EV0 Enable Set

Figure 8-338. AID2 EE_SIE_B EV0 ENABLE SET

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-389. AID2 EE_SIE_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.61 AID2 EE_SIE_B EV0 ENABLE CLEAR [Address = 0x1_01F8]

EV0 Enable Clear

Figure 8-339. AID2 EE_SIE_B EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-390. AID2 EE_SIE_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.62 AID2 EE_SIE_B EV1 ENABLE STATUS [Address = 0x1_01FC]

EV1 Enable Status

Figure 8-340. AID2 EE_SIE_B EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-391. AID2 EE_SIE_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.63 AID2 EE_SIE_B EV1 ENABLE SET [Address = 0x1_0200]

EV1 Enable Set

Figure 8-341. AID2 EE_SIE_B EV1 ENABLE SET

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-392. AID2 EE_SIE_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.64 AID2 EE_SIE_B EV1 ENABLE CLEAR [Address = 0x1_0204]

EV1 Enable Clear

Figure 8-342. AID2 EE_SIE_B EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-393. AID2 EE_SIE_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.65 AID2 EE_SIE_B EV0 ENABLED STATUS [Address = 0x1_0208]

EV0 Enabled Status

Figure 8-343. AID2 EE_SIE_B EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-394. AID2 EE_SIE_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.66 AID2 EE_SIE_B EV1 ENABLED STATUS [Address = 0x1_020C]

EV1 Enabled Status

Figure 8-344. AID2 EE_SIE_B EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-395. AID2 EE_SIE_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.67 AID2 EE_SIE_C RAW INTERRUPT STATUS [Address = 0x1_0210]

SI si_e CTL per-channel SOP transmitted to ICC

Figure 8-345. AID2 EE_SIE_C RAW INTERRUPT STATUS

31 16	15 0
Reserved	SI_EGR_CTL_ICC_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-396. AID2 EE_SIE_C RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	SI Egress CTL per channel SOP transmitted to ICC

8.5.25.68 AID2 EE_SIE_C RAW SET [Address = 0x1_0214]

Raw Set

Figure 8-346. AID2 EE_SIE_C RAW SET

31 16	15 0
Reserved	SI_EGR_CTL_ICC_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-397. AID2 EE_SIE_C RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.69 AID2 EE_SIE_C RAW CLEAR [Address = 0x1_0218]

Raw Clear

Figure 8-347. AID2 EE_SIE_C RAW CLEAR

31 16	15 0
Reserved	SI_EGR_CTL_ICC_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-398. AID2 EE_SIE_C RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.25.70 AID2 EE_SIE_C EV0 ENABLE STATUS [Address = 0x1_021C]

EV0 Enable Status

Figure 8-348. AID2 EE_SIE_C EV0 ENABLE STATUS

31	16	15	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-399. AID2 EE_SIE_C EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.25.71 AID2 EE_SIE_C EV0 ENABLE SET [Address = 0x1_0220]

EV0 Enable Set

Figure 8-349. AID2 EE_SIE_C EV0 ENABLE SET

31	16	15	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-400. AID2 EE_SIE_C EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.72 AID2 EE_SIE_C EV0 ENABLE CLEAR [Address = 0x1_0224]

EV0 Enable Clear

Figure 8-350. AID2 EE_SIE_C EV0 ENABLE CLEAR

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-401. AID2 EE_SIE_C EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.25.73 AID2 EE_SIE_C EV1 ENABLE STATUS [Address = 0x1_0228]

EV1 Enable Status

Figure 8-351. AID2 EE_SIE_C EV1 ENABLE STATUS

31 16	15 0
Reserved	SI_EGR_CTL_ICC_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-402. AID2 EE_SIE_C EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.25.74 AID2 EE_SIE_C EV1 ENABLE SET [Address = 0x1_022C]

EV1 Enable Set

Figure 8-352. AID2 EE_SIE_C EV1 ENABLE SET

31	16	15	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-403. AID2 EE_SIE_C EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.75 AID2 EE_SIE_C EV1 ENABLE CLEAR [Address = 0x1_0230]

EV1 Enable Clear

Figure 8-353. AID2 EE_SIE_C EV1 ENABLE CLEAR

31	16	15	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-404. AID2 EE_SIE_C EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.25.76 AID2 EE_SIE_C EV0 ENABLED STATUS [Address = 0x1_0234]

EV0 Enabled Status

Figure 8-354. AID2 EE_SIE_C EV0 ENABLED STATUS

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-405. AID2 EE_SIE_C EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.25.77 AID2 EE_SIE_C EV1 ENABLED STATUS [Address = 0x1_0238]

EV1 Enabled Status

Figure 8-355. AID2 EE_SIE_C EV1 ENABLED STATUS

31	16	15	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-406. AID2 EE_SIE_C EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.25.78 AID2 SYSCLK_ORIG_REG [Address = 0x1_02C0]

This is the origination register indicating which interrupt register group caused the interrupt.

Figure 8-356. AID2 SYSCLK_ORIG_REG

31	16	15	14	13
Reserved		ORIG_EE_15	ORIG_EE_14	ORIG_EE_13
NA-0		R-0	R-0	R-0

12	11	10	9	8
ORIG_EE_12	ORIG_EE_11	ORIG_EE_10	ORIG_EE_9	ORIG_EE_8
R-0	R-0	R-0	R-0	R-0

7	6	5	4	3	2	1	0
ORIG_EE_7	ORIG_EE_6	ORIG_EE_5	ORIG_EE_4	ORIG_EE_3	ORIG_EE_2	ORIG_EE_1	ORIG_EE_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-407. AID2 SYSCLK_ORIG_REG Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved
15	ORIG_EE_15	Undefined for AID2. Always read as 0.
14	ORIG_EE_14	Undefined for AID2. Always read as 0.
13	ORIG_EE_13	Undefined for AID2. Always read as 0.
12	ORIG_EE_12	If set a bit is set in the ee_sie_c register.
11	ORIG_EE_11	If set a bit is set in the ee_sie_b register.
10	ORIG_EE_10	If set a bit is set in the ee_sie_a register.
9	ORIG_EE_9	Undefined for AID2. Always read as 0.
8	ORIG_EE_8	Undefined for AID2. Always read as 0.
7	ORIG_EE_7	Undefined for AID2. Always read as 0.
6	ORIG_EE_6	If set a bit is set in the ee_sii_d register.
5	ORIG_EE_5	Undefined for AID2. Always read as 0.
4	ORIG_EE_4	Undefined for AID2. Always read as 0.
3	ORIG_EE_3	Undefined for AID2. Always read as 0.
2	ORIG_EE_2	If set a bit is set in the ee_sii_c register.
1	ORIG_EE_1	If set a bit is set in the ee_sii_b register.
0	ORIG_EE_0	If set a bit is set in the ee_sii_a register.

8.5.26 AID2_EE_DFE [Address = 0x1_1000]

Table 8-408. AID2_EE_DFE

Offset	Acronym	Register Description	Section
0x1_1000	AID2 DFE_EE_A RAW INTERRUPT STATUS	DFE interrupts.	Section 8.5.26.1
0x1_1004	AID2 DFE_EE_A RAW SET	Raw Set	Section 8.5.26.2
0x1_1008	AID2 DFE_EE_A RAW CLEAR	Raw Clear	Section 8.5.26.3
0x1_100C	AID2 DFE_EE_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.26.4
0x1_1010	AID2 DFE_EE_A EV0 ENABLE SET	EV0 Enable Set	Section 8.5.26.5
0x1_1014	AID2 DFE_EE_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.26.6
0x1_1018	AID2 DFE_EE_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.26.7
0x1_101C	AID2 DFE_EE_A EV1 ENABLE SET	EV1 Enable Set	Section 8.5.26.8
0x1_1020	AID2 DFE_EE_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.26.9
0x1_1024	AID2 DFE_EE_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.26.10
0x1_1028	AID2 DFE_EE_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.26.11

8.5.26.1 AID2 DFE_EE_A RAW INTERRUPT STATUS [Address = 0x1_1000]

DFE interrupts.

Figure 8-357. AID2 DFE_EE_A RAW INTERRUPT STATUS

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-409. AID2 DFE_EE_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	DFE error interrupts

8.5.26.2 AID2 DFE_EE_A RAW SET [Address = 0x1_1004]

Raw Set

Figure 8-358. AID2 DFE_EE_A RAW SET

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-410. AID2 DFE_EE_A RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.26.3 AID2 DFE_EE_A RAW CLEAR [Address = 0x1_1008]

Raw Clear

Figure 8-359. AID2 DFE_EE_A RAW CLEAR

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-411. AID2 DFE_EE_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.26.4 AID2 DFE_EE_A EV0 ENABLE STATUS [Address = 0x1_100C]

EV0 Enable Status

Figure 8-360. AID2 DFE_EE_A EV0 ENABLE STATUS

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-412. AID2 DFE_EE_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.26.5 AID2 DFE_EE_A EV0 ENABLE SET [Address = 0x1_1010]

EV0 Enable Set

Figure 8-361. AID2 DFE_EE_A EV0 ENABLE SET

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-413. AID2 DFE_EE_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.26.6 AID2 DFE_EE_A EV0 ENABLE CLEAR [Address = 0x1_1014]

EV0 Enable Clear

Figure 8-362. AID2 DFE_EE_A EV0 ENABLE CLEAR

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-414. AID2 DFE_EE_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.26.7 AID2 DFE_EE_A EV1 ENABLE STATUS [Address = 0x1_1018]

EV1 Enable Status

Figure 8-363. AID2 DFE_EE_A EV1 ENABLE STATUS

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-415. AID2 DFE_EE_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.26.8 AID2 DFE_EE_A EV1 ENABLE SET [Address = 0x1_101C]

EV1 Enable Set

Figure 8-364. AID2 DFE_EE_A EV1 ENABLE SET

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-416. AID2 DFE_EE_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.26.9 AID2 DFE_EE_A EV1 ENABLE CLEAR [Address = 0x1_1020]

EV1 Enable Clear

Figure 8-365. AID2 DFE_EE_A EV1 ENABLE CLEAR

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-417. AID2 DFE_EE_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.26.10 AID2 DFE_EE_A EV0 ENABLED STATUS [Address = 0x1_1024]

EV0 Enabled Status

Figure 8-366. AID2 DFE_EE_A EV0 ENABLED STATUS

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-418. AID2 DFE_EE_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.26.11 AID2 DFE_EE_A EV1 ENABLED STATUS [Address = 0x1_1028]

EV1 Enabled Status

Figure 8-367. AID2 DFE_EE_A EV1 ENABLED STATUS

31	2	1	0
Reserved		DFE_IQN_AID2_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-419. AID2 DFE_EE_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1-0	DFE_IQN_AID2_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27 AID2_IQN_AID2_EE_VBUSCLK_EE [Address = 0x1_2000]

Table 8-420. AID2_IQN_AID2_EE_VBUSCLK_EE

Offset	Acronym	Register Description	Section
0x1_2000	AID2 EE_SII_E RAW INTERRUPT STATUS	SI si_i IQ info.	Section 8.5.27.1
0x1_2004	AID2 EE_SII_E RAW SET	Raw Set	Section 8.5.27.2
0x1_2008	AID2 EE_SII_E RAW CLEAR	Raw Clear	Section 8.5.27.3
0x1_200C	AID2 EE_SII_E EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.4
0x1_2010	AID2 EE_SII_E EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.5
0x1_2014	AID2 EE_SII_E EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.6
0x1_2018	AID2 EE_SII_E EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.7
0x1_201C	AID2 EE_SII_E EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.8
0x1_2020	AID2 EE_SII_E EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.9
0x1_2024	AID2 EE_SII_E EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.10
0x1_2028	AID2 EE_SII_E EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.11
0x1_202C	AID2 EE_SII_F RAW INTERRUPT STATUS	SI si_i CTL info.	Section 8.5.27.12
0x1_2030	AID2 EE_SII_F RAW SET	Raw Set	Section 8.5.27.13
0x1_2034	AID2 EE_SII_F RAW CLEAR	Raw Clear	Section 8.5.27.14
0x1_2038	AID2 EE_SII_F EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.15
0x1_203C	AID2 EE_SII_F EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.16
0x1_2040	AID2 EE_SII_F EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.17
0x1_2044	AID2 EE_SII_F EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.18
0x1_2048	AID2 EE_SII_F EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.19
0x1_204C	AID2 EE_SII_F EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.20
0x1_2050	AID2 EE_SII_F EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.21
0x1_2054	AID2 EE_SII_F EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.22

Table 8-420. AID2_IQN_AID2_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_2058	AID2 EE_SII_G RAW INTERRUPT STATUS	SI si_i IQ per-channel SOP transmitted to PSI info	Section 8.5.27.23
0x1_205C	AID2 EE_SII_G RAW SET	Raw Set	Section 8.5.27.24
0x1_2060	AID2 EE_SII_G RAW CLEAR	Raw Clear	Section 8.5.27.25
0x1_2064	AID2 EE_SII_G EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.26
0x1_2068	AID2 EE_SII_G EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.27
0x1_206C	AID2 EE_SII_G EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.28
0x1_2070	AID2 EE_SII_G EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.29
0x1_2074	AID2 EE_SII_G EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.30
0x1_2078	AID2 EE_SII_G EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.31
0x1_207C	AID2 EE_SII_G EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.32
0x1_2080	AID2 EE_SII_G EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.33
0x1_2108	AID2 EE_SII_H RAW INTERRUPT STATUS	SI si_i CTL per-channel SOP transmitted to PSI info	Section 8.5.27.34
0x1_210C	AID2 EE_SII_H RAW SET	Raw Set	Section 8.5.27.35
0x1_2110	AID2 EE_SII_H RAW CLEAR	Raw Clear	Section 8.5.27.36
0x1_2114	AID2 EE_SII_H EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.37
0x1_2118	AID2 EE_SII_H EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.38
0x1_211C	AID2 EE_SII_H EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.39
0x1_2120	AID2 EE_SII_H EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.40
0x1_2124	AID2 EE_SII_H EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.41
0x1_2128	AID2 EE_SII_H EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.42

Table 8-420. AID2_IQN_AID2_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_212C	AID2 EE_SII_H EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.43
0x1_2130	AID2 EE_SII_H EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.44
0x1_21B8	AID2 EE_SIE_D RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.5.27.45
0x1_21BC	AID2 EE_SIE_D RAW SET	Raw Set	Section 8.5.27.46
0x1_21C0	AID2 EE_SIE_D RAW CLEAR	Raw Clear	Section 8.5.27.47
0x1_21C4	AID2 EE_SIE_D EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.48
0x1_21C8	AID2 EE_SIE_D EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.49
0x1_21CC	AID2 EE_SIE_D EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.50
0x1_21D0	AID2 EE_SIE_D EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.51
0x1_21D4	AID2 EE_SIE_D EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.52
0x1_21D8	AID2 EE_SIE_D EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.53
0x1_21DC	AID2 EE_SIE_D EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.54
0x1_21E0	AID2 EE_SIE_D EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.55
0x1_21E4	AID2 EE_SIE_E RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.5.27.56
0x1_21E8	AID2 EE_SIE_E RAW SET	Raw Set	Section 8.5.27.57
0x1_21EC	AID2 EE_SIE_E RAW CLEAR	Raw Clear	Section 8.5.27.58
0x1_21F0	AID2 EE_SIE_E EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.59
0x1_21F4	AID2 EE_SIE_E EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.60
0x1_21F8	AID2 EE_SIE_E EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.61
0x1_21FC	AID2 EE_SIE_E EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.62

Table 8-420. AID2_IQN_AID2_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_2200	AID2 EE_SIE_E EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.63
0x1_2204	AID2 EE_SIE_E EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.64
0x1_2208	AID2 EE_SIE_E EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.65
0x1_220C	AID2 EE_SIE_E EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.66
0x1_2210	AID2 EE_SIE_F RAW INTERRUPT STATUS	SI si_e IQ per-channel SOP received from PSI info	Section 8.5.27.67
0x1_2214	AID2 EE_SIE_F RAW SET	Raw Set	Section 8.5.27.68
0x1_2218	AID2 EE_SIE_F RAW CLEAR	Raw Clear	Section 8.5.27.69
0x1_221C	AID2 EE_SIE_F EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.70
0x1_2220	AID2 EE_SIE_F EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.71
0x1_2224	AID2 EE_SIE_F EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.72
0x1_2228	AID2 EE_SIE_F EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.73
0x1_222C	AID2 EE_SIE_F EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.74
0x1_2230	AID2 EE_SIE_F EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.75
0x1_2234	AID2 EE_SIE_F EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.76
0x1_2238	AID2 EE_SIE_F EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.77
0x1_22C0	AID2 EE_SIE_G RAW INTERRUPT STATUS	SI si_e CTL per-channel SOP received from PSI info	Section 8.5.27.78
0x1_22C4	AID2 EE_SIE_G RAW SET	Raw Set	Section 8.5.27.79
0x1_22C8	AID2 EE_SIE_G RAW CLEAR	Raw Clear	Section 8.5.27.80
0x1_22CC	AID2 EE_SIE_G EV0 ENABLE STATUS	EV0 Enable Status	Section 8.5.27.81
0x1_22D0	AID2 EE_SIE_G EV0 ENABLE SET	EV0 Enable Set	Section 8.5.27.82

Table 8-420. AID2_IQN_AID2_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x1_22D4	AID2 EE_SIE_G EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.5.27.83
0x1_22D8	AID2 EE_SIE_G EV1 ENABLE STATUS	EV1 Enable Status	Section 8.5.27.84
0x1_22DC	AID2 EE_SIE_G EV1 ENABLE SET	EV1 Enable Set	Section 8.5.27.85
0x1_22E0	AID2 EE_SIE_G EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.5.27.86
0x1_22E4	AID2 EE_SIE_G EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.5.27.87
0x1_22E8	AID2 EE_SIE_G EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.5.27.88
0x1_2370	AID2 VBUSCLK_ORIG_REG	This is the origination register indicating which interrupt register group caused the interrupt.	Section 8.5.27.89

8.5.27.1 AID2 EE_SII_E RAW INTERRUPT STATUS [Address = 0x1_2000]

SI si_i IQ info.

Figure 8-368. AID2 EE_SII_E RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-421. AID2 EE_SII_E RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	SI Ingress IQ data transmitted to PSI
0	SI_ING_IQ_PSI_EOP_INFO	SI Ingress IQ EOP transmitted to PSI

8.5.27.2 AID2 EE_SII_E RAW SET [Address = 0x1_2004]

Raw Set

Figure 8-369. AID2 EE_SII_E RAW SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-422. AID2 EE_SII_E RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.3 AID2 EE_SII_E RAW CLEAR [Address = 0x1_2008]

Raw Clear

Figure 8-370. AID2 EE_SII_E RAW CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-423. AID2 EE_SII_E RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.4 AID2 EE_SII_E EV0 ENABLE STATUS [Address = 0x1_200C]

EV0 Enable Status

Figure 8-371. AID2 EE_SII_E EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-424. AID2 EE_SII_E EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.5 AID2 EE_SII_E EV0 ENABLE SET [Address = 0x1_2010]

EV0 Enable Set

Figure 8-372. AID2 EE_SII_E EV0 ENABLE SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-425. AID2 EE_SII_E EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.6 AID2 EE_SII_E EV0 ENABLE CLEAR [Address = 0x1_2014]

EV0 Enable Clear

Figure 8-373. AID2 EE_SII_E EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-426. AID2 EE_SII_E EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.7 AID2 EE_SII_E EV1 ENABLE STATUS [Address = 0x1_2018]

EV1 Enable Status

Figure 8-374. AID2 EE_SII_E EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-427. AID2 EE_SII_E EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.8 AID2 EE_SII_E EV1 ENABLE SET [Address = 0x1_201C]

EV1 Enable Set

Figure 8-375. AID2 EE_SII_E EV1 ENABLE SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-428. AID2 EE_SII_E EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.9 AID2 EE_SII_E EV1 ENABLE CLEAR [Address = 0x1_2020]

EV1 Enable Clear

Figure 8-376. AID2 EE_SII_E EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-429. AID2 EE_SII_E EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.10 AID2 EE_SII_E EV0 ENABLED STATUS [Address = 0x1_2024]

EV0 Enabled Status

Figure 8-377. AID2 EE_SII_E EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-430. AID2 EE_SII_E EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.11 AID2 EE_SII_E EV1 ENABLED STATUS [Address = 0x1_2028]

EV1 Enabled Status

Figure 8-378. AID2 EE_SII_E EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-431. AID2 EE_SII_E EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.12 AID2 EE_SII_F RAW INTERRUPT STATUS [Address = 0x1_202C]

SI si_i CTL info.

Figure 8-379. AID2 EE_SII_F RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-432. AID2 EE_SII_F RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	SI Ingress CTL data transmitted to PSI
0	SI_ING_CTL_PSI_EOP_INFO	SI Ingress CTL EOP transmitted to PSI

8.5.27.13 AID2 EE_SII_F RAW SET [Address = 0x1_2030]

Raw Set

Figure 8-380. AID2 EE_SII_F RAW SET

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-433. AID2 EE_SII_F RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.14 AID2 EE_SII_F RAW CLEAR [Address = 0x1_2034]

Raw Clear

Figure 8-381. AID2 EE_SII_F RAW CLEAR

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-434. AID2 EE_SII_F RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.15 AID2 EE_SII_F EV0 ENABLE STATUS [Address = 0x1_2038]

EV0 Enable Status

Figure 8-382. AID2 EE_SII_F EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-435. AID2 EE_SII_F EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.16 AID2 EE_SII_F EV0 ENABLE SET [Address = 0x1_203C]

EV0 Enable Set

Figure 8-383. AID2 EE_SII_F EV0 ENABLE SET

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-436. AID2 EE_SII_F EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.17 AID2 EE_SII_F EV0 ENABLE CLEAR [Address = 0x1_2040]

EV0 Enable Clear

Figure 8-384. AID2 EE_SII_F EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-437. AID2 EE_SII_F EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.18 AID2 EE_SII_F EV1 ENABLE STATUS [Address = 0x1_2044]

EV1 Enable Status

Figure 8-385. AID2 EE_SII_F EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-438. AID2 EE_SII_F EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.19 AID2 EE_SII_F EV1 ENABLE SET [Address = 0x1_2048]

EV1 Enable Set

Figure 8-386. AID2 EE_SII_F EV1 ENABLE SET

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-439. AID2 EE_SII_F EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.20 AID2 EE_SII_F EV1 ENABLE CLEAR [Address = 0x1_204C]

EV1 Enable Clear

Figure 8-387. AID2 EE_SII_F EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-440. AID2 EE_SII_F EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.21 AID2 EE_SII_F EV0 ENABLED STATUS [Address = 0x1_2050]

EV0 Enabled Status

Figure 8-388. AID2 EE_SII_F EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-441. AID2 EE_SII_F EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.22 AID2 EE_SII_F EV1 ENABLED STATUS [Address = 0x1_2054]

EV1 Enabled Status

Figure 8-389. AID2 EE_SII_F EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

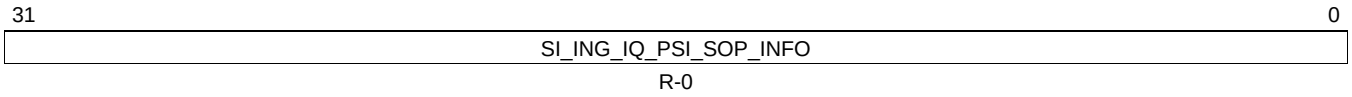
Table 8-442. AID2 EE_SII_F EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.23 AID2 EE_SII_G RAW INTERRUPT STATUS [Address = 0x1_2058]

SI si_i IQ per-channel SOP transmitted to PSI info

Figure 8-390. AID2 EE_SII_G RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-443. AID2 EE_SII_G RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	SI Ingress IQ SOP transmitted to PSI

8.5.27.24 AID2 EE_SII_G RAW SET [Address = 0x1_205C]

Raw Set

Figure 8-391. AID2 EE_SII_G RAW SET

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-444. AID2 EE_SII_G RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.25 AID2 EE_SII_G RAW CLEAR [Address = 0x1_2060]

Raw Clear

Figure 8-392. AID2 EE_SII_G RAW CLEAR

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-445. AID2 EE_SII_G RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.26 AID2 EE_SII_G EV0 ENABLE STATUS [Address = 0x1_2064]

EV0 Enable Status

Figure 8-393. AID2 EE_SII_G EV0 ENABLE STATUS

31	0
SI_ING_IQ_PSI_SOP_INFO	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-446. AID2 EE_SII_G EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.27 AID2 EE_SII_G EV0 ENABLE SET [Address = 0x1_2068]

EV0 Enable Set

Figure 8-394. AID2 EE_SII_G EV0 ENABLE SET

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-447. AID2 EE_SII_G EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.28 AID2 EE_SII_G EV0 ENABLE CLEAR [Address = 0x1_206C]

EV0 Enable Clear

Figure 8-395. AID2 EE_SII_G EV0 ENABLE CLEAR

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

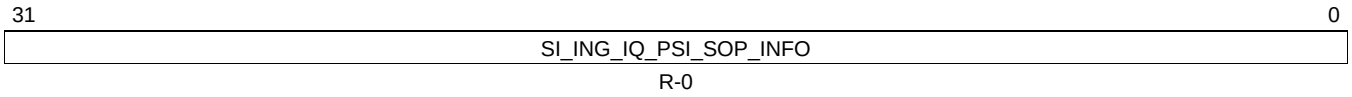
Table 8-448. AID2 EE_SII_G EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.29 AID2 EE_SII_G EV1 ENABLE STATUS [Address = 0x1_2070]

EV1 Enable Status

Figure 8-396. AID2 EE_SII_G EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-449. AID2 EE_SII_G EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.30 AID2 EE_SII_G EV1 ENABLE SET [Address = 0x1_2074]

EV1 Enable Set

Figure 8-397. AID2 EE_SII_G EV1 ENABLE SET

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

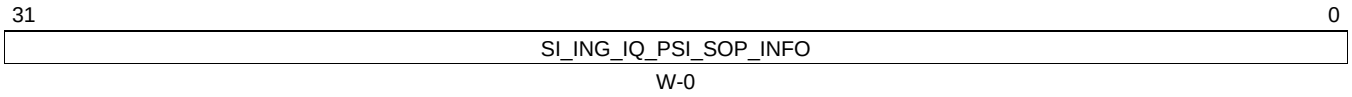
Table 8-450. AID2 EE_SII_G EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.31 AID2 EE_SII_G EV1 ENABLE CLEAR [Address = 0x1_2078]

EV1 Enable Clear

Figure 8-398. AID2 EE_SII_G EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-451. AID2 EE_SII_G EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.32 AID2 EE_SII_G EV0 ENABLED STATUS [Address = 0x1_207C]

EV0 Enabled Status

Figure 8-399. AID2 EE_SII_G EV0 ENABLED STATUS

31	0
SI_ING_IQ_PSI_SOP_INFO	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-452. AID2 EE_SII_G EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.33 AID2 EE_SII_G EV1 ENABLED STATUS [Address = 0x1_2080]

EV1 Enabled Status

Figure 8-400. AID2 EE_SII_G EV1 ENABLED STATUS

31	0
SI_ING_IQ_PSI_SOP_INFO	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-453. AID2 EE_SII_G EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.34 AID2 EE_SII_H RAW INTERRUPT STATUS [Address = 0x1_2108]

SI si_i CTL per-channel SOP transmitted to PSI info

Figure 8-401. AID2 EE_SII_H RAW INTERRUPT STATUS

31 16	15 0
Reserved	SI_ING_CTL_PSI_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-454. AID2 EE_SII_H RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	SI Ingress CTL per channel SOP transmitted to PSI

8.5.27.35 AID2 EE_SII_H RAW SET [Address = 0x1_210C]

Raw Set

Figure 8-402. AID2 EE_SII_H RAW SET

31 16	15 0
Reserved	SI_ING_CTL_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-455. AID2 EE_SII_H RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.36 AID2 EE_SII_H RAW CLEAR [Address = 0x1_2110]

Raw Clear

Figure 8-403. AID2 EE_SII_H RAW CLEAR

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-456. AID2 EE_SII_H RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.37 AID2 EE_SII_H EV0 ENABLE STATUS [Address = 0x1_2114]

EV0 Enable Status

Figure 8-404. AID2 EE_SII_H EV0 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-457. AID2 EE_SII_H EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.38 AID2 EE_SII_H EV0 ENABLE SET [Address = 0x1_2118]

EV0 Enable Set

Figure 8-405. AID2 EE_SII_H EV0 ENABLE SET

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-458. AID2 EE_SII_H EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.39 AID2 EE_SII_H EV0 ENABLE CLEAR [Address = 0x1_211C]

EV0 Enable Clear

Figure 8-406. AID2 EE_SII_H EV0 ENABLE CLEAR

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-459. AID2 EE_SII_H EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.40 AID2 EE_SII_H EV1 ENABLE STATUS [Address = 0x1_2120]

EV1 Enable Status

Figure 8-407. AID2 EE_SII_H EV1 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-460. AID2 EE_SII_H EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.41 AID2 EE_SII_H EV1 ENABLE SET [Address = 0x1_2124]

EV1 Enable Set

Figure 8-408. AID2 EE_SII_H EV1 ENABLE SET

31 16	15 0
Reserved	SI_ING_CTL_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

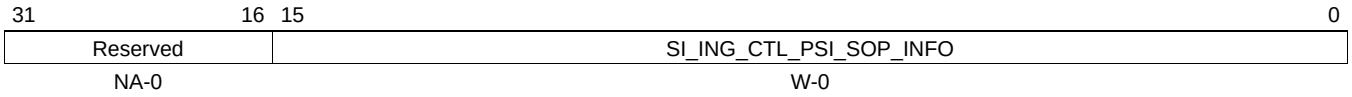
Table 8-461. AID2 EE_SII_H EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.42 AID2 EE_SII_H EV1 ENABLE CLEAR [Address = 0x1_2128]

EV1 Enable Clear

Figure 8-409. AID2 EE_SII_H EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-462. AID2 EE_SII_H EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.43 AID2 EE_SII_H EV0 ENABLED STATUS [Address = 0x1_212C]

EV0 Enabled Status

Figure 8-410. AID2 EE_SII_H EV0 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-463. AID2 EE_SII_H EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.44 AID2 EE_SII_H EV1 ENABLED STATUS [Address = 0x1_2130]

EV1 Enabled Status

Figure 8-411. AID2 EE_SII_H EV1 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

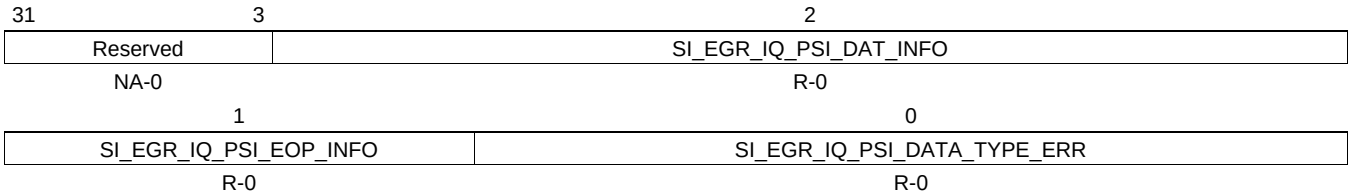
Table 8-464. AID2 EE_SII_H EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.45 AID2 EE_SIE_D RAW INTERRUPT STATUS [Address = 0x1_21B8]

SI si_e IQ errors and info.

Figure 8-412. AID2 EE_SIE_D RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-465. AID2 EE_SIE_D RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	SI Egress IQ valid data received from PSI
1	SI_EGR_IQ_PSI_EOP_INFO	SI Egress IQ EOP received from PSI
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	SI Egress IQ PSI data type error

8.5.27.46 AID2 EE_SIE_D RAW SET [Address = 0x1_21BC]

Raw Set

Figure 8-413. AID2 EE_SIE_D RAW SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-466. AID2 EE_SIE_D RAW SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.47 AID2 EE_SIE_D RAW CLEAR [Address = 0x1_21C0]

Raw Clear

Figure 8-414. AID2 EE_SIE_D RAW CLEAR

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

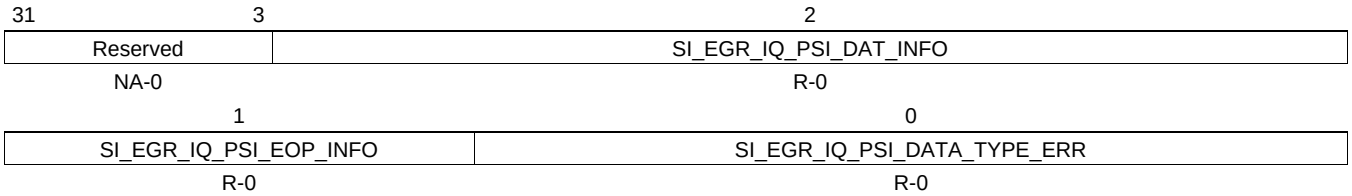
Table 8-467. AID2 EE_SIE_D RAW CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.48 AID2 EE_SIE_D EV0 ENABLE STATUS [Address = 0x1_21C4]

EV0 Enable Status

Figure 8-415. AID2 EE_SIE_D EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-468. AID2 EE_SIE_D EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.49 AID2 EE_SIE_D EV0 ENABLE SET [Address = 0x1_21C8]

EV0 Enable Set

Figure 8-416. AID2 EE_SIE_D EV0 ENABLE SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-469. AID2 EE_SIE_D EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.50 AID2 EE_SIE_D EV0 ENABLE CLEAR [Address = 0x1_21CC]

EV0 Enable Clear

Figure 8-417. AID2 EE_SIE_D EV0 ENABLE CLEAR

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

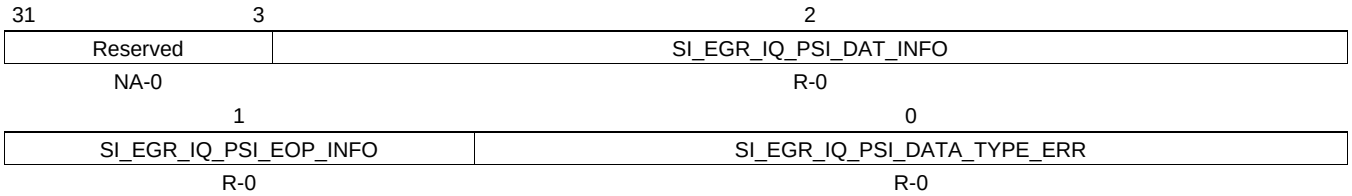
Table 8-470. AID2 EE_SIE_D EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.51 AID2 EE_SIE_D EV1 ENABLE STATUS [Address = 0x1_21D0]

EV1 Enable Status

Figure 8-418. AID2 EE_SIE_D EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-471. AID2 EE_SIE_D EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.52 AID2 EE_SIE_D EV1 ENABLE SET [Address = 0x1_21D4]

EV1 Enable Set

Figure 8-419. AID2 EE_SIE_D EV1 ENABLE SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

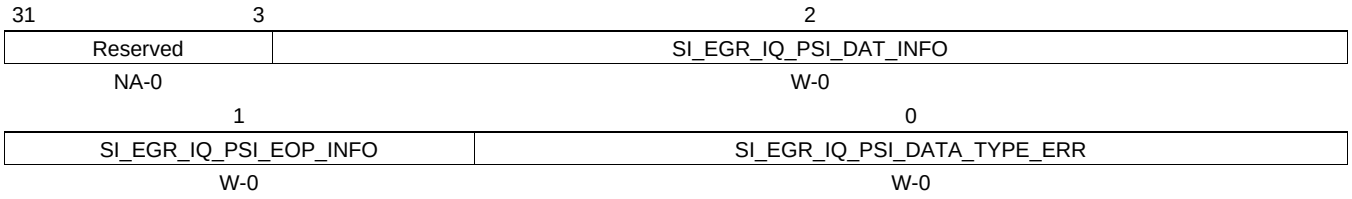
Table 8-472. AID2 EE_SIE_D EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.53 AID2 EE_SIE_D EV1 ENABLE CLEAR [Address = 0x1_21D8]

EV1 Enable Clear

Figure 8-420. AID2 EE_SIE_D EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-473. AID2 EE_SIE_D EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.54 AID2 EE_SIE_D EV0 ENABLED STATUS [Address = 0x1_21DC]

EV0 Enabled Status

Figure 8-421. AID2 EE_SIE_D EV0 ENABLED STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

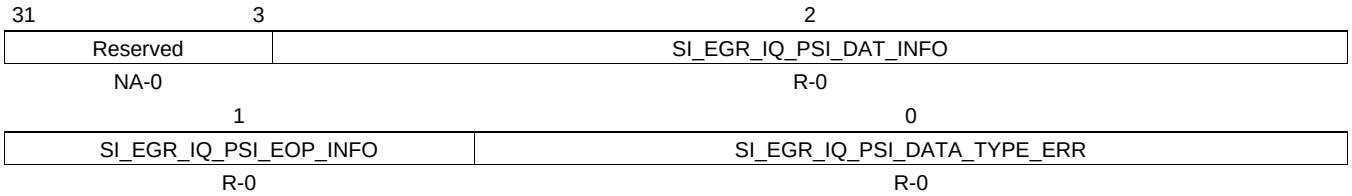
Table 8-474. AID2 EE_SIE_D EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.55 AID2 EE_SIE_D EV1 ENABLED STATUS [Address = 0x1_21E0]

EV1 Enabled Status

Figure 8-422. AID2 EE_SIE_D EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

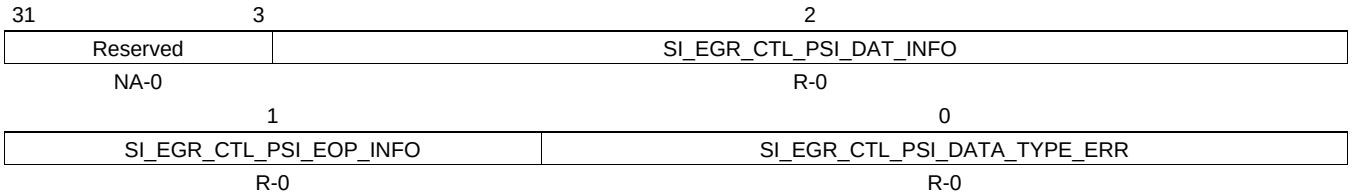
Table 8-475. AID2 EE_SIE_D EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.56 AID2 EE_SIE_E RAW INTERRUPT STATUS [Address = 0x1_21E4]

SI si_e IQ errors and info.

Figure 8-423. AID2 EE_SIE_E RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-476. AID2 EE_SIE_E RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	SI Egress CTL valid data received from PSI
1	SI_EGR_CTL_PSI_EOP_INFO	SI Egress CTL EOP received from PSI
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	SI Egress CTL PSI data type error

8.5.27.57 AID2 EE_SIE_E RAW SET [Address = 0x1_21E8]

Raw Set

Figure 8-424. AID2 EE_SIE_E RAW SET

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-477. AID2 EE_SIE_E RAW SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.58 AID2 EE_SIE_E RAW CLEAR [Address = 0x1_21EC]

Raw Clear

Figure 8-425. AID2 EE_SIE_E RAW CLEAR

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

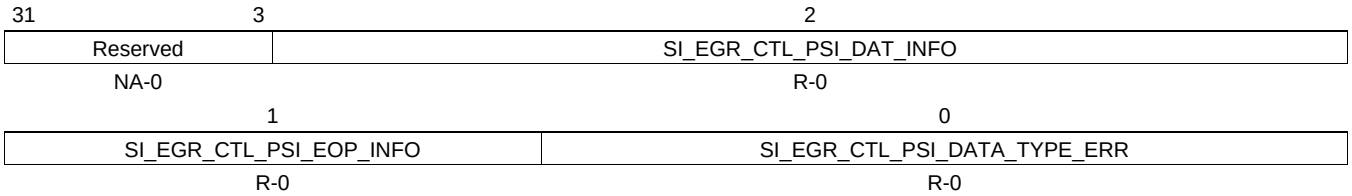
Table 8-478. AID2 EE_SIE_E RAW CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.59 AID2 EE_SIE_E EV0 ENABLE STATUS [Address = 0x1_21F0]

EV0 Enable Status

Figure 8-426. AID2 EE_SIE_E EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-479. AID2 EE_SIE_E EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.60 AID2 EE_SIE_E EV0 ENABLE SET [Address = 0x1_21F4]

EV0 Enable Set

Figure 8-427. AID2 EE_SIE_E EV0 ENABLE SET

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1	0	
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

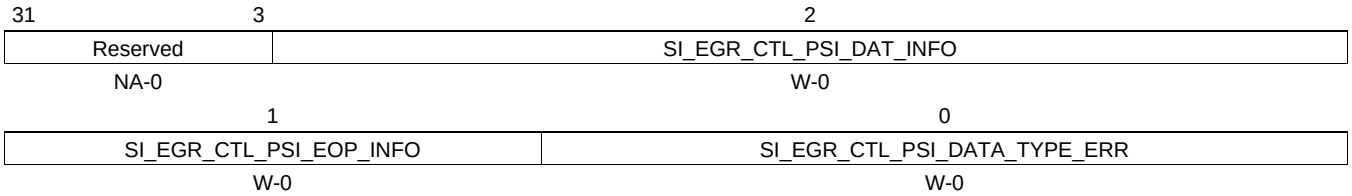
Table 8-480. AID2 EE_SIE_E EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.61 AID2 EE_SIE_E EV0 ENABLE CLEAR [Address = 0x1_21F8]

EV0 Enable Clear

Figure 8-428. AID2 EE_SIE_E EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

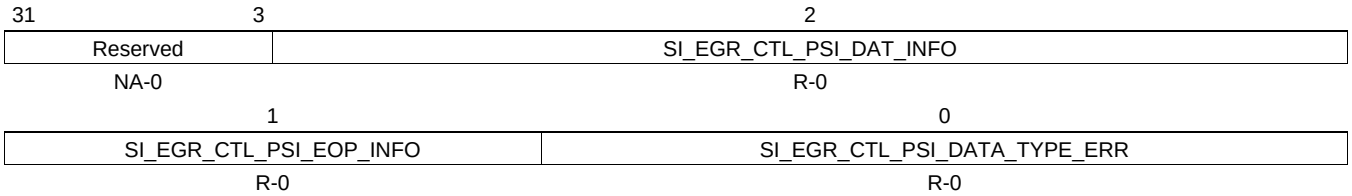
Table 8-481. AID2 EE_SIE_E EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.62 AID2 EE_SIE_E EV1 ENABLE STATUS [Address = 0x1_21FC]

EV1 Enable Status

Figure 8-429. AID2 EE_SIE_E EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-482. AID2 EE_SIE_E EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.63 AID2 EE_SIE_E EV1 ENABLE SET [Address = 0x1_2200]

EV1 Enable Set

Figure 8-430. AID2 EE_SIE_E EV1 ENABLE SET

31	3	2	0
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
1			0
SI_EGR_CTL_PSI_EOP_INFO			SI_EGR_CTL_PSI_DATA_TYPE_ERR
W-0			W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

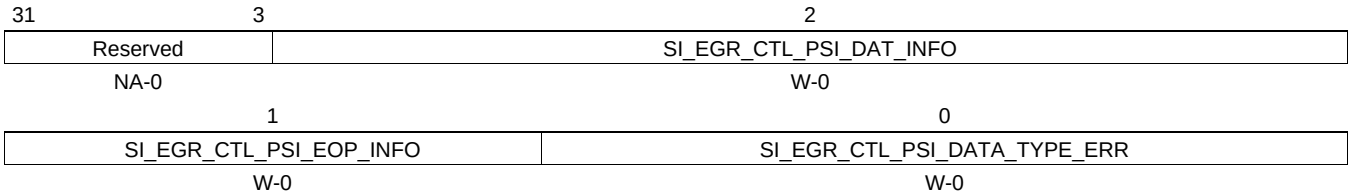
Table 8-483. AID2 EE_SIE_E EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.64 AID2 EE_SIE_E EV1 ENABLE CLEAR [Address = 0x1_2204]

EV1 Enable Clear

Figure 8-431. AID2 EE_SIE_E EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

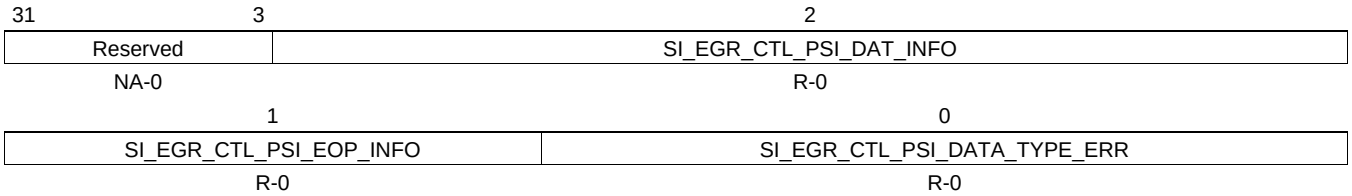
Table 8-484. AID2 EE_SIE_E EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.65 AID2 EE_SIE_E EV0 ENABLED STATUS [Address = 0x1_2208]

EV0 Enabled Status

Figure 8-432. AID2 EE_SIE_E EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

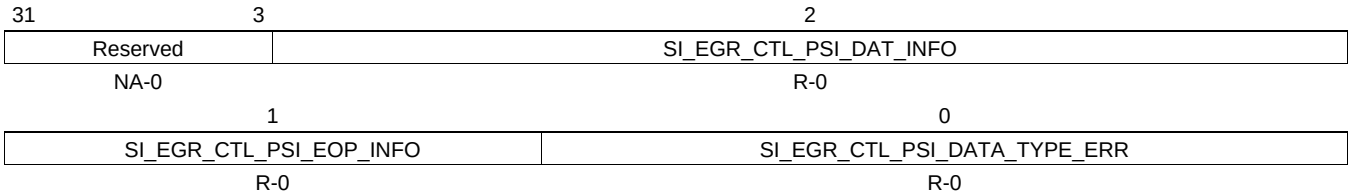
Table 8-485. AID2 EE_SIE_E EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.66 AID2 EE_SIE_E EV1 ENABLED STATUS [Address = 0x1_220C]

EV1 Enabled Status

Figure 8-433. AID2 EE_SIE_E EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

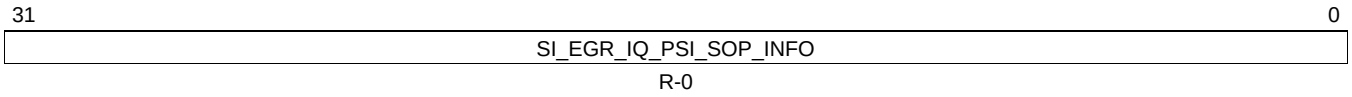
Table 8-486. AID2 EE_SIE_E EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.67 AID2 EE_SIE_F RAW INTERRUPT STATUS [Address = 0x1_2210]

SI si_e IQ per-channel SOP received from PSI info

Figure 8-434. AID2 EE_SIE_F RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-487. AID2 EE_SIE_F RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	SI Ingress IQ per channel SOP received from PSI

8.5.27.68 AID2 EE_SIE_F RAW SET [Address = 0x1_2214]

Raw Set

Figure 8-435. AID2 EE_SIE_F RAW SET

31	0
SI_EGR_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-488. AID2 EE_SIE_F RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.69 AID2 EE_SIE_F RAW CLEAR [Address = 0x1_2218]

Raw Clear

Figure 8-436. AID2 EE_SIE_F RAW CLEAR

31	0
SI_EGR_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

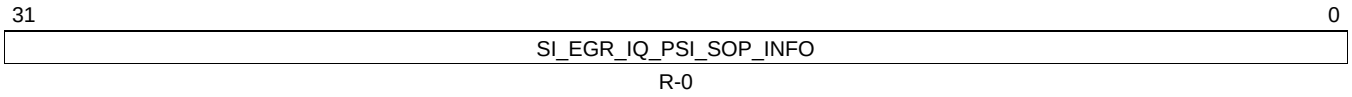
Table 8-489. AID2 EE_SIE_F RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.70 AID2 EE_SIE_F EV0 ENABLE STATUS [Address = 0x1_221C]

EV0 Enable Status

Figure 8-437. AID2 EE_SIE_F EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-490. AID2 EE_SIE_F EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.71 AID2 EE_SIE_F EV0 ENABLE SET [Address = 0x1_2220]

EV0 Enable Set

Figure 8-438. AID2 EE_SIE_F EV0 ENABLE SET

31	0
SI_EGR_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

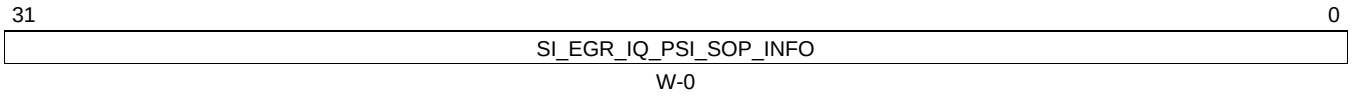
Table 8-491. AID2 EE_SIE_F EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.72 AID2 EE_SIE_F EV0 ENABLE CLEAR [Address = 0x1_2224]

EV0 Enable Clear

Figure 8-439. AID2 EE_SIE_F EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

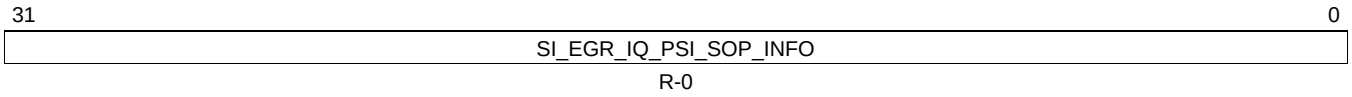
Table 8-492. AID2 EE_SIE_F EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.73 AID2 EE_SIE_F EV1 ENABLE STATUS [Address = 0x1_2228]

EV1 Enable Status

Figure 8-440. AID2 EE_SIE_F EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

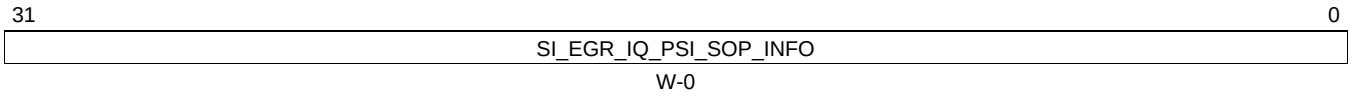
Table 8-493. AID2 EE_SIE_F EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.74 AID2 EE_SIE_F EV1 ENABLE SET [Address = 0x1_222C]

EV1 Enable Set

Figure 8-441. AID2 EE_SIE_F EV1 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

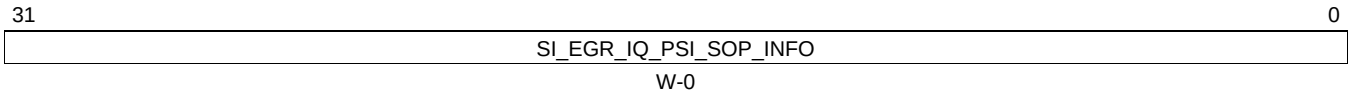
Table 8-494. AID2 EE_SIE_F EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.75 AID2 EE_SIE_F EV1 ENABLE CLEAR [Address = 0x1_2230]

EV1 Enable Clear

Figure 8-442. AID2 EE_SIE_F EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

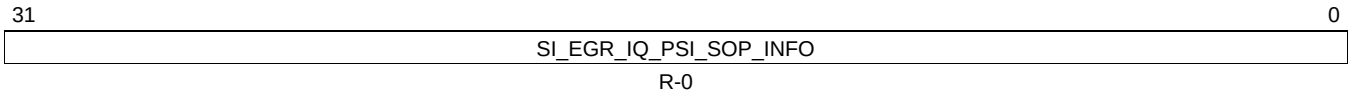
Table 8-495. AID2 EE_SIE_F EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.76 AID2 EE_SIE_F EV0 ENABLED STATUS [Address = 0x1_2234]

EV0 Enabled Status

Figure 8-443. AID2 EE_SIE_F EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

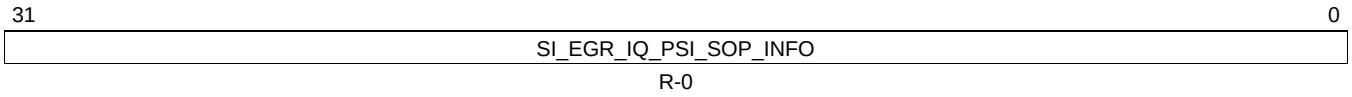
Table 8-496. AID2 EE_SIE_F EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.77 AID2 EE_SIE_F EV1 ENABLED STATUS [Address = 0x1_2238]

EV1 Enabled Status

Figure 8-444. AID2 EE_SIE_F EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-497. AID2 EE_SIE_F EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.78 AID2 EE_SIE_G RAW INTERRUPT STATUS [Address = 0x1_22C0]

SI si_e CTL per-channel SOP received from PSI info

Figure 8-445. AID2 EE_SIE_G RAW INTERRUPT STATUS

31	16	15	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-498. AID2 EE_SIE_G RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	SI Egress CTL per channel SOP received from PSI

8.5.27.79 AID2 EE_SIE_G RAW SET [Address = 0x1_22C4]

Raw Set

Figure 8-446. AID2 EE_SIE_G RAW SET

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-499. AID2 EE_SIE_G RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.80 AID2 EE_SIE_G RAW CLEAR [Address = 0x1_22C8]

Raw Clear

Figure 8-447. AID2 EE_SIE_G RAW CLEAR

31	16	15	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

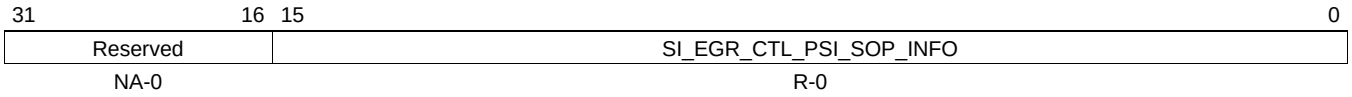
Table 8-500. AID2 EE_SIE_G RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.5.27.81 AID2 EE_SIE_G EV0 ENABLE STATUS [Address = 0x1_22CC]

EV0 Enable Status

Figure 8-448. AID2 EE_SIE_G EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-501. AID2 EE_SIE_G EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.5.27.82 AID2 EE_SIE_G EV0 ENABLE SET [Address = 0x1_22D0]

EV0 Enable Set

Figure 8-449. AID2 EE_SIE_G EV0 ENABLE SET

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-502. AID2 EE_SIE_G EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.83 AID2 EE_SIE_G EV0 ENABLE CLEAR [Address = 0x1_22D4]

EV0 Enable Clear

Figure 8-450. AID2 EE_SIE_G EV0 ENABLE CLEAR

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-503. AID2 EE_SIE_G EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.5.27.84 AID2 EE_SIE_G EV1 ENABLE STATUS [Address = 0x1_22D8]

EV1 Enable Status

Figure 8-451. AID2 EE_SIE_G EV1 ENABLE STATUS

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-504. AID2 EE_SIE_G EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.5.27.85 AID2 EE_SIE_G EV1 ENABLE SET [Address = 0x1_22DC]

EV1 Enable Set

Figure 8-452. AID2 EE_SIE_G EV1 ENABLE SET

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-505. AID2 EE_SIE_G EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.86 AID2 EE_SIE_G EV1 ENABLE CLEAR [Address = 0x1_22E0]

EV1 Enable Clear

Figure 8-453. AID2 EE_SIE_G EV1 ENABLE CLEAR

31	16	15	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-506. AID2 EE_SIE_G EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.5.27.87 AID2 EE_SIE_G EV0 ENABLED STATUS [Address = 0x1_22E4]

EV0 Enabled Status

Figure 8-454. AID2 EE_SIE_G EV0 ENABLED STATUS

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-507. AID2 EE_SIE_G EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.5.27.88 AID2 EE_SIE_G EV1 ENABLED STATUS [Address = 0x1_22E8]

EV1 Enabled Status

Figure 8-455. AID2 EE_SIE_G EV1 ENABLED STATUS

31 16	15 0
Reserved	SI_EGR_CTL_PSI_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-508. AID2 EE_SIE_G EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.5.27.89 AID2 VBUSCLK_ORIG_REG [Address = 0x1_2370]

This is the origination register indicating which interrupt register group caused the interrupt.

Figure 8-456. AID2 VBUSCLK_ORIG_REG

31	20	19	18	17	16
Reserved		ORIG_EE_19	ORIG_EE_18	ORIG_EE_17	ORIG_EE_16
NA-0		R-0	R-0	R-0	R-0

15	14	13	12	11	10
ORIG_EE_15	ORIG_EE_14	ORIG_EE_13	ORIG_EE_12	ORIG_EE_11	ORIG_EE_10
R-0	R-0	R-0	R-0	R-0	R-0

9	8	7	6	5	4	3	2	1	0
ORIG_EE_9	ORIG_EE_8	ORIG_EE_7	ORIG_EE_6	ORIG_EE_5	ORIG_EE_4	ORIG_EE_3	ORIG_EE_2	ORIG_EE_1	ORIG_EE_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-509. AID2 VBUSCLK_ORIG_REG Field Descriptions

Bits	Name	Description
31-20	Reserved	Reserved
19	ORIG_EE_19	Undefined for AID2. Always read as 0.
18	ORIG_EE_18	Undefined for AID2. Always read as 0.
17	ORIG_EE_17	Undefined for AID2. Always read as 0.
16	ORIG_EE_16	If set a bit is set in the ee_sie_g register.
15	ORIG_EE_15	Undefined for AID2. Always read as 0.
14	ORIG_EE_14	Undefined for AID2. Always read as 0.
13	ORIG_EE_13	Undefined for AID2. Always read as 0.
12	ORIG_EE_12	If set a bit is set in the ee_sie_f register.
11	ORIG_EE_11	If set a bit is set in the ee_sie_e register.
10	ORIG_EE_10	If set a bit is set in the ee_sie_d register.
9	ORIG_EE_9	Undefined for AID2. Always read as 0.
8	ORIG_EE_8	Undefined for AID2. Always read as 0.
7	ORIG_EE_7	Undefined for AID2. Always read as 0.
6	ORIG_EE_6	If set a bit is set in the ee_sii_h register.
5	ORIG_EE_5	Undefined for AID2. Always read as 0.
4	ORIG_EE_4	Undefined for AID2. Always read as 0.
3	ORIG_EE_3	Undefined for AID2. Always read as 0.
2	ORIG_EE_2	If set a bit is set in the ee_sii_g register.
1	ORIG_EE_1	If set a bit is set in the ee_sii_f register.
0	ORIG_EE_0	If set a bit is set in the ee_sii_e register.

8.6 AIL Registers

Table 8-510. AIL Register Groups

Offset	Acronym	Description	Section
0x0000	AIL_SI_IQ_EFE_CONFIG_GROUP	Group containing EFE Channel Configuration registers	Section 8.6.1
0x0400	AIL_SI_IQ_EFE_RADIO_STANDARD_GROUP	Group of registers containing EFE configuration which is radio standard specific. Eight radio standards are supported, individual AxC channels are each assigned to one of these.	Section 8.6.2
0x0600	AIL_IQ_EFE_CHAN_AXC_OFFSET	Group containing IQ_EFE_CHAN_AXC_OFFSET RAM	Section 8.6.3
0x0800	AIL_IQ_EFE_FRM_SAMP_TC_MMR_RAM	Group containing Egress Sample Terminal Count Configuration registers	Section 8.6.4
0x0C00	AIL_SI_IQ_E_TDM_LUT_RAM	iq_pe_tdm_lut_cfg RAM	Section 8.6.5
0x1000	AIL_SI_IQ_E_SCH_PHY	iqn_si_e_ail Group containing PHY specific control and status registers	Section 8.6.6
0x1080	AIL_SI_IQ_E_OBSAI_MODTXRULE	iqn_si_e_ail Group containing OBSAI Modulo TX Rule specific control registers	Section 8.6.7
0x1100	AIL_SI_IQ_E_OBSAI_DBM_RULE_RAM	iqn_si_e_ail Group containing OBSAI Dual Bit Map Rule specific control registers	Section 8.6.8
0x1400	AIL_SI_IQ_E_OBSAI_DBM_BITMAP_RAM		Section 8.6.9
0x1800	AIL_SI_IQ_E_SCH_CPRI	iqn_si_e_ail Group containing CPRI specific control registers	Section 8.6.10
0x2000	AIL_IQ_IFE_CHANNEL_CONFIGURATION_GROUP	Group containing IFE Radio Stanadard registers	Section 8.6.11
0x2200	AIL_IQ_IFE_RADIO_STANDARD_GROUP	Group containing IFE Radio Stanadard registers	Section 8.6.12
0x2340	AIL_IQ_IFE_CONFIG_GROUP	Group containing IFE Configuration registers	Section 8.6.13
0x2384	AIL_IQ_IDC_GENERAL_STATUS_GROUP	Group containing IDC Status registers	Section 8.6.14
0x23C0	AIL_IQ_IDC_CONFIGURATION_GROUP	Group containing IFE Radio Stanadard registers	Section 8.6.15
0x2400	AIL_IQ_IDC_CHANNEL_CONFIG_GROUP	Group containing IDC Channel Configuration registers	Section 8.6.16
0x2800	AIL_IFE_FRM_SAMP_TC_MMR_RAM	Group containing Sample Terminal Count Configuration registers	Section 8.6.17
0x3000	AIL_ECTL_PKT_IF	Group containing ECTL Configuration and Status Registers in the VBUS_CLK domain	Section 8.6.18
0x4000	AIL_ICTL_IDC_IF	Group containing ICTL IDC Configuration registers	Section 8.6.19
0x4280	AIL_ICTL_PKT_IF	Group containing ICTL Packet Interface Configuration registers	Section 8.6.20
0x5000	AIL_UAT_GEN_CTL	Run bit for all uAT timers and BCN registers	Section 8.6.21
0x5010	AIL_UAT_AIL_REGS	BCN related Registers which are for AIL use only. (not used for DIO or AID2)	Section 8.6.22
0x5080	AIL_UAT_EGR_RADT	Egress RADT registers	Section 8.6.23
0x5100	AIL_UAT_ING_RADT	Ingress RADT registers	Section 8.6.24
0x5200	AIL_UAT_RADT_EVT	(Unused for AIL) RADT event compare registers for Frame strobe and iteration strobe counter config for 4sample Iteration strobe. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress	Section 8.6.25

Table 8-510. AIL Register Groups (continued)

Offset	Acronym	Description	Section
0x8000	AIL_IQ_EDC_REGISTER_GROUP	Group containing EDC Configuration registers	Section 8.6.26
0xA000	AIL_IQ_INGRESS_VBUS_MMR _GROUP	Group containing VBUS Ingress IQ MMR registers	Section 8.6.27
0xB000	AIL_ECTL_REGISTER_GROUP	Group containing ECTL Configuration registers	Section 8.6.28
0xC000	AIL_CTL_INGRESS_VBUS_MMR _GROUP	Group containing VBUS Ingress CTL MMR registers	Section 8.6.29
0x2_0000	AIL_PE_COMMON	Group containing IQN_AIL_PE GLOBAL & AxC & OBSAI_Pkt configuration registers which are used for both OBSAI and CPRI operating modes	Section 8.6.30
0x2_0200	AIL_PE_OBSAI_HEADER_LUT	Group containing IQN_AIL_PE OBSAI_Pkt LUT, a RAM based set of MMRs which control the OBSAI header for each channel.	Section 8.6.31
0x2_1000	AIL_PE_CPRI_CW	Group containing IQN_AIL_PE CPRI CW configuration registers	Section 8.6.32
0x2_8100	AIL_PD_COMMON_CHAN_CFG	PD Common channel registers	Section 8.6.33
0x2_8800	AIL_PD_CPRI_AXC_CFG	PD CPRI AXC registers	Section 8.6.34
0x2_8C00	AIL_PD_CPRI_AXC_TDM_LUT_CFG	PD CPRI AxC TDM RAM	Section 8.6.35
0x2_9000	AIL_PD_CPRI_CW_CFG	PD CPRI CW registers	Section 8.6.36
0x2_A000	AIL_PD_OBSAI_CFG	PD OBSAI control	Section 8.6.37
0x2_A100	AIL_PD_OBSAI_LUT_CFG	PD OBSAI LUTs	Section 8.6.38
0x2_A400	AIL_PD_OBSAI_FRM_MSG_TC_CFG	pd_obsai_frm_msg_tc_cfg RAM	Section 8.6.39
0x3_0000	AIL_phy_glb	Group of Global Configuration Registers	Section 8.6.40
0x3_0040	AIL_phy_rt	Group of RT Registers	Section 8.6.41
0x3_0080	AIL_phy_ci_lut	Group of CI LUT Registers	Section 8.6.42
0x3_00C0	AIL_phy_co_lut	Group of CO LUT Registers	Section 8.6.43
0x3_0100	AIL_phy_ci_lut_a	Group of CI LUT A Registers	Section 8.6.44
0x3_0140	AIL_phy_ci_lut_b	Group of CI LUT B Registers	Section 8.6.45
0x3_0180	AIL_phy_co_lut_a	Group of CO LUT A Registers	Section 8.6.46
0x3_01C0	AIL_phy_co_lut_b	Group of CO LUT B Registers	Section 8.6.47
0x3_0200	AIL_phy_tm	Group of PHY TM Registers	Section 8.6.48
0x3_0280	AIL_phy_rm	PHY RM Registers	Section 8.6.49
0x3_2000	AIL_IQN_AIL_EE_VBUSCLK_EE	IQN_AIL_EE_VBUSCLK EE register group	Section 8.6.50
0x3_4000	AIL_IQN_AIL_EE_SYSCLK_PHY_EE	IQN_AIL_EE_SYSCLK_PHY EE register group	Section 8.6.51
0x3_4800	AIL_IQN_AIL_EE_SYSCLK_EE	IQN_AIL_EE_SYSCLK EE register group	Section 8.6.52

8.6.1 AIL_SI_IQ_EFE_CONFIG_GROUP [Address = 0x0000]

Table 8-511. AIL_SI_IQ_EFE_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x0000	AIL IQ EFE CHANNEL CONFIGURATION REGISTER	IFE DMA Channel Configuration Register	Section 8.6.1.1
0x0200	AIL IQ EFE CONFIGURATION REGISTER	EFE Rx to Tx Loopback Configuration Register	Section 8.6.1.2
0x0240	AIL IQ EFE GLOBAL ENABLE SET REG	Set Global Enable for EFE	Section 8.6.1.3
0x0244	AIL IQ EFE GLOBAL ENABLE CLEAR REG	Clear Global Enable for EFE	Section 8.6.1.4
0x0248	AIL IQ EFE GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, EFE may still be closing out packets.	Section 8.6.1.5
0x0260	AIL IQ EFE CHANNEL ON STATUS REG	Gives current On/Off Status of every available AxC stream. One bit per channel (bit0:ch0 ~ bit31:ch31). Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.6.1.6
0x0280	AIL IQ EFE IN PACKET STATUS REGISTERS	Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP. Not used for DIO SI	Section 8.6.1.7
0x02A0	AIL IQ EFE DMA SYNC STATUS REGISTERS	Gives current DMA SYNC state of AxC channels only. Bits are always zero for OBSAI control channels. Bit is activated when symbol 0 (non-TDD configuation) or first TDD-ON symbol (TDD configuration) of a frame is read from the Residual Buffer and the channel is in the CHAN_ON state. Bit is deactivated on the next SYM/SLOT boundary when channel is disabled or EFE is shutdown. Bit is deactivated immediately when the channel experiences starvation or a protocol error.	Section 8.6.1.8

8.6.1.1 AIL IQ EFE CHANNEL CONFIGURATION REGISTER [Address = 0x0000 + (*S* × 0x0004)]

Size (*S*) = 0:63

IFE DMA Channel Configuration Register

Figure 8-457. AIL IQ EFE CHANNEL CONFIGURATION REGISTER

31 15	14 12	11 9	8 7	6
Reserved	CHAN_RADIO_SEL	Reserved	CHAN_TDD_FRC_OFF	Reserved
NA-0	R/W-0	NA-0	R/W-0	NA-0

5 4	3	2	1	0
AXC_FINE_OFFSET	Reserved	CHAN_ENET_CTL	CHAN_OBSAI_CTL	CHAN_EN
R/W-0	NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-512. AIL IQ EFE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-15	Reserved	RESERVED
14-12	CHAN_RADIO_SEL	Assigns each channel to one of eight radio standard groups. i.e. radio standard 0 may be LTE 20MHz • RS0 (0) = Radio Standard 0 • RS1 (1) = Radio Standard 1 • RS2 (2) = Radio Standard 2 • RS3 (3) = Radio Standard 3 • RS4 (4) = Radio Standard 4 • RS5 (5) = Radio Standard 5 • RS6 (6) = Radio Standard 6 • RS7 (7) = Radio Standard 7
11-9	Reserved	RESERVED
8	CHAN_TDD_FRC_OFF	Alternate TDD mode for controlling TDD also used for GSM Base Band Hopping. APP SW controls updates this bit each symbol of time to control whether the next symbol will be TDD OFF. TDD OFF channels generate no Ingress DMA traffic and expect no Egress DMA traffic. Zeros are sent over the PHY. In BBHop mode, the same applies and in OBSAI, empty_msg is sent over the PHY instead of zeroed traffic • FRC_SYM_OFF (1) = Force symbols off • NO_FRC_OFF_SYM (0) = No forcing off of symbols
7-6	Reserved	RESERVED
5-4	AXC_FINE_OFFSET	Selects sample in a QWD that would be the start of the frame.
3	Reserved	RESERVED
2	CHAN_ENET_CTL	(OBSAI only) ENET mode selection. Assign more space for 8 bit ethernet header that will be attached by PE when set • NON_ENET (0) = Non-ENET mode • ENET (1) = ENET mode
1	CHAN_OBSAI_CTL	(OBSAI only) Selects when OBSAI CTL(Packet) traffic is being passed on an SI_IQ channel (CPRI CTL traffic is passed on the SI_CTL). CTL traffic is on-demand while AxC traffic is streaming. Prevents SI_IQ from activating the starvation handling circuits when packet traffic is unavailable. this also should be set for OBSAI Generic Packet mode • NON_OBSAI_CTL (0) = CPRI or OBSAI AXC traffic • OBSAI_CTL (1) = OBSAI CTL traffic
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.6.1.2 AIL IQ EFE CONFIGURATION REGISTER [Address = 0x0200]

EFE Rx to Tx Loopback Configuration Register

Figure 8-458. AIL IQ EFE CONFIGURATION REGISTER

31	1	0
Reserved		LOOPBACK_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-513. AIL IQ EFE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	LOOPBACK_EN	(TI use Only) 0x1: Ingress data from ICC is looped back to Egress data to ICC. DMA traffic is unused. (i.e. for purpose of DFE only testing)

8.6.1.3 AIL IQ EFE GLOBAL ENABLE SET REG [Address = 0x0240]

Set Global Enable for EFE

Figure 8-459. AIL IQ EFE GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-514. AIL IQ EFE GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.6.1.4 AIL IQ EFE GLOBAL ENABLE CLEAR REG [Address = 0x0244]

Clear Global Enable for EFE

Figure 8-460. AIL IQ EFE GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-515. AIL IQ EFE GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.6.1.5 AIL IQ EFE GLOBAL ENABLE STATUS [Address = 0x0248]

Read Only status of global enable state. Even if this register is OFF, EFE may still be closing out packets.

Figure 8-461. AIL IQ EFE GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-516. AIL IQ EFE GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: efe_ON 0x0:efe_OFF

8.6.1.6 AIL IQ EFE CHANNEL ON STATUS REG [Address = 0x0260 + (*S* × 0x0004)]

Size (*S*) = 0:1

Gives current On/Off Status of every available AxC stream. One bit per channel (bit0:ch0 ~ bit31:ch31). Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-462. AIL IQ EFE CHANNEL ON STATUS REG

31	0
CHAN_ON	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-517. AIL IQ EFE CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.6.1.7 AIL IQ EFE IN PACKET STATUS REGISTERS [Address = 0x0280 + (*S* × 0x0004)]

Size (*S*) = 0:1

Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP. Not used for DIO SI

Figure 8-463. AIL IQ EFE IN PACKET STATUS REGISTERS

31	0
IN_PKT	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-518. AIL IQ EFE IN PACKET STATUS REGISTERS Field Descriptions

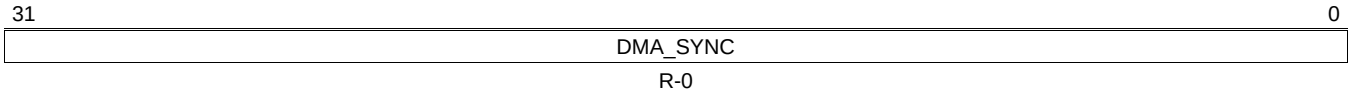
Bits	Name	Description
31-0	IN_PKT	0x1: IN_PKT 0x0:OUT_PKT

8.6.1.8 AIL IQ EFE DMA SYNC STATUS REGISTERS [Address = 0x02A0 + (*S* × 0x0004)]

Size (*S*) = 0:1

Gives current DMA SYNC state of AxC channels only. Bits are always zero for OBSAI control channels. Bit is activated when symbol 0 (non-TDD configuation) or first TDD-ON symbol (TDD configuration) of a frame is read from the Residual Buffer and the channel is in the CHAN_ON state. Bit is deactivated on the next SYM/SLOT boundary when channel is disabled or EFE is shutdown. Bit is deactivated immediately when the channel experiences starvation or a protocol error.

Figure 8-464. AIL IQ EFE DMA SYNC STATUS REGISTERS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-519. AIL IQ EFE DMA SYNC STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-0	DMA_SYNC	0x1: DMA synchronized to radio timing for this channel 0x0:DMA not synchronized to radio timing for this channel. Channel is in in re-sync mode.

8.6.2 AIL_SI_IQ_EFE_RADIO_STANDARD_GROUP [Address = 0x0400]

Table 8-520. AIL_SI_IQ_EFE_RADIO_STANDARD_GROUP

Offset	Acronym	Register Description	Section
0x0400	AIL IQ EFE FRAME COUNT REGISTER	EFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants	Section 8.6.2.1
0x0420	AIL SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER	EFE Radio Standard Configuration Register	Section 8.6.2.2
0x0440	AIL IQ EFE RADIO STANDARD 0 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.3
0x0460	AIL IQ EFE RADIO STANDARD 1 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.4
0x0480	AIL IQ EFE RADIO STANDARD 2 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.5
0x04A0	AIL IQ EFE RADIO STANDARD 3 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.6
0x04C0	AIL IQ EFE RADIO STANDARD 4 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.7
0x04E0	AIL IQ EFE RADIO STANDARD 5 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.8
0x0500	AIL IQ EFE RADIO STANDARD 6 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.9
0x0520	AIL IQ EFE RADIO STANDARD 7 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.2.10

8.6.2.1 AIL IQ EFE FRAME COUNT REGISTER [Address = 0x0400 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants

Figure 8-465. AIL IQ EFE FRAME COUNT REGISTER

31 24	23 16	15 8	7 0
Reserved	INDEX_TC	INDEX_SC	SYM_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-521. AIL IQ EFE FRAME COUNT REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	INDEX_TC	Radio Framing Counter. Index Counter Terminal Count. Index counter terminal count which is the last value of the Index Counter before it wraps. For simple use case, program same as frm_sym_tc.
15-8	INDEX_SC	Radio Framing Counter. Index Counter Starting Location. Starting location of the Sample Terminal Count LUT loaded into the Index Counter when it first starts and each time it wraps. Depending on the radio standard, the index will wrap once per radio frame such as WCDMA or multiple times per frame as in LTE. Index is the address for XXX_IQ_EFE_FRM_SAMP_TC
7-0	SYM_TC	Radio Framing Counter. Symbol Count. Number of symbols per frame programmed as a terminal count.

8.6.2.2 AIL SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER [Address = 0x0420 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Radio Standard Configuration Register

Figure 8-466. AIL SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER

31	11	10	9	8	7	0
Reserved		GSM_CMP_MODE	GSM_AXC_BBHOP_MODE	TDD_LUT_EN	TDD_FIRST_SYM	
NA-0		R/W-0	R/W-0	R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-522. AIL SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-11	Reserved	RESERVED
10	GSM_CMP_MODE	Enables GSM Compressed mode • ENABLED (1) = GSM Compression enabled for this radio standard • DISABLED (0) = GSM Compression disabled for this radio standard
9	GSM_AXC_BBHOP_MODE	Enables Base-band Hopping mode • ENABLED (1) = GSM Baseband hopping enabled for this radio standard • DISABLED (0) = GSM Baseband hopping disabled for this radio standard
8	TDD_LUT_EN	Enable use of iq_efe_tdd_en_cfg and use of TDD_FIRST_SYM. Does not impact CHAN_TDD_FRC_OFF operation (which does not use TDD_FIRST_SYM) • ENABLED (1) = TDD enabled for this radio standard • DISABLED (0) = TDD disabled for this radio standard
7-0	TDD_FIRST_SYM	Selects first symbol to start TDD

8.6.2.3 AIL IQ EFE RADIO STANDARD 0 TDD ENABLE LUT [Address = 0x0440 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-467. AIL IQ EFE RADIO STANDARD 0 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-523. AIL IQ EFE RADIO STANDARD 0 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.4 AIL IQ EFE RADIO STANDARD 1 TDD ENABLE LUT [Address = 0x0460 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-468. AIL IQ EFE RADIO STANDARD 1 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-524. AIL IQ EFE RADIO STANDARD 1 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.5 AIL IQ EFE RADIO STANDARD 2 TDD ENABLE LUT [Address = 0x0480 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-469. AIL IQ EFE RADIO STANDARD 2 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-525. AIL IQ EFE RADIO STANDARD 2 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.6 AIL IQ EFE RADIO STANDARD 3 TDD ENABLE LUT [Address = 0x04A0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-470. AIL IQ EFE RADIO STANDARD 3 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-526. AIL IQ EFE RADIO STANDARD 3 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.7 AIL IQ EFE RADIO STANDARD 4 TDD ENABLE LUT [Address = 0x04C0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-471. AIL IQ EFE RADIO STANDARD 4 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-527. AIL IQ EFE RADIO STANDARD 4 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.8 AIL IQ EFE RADIO STANDARD 5 TDD ENABLE LUT [Address = 0x04E0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-472. AIL IQ EFE RADIO STANDARD 5 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-528. AIL IQ EFE RADIO STANDARD 5 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.9 AIL IQ EFE RADIO STANDARD 6 TDD ENABLE LUT [Address = 0x0500 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-473. AIL IQ EFE RADIO STANDARD 6 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-529. AIL IQ EFE RADIO STANDARD 6 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.2.10 AIL IQ EFE RADIO STANDARD 7 TDD ENABLE LUT [Address = 0x0520 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-474. AIL IQ EFE RADIO STANDARD 7 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-530. AIL IQ EFE RADIO STANDARD 7 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.3 AIL_IQ_EFE_CHAN_AXC_OFFSET [Address = 0x0600 + (*R* × 0x0004)]

Table 8-531. AIL_IQ_EFE_CHAN_AXC_OFFSET

Offset	Acronym	Register Description	Section
0x0600 + (*R* × 0x0004)	AIL IQ EFE CHANNEL AXC OFFSET REG	Sets the AXC offset for each channel.	Section 8.6.3.1

8.6.3.1 AIL IQ EFE CHANNEL AXC OFFSET REG [Address = 0x0600 + (*R* × 0x0004)]

Range (*R*) = 0:63

Sets the AXC offset for each channel.

Figure 8-475. AIL IQ EFE CHANNEL AXC OFFSET REG

31 25	24 0
Reserved	AXC_OFFSET
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-532. AIL IQ EFE CHANNEL AXC OFFSET REG Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	AXC_OFFSET	AxC-by-AxC delay control. Allows different timing alignments for each AxC. DIO & AID: this is a 4 sample offset relative to the group or TDM of AxC. AIL CPRI: this is a sample offset relative to the CPRI AxC Group. AIL OBSAI: this is a Radio Timer compare value (unit is sys_clk). Other than OBSAI, for most customer applications, these fields are programmed as zero.

8.6.4 AIL_IQ_EFE_FRM_SAMP_TC_MMR_RAM [Address = 0x0800 + (R × 0x0004)]

Table 8-533. AIL_IQ_EFE_FRM_SAMP_TC_MMR_RAM

Offset	Acronym	Register Description	Section
0x0800 + (*R* × 0x0004)	AIL IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER	EFE AxC Radio Framing Sample Terminal Count Configuration Register	Section 8.6.4.1

8.6.4.1 AIL IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER [Address = 0x0800 + (R × 0x0004)]

Range (*R*) = 0:255

EFE AxC Radio Framing Sample Terminal Count Configuration Register

Figure 8-476. AIL IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER

31	18	17	0
Reserved		SAMP_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-534. AIL IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-18	Reserved	Reserved
17-0	SAMP_TC	Radio Framing Counter. Number of samples (4 Bytes) per radio symbol programmed as a terminal count

8.6.5 AIL_SI_IQ_E_TDM_LUT_RAM [Address = 0x0C00 + (R × 0x0004)]

Table 8-535. AIL_SI_IQ_E_TDM_LUT_RAM

Offset	Acronym	Register Description	Section
0x0C00 + (*R* × 0x0004)	AIL SI PE AXC TDM LOOK_UP_TABLE	TDM AxC LUT. CPRI: Used to map steams of CPRI containers to appropriate AxC. AxC are listed in TDM order within each group (radio standard). Different portions of LUT allocated to different groups (radio standards). OBSAI: AxC are listed in TDM order per OBSAI DBMR. Different portions of LUT are allocated to different DBMR.	Section 8.6.5.1

8.6.5.1 AIL SI PE AXC TDM LOOK_UP_TABLE [Address = 0x0C00 + (R × 0x0004)]

Range (*R*) = 0:255

TDM AxC LUT.

CPRI: Used to map steams of CPRI containers to appropriate AxC. AxC are listed in TDM order within each group (radio standard). Different portions of LUT allocated to different groups (radio standards).

OBSAI: AxC are listed in TDM order per OBSAI DBMR. Different portions of LUT are allocated to different DBMR.

Figure 8-477. AIL SI PE AXC TDM LOOK_UP_TABLE

31	8	7	6	5	0
Reserved		EN	Reserved	AXC	
NA-0		R/W-0	NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-536. AIL SI PE AXC TDM LOOK_UP_TABLE Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7	EN	Enables each entry. Disabled entries will result in zeroed CPRI containers. This disable used when application SW is not required to maintain unique AxC value for unused containers.
6	Reserved	RESERVED
5-0	AXC	List of AxC indexes giving TDM AxC order over CPRI or OBSAI link

8.6.6 AIL_SI_IQ_E_SCH_PHY [Address = 0x1000]

Table 8-537. AIL_SI_IQ_E_SCH_PHY

Offset	Acronym	Register Description	Section
0x1000	AIL SI PE PHY CONFIGURATION REGISTER	PE PHY enable Register	Section 8.6.6.1
0x1004	AIL SI PE PHY STATUS REGISTER	PE PHY status Register	Section 8.6.6.2

8.6.6.1 AIL SI PE PHY CONFIGURATION REGISTER [Address = 0x1000]

PE PHY enable Register

Figure 8-478. AIL SI PE PHY CONFIGURATION REGISTER

31	1	0
Reserved		PHY_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-538. AIL SI PE PHY CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	PHY_EN	SI Egress AIL scheduler, PHY FSM is enabled to turn ON, will turn on next PE_FB from uAT

8.6.6.2 AIL SI PE PHY STATUS REGISTER [Address = 0x1004]

PE PHY status Register

Figure 8-479. AIL SI PE PHY STATUS REGISTER

31	1	0
Reserved		PHY_ON
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-539. AIL SI PE PHY STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	PHY_ON	SI Egress AIL scheduler, active high, indicating that the PE PHY is in ON state. PE PHY will only turn ON/OFF on PE_FB boundaries.

8.6.7 AIL_SI_IQ_E_OBSAI_MODTXRULE [Address = 0x1080]

Table 8-540. AIL_SI_IQ_E_OBSAI_MODTXRULE

Offset	Acronym	Register Description	Section
0x1080	AIL SI PE OBSAI MODULO TRANSMIT RULE CONFIGURATION REGISTER	PE Modulo Terminal Count Register	Section 8.6.7.1

8.6.7.1 AIL SI PE OBSAI MODULO TRANSMIT RULE CONFIGURATION REGISTER [Address = 0x1080 + (*S* × 0x0004)]

Size (*S*) = 0:31

PE Modulo Terminal Count Register

Figure 8-480. AIL SI PE OBSAI MODULO TRANSMIT RULE CONFIGURATION REGISTER

31 28	27 16	15 14	13	12	11 0
Reserved	RULE_INDEX	Reserved	RULE_CTL_MSG	RULE_EN	RULE_MOD
NA-0	R/W-0	NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-541. AIL SI PE OBSAI MODULO TRANSMIT RULE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-16	RULE_INDEX	Index. Transmission Rule. Index indicates at which count the rule will fire.
15-14	Reserved	RESERVED
13	RULE_CTL_MSG	1: Module Rule operations on OBSAI control messages 0: AxC messages
12	RULE_EN	Transmission Rule Enable.
11-0	RULE_MOD	Modulo Terminal count of the rule counter. Dictates the period of the rule. Terminal count is the OBSAI Modulo minus 1.

8.6.8 AIL_SI_IQ_E_OBSAI_DBM_RULE_RAM [Address = 0x1100 + (R × 0x0008)]

Table 8-542. AIL_SI_IQ_E_OBSAI_DBM_RULE_RAM

Offset	Acronym	Register Description	Section
0x1100 + (*R* × 0x0008)	AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART0	PE OBSAI DBMF Register. OBSAI DBM counts through quad-samples (16 bytes per AxC)	Section 8.6.8.1
0x1104 + (*R* × 0x0008)	AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART1	PE OBSAI DBMF Register. OBSAI DBM counts through quad-samples (16 bytes per AxC)	Section 8.6.8.2

8.6.8.1 AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART0 [Address = 0x1100 + (R × 0x0008)]

Range (*R*) = 0:31

PE OBSAI DBMF Register. OBSAI DBM counts through quad-samples (16 bytes per AxC)

Figure 8-481. AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART0

31 21	20 16	15	14 8	7	6 3	2 1	0
Reserved	DBM_1MULT	Reserved	DBM_X	Reserved	DBM_RADSTD	Reserved	DBM_EN
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-543. AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART0 Field Descriptions

Bits	Name	Description
31-21	Reserved	RESERVED
20-16	DBM_1MULT	DBMF repetitions of map1. (Set N-1)
15	Reserved	RESERVED
14-8	DBM_X	DBMF max number of supported channels. It is Max number, because not all channel position need to be enabled, but still needed to correctly space out the rule. (Set N-1)
7	Reserved	RESERVED
6-3	DBM_RADSTD	Radio Standard 0-7 corresponding to the given rule. Controls which RADT to be used flr AxC_Offset comparison. Highly recommended to use a single rule per radio standard to simplify AxC_Offset calculations
2-1	Reserved	RESERVED
0	DBM_EN	DBMF Enable: When disabled and MOD rule fires, first AxC LUT entry is used and other DBM programming is disregarded

8.6.8.2 AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART1 [Address = 0x1104 + (*R* × 0x0008)]

Range (*R*) = 0:31

PE OBSAI DBMF Register. OBSAI DBM counts through quad-samples (16 bytes per AxC)

Figure 8-482. AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART1

31	30 24	23 16	15	14 8	7	6 0
Reserved	DBM_XBUBBLE	DBM_LUTSTRT	Reserved	DBM _2SIZE	Reserved	DBM _1SIZE
NA-0	R/W-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-544. AIL SI PE OBSAI DUAL BIT MAP RULE CONFIGURATION REGISTER PART1 Field Descriptions

Bits	Name	Description
31	Reserved	RESERVED
30-24	DBM_XBUBBLE	Normally programmed to 0 corresponding to 1 bubble when a bubble is indicated by Map1 or Map2 pattern. This feature allows a burst of bubbles to be inserted. Burst length indicated by this field
23-16	DBM_LUTSTRT	DBMF Starting address (index of array) for PE AXC TDM LUT RAM. LUT is shared by all 32 DBM rules. Starting address indicates where pattern for this rule starts
15	Reserved	RESERVED
14-8	DBM_2SIZE	DBMF number of bits of bit map2 to use. (Set N) NOTE: programming a value of 0x0 effectively disables Map2
7	Reserved	RESERVED
6-0	DBM_1SIZE	DBMF number of bits of bit map1 to use. (Set N-1)

8.6.9 AIL_SI_IQ_E_OBSAI_DBM_BITMAP_RAM [Address = 0x1400 + (R × 0x0004)]

Table 8-545. AIL_SI_IQ_E_OBSAI_DBM_BITMAP_RAM

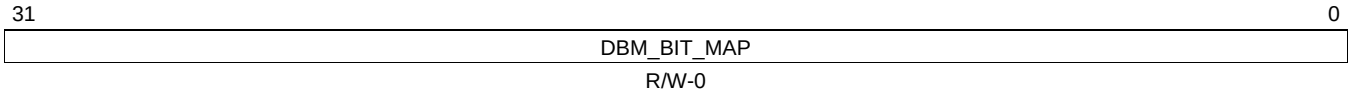
Offset	Acronym	Register Description	Section
0x1400 + (*R* × 0x0004)	AIL SI PE OBSAI DUAL BIT MAP RULE, BIT MAP LOOK_UP_TABLE	PE DBMF Bit Map 1 & 2 Register, eight locations for each of 32 different rules (3 address LSBs address 0-7 entries per each of 64 rules) (bit_2==0: bit map1 bit_2==1: bit map2. 000:map1(31:0) 001:map1(63:32) 010:map1(95:64) 011:map1(127:96) 100:map2(31:0) 101:map2(63:32) 110:map2(95:64) 111:unused	Section 8.6.9.1

8.6.9.1 AIL SI PE OBSAI DUAL BIT MAP RULE, BIT MAP LOOK_UP_TABLE [Address = 0x1400 + (R × 0x0004)]

Range (*R*) = 0:255

PE DBMF Bit Map 1 & 2 Register, eight locations for each of 32 different rules (3 address LSBs address 0-7 entries per each of 64 rules) (bit_2==0: bit map1 bit_2==1: bit map2. 000:map1(31:0) 001:map1(63:32) 010:map1(95:64) 011:map1(127:96) 100:map2(31:0) 101:map2(63:32) 110:map2(95:64) 111:unused

Figure 8-483. AIL SI PE OBSAI DUAL BIT MAP RULE, BIT MAP LOOK_UP_TABLE



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-546. AIL SI PE OBSAI DUAL BIT MAP RULE, BIT MAP LOOK_UP_TABLE Field Descriptions

Bits	Name	Description
31-0	DBM_BIT_MAP	DBMF bit map 1&2

8.6.10 AIL_SI_IQ_E_SCH_CPRI [Address = 0x1800]

Table 8-547. AIL_SI_IQ_E_SCH_CPRI

Offset	Acronym	Register Description	Section
0x1800	AIL SI PE CPRI CONFIGURATION REGISTER	PE CPRI container terminal count register	Section 8.6.10.1
0x1820	AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART1	One-to-one mapping to each radio standard, CPRI Mapping Method 3, Bubble insertion state machine control for total of 8 separate FSMs, one per 8 groups/radio_standards	Section 8.6.10.2
0x1840	AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART2	One-to-one mapping to each radio standard, CPRI Mapping Method 3, Bubble insertion state machine control for total of 8 separate FSMs, one per 8 groups/radio_standards. If there are any bubbles present, bub_gap indicates space between bubbles. Program BUB_GAP_INT .GE. KNC for no bubbles	Section 8.6.10.3
0x1860	AIL SI PE CPRI TDM FSM CONFIGURATION REGISTER	One-to-one mapping to each radio standard, CPRI AxC TDM. Intended use is one TDM FSM per radio standard (matching AIL_PHY_CI groups)	Section 8.6.10.4
0x1880	AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART0	Enables each individual radio standard for the PD for up to 8 radio standards	Section 8.6.10.5
0x18A0	AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART1	Defines the Radio Standard level Offset per radio standard. Relative to the PHY SOF. In units of basic frames and hyperframes.	Section 8.6.10.6
0x18C0	AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART2	Defines the number of Basic Frames per radio standard frame. i.e. 38,400 (set 38,399) for LTE & WCDMA	Section 8.6.10.7
0x18E0	AIL SI PE CPRI RADIO STANDARD STATUS REGISTER	Read Only status of each radio status reflecting enable and satisfying basic frame offset	Section 8.6.10.8
0x1900	AIL SI PE CPRI CONTAINER LOOK_UP_TABLE	PE CPRI PHY Container LUT: Maps CPRI containers within a basic frame to 1 of 8 groups (radio standard). LUT replays each basic frame. Only CPRI16x can use full 64 depth of LUT	Section 8.6.10.9

8.6.10.1 AIL SI PE CPRI CONFIGURATION REGISTER [Address = 0x1800]

PE CPRI container terminal count register

Figure 8-484. AIL SI PE CPRI CONFIGURATION REGISTER

31	7	6	0
Reserved		AXC_CONT_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-548. AIL SI PE CPRI CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-7	Reserved	RESERVED
6-0	AXC_CONT_TC	Indicating how many CPRI AxC containers are supported within each basic frame. Value must be consistently programmed with AIL_PHY_Egress programmed values or erroneous operation will result.. Programmed values 0-to-63 correspond to length 1-to-64. Circuit using this value, sample and hold the value for each PHY frame allowing SW to change the value between frames.

8.6.10.2 AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART1 [Address = 0x1820 + (*S* × 0x0004)]

Size (*S*) = 0:7

One-to-one mapping to each radio standard, CPRI Mapping Method 3, Bubble insertion state machine control for total of 8 separate FSMs, one per 8 groups/radio_standards

Figure 8-485. AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART1

31	14	13	0
KNC		Reserved	
R/W-0		NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-549. AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART1 Field Descriptions

Bits	Name	Description
31-14	KNC	(K x Nc) total number of containers per AxC container group(block). if the bubble FSM is not used, this should be matched with ncont value in TDM FSM config. Set N-1
13-0	Reserved	RESERVED

8.6.10.3 AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART2 [Address = 0x1840 + (*S* × 0x0004)]

Size (*S*) = 0:7

One-to-one mapping to each radio standard, CPRI Mapping Method 3, Bubble insertion state machine control for total of 8 separate FSMs, one per 8 groups/radio_standards. If there are any bubbles present, bub_gap indicates space between bubbles. Program BUB_GAP_INT .GE. KNC for no bubbles

Figure 8-486. AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART2

31	30	29	12	11	0
Reserved		GAP_INT		GAP_FRAC	
NA-0		R/W-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-550. AIL SI PE CPRI BUBBLE FSM CONFIGURATION REGISTER PART2 Field Descriptions

Bits	Name	Description
31-30	Reserved	RESERVED
29-12	GAP_INT	fsm-by-fsm, integer number of containers between bubbles. set equal or bigger value to KNC,if no bubble is required. Algorithm rewinds at the beginning of each AxC Container Block
11-0	GAP_FRAC	fsm-by-fsm, fractional number of containers between bubbles. set 0 means zero. (i.e. Set 25 for 0.25) Value is accumulated every bubble, in this way, a non-zero fraction eventually accumulates into the integer field

8.6.10.4 AIL SI PE CPRI TDM FSM CONFIGURATION REGISTER [Address = 0x1860 + (*S* × 0x0004)]

Size (*S*) = 0:7

One-to-one mapping to each radio standard, CPRI AxC TDM. Intended use is one TDM FSM per radio standard (matching AIL_PHY_CI groups)

Figure 8-487. AIL SI PE CPRI TDM FSM CONFIGURATION REGISTER

31 24	23 16	15 8	7 0
Reserved	LUTSTRT	NCONT	Reserved
NA-0	R/W-0	R/W-0	NA-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-551. AIL SI PE CPRI TDM FSM CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	LUTSTRT	first TDM_LUT entry for this fsm. Effectively controls how the table is shared between up to 8 groups or fsm
15-8	NCONT	number of TDM_LUT entries for this FSM.(Set N-1) For each LTE20, 8 sequential entries within TDM_LUT used.
7-0	Reserved	RESERVED

8.6.10.5 AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART0 [Address = 0x1880 + (*S* × 0x0004)]

Size (*S*) = 0:7

Enables each individual radio standard for the PD for up to 8 radio standards

Figure 8-488. AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART0

31	1	0
Reserved		EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-552. AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART0 Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EN	Enable bit for the corresponding radio standard

8.6.10.6 AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART1 [Address = 0x18A0 + (*S* × 0x0004)]

Size (*S*) = 0:7

Defines the Radio Standard level Offset per radio standard. Relative to the PHY SOF. In units of basic frames and hyperframes.

Figure 8-489. AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART1

31 16	15 8	7 0
Reserved	HFRM_OFFSET	BFRM_OFFSET
NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-553. AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART1 Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-8	HFRM_OFFSET	Hyper Frame Index of Radio Standard Offset
7-0	BFRM_OFFSET	Basic Frame Index of Radio Standard Offset

8.6.10.7 AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART2 [Address = 0x18C0 + (*S* × 0x0004)]

Size (*S*) = 0:7

Defines the number of Basic Frames per radio standard frame. i.e. 38,400 (set 38,399) for LTE & WCDMA

Figure 8-490. AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART2

31	18	17	0
Reserved		BFRM_NUM	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-554. AIL SI PE CPRI RADIO STANDARD CONFIGURATION REGISTER PART2 Field Descriptions

Bits	Name	Description
31-18	Reserved	RESERVED
17-0	BFRM_NUM	Number of Basic Frames in a Radio Standard. Set N-1

8.6.10.8 AIL SI PE CPRI RADIO STANDARD STATUS REGISTER [Address = 0x18E0 + (*S* × 0x0004)]

Size (*S*) = 0:7

Read Only status of each radio status reflecting enable and satisfying basic frame offset

Figure 8-491. AIL SI PE CPRI RADIO STANDARD STATUS REGISTER

31	1	0
Reserved		ON
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-555. AIL SI PE CPRI RADIO STANDARD STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ON	0x1: RADSTD_ON 0x0:RADSTD_OFF

8.6.10.9 AIL SI PE CPRI CONTAINER LOOK_UP_TABLE [Address = 0x1900 + (*S* × 0x0004)]

Size (*S*) = 0:63

PE CPRI PHY Container LUT: Maps CPRI containers within a basic frame to 1 of 8 groups (radio standard). LUT replays each basic frame. Only CPRI16x can use full 64 depth of LUT

Figure 8-492. AIL SI PE CPRI CONTAINER LOOK_UP_TABLE

31	4	3	2	0
Reserved		LUT_EN	LUT_GRP	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-556. AIL SI PE CPRI CONTAINER LOOK_UP_TABLE Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3	LUT_EN	Enable or Disable of each container, even if disabled, CONT_LUT_GRP must be programmed correctly • CONT_DIS (0) = container is unused by PE. Later AxC LUT entry will be unused. PHY will be driven with zero for this container • CONT_EN (1) = container is mapped by cont_lut_grp
2-0	LUT_GRP	Group (radio standard) which container belongs to, 0-to-7. When programming must exactly match the AIL_PHY_CO programmed operation.

8.6.11 AIL_IQ_IFE_CHANNEL_CONFIGURATION_GROUP [Address = 0x2000]

Table 8-557. AIL_IQ_IFE_CHANNEL_CONFIGURATION_GROUP

Offset	Acronym	Register Description	Section
0x2000	AIL IQ IFE CHANNEL CONFIGURATION REGISTER	IFE DMA Channel Configuration Register	Section 8.6.11.1

8.6.11.1 AIL IQ IFE CHANNEL CONFIGURATION REGISTER [Address = 0x2000 + (*S* × 0x0004)]

Size (*S*) = 0:63

IFE DMA Channel Configuration Register

Figure 8-493. AIL IQ IFE CHANNEL CONFIGURATION REGISTER

31	11	10	9	8
Reserved		CHAN_ENET_CTL	CHAN_OBSAI_CTL	CHAN_TDD_FRC_OFF
NA-0		R/W-0	R/W-0	R/W-0

7	6	4	3	2	1	0
Reserved	CHAN_RADIO_SEL		CHAN_AXC_OFFSET		Reserved	CHAN_EN
NA-0	R/W-0		R/W-0		NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-558. AIL IQ IFE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-11	Reserved	RESERVED
10	CHAN_ENET_CTL	(OBSAI only) Selects between OBSAI ENET when high or OBSAI NON_ENET when low. Only valid when CHAN_OBSAI_CTL is set • ENET (1) = Enet mode • NON_ENET (0) = Non Enet mode
9	CHAN_OBSAI_CTL	(OBSAI only) Selects when OBSAI CTL traffic is being passed on an SI_IQ channel. CTL traffic is on-demand while AxC traffic is streaming. Prevents SI_IQ from activating the starvation handling circuits when packet traffic is unavailable. • OBSAI_CTL (1) = OBSAI CTL traffic • NON_OBSAI_CTL (0) = CPRI or OBSAI AXC traffic
8	CHAN_TDD_FRC_OFF	Forces a channel into the TDD OFF state on the next symbol after it is set to a 1 regardless of the TDD configuration of the radio standard variant the channel is assigned to. • FRC_SYM_OFF (1) = Force symbols off • NO_FRC_OFF_SYM (0) = No forcing off of symbols
7	Reserved	RESERVED
6-4	CHAN_RADIO_SEL	Radio Standard Select for channel • RS0 (0) = Radio Standard 0 • RS1 (1) = Radio Standard 1 • RS2 (2) = Radio Standard 2 • RS3 (3) = Radio Standard 3 • RS4 (4) = Radio Standard 4 • RS5 (5) = Radio Standard 5 • RS6 (6) = Radio Standard 6 • RS7 (7) = Radio Standard 7
3-2	CHAN_AXC_OFFSET	Fine AxC Offset within Quad Word • NONE (0) = No offset • ONE (1) = One sample offset • TWO (2) = Two sample offset • THREE (3) = Three sample offset
1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.6.12 AIL_IQ_IFE_RADIO_STANDARD_GROUP [Address = 0x2200]

Table 8-559. AIL_IQ_IFE_RADIO_STANDARD_GROUP

Offset	Acronym	Register Description	Section
0x2200	AIL IQ IFE FRAME COUNT REGISTER	IFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants	Section 8.6.12.1
0x2220	AIL IQ IFE RADIO STANDARD CONFIGURATION REGISTER	IFE Radio Standard Configuration Register	Section 8.6.12.2
0x2240	AIL IQ IFE RADIO STANDARD 0 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.3
0x2260	AIL IQ IFE RADIO STANDARD 1 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.4
0x2280	AIL IQ IFE RADIO STANDARD 2 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.5
0x22A0	AIL IQ IFE RADIO STANDARD 3 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.6
0x22C0	AIL IQ IFE RADIO STANDARD 4 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.7
0x22E0	AIL IQ IFE RADIO STANDARD 5 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.8
0x2300	AIL IQ IFE RADIO STANDARD 6 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.9
0x2320	AIL IQ IFE RADIO STANDARD 7 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.6.12.10

8.6.12.1 AIL IQ IFE FRAME COUNT REGISTER [Address = 0x2200 + (*S* × 0x0004)]

Size (*S*) = 0:7

IFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants

Figure 8-494. AIL IQ IFE FRAME COUNT REGISTER

31 24	23 16	15 8	7 0
Reserved	INDEX_TC	INDEX_SC	SYM_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-560. AIL IQ IFE FRAME COUNT REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	INDEX_TC	Radio Framing Counter. Index Counter Terminal Count. Index counter terminal count which is the last value of the Index Counter before it wraps. For simple use case, program same as frm_sym_tc.
15-8	INDEX_SC	Radio Framing Counter. Index Counter Starting Location. Starting location of the Sample Terminal Count LUT loaded into the Index Counter when it first starts and each time it wraps.
7-0	SYM_TC	Radio Framing Counter. Symbol Count. Number of symbols per frame programmed as a terminal count.

8.6.12.2 AIL IQ IFE RADIO STANDARD CONFIGURATION REGISTER [Address = 0x2220 + (*S* × 0x0004)]

Size (*S*) = 0:7

IFE Radio Standard Configuration Register

Figure 8-495. AIL IQ IFE RADIO STANDARD CONFIGURATION REGISTER

31	1	0
Reserved		TDD_LUT_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-561. AIL IQ IFE RADIO STANDARD CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	TDD_LUT_EN	Enable TDD • ENABLED (1) = TDD enabled for this radio standard • DISABLED (0) = TDD disabled for this radio standard

8.6.12.3 AIL IQ IFE RADIO STANDARD 0 TDD ENABLE LUT [Address = 0x2240 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-496. AIL IQ IFE RADIO STANDARD 0 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-562. AIL IQ IFE RADIO STANDARD 0 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.4 AIL IQ IFE RADIO STANDARD 1 TDD ENABLE LUT [Address = 0x2260 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-497. AIL IQ IFE RADIO STANDARD 1 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-563. AIL IQ IFE RADIO STANDARD 1 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.5 AIL IQ IFE RADIO STANDARD 2 TDD ENABLE LUT [Address = 0x2280 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-498. AIL IQ IFE RADIO STANDARD 2 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-564. AIL IQ IFE RADIO STANDARD 2 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.6 AIL IQ IFE RADIO STANDARD 3 TDD ENABLE LUT [Address = 0x22A0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-499. AIL IQ IFE RADIO STANDARD 3 TDD ENABLE LUT

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-565. AIL IQ IFE RADIO STANDARD 3 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.7 AIL IQ IFE RADIO STANDARD 4 TDD ENABLE LUT [Address = 0x22C0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-500. AIL IQ IFE RADIO STANDARD 4 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-566. AIL IQ IFE RADIO STANDARD 4 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.8 AIL IQ IFE RADIO STANDARD 5 TDD ENABLE LUT [Address = 0x22E0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-501. AIL IQ IFE RADIO STANDARD 5 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-567. AIL IQ IFE RADIO STANDARD 5 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.9 AIL IQ IFE RADIO STANDARD 6 TDD ENABLE LUT [Address = 0x2300 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-502. AIL IQ IFE RADIO STANDARD 6 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-568. AIL IQ IFE RADIO STANDARD 6 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.12.10 AIL IQ IFE RADIO STANDARD 7 TDD ENABLE LUT [Address = 0x2320 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-503. AIL IQ IFE RADIO STANDARD 7 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-569. AIL IQ IFE RADIO STANDARD 7 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.6.13 AIL_IQ_IFE_CONFIG_GROUP [Address = 0x2340]

Table 8-570. AIL_IQ_IFE_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x2340	AIL IQ IFE GLOBAL ENABLE SET REG	Set Global Enable for IFE	Section 8.6.13.1
0x2344	AIL IQ IFE GLOBAL ENABLE CLEAR REG	Clear Global Enable for IFE	Section 8.6.13.2
0x2348	AIL IQ IFE GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, IFE may still be closing out packets.	Section 8.6.13.3
0x2350	AIL IQ IFE CHANNEL ON STATUS REG	Gives current On/Off Status of every available AxC stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.6.13.4
0x2360	AIL IQ IFE IN PACKET STATUS REGISTERS	Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP.	Section 8.6.13.5

8.6.13.1 AIL IQ IFE GLOBAL ENABLE SET REG [Address = 0x2340]

Set Global Enable for IFE

Figure 8-504. AIL IQ IFE GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-571. AIL IQ IFE GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.6.13.2 AIL IQ IFE GLOBAL ENABLE CLEAR REG [Address = 0x2344]

Clear Global Enable for IFE

Figure 8-505. AIL IQ IFE GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-572. AIL IQ IFE GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.6.13.3 AIL IQ IFE GLOBAL ENABLE STATUS [Address = 0x2348]

Read Only status of global enable state. Even if this register is OFF, IFE may still be closing out packets.

Figure 8-506. AIL IQ IFE GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-573. AIL IQ IFE GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ife_ON 0x0:ife_OFF

8.6.13.4 AIL IQ IFE CHANNEL ON STATUS REG [Address = 0x2350 + (*S* × 0x0004)]

Size (*S*) = 0:1

Gives current On/Off Status of every available AxC stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-507. AIL IQ IFE CHANNEL ON STATUS REG

31	0
CHAN_ON	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-574. AIL IQ IFE CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.6.13.5 AIL IQ IFE IN PACKET STATUS REGISTERS [Address = 0x2360 + (*S* × 0x0004)]

Size (*S*) = 0:1

Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP.

Figure 8-508. AIL IQ IFE IN PACKET STATUS REGISTERS

31	0
IN_PKT	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-575. AIL IQ IFE IN PACKET STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-0	IN_PKT	0x1: IN_PKT 0x0:OUT_PKT

8.6.14 AIL_IQ_IDC_GENERAL_STATUS_GROUP [Address = 0x2384]

Table 8-576. AIL_IQ_IDC_GENERAL_STATUS_GROUP

Offset	Acronym	Register Description	Section
0x2384	AIL IQ IDC STATUS REGISTER	IDC Status register.	Section 8.6.14.1
0x2390	AIL IQ IDC IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the IFE	Section 8.6.14.2

8.6.14.1 AIL IQ IDC STATUS REGISTER [Address = 0x2384]

IDC Status register.

Figure 8-509. AIL IQ IDC STATUS REGISTER

31	1	0
Reserved		EMPTY
NA-0		R-0x0001

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-577. AIL IQ IDC STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EMPTY	Empty indicator for IDC internal FIFOs • FIFO_NOT_EMPTY (0) = FIFOs are not empty • FIFO_EMPTY (1) = FIFOs are empty

8.6.14.2 AIL IQ IDC IN PACKET STATUS REGISTER [Address = 0x2390 + (*S* × 0x0004)]

Size (*S*) = 0:1

Indicates when a channel is actively receiving a packet from the IFE

Figure 8-510. AIL IQ IDC IN PACKET STATUS REGISTER

31	0
INPKT	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-578. AIL IQ IDC IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-0	INPKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[15] is associated with channel 15

8.6.15 AIL_IQ_IDC_CONFIGURATION_GROUP [Address = 0x23C0]

Table 8-579. AIL_IQ_IDC_CONFIGURATION_GROUP

Offset	Acronym	Register Description	Section
0x23C0	AIL IQ IDC CONFIGURATION REGISTER	IDC Configuration Register	Section 8.6.15.1

8.6.15.1 AIL IQ IDC CONFIGURATION REGISTER [Address = 0x23C0]

IDC Configuration Register

Figure 8-511. AIL IQ IDC CONFIGURATION REGISTER

31	3	2	1	0
Reserved		RM_FAIL_FRC_OFF_EN	FRC_OFF_ALL	FAIL_MARK_ONLY
NA-0		R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-580. AIL IQ IDC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2	RM_FAIL_FRC_OFF_EN	Forces off all Ingress channels without waiting for an end of symbol or time slot if there is an RM failure. All open packets are automatically closed by creating an EOP for each open packet. This bit is also sent to the SI Ingress Control module to force off all of its open packets in the same manner. • FRC_OFF (1) = Force off on RM failure. • NOP (0) = No effect
1	FRC_OFF_ALL	Forces off all Ingress channels without waiting for an end of symbol or time slot. All open packets are automatically closed by creating an EOP for each open packet • FRC_OFF (1) = Force all channels off and close all open packets • NOP (0) = No effect
0	FAIL_MARK_ONLY	Controls how the IDC handles packet errors detected by IFE • DROP (0) = Drop Error packets • MARK (1) = Only Mark Packets With Errors

8.6.16 AIL_IQ_IDC_CHANNEL_CONFIG_GROUP [Address = 0x2400]

Table 8-581. AIL_IQ_IDC_CHANNEL_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x2400	AIL IQ IDC CHANNEL CONFIGURATION REGISTERS	IDC Channel configuration registers.	Section 8.6.16.1

8.6.16.1 AIL IQ IDC CHANNEL CONFIGURATION REGISTERS [Address = 0x2400 + (*S* × 0x0004)]

Size (*S*) = 0:63

IDC Channel configuration registers.

Figure 8-512. AIL IQ IDC CHANNEL CONFIGURATION REGISTERS

31 25	24	23 21	20 16	15 6	5 4	3 2	1 0
Reserved	CHAN_FRC_OFF	Reserved	PKT_TYPE	Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-582. AIL IQ IDC CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24	CHAN_FRC_OFF	Forces off all channel without waiting for an end of symbol or time slot. If channel has an open packet it is automatically closed by creating an EOP • FRC_OFF (0) = Force off channel and close an existing open packet • NOP (1) = No effect
23-21	Reserved	RESERVED
20-16	PKT_TYPE	Programmable packet type that is inserted into pkt_type field of PKTDMA Info Word 0.
15-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.6.17 AIL_IFE_FRM_SAMP_TC_MMR_RAM [Address = 0x2800 + (R × 0x0004)]

Table 8-583. AIL_IFE_FRM_SAMP_TC_MMR_RAM

Offset	Acronym	Register Description	Section
0x2800 + (*R* × 0x0004)	AIL IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER	IFE AxC Framing Sample Terminal Count Configuration Register	Section 8.6.17.1

8.6.17.1 AIL IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER [Address = 0x2800 + (R × 0x0004)]

Range (*R*) = 0:255

IFE AxC Framing Sample Terminal Count Configuration Register

Figure 8-513. AIL IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER

31	18	17	0
Reserved		SAMP_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-584. AIL IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-18	Reserved	Reserved
17-0	SAMP_TC	Radio Framing Counter. Number of samples (4 Bytes) per radio symbol programmed as a terminal count

8.6.18 AIL_ECTL_PKT_IF [Address = 0x3000]

Table 8-585. AIL_ECTL_PKT_IF

Offset	Acronym	Register Description	Section
0x3000	AIL ECTL GLOBAL ENABLE SET REG	Set Global Enable for ECTL	Section 8.6.18.1
0x3004	AIL ECTL GLOBAL ENABLE CLEAR REG	Clear Global Enable for ECTL	Section 8.6.18.2
0x3008	AIL ECTL GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, ECTL may still be closing out packets.	Section 8.6.18.3
0x3100	AIL ECTL CHANNEL ON STATUS REG	Gives current On/Off Status of every available CPRI control stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.6.18.4
0x3140	AIL ECTL IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the ECTL	Section 8.6.18.5
0x3200	AIL ECTL CHANNEL ENABLE CONFIGURATION REGISTER	ECTL Channel Configuration Enable Register	Section 8.6.18.6
0x3400	AIL ECTL DB THRESHOLD REGISTER	ECTL Database Threshold Register	Section 8.6.18.7

8.6.18.1 AIL ECTL GLOBAL ENABLE SET REG [Address = 0x3000]

Set Global Enable for ECTL

Figure 8-514. AIL ECTL GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-586. AIL ECTL GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.6.18.2 AIL ECTL GLOBAL ENABLE CLEAR REG [Address = 0x3004]

Clear Global Enable for ECTL

Figure 8-515. AIL ECTL GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-587. AIL ECTL GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.6.18.3 AIL ECTL GLOBAL ENABLE STATUS [Address = 0x3008]

Read Only status of global enable state. Even if this register is OFF, ECTL may still be closing out packets.

Figure 8-516. AIL ECTL GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-588. AIL ECTL GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ectl_ON 0x0:ectl_OFF

8.6.18.4 AIL ECTL CHANNEL ON STATUS REG [Address = 0x3100]

Gives current On/Off Status of every available CPRI control stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-517. AIL ECTL CHANNEL ON STATUS REG

31	4	3	0
Reserved		CHAN_ON	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-589. AIL ECTL CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.6.18.5 AIL ECTL IN PACKET STATUS REGISTER [Address = 0x3140]

Indicates when a channel is actively receiving a packet from the ECTL

Figure 8-518. AIL ECTL IN PACKET STATUS REGISTER

31	4	3	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-590. AIL ECTL IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	IN_PKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[3] is associated with channel 3

8.6.18.6 AIL ECTL CHANNEL ENABLE CONFIGURATION REGISTER [Address = 0x3200 + (*S* × 0x0004)]

Size (*S*) = 0:3

ECTL Channel Configuration Enable Register

Figure 8-519. AIL ECTL CHANNEL ENABLE CONFIGURATION REGISTER

31	1	0
Reserved		CHAN_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-591. AIL ECTL CHANNEL ENABLE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.6.18.7 AIL ECTL DB THRESHOLD REGISTER [Address = 0x3400 + (*S* × 0x0004)]

Size (*S*) = 0:3

ECTL Database Threshold Register

Figure 8-520. AIL ECTL DB THRESHOLD REGISTER

31	5	4	0
Reserved		CHANNEL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-592. AIL ECTL DB THRESHOLD REGISTER Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved
4-0	CHANNEL	Data Buffer Threshold value before indicating data available per channel. Unit is QWD and normally set to zero

8.6.19 AIL_ICTL_IDC_IF [Address = 0x4000]

Table 8-593. AIL_ICTL_IDC_IF

Offset	Acronym	Register Description	Section
0x4000	AIL ICTL CHANNEL CONFIGURATION REGISTERS	Per-channel configuration registers.	Section 8.6.19.1
0x4200	AIL ICTL CONFIGURATION REGISTER	ICTL Configuration Register	Section 8.6.19.2
0x4204	AIL ICTL STATUS REGISTER	ICTL Status register.	Section 8.6.19.3
0x4210	AIL ICTL IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the ICTL	Section 8.6.19.4

8.6.19.1 AIL ICTL CHANNEL CONFIGURATION REGISTERS [Address = 0x4000 + (*S* × 0x0004)]

Size (*S*) = 0:3

Per-channel configuration registers.

Figure 8-521. AIL ICTL CHANNEL CONFIGURATION REGISTERS

31 25	24	23 21	20 16	15 6	5 4	3 2	1 0
Reserved	CHAN_FRC_OFF	Reserved	PKT_TYPE	Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-594. AIL ICTL CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24	CHAN_FRC_OFF	Forces off all channel without waiting for an EOP. If channel has an open packet it is automatically closed by creating an EOP • FRC_OFF (0) = Force off channel and close an existing open packet • NOP (1) = No effect
23-21	Reserved	RESERVED
20-16	PKT_TYPE	Programmable packet type that is inserted into pkt_type field of PKTDMA Info Word 0.
15-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.6.19.2 AIL ICTL CONFIGURATION REGISTER [Address = 0x4200]

ICTL Configuration Register

Figure 8-522. AIL ICTL CONFIGURATION REGISTER

31	2	1	0
Reserved		FRC_OFF_ALL	FAIL_MARK_ONLY
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-595. AIL ICTL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved
1	FRC_OFF_ALL	Forces off all Ingress channels without waiting for an EOP. All open packets are automatically closed by creating an EOP for each open packet • FRC_OFF (1) = Force all channels off and close all open packets • NOP (0) = No effect
0	FAIL_MARK_ONLY	Controls how the ICTL handles packet errors detected by ICTL • DROP (0) = Drop Error Packets • MARK (1) = Only Mark Packets With Errors

8.6.19.3 AIL ICTL STATUS REGISTER [Address = 0x4204]

ICTL Status register.

Figure 8-523. AIL ICTL STATUS REGISTER

31	1	0
Reserved		EMPTY
NA-0		R-0x0001

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-596. AIL ICTL STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EMPTY	Empty indicator for ICTL internal FIFOs • FIFO_NOT_EMPTY (0) = FIFOs are not empty • FIFO_EMPTY (1) = FIFOs are empty

8.6.19.4 AIL ICTL IN PACKET STATUS REGISTER [Address = 0x4210]

Indicates when a channel is actively receiving a packet from the ICTL

Figure 8-524. AIL ICTL IN PACKET STATUS REGISTER

31	4	3	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-597. AIL ICTL IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	IN_PKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[3] is associated with channel 3

8.6.20 AIL_ICTL_PKT_IF [Address = 0x4280]

Table 8-598. AIL_ICTL_PKT_IF

Offset	Acronym	Register Description	Section
0x4280	AIL ICTL GLOBAL ENABLE SET REG	Set Global Enable for ICTL	Section 8.6.20.1
0x4284	AIL ICTL GLOBAL ENABLE CLEAR REG	Clear Global Enable for ICTL	Section 8.6.20.2
0x4288	AIL ICTL GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, ICTL may still be closing out packets.	Section 8.6.20.3
0x42A0	AIL ICTL CHANNEL ON STATUS REG	Gives current On/Off Status of every available stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.6.20.4
0x4400	AIL ICTL CHANNEL ENABLE CONFIGURATION REGISTER	ICTL Channel Configuration Enable Register	Section 8.6.20.5

8.6.20.1 AIL ICTL GLOBAL ENABLE SET REG [Address = 0x4280]

Set Global Enable for ICTL

Figure 8-525. AIL ICTL GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-599. AIL ICTL GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.6.20.2 AIL ICTL GLOBAL ENABLE CLEAR REG [Address = 0x4284]

Clear Global Enable for ICTL

Figure 8-526. AIL ICTL GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-600. AIL ICTL GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.6.20.3 AIL ICTL GLOBAL ENABLE STATUS [Address = 0x4288]

Read Only status of global enable state. Even if this register is OFF, ICTL may still be closing out packets.

Figure 8-527. AIL ICTL GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-601. AIL ICTL GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ictl_ON 0x0:ictl_OFF

8.6.20.4 AIL ICTL CHANNEL ON STATUS REG [Address = 0x42A0]

Gives current On/Off Status of every available stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-528. AIL ICTL CHANNEL ON STATUS REG

31	4	3	0
Reserved		CHAN_ON	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-602. AIL ICTL CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.6.20.5 AIL ICTL CHANNEL ENABLE CONFIGURATION REGISTER [Address = 0x4400 + (*S* × 0x0004)]

Size (*S*) = 0:3

ICTL Channel Configuration Enable Register

Figure 8-529. AIL ICTL CHANNEL ENABLE CONFIGURATION REGISTER

31	1	0
Reserved		CHAN_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-603. AIL ICTL CHANNEL ENABLE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.6.21 AIL_UAT_GEN_CTL [Address = 0x5000]

Table 8-604. AIL_UAT_GEN_CTL

Offset	Acronym	Register Description	Section
0x5000	AIL UAT CONFIG REGISTER	This register simply starts the uAT timers running. It is implied that SW is unable to precisely time the start of timers. The intent is for the SW to correct the timers by later writting to the offset register of each timer.	Section 8.6.21.1
0x5004	AIL UAT BCN TERMINAL COUNT REGISTER	UAT BCN terminal count Register	Section 8.6.21.2
0x5008	AIL UAT BCN OFFSET REGISTER	UAT BCN offset Register	Section 8.6.21.3
0x500C	AIL UAT SYNC BCN CAPTURE REGISTER	UAT SYNC BCN capture Register	Section 8.6.21.4

8.6.21.1 AIL UAT CONFIG REGISTER [Address = 0x5000]

This register simply starts the uAT timers running. It is implied that SW is unable to precisely time the start of timers. The intent is for the SW to correct the timers by later writting to the offset register of each timer.

Figure 8-530. AIL UAT CONFIG REGISTER

31	2	1	0
Reserved		DIAG_SYNC	UAT_RUN
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-605. AIL UAT CONFIG REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	RESERVED
1	DIAG_SYNC	diag_sync = 1 starts the BCN and RAD counters if uat_run is set and an AT sync is received. This is only used in simulation and for diagnostics
0	UAT_RUN	UAT run starts the BCN and RAD counters free running

8.6.21.2 AIL UAT BCN TERMINAL COUNT REGISTER [Address = 0x5004]

UAT BCN terminal count Register

Figure 8-531. AIL UAT BCN TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-606. AIL UAT BCN TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT BCN terminal count. BCN counts from zero to this limit and wraps to zero. Program as 2,457,599 for sys_clk=245.76MHz and 3,071,999 for sys_clk=307.2MHz

8.6.21.3 AIL UAT BCN OFFSET REGISTER [Address = 0x5008]

UAT BCN offset Register

Figure 8-532. AIL UAT BCN OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-607. AIL UAT BCN OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	Offset correction to the raw uAT BCN counter. Used to correct the alignment of the local uAT BCN to the master AT2 BCN. BCN is initially randomly started. SW uses uat_sync_bcn_capture_sts rd_val to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.6.21.4 AIL UAT SYNC BCN CAPTURE REGISTER [Address = 0x500C]

UAT SYNC BCN capture Register

Figure 8-533. AIL UAT SYNC BCN CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-608. AIL UAT SYNC BCN CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	uAT raw BCN value captured each frame boundary of AT2 master BCN. Used to calculate uAT BCN offset value for the purpose of aligning uAT to AT2 BCN.

8.6.22 AIL_UAT_AIL_REGS [Address = 0x5010]

Table 8-609. AIL_UAT_AIL_REGS

Offset	Acronym	Register Description	Section
0x5010	AIL UAT PI BCN CAPTURE REGISTER	UAT pi BCN capture Register	Section 8.6.22.1
0x5014	AIL UAT_PIMAX_CFG	AT AIL pi max register	Section 8.6.22.2
0x5018	AIL UAT_PIMIN_CFG	AT AIL pi min register	Section 8.6.22.3
0x501C	AIL UAT RP301 BCN CAPTURE REGISTER	UAT rp3-01 BCN capture Register	Section 8.6.22.4
0x5020	AIL UAT TM FRAME CONFIGURATION REGISTER	UAT TM Frame Count (BFN) configuration	Section 8.6.22.5
0x5024	AIL UAT TM FRAME STATUS REGISTER	UAT TM Frame status	Section 8.6.22.6
0x5028	AIL UAT RT FB REGISTER	UAT RT frame boundary compare Register	Section 8.6.22.7
0x502C	AIL UAT PE FB REGISTER	UAT pe frame boundary compare Register	Section 8.6.22.8
0x5030	AIL UAT TM FB REGISTER	UAT tm frame boundary (Delta) compare Register	Section 8.6.22.9

8.6.22.1 AIL UAT PI BCN CAPTURE REGISTER [Address = 0x5010]

UAT pi BCN capture Register

Figure 8-534. AIL UAT PI BCN CAPTURE REGISTER

31	30 25	24 0
KCHAR_POSITION	Reserved	RD_VAL
R-0	NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-610. AIL UAT PI BCN CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31	KCHAR_POSITION	(AIL use only) uAT pi K character position. Captures the k character position when the AIL_PHY_RM detects a CPRI or OBSAI PHY frame boundary (SOF). 0 means that the kchar for SOF was detected on the lower byte of the SERDES receive data, 1 means upper byte.
30-25	Reserved	RESERVED
24-0	RD_VAL	(AIL use only) uAT pi BCN capture. Captures the BCN timer value when the AIL_PHY_RM detects a CPRI or OBSAI PHY frame boundary (SOF).

8.6.22.2 AIL UAT_PIMAX_CFG [Address = 0x5014]

AT AIL pi max register

Figure 8-535. AIL UAT_PIMAX_CFG

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-611. AIL UAT_PIMAX_CFG Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(AIL use only) PI max window. One of two values which indicate the legal range for OBSAI or CPRI PHY SOF. When an SOF is recieved outside this window, error is indicated by EE

8.6.22.3 AIL UAT_PIMIN_CFG [Address = 0x5018]

AT AIL pi min register

Figure 8-536. AIL UAT_PIMIN_CFG

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-612. AIL UAT_PIMIN_CFG Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(AIL use only) PI min window. One of two values which indicate the legal range for OBSAI or CPRI PHY SOF. When an SOF is recieved outside this window, error is indicated by EE

8.6.22.4 AIL UAT RP301 BCN CAPTURE REGISTER [Address = 0x501C]

UAT rp3-01 BCN capture Register

Figure 8-537. AIL UAT RP301 BCN CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-613. AIL UAT RP301 BCN CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	(AIL use only) uAT RP3-01 BCN capture. Captures the BCN offset count when the phy detects an OBSAI RP3-01 strobe from the AIL_PD.

8.6.22.5 AIL UAT TM FRAME CONFIGURATION REGISTER [Address = 0x5020]

UAT TM Frame Count (BFN) configuration

Figure 8-538. AIL UAT TM FRAME CONFIGURATION REGISTER

31	12	11	0
Reserved		WR_VAL	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-614. AIL UAT TM FRAME CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	WR_VAL	(AIL CPRI use only) uAT CPRI BFN count value (Write only). SW overwrite current value. uAT will increment every TM_FRM_STB

8.6.22.6 AIL UAT TM FRAME STATUS REGISTER [Address = 0x5024]

UAT TM Frame status

Figure 8-539. AIL UAT TM FRAME STATUS REGISTER

31	12	11	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-615. AIL UAT TM FRAME STATUS REGISTER Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	RD_VAL	(AIL CPRI use only) uAT CPRI BFN count value (Read only). Initially set by uat_tm_bfn_cfg, increments every CPRI PHY frame.

8.6.22.7 AIL UAT RT FB REGISTER [Address = 0x5028]

UAT RT frame boundary compare Register

Figure 8-540. AIL UAT RT FB REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-616. AIL UAT RT FB REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(AIL use only) uAT BCN compare value which cause RT_STB to fire. Used for Egress PHY timing. RT_STB is the latest moment that RT will wait for PE and CI SOF contribution before progressing without either input.

8.6.22.8 AIL UAT PE FB REGISTER [Address = 0x502C]

UAT pe frame boundary compare Register

Figure 8-541. AIL UAT PE FB REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-617. AIL UAT PE FB REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(AIL use only) uAT BCN compare value which cause PE_STB to fire. Used for Egress PROTO & PHY timing. PE_STB is the exact time which PE will start building the PHY protocol. It also represents the latest timing for incoming DMA data to contribute to the PHY. Late DMA data is rejected by PE

8.6.22.9 AIL UAT TM FB REGISTER [Address = 0x5030]

UAT tm frame boundary (Delta) compare Register

Figure 8-542. AIL UAT TM FB REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-618. AIL UAT TM FB REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(AIL use only) uAT BCN compare value which cause TM_STB to fire. Used for Egress PHY timing. TM_STB (OBSAI Delta) is the precise time at which TM exports the CPRI or OBSAI PHY SOF

8.6.23 AIL_UAT_EGR_RADT [Address = 0x5080 + (R × 0x0010)]

Table 8-619. AIL_UAT_EGR_RADT

Offset	Acronym	Register Description	Section
0x5080 + (*R* × 0x0010)	AIL UAT RADT TERMINAL COUNT REGISTER	UAT RADT terminal count Register	Section 8.6.23.1
0x5084 + (*R* × 0x0010)	AIL UAT RADT OFFSET REGISTER	UAT RADT offset Register	Section 8.6.23.2
0x5088 + (*R* × 0x0010)	AIL UAT SYNC RADT CAPTURE REGISTER	UAT SYNC RADT capture Register	Section 8.6.23.3

8.6.23.1 AIL UAT RADT TERMINAL COUNT REGISTER [Address = 0x5080 + (R × 0x0010)]

Range (*R*) = 0:7

UAT RADT terminal count Register

Figure 8-543. AIL UAT RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-620. AIL UAT RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.6.23.2 AIL UAT RADT OFFSET REGISTER [Address = 0x5084 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT offset Register

Figure 8-544. AIL UAT RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-621. AIL UAT RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.6.23.3 AIL UAT SYNC RADT CAPTURE REGISTER [Address = 0x5088 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT SYNC RADT capture Register

Figure 8-545. AIL UAT SYNC RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-622. AIL UAT SYNC RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	UAT RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.6.24 AIL_UAT_ING_RADT [Address = 0x5100 + (R × 0x0010)]

Table 8-623. AIL_UAT_ING_RADT

Offset	Acronym	Register Description	Section
0x5100 + (*R* × 0x0010)	AIL UAT RADT TERMINAL COUNT REGISTER	UAT RADT terminal count Register	Section 8.6.24.1
0x5104 + (*R* × 0x0010)	AIL UAT RADT OFFSET REGISTER	UAT RADT offset Register	Section 8.6.24.2
0x5108 + (*R* × 0x0010)	AIL UAT SYNC RADT CAPTURE REGISTER	UAT SYNC RADT capture Register	Section 8.6.24.3

8.6.24.1 AIL UAT RADT TERMINAL COUNT REGISTER [Address = 0x5100 + (R × 0x0010)]

Range (*R*) = 0:7

UAT RADT terminal count Register

Figure 8-546. AIL UAT RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-624. AIL UAT RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.6.24.2 AIL UAT RADT OFFSET REGISTER [Address = 0x5104 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT offset Register

Figure 8-547. AIL UAT RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-625. AIL UAT RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.6.24.3 AIL UAT SYNC RADT CAPTURE REGISTER [Address = 0x5108 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT SYNC RADT capture Register

Figure 8-548. AIL UAT SYNC RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-626. AIL UAT SYNC RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	UAT RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.6.25 AIL_UAT_RADT_EVT [Address = 0x5200 + (R × 0x0008)]

Table 8-627. AIL_UAT_RADT_EVT

Offset	Acronym	Register Description	Section
0x5200 + (*R* × 0x0008)	AIL UAT RADT EVENT COMPARE REGISTER	UAT RADT event compare Register per RADT. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress	Section 8.6.25.1
0x5204 + (*R* × 0x0008)	AIL UAT RADT EVENT CLOCK COUNT TC REGISTER	UAT RADT event clock counter terminal count Register per RADT	Section 8.6.25.2

8.6.25.1 AIL UAT RADT EVENT COMPARE REGISTER [Address = 0x5200 + (R × 0x0008)]

Range (*R*) = 0:21

UAT RADT event compare Register per RADT. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

Figure 8-549. AIL UAT RADT EVENT COMPARE REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-628. AIL UAT RADT EVENT COMPARE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT event compare per RADT. When compare value equals RADT count, frame rate event is generated. Also periodic event (i.e. 4SAMP) is started. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

8.6.25.2 AIL UAT RADT EVENT CLOCK COUNT TC REGISTER [Address = 0x5204 + (*R* × 0x0008)]

Range (*R*) = 0:21

UAT RADT event clock counter terminal count Register per RADT

Figure 8-550. AIL UAT RADT EVENT CLOCK COUNT TC REGISTER

31	16	15	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-629. AIL UAT RADT EVENT CLOCK COUNT TC REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	VAL	UAT RADT event clock counter terminal count controls spacing of the periodic strobe (i.e. 4SAMP). Once the uat_evt_radt_cmp_cfg equals the RADT, the period strobe will fire and re-fire every time a clock counter reaches this terminal count. The The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

8.6.26 AIL_IQ_EDC_REGISTER_GROUP [Address = 0x8000]

Table 8-630. AIL_IQ_EDC_REGISTER_GROUP

Offset	Acronym	Register Description	Section
0x8000	AIL IQ EDC CONFIGURATION REGISTER	EDC Configuration Register	Section 8.6.26.1
0x8004	AIL IQ EDC SOP COUNTER STATUS REGISTER	Counts the number of SOPs seen by the IQ EDC	Section 8.6.26.2
0x8008	AIL IQ EDC EOP COUNTER STATUS REGISTER	Counts the number of EOPs seen by the IQ EDC	Section 8.6.26.3
0x8080	AIL IQ EDC OCCUPANCY COUNTER STATUS REGISTER	EDC Status Occupancy counter for each channel register. User can ignore this (TI debug only)	Section 8.6.26.4
0x8200	AIL IQ EDC CHANNEL CONFIGURATION REGISTERS	Per-channel configuration registers.	Section 8.6.26.5

8.6.26.1 AIL IQ EDC CONFIGURATION REGISTER [Address = 0x8000]

EDC Configuration Register

Figure 8-551. AIL IQ EDC CONFIGURATION REGISTER

31	1	0
Reserved		PSI_ERR_CHK_DISABLE
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-631. AIL IQ EDC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	Reserved
0	PSI_ERR_CHK_DISABLE	Controls how the EDC handles packet errors detected by efe • DROP (0) = Drop the rest of the packet on errors • NO_DROP (1) = Do not drop packet on errors

8.6.26.2 AIL IQ EDC SOP COUNTER STATUS REGISTER [Address = 0x8004]

Counts the number of SOPs seen by the IQ EDC

Figure 8-552. AIL IQ EDC SOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-632. AIL IQ EDC SOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	SOP_CNT	Count of the number of SOPs seen by the IQ EDC

8.6.26.3 AIL IQ EDC EOP COUNTER STATUS REGISTER [Address = 0x8008]

Counts the number of EOPs seen by the IQ EDC

Figure 8-553. AIL IQ EDC EOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-633. AIL IQ EDC EOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	EOP_CNT	Count of the number of EOPs seen by the IQ EDC

8.6.26.4 AIL IQ EDC OCCUPANCY COUNTER STATUS REGISTER [Address = 0x8080 + (*S* × 0x0004)]

Size (*S*) = 0:15

EDC Status Occupancy counter for each channel register. User can ignore this (TI debug only)

Figure 8-554. AIL IQ EDC OCCUPANCY COUNTER STATUS REGISTER

31 24	23 16	15 8	7 0
OCC_CNTR_D	OCC_CNTR_C	OCC_CNTR_B	OCC_CNTR_A
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-634. AIL IQ EDC OCCUPANCY COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	OCC_CNTR_D	Occupancy Counter for register D for this address
23-16	OCC_CNTR_C	Occupancy Counter for register C for this address
15-8	OCC_CNTR_B	Occupancy Counter for register B for this address
7-0	OCC_CNTR_A	Occupancy Counter for register A for this address

8.6.26.5 AIL IQ EDC CHANNEL CONFIGURATION REGISTERS [Address = 0x8200 + (*S* × 0x0004)]

Size (*S*) = 0:63

Per-channel configuration registers.

Figure 8-555. AIL IQ EDC CHANNEL CONFIGURATION REGISTERS

31 6	5 4	3 2	1 0
Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-635. AIL IQ EDC CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.6.27 AIL_IQ_INGRESS_VBUS_MMR_GROUP [Address = 0xA000]

Table 8-636. AIL_IQ_INGRESS_VBUS_MMR_GROUP

Offset	Acronym	Register Description	Section
0xA000	AIL IQ IDC RATE CONTROL CONFIGURATION REGISTER	IDC Rate Control Configuration register. Programmable rate control for OBSAI control word and generic packet mode	Section 8.6.27.1
0xA004	AIL IQ IDC SOP COUNTER REGISTER	This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.6.27.2
0xA008	AIL IQ IDC EOP COUNTER REGISTER	This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.6.27.3

8.6.27.1 AIL IQ IDC RATE CONTROL CONFIGURATION REGISTER [Address = 0xA000]

IDC Rate Control Configuration register. Programmable rate control for OBSAI control word and generic packet mode

Figure 8-556. AIL IQ IDC RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-637. AIL IQ IDC RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the IDC to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the IDC to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.6.27.2 AIL IQ IDC SOP COUNTER REGISTER [Address = 0xA004]

This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-557. AIL IQ IDC SOP COUNTER REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-638. AIL IQ IDC SOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	SOP_CNT	Wrapping count of SOPs sent on PSI.

8.6.27.3 AIL IQ IDC EOP COUNTER REGISTER [Address = 0xA008]

This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-558. AIL IQ IDC EOP COUNTER REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-639. AIL IQ IDC EOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	EOP_CNT	Wrapping count of EOPs sent on PSI.

8.6.28 AIL_ECTL_REGISTER_GROUP [Address = 0xB000]

Table 8-640. AIL_ECTL_REGISTER_GROUP

Offset	Acronym	Register Description	Section
0xB000	AIL ECTL RATE CONTROL CONFIGURATION REGISTER	ECTL Rate Control Configuration register. Programmable rate control for Rate Controller.	Section 8.6.28.1
0xB004	AIL ECTL SOP COUNTER STATUS REGISTER	Counts the number of SOPs seen by the ECTL	Section 8.6.28.2
0xB008	AIL ECTL EOP COUNTER STATUS REGISTER	Counts the number of EOPs seen by the ECTL	Section 8.6.28.3
0xB100	AIL ECTL OCCUPANCY COUNTER STATUS REGISTER	ECTL Status Occupancy counter for each channel register. User can ignore this (TI debug only)	Section 8.6.28.4
0xB200	AIL ECTL CHANNEL CONFIGURATION REGISTERS	ECTL Per-channel configuration registers.	Section 8.6.28.5

8.6.28.1 AIL ECTL RATE CONTROL CONFIGURATION REGISTER [Address = 0xB000]

ECTL Rate Control Configuration register. Programmable rate control for Rate Controller.

Figure 8-559. AIL ECTL RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-641. AIL ECTL RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the ECTL to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the ICTL to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.6.28.2 AIL ECTL SOP COUNTER STATUS REGISTER [Address = 0xB004]

Counts the number of SOPs seen by the ECTL

Figure 8-560. AIL ECTL SOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-642. AIL ECTL SOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	SOP_CNT	Count of the number of SOPs seen by the ECTL

8.6.28.3 AIL ECTL EOP COUNTER STATUS REGISTER [Address = 0xB008]

Counts the number of EOPs seen by the ECTL

Figure 8-561. AIL ECTL EOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-643. AIL ECTL EOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	EOP_CNT	Count of the number of EOPs seen by the ECTL

8.6.28.4 AIL ECTL OCCUPANCY COUNTER STATUS REGISTER [Address = 0xB100]

ECTL Status Occupancy counter for each channel register. User can ignore this (TI debug only)

Figure 8-562. AIL ECTL OCCUPANCY COUNTER STATUS REGISTER

31 24	23 16	15 8	7 0
OCC_CNTR_D	OCC_CNTR_C	OCC_CNTR_B	OCC_CNTR_A
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-644. AIL ECTL OCCUPANCY COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	OCC_CNTR_D	Occupancy Counter for register D for this address
23-16	OCC_CNTR_C	Occupancy Counter for register C for this address
15-8	OCC_CNTR_B	Occupancy Counter for register B for this address
7-0	OCC_CNTR_A	Occupancy Counter for register A for this address

8.6.28.5 AIL ECTL CHANNEL CONFIGURATION REGISTERS [Address = 0xB200 + (*S* × 0x0004)]

Size (*S*) = 0:3

ECTL Per-channel configuration registers.

Figure 8-563. AIL ECTL CHANNEL CONFIGURATION REGISTERS

31	6	5	4	3	2	1	0
Reserved		IQ_ORDER		Reserved		DAT_SWAP	
NA-0		R/W-0		NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-645. AIL ECTL CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.6.29 AIL_CTL_INGRESS_VBUS_MMR_GROUP [Address = 0xC000]

Table 8-646. AIL_CTL_INGRESS_VBUS_MMR_GROUP

Offset	Acronym	Register Description	Section
0xC000	AIL ICTL RATE CONTROL CONFIGURATION REGISTER	ICTL Rate Control Configuration register. Programmable rate control for Rate Controller.	Section 8.6.29.1
0xC004	AIL ICTL SOP COUNTER REGISTER	This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.6.29.2
0xC008	AIL ICTL EOP COUNTER REGISTER	This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.6.29.3

8.6.29.1 AIL ICTL RATE CONTROL CONFIGURATION REGISTER [Address = 0xC000]

ICTL Rate Control Configuration register. Programmable rate control for Rate Controller.

Figure 8-564. AIL ICTL RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-647. AIL ICTL RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the ICTL to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the ICTL to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.6.29.2 AIL ICTL SOP COUNTER REGISTER [Address = 0xC004]

This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-565. AIL ICTL SOP COUNTER REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-648. AIL ICTL SOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	SOP_CNT	Wrapping count of SOPs sent on PSI.

8.6.29.3 AIL ICTL EOP COUNTER REGISTER [Address = 0xC008]

This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-566. AIL ICTL EOP COUNTER REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-649. AIL ICTL EOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	EOP_CNT	Wrapping count of EOPs sent on PSI.

8.6.30 AIL_PE_COMMON [Address = 0x2_0000]

Table 8-650. AIL_PE_COMMON

Offset	Acronym	Register Description	Section
0x2_0000	AIL PE GLOBAL CONFIGURATION REGISTER	AIL PE Global Register	Section 8.6.30.1
0x2_0100	AIL PE CHANNEL CONFIGURATION REGSITER	Channel-by-Channel control. OBSAI: 64 generic AxC or control channels CPRI: 64 AxC Channels, 4 CPRI control channels are configured elsewhere. For CPRI, only RT_CTL field is used	Section 8.6.30.2

8.6.30.1 AIL PE GLOBAL CONFIGURATION REGISTER [Address = 0x2_0000]

AIL PE Global Register

Figure 8-567. AIL PE GLOBAL CONFIGURATION REGISTER

31	9	8	7	0
Reserved		ENET_HDR_SEL	Reserved	
NA-0		R/W-0	NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-651. AIL PE GLOBAL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	ENET_HDR_SEL	OBSAI Ethernet only, Preamble pattern and SOF select (bit reversal) 0: 0xAAAAAAAB 1: 0x555555D5
7-0	Reserved	RESERVED

8.6.30.2 AIL PE CHANNEL CONFIGURATION REGISTER [Address = 0x2_0100 + (*S* × 0x0004)]

Size (*S*) = 0:63

Channel-by-Channel control. OBSAI: 64 generic AxC or control channels CPRI: 64 AxC Channels, 4 CPRI control channels are configured elsewhere. For CPRI, only RT_CTL field is used

Figure 8-568. AIL PE CHANNEL CONFIGURATION REGISTER

31 17	16	15 13	12	11 10	9	8 7	6 1	0
Reserved	CRC_HDR	Reserved	ETHERNET	Reserved	CRC_TYPE	RT_CTL	Reserved	CRC_EN
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-652. AIL PE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-17	Reserved	RESERVED
16	CRC_HDR	OBSAI CRC16 is calculated over OBSAI header as well as payload (only valid for OBSAI TYPES CONTROL (0x0) & MEASUREMENT (0x1) • CRC_HDR_ON (1) = CRC16 is calculated over 3 byte OBSAI header and 14 bytes of 16 byte payload. Only valid for 19 byte OBSAI messages utilizing CRC16 • CRC_HDR_OFF (0) = do not perform CRC over OBSAI Header (program to OFF for CPRI and for most OBSAI types)
15-13	Reserved	RESERVED
12	ETHERNET	OBSAI Channel is ethernet. This field controls insertion of the Ethernet Preamble and SOF (and prevents CRC of these bytes) • ENET_ON (1) = channel is ethernet • ENET_OFF (0) = channel is not ethernet
11-10	Reserved	RESERVED
9	CRC_TYPE	OBSAI CRC: length of CRC • 32BIT_CRC (0) = 32BIT_CRC • 16BIT_CRC (1) = 16BIT_CRC
8-7	RT_CTL	OBSAI/CPRI Controls RT to perform appropriate insertion/aggregation into PHY applied on msg-by-msg basis for OBSAI or sample-by-sample basis for CPRI • ADD8 (3) = Aggregate/add both PE and RM contributions, samples are 8bit I and Q -or- 7bit I and Q • ADD16 (2) = Aggregate/add both PE and RM contributions, samples are 16bit I and Q -or- 15bit I and Q • INSERTPE (1) = Insert the PE contribution, ignoring any possible RM contribution • FWD_RM (0) = Forward the RM contribution ignoring the PE contribution
6-1	Reserved	RESERVED
0	CRC_EN	OBSAI CRC: enable CRC generation and insertion on AxC by AxC basis

8.6.31 AIL_PE_OBSAI_HEADER_LUT [Address = 0x2_0200 + (R × 0x0004)]

Table 8-653. AIL_PE_OBSAI_HEADER_LUT

Offset	Acronym	Register Description	Section
0x2_0200 + (*R* × 0x0004)	AIL PE OBSAI HEADER CONFIGURATION REGISTER	OBSAI chan-by-chan, control of OBSAI header creation	Section 8.6.31.1

8.6.31.1 AIL PE OBSAI HEADER CONFIGURATION REGISTER [Address = 0x2_0200 + (R × 0x0004)]

Range (*R*) = 0:63

OBSAI chan-by-chan, control of OBSAI header creation

Figure 8-569. AIL PE OBSAI HEADER CONFIGURATION REGISTER

31 30	29	28 26	25 24	23 11	10 6	5 0
PS_INSERT	Reserved	TS_FRMT	TS_MASK	ADR	TYP	TS_ADR
R/W-0	NA-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-654. AIL PE OBSAI HEADER CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-30	PS_INSERT	Normal header processing is performed except the above MMR adr, type, ts_adr fields are unsed and instead this information is replaced with the protocol specific (PS) data. Effectively, when used, ps data allows APP SW to control OBSAI header on packet by packet basis. Used for Base Band Hopping of GSM control packets. PS data is not available for AxC Packets • NO_PS (0) = normal, PS is unused • ADR_PS (1) = MMR pe_obsai_hdr_cfg.adr MMR field above is not used and instead replaced by PS data • ALL_PS (2) = MMR pe_obsai_hdr_cfg.adr, type, ts_adr fields above are not used and instead replaced by PS data • RSVD_PS (3) = Reserved
29	Reserved	RESERVED
28-26	TS_FRMT	TS: OBSAI time stamp generation algorithm • NO_TS (0) = No time stamp insertion -or- OBSAI Generic Control Message, one message packet with inferred SOP & EOP in same OBSAI message. • NORM_TS (1) = Normal time stamp format • GSM_UL (2) = GSM OBSAI Time Stamp, UL time stamp format msb=1 first four msg. DL time stamp format msb=1 first msg • GEN_PKT (3) = OBSAI Generic Packet (SOP=10, MOP=00, EOP=11) • ETHERNET (4) = Ethernet Type where last TS indicates number of valid bytes in last transfer • CTR_PKT (5) = OBSAI Control Message for Air Interface Sync Operations, one message packet with inferred SOP & EOP in same OBSAI message. • GSM_DL (6) = GSM OBSAI Time Stamp, UL time stamp format msb=1 first four msg. DL time stamp format msb=1 first msg
25-24	TS_MASK	Controls which parts of the OBSAI TS field are inserted vs. calculated • NONE (0) = All TS bits are genrated as actual time stamp by PE circuits (normal AxC TS), obsai_ts_adr is not inserted and is unused • 4LSB (1) = 4 lsb bits of obsai_ts_adr are inserted into the TS field as and extention of addressing, 2 msb are generated as packet demarkation • ALL (2) = All TS(5:0) bits are inserted from pe_obsai_hdr_cfg.ts_adr(5:0) as an extention of addressing • RSVD_MSK (3) = Reserved
23-11	ADR	OBSAI hdr(23:11)ADR : inserted into OBSAI header ADDRESS field
10-6	TYP	OBSAI hdr(10:6) TYPE: inserted into OBSAI header TYPE field
5-0	TS_ADR	OBSAI hdr(5:0) TS : only used if TS is inserted instead of generated

8.6.32 AIL_PE_CPRI_CW [Address = 0x2_1000]

Table 8-655. AIL_PE_CPRI_CW

Offset	Acronym	Register Description	Section
0x2_1000	AIL PE CPRI CONTROL WORD CHANNEL CONFIGURATION REGISTER	PE CPRI, Primary register for configuring CPRI Control words. Contains primary selection of dilineation type plus many fields which are common. One MMR per each of four channels	Section 8.6.32.1
0x2_1010	AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART0	PE CPRI Hyperframe Enable Part0, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 0 ~ 31)	Section 8.6.32.2
0x2_1014	AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART1	PE CPRI Hyperframe Enable Part1, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 32 ~ 63)	Section 8.6.32.3
0x2_1018	AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART2	PE CPRI Hyperframe Enable Part2, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 64 ~ 95)	Section 8.6.32.4
0x2_101C	AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART3	PE CPRI Hyperframe Enable Part3, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 96 ~ 127)	Section 8.6.32.5
0x2_1020	AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART4	PE CPRI Hyperframe Enable Part4, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 128 ~ 149)	Section 8.6.32.6
0x2_1024	AIL PE CPRI CW NULL CHARACTER CONFIGURATION REGISTER	PE CPRI NULL delineator register	Section 8.6.32.7
0x2_1028	AIL PE CPRI CW CRC8 CONFIGURATION REGISTER	PE CPRI CRC8 control register	Section 8.6.32.8
0x2_102C	AIL PE CPRI CW STATUS REGISTER	channel-by-channel packet status. When shutting down a link, it is good practice for APP SW to wait until all channels are out of packet	Section 8.6.32.9
0x2_1030	AIL PE CPRI CW FAST ETHERNET 4B5B CONFIGURATION REGISTER	PE CPRI fast ethernet control register	Section 8.6.32.10
0x2_1400	AIL PE CPRI CW LOOK_UP_TABLE	CPRI CW Channel Register, one register location for each of 256 possible CPRI CW per Hyperframe. Maps the CW to one of four control flows, or unallocated BW	Section 8.6.32.11

8.6.32.1 AIL PE CPRI CONTROL WORD CHANNEL CONFIGURATION REGISTER [Address = 0x2_1000 + (*S* × 0x0004)]

Size (*S*) = 0:3

PE CPRI, Primary register for configuring CPRI Control words. Contains primary selection of dilineation type plus many fields which are common. One MMR per each of four channels

Figure 8-570. AIL PE CPRI CONTROL WORD CHANNEL CONFIGURATION REGISTER

31 16	15 14	13 12	11 10	9 8	7	6	5 4	3 2	1 0
BYTE_EN	RT_CTL	IMUX	DLMT_OMUX	DLMT_IMUX	HF_LUT_EN	CRC_INIT	CRC_SEL	DELIN_SEL	CRC_RVRS
R/W-0xFFFF	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-656. AIL PE CPRI CONTROL WORD CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-16	BYTE_EN	CW byte Enable, used to disable CW bytes for some low rate HDLC or 5x/10x RTWP. (normally set to 0xffff)
15-14	RT_CTL	Controls AIL_PHY_RT to perform appropriate insertion/aggregation into PHY, applied on sample by sample basis. • ADD8 (3) = Aggregate/add both PE and RM contributions, samples are 8bit I and Q (not be appropriate for control data) • ADD16 (2) = Aggregate/add both PE and RM contributions, samples are 16bit I and Q (not be appropriate for control data) • INSERTPE (1) = Insert the PE contribution, ignoring any possible RM contribution • FWD_RM (0) = Forward the RM contribution, discarding any PE contribution.
13-12	IMUX	CW circuit input swapper (Nibble or bits within each byte). Before CRC calcuation and before Delim, effects both CRC result and effects input to Delim circuit. • NO_SWAP (0) = No swapping is done (Always used) • SWAP_NIBBLES (1) = Swaps the two nibbles in each byte (Never Used) • SWAP_NIBBLE_BITS (2) = Reverses the bits within each nibble (Never Used) • SWAP_BOTH (3) = Reverses the order of the bits in the byte (AIF2 backward compatibility)
11-10	DLMT_OMUX	Delim Circuit output swapper mux (Nibble or bits within each byte). After CRC operation, after Delim operation • NO_SWAP (0) = No swapping (Use with HDLC, HYP_FRM, and NULL) • SWAP_NIBBLES (1) = Swaps the two nibbles within each byte (Never Used) • SWAP_NIBBLE_BITS (2) = Reverses the bits within each nibble (Never Used) • SWAP_BOTH (3) = Reverses the order of the bits within each byte (AIF2 backward compatibility)
9-8	DLMT_IMUX	Delim Circuit input swapper mux (Nibble or bits within each byte). After CRC operation, Before Delim operation • NO_SWAP (0) = No swapping (Use with HDLC, HYP_FRM, and NULL) • SWAP_NIBBLES (1) = Swaps the two nibbles within each byte (Use with 4B5B) • SWAP_NIBBLE_BITS (2) = Reverses the bits within each nibble (Never Used) • SWAP_BOTH (3) = Reverses the order of the bits within each byte (Never Used)
7	HF_LUT_EN	Enable use of hyperframe_lut (which limits usable hyperframes), intended use is RTWP (normally not used) • DISABLE (0) = When 0 the LUT is disabled • ENABLE (1) = When 1 the LUT is enabled
6	CRC_INIT	Selects if the CRC starts with a value of 0 or -1 at the start of a packet. • ZEROS (0) = CRC starts with a 0. May be used for CRC 8 depending on the polynomial used. • ONES (1) = CRC starts with all 1s. Used for CRC 32 and 16. May be used for CRC 8 depending on the polynomial used.

Table 8-656. AIL PE CPRI CONTROL WORD CHANNEL CONFIGURATION REGISTER Field Descriptions (continued)

Bits	Name	Description
5-4	CRC_SEL	Select which form of CRC generation and insertion is to be used • NO_CRC (0) = no CRC is used (Users may wish to use processors to generate CRC or use CRC passed by NetCP Ethernet) • CRC32 (1) = CRC32 is used with fixed polynomial (Used for 4B5B) • CRC16 (2) = CRC16 is used with fixed polynomial (Used for HDLC, May be used for NULL) • CRC8 (3) = CRC8 is used with programmable polynomial (Typically used for NULL)
3-2	DELIN_SEL	Select which form of delineation is to be used for this chan • NULL (0) = Null delineated, null character indicates lack of traffic, SOP: null-to-non_null EOP: non_null-to-null • FAST_ETH (1) = Fast Ethernet, 4B5B encoding • HYP_FRM (2) = hyper frame delineated, capture all indictated CW for enabled hyperframes, creating CPPI packet • HDLC (3) = HDLC
1-0	CRC_RVRS	CRC reverse option for crc16 byte order (illegal for CRC8 or CRC32) • NO_RVRS (0) = No swapping is done. (Used for CRC32 and CRC8. May be used for non-HDLC CRC16) • RVRS_BITS (1) = Swaps the two nibbles in each byte • RVRS_BYTES (2) = Reverses the bits within each nibble • RVRS_BOTH (3) = Reverses the order of the bits in the byte as the bytes first come in to the PE. (Used for HDLC CRC16)

8.6.32.2 AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART0 [Address = 0x2_1010]

PE CPRI Hyperframe Enable Part0, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 0 ~ 31)

Figure 8-571. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART0

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-657. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART0 Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.32.3 AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART1 [Address = 0x2_1014]

PE CPRI Hyperframe Enable Part1, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 32 ~ 63)

Figure 8-572. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART1

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-658. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART1 Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.32.4 AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART2 [Address = 0x2_1018]

PE CPRI Hyperframe Enable Part2, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 64 ~ 95)

Figure 8-573. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART2

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-659. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART2 Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.32.5 AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART3 [Address = 0x2_101C]

PE CPRI Hyperframe Enable Part3, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 96 ~ 127)

Figure 8-574. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART3

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-660. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART3 Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.32.6 AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART4 [Address = 0x2_1020]

PE CPRI Hyperframe Enable Part4, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels (Hyper frame 128 ~ 149)

Figure 8-575. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART4

31	22	21	0
Reserved		HF_EN	
NA-0		R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-661. AIL PE CPRI CW HYPERFRAME LOOK_UP_TABLE PART4 Field Descriptions

Bits	Name	Description
31-22	Reserved	RESERVED
21-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.32.7 AIL PE CPRI CW NULL CHARACTER CONFIGURATION REGISTER [Address = 0x2_1024]

PE CPRI NULL delineator register

Figure 8-576. AIL PE CPRI CW NULL CHARACTER CONFIGURATION REGISTER

31	9	8	0
Reserved		NULL_CHAR	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-662. AIL PE CPRI CW NULL CHARACTER CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8-0	NULL_CHAR	Null Delineator Character: bit8 indicates bit0~7 is k_char. it is safe to use k_char which is not used for CPRI

8.6.32.8 AIL PE CPRI CW CRC8 CONFIGURATION REGISTER [Address = 0x2_1028]

PE CPRI CRC8 control register

Figure 8-577. AIL PE CPRI CW CRC8 CONFIGURATION REGISTER

31	8	7	0
Reserved		CRC8_POLY	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-663. AIL PE CPRI CW CRC8 CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	CRC8_POLY	CRC8 programmable polynomial

8.6.32.9 AIL PE CPRI CW STATUS REGISTER [Address = 0x2_102C]

channel-by-channel packet status. When shutting down a link, it is good practice for APP SW to wait until all channels are out of packet

Figure 8-578. AIL PE CPRI CW STATUS REGISTER

31	4	3	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-664. AIL PE CPRI CW STATUS REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	IN_PKT	Each bit indicates if the corresponding channel is active or not. A 1 indicates the channel is currently in the middle of a packet. A 0 indicatest the channel is out of packet

8.6.32.10 AIL PE CPRI CW FAST ETHERNET 4B5B CONFIGURATION REGISTER [Address = 0x2_1030 + (*S* × 0x0004)]

Size (*S*) = 0:3

PE CPRI fast ethernet control register

Figure 8-579. AIL PE CPRI CW FAST ETHERNET 4B5B CONFIGURATION REGISTER

31 24	23 16	15 14	13 2	1	0
HDR_SOP	HDR_PREAMBLE	HDR	Reserved	SSD_ORDER	BIT_ORDER
R/W-0	R/W-0	R/W-0	NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-665. AIL PE CPRI CW FAST ETHERNET 4B5B CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-24	HDR_SOP	Ethernet header byte to send as the last byte of the preamble (program as 0xD5)
23-16	HDR_PREAMBLE	Ethernet header byte to send as the first 6 or 7 bytes of the preamble (program as 0x55)
15-14	HDR	Selects the number of bytes of the preamble added between the SSD and ESD and the first byte of data. • NO_PREAMBLE (0) = No preamble is used • PREAMBLE_7 (1) = Preamble is 7 bytes. The correct CPRI Fast Ethernet preamble length(normally used with 4B5B) • PREAMBLE_8 (2) = Preamble is 8 bytes (AIF2 backwards compatability) • PREAMBLE_RES (3) = Preamble setting is reserved, do not use.
13-2	Reserved	RESERVED
1	SSD_ORDER	Swaps the order of the 2 SSD and ESD 5 bit values when high • NO_SWAP (0) = No swapping. SSD1 then SSD2. ESD1 then ESD2 (Always Used) • SWAP_NIBBLES (1) = Swap. SSD2 then SSD1. ESD2 then ESD1 (Never Used)
0	BIT_ORDER	Reverses the bit order of the 5 bit 4b5b data when high (applied to both header and data) • NO_SWAP (0) = No swapping (Never Used) • BIT_SWAP (1) = Reverses the bit order (Always Used)

8.6.32.11 AIL PE CPRI CW LOOK_UP_TABLE [Address = 0x2_1400 + (*S* × 0x0004)]

Size (*S*) = 0:255

CPRI CW Channel Register, one register location for each of 256 possible CPRI CW per Hyperframe. Maps the CW to one of four control flows, or unallocated BW

Figure 8-580. AIL PE CPRI CW LOOK_UP_TABLE

31	3	2	1	0
Reserved		CW_EN	CW_CHAN	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-666. AIL PE CPRI CW LOOK_UP_TABLE Field Descriptions

Bits	Name	Description
31-3	Reserved	RESERVED
2	CW_EN	All possible CPRI sub-channel. Dictates whether the control word should be captured or not • DISABLE (0) = When 0 this CW is ignored • ENABLE (1) = When 1 this CW is transferred
1-0	CW_CHAN	Selects which of the 4 channels to use for this basic frame if the enable bit is set

8.6.33 AIL_PD_COMMON_CHAN_CFG [Address = 0x2_8100 + (R × 0x0004)]

Table 8-667. AIL_PD_COMMON_CHAN_CFG

Offset	Acronym	Register Description	Section
0x2_8100 + (*R* × 0x0004)	AIL PD_CHAN_CFG	PD channel 0-63: configuration register	Section 8.6.33.1

8.6.33.1 AIL PD_CHAN_CFG [Address = 0x2_8100 + (R × 0x0004)]

Range (*R*) = 0:63

PD channel 0-63: configuration register

Figure 8-581. AIL PD_CHAN_CFG

31	30 28	27 25	24 0
Reserved	RAD_STD	Reserved	AXC_OFFSET
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-668. AIL PD_CHAN_CFG Field Descriptions

Bits	Name	Description
31	Reserved	RESERVED
30-28	RAD_STD	assign each channel to one of 8 radio standards. Used for radio standard FSM and RadT selection
27-25	Reserved	RESERVED
24-0	AXC_OFFSET	OBSAI: Antenna Carrier offset programmed in 307.2MHz clocks and relative to the Frame Boundary of the RadT AT timer. Specifies the center of the receive window for an AxC offset. CPRI: Antenna Carrier Offset programmed in (non-oversampled) samples, relative to the Radio frame boundary. This concept of an AxC_Offset in addition to the Radio Standard Offset seems go beyond the CPRI standard. It is expected that most CPRI users will program this field as zero.

8.6.34 AIL_PD_CPRI_AXC_CFG [Address = 0x2_8800]

Table 8-669. AIL_PD_CPRI_AXC_CFG

Offset	Acronym	Register Description	Section
0x2_8800	AIL PD_CPRI_AXC0_CFG	PD CPRI PHY Container LUT: Maps CPRI transports containers to 1 of 8 groups (radio standard), Only CPRI16x can use full 64 depth of LUT	Section 8.6.34.1
0x2_8900	AIL PD_CPRI_BUB_FSM_CFG	CPRI Mapping Method 3, Bubble insertion state machine control, total of 8 separate FSMs, one per 8 groups/radio_standards	Section 8.6.34.2
0x2_8920	AIL PD_CPRI_BUB_FSM2_CFG	CPRI Mapping Method 3, Bubble insertion state machine control, total of 8 separate FSMs, one per 8 groups/radio_standards	Section 8.6.34.3
0x2_8940	AIL PD_CPRI_TDM_FSM_CFG	FSM-by-FSM, CPRI AxC TDM. Intended use is one FSM per radio standard (matching AIL_PHY_CI groups)	Section 8.6.34.4
0x2_8960	AIL PD_CPRI_RADSTD_CFG	Enables each individual radio standard for the PD for up to 8 radio standards	Section 8.6.34.5
0x2_8980	AIL PD_CPRI_RADSTD1_CFG	Defines the Radio Standard Offset per radio standard	Section 8.6.34.6
0x2_89A0	AIL PD_CPRI_RADSTD2_CFG	Defines the number of Basic Frames per radio standard	Section 8.6.34.7
0x2_89C0	AIL PD_CPRI_RADSTD_STS	Read Only status of each radio status reflecting enable and satisfying basic frame offset	Section 8.6.34.8

8.6.34.1 AIL PD_CPRI_AXC0_CFG [Address = 0x2_8800 + (*S* × 0x0004)]

Size (*S*) = 0:63

PD CPRI PHY Container LUT: Maps CPRI transports containers to 1 of 8 groups (radio standard), Only CPRI16x can use full 64 depth of LUT

Figure 8-582. AIL PD_CPRI_AXC0_CFG

31	4	3	2	0
Reserved		CONT_LUT_EN	CONT_LUT_GRP	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-670. AIL PD_CPRI_AXC0_CFG Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3	CONT_LUT_EN	0: container is unused by PD 1: container is mapped by cont_lut_grp • CONT_DIS (0) = CONT_DIS • CONT_EN (1) = CONT_EN
2-0	CONT_LUT_GRP	Group (radio standard) which container belongs to, 0-to-7

8.6.34.2 AIL PD_CPRI_BUB_FSM_CFG [Address = 0x2_8900 + (*S* × 0x0004)]

Size (*S*) = 0:7

CPRI Mapping Method 3, Bubble insertion state machine control, total of 8 separate FSMs, one per 8 groups/radio_standards

Figure 8-583. AIL PD_CPRI_BUB_FSM_CFG

31	18	17	0
Reserved		KNC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-671. AIL PD_CPRI_BUB_FSM_CFG Field Descriptions

Bits	Name	Description
31-18	Reserved	RESERVED
17-0	KNC	(K x Nc) total number of containers per AxC container group(block). if the bubble FSM is not used, this should be matched with ncont value in TDM FSM config. Set N-1

8.6.34.3 AIL PD_CPRI_BUB_FSM2_CFG [Address = 0x2_8920 + (*S* × 0x0004)]

Size (*S*) = 0:7

CPRI Mapping Method 3, Bubble insertion state machine control, total of 8 separate FSMs, one per 8 groups/radio_standards

Figure 8-584. AIL PD_CPRI_BUB_FSM2_CFG

31	30	29	18	17	0
Reserved		GAP_FRAC		GAP_INT	
NA-0		R/W-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-672. AIL PD_CPRI_BUB_FSM2_CFG Field Descriptions

Bits	Name	Description
31-30	Reserved	RESERVED
29-18	GAP_FRAC	Bubble Gap Fractional portion configuration (eg. set 25 for 0.25)
17-0	GAP_INT	Bubble Gap Integer portion configuration. set 0,if no bubble is required.

8.6.34.4 AIL PD_CPRI_TDM_FSM_CFG [Address = 0x2_8940 + (*S* × 0x0004)]

Size (*S*) = 0:7

FSM-by-FSM, CPRI AxC TDM. Intended use is one FSM per radio standard (matching AIL_PHY_CI groups)

Figure 8-585. AIL PD_CPRI_TDM_FSM_CFG

31 24	23 16	15 8	7 0
Reserved	STRT_LUT	NCONT	Reserved
NA-0	R/W-0	R/W-0	NA-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-673. AIL PD_CPRI_TDM_FSM_CFG Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	STRT_LUT	first TDM_LUT entry for this fsm.
15-8	NCONT	number of TDM_LUT entries (containers) for this FSM (For LTE20, 8 sequential entries within TDM_LUT). Set N-1
7-0	Reserved	RESERVED

8.6.34.5 AIL PD_CPRI_RADSTD_CFG [Address = 0x2_8960 + (*S* × 0x0004)]

Size (*S*) = 0:7

Enables each individual radio standard for the PD for up to 8 radio standards

Figure 8-586. AIL PD_CPRI_RADSTD_CFG

31	1	0
Reserved		EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-674. AIL PD_CPRI_RADSTD_CFG Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EN	Enable bit for the corresponding radio standard

8.6.34.6 AIL PD_CPRI_RADSTD1_CFG [Address = 0x2_8980 + (*S* × 0x0004)]

Size (*S*) = 0:7

Defines the Radio Standard Offset per radio standard

Figure 8-587. AIL PD_CPRI_RADSTD1_CFG

31 16	15 8	7 0
Reserved	HFRM_OFFSET	BFRM_OFFSET
NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-675. AIL PD_CPRI_RADSTD1_CFG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-8	HFRM_OFFSET	Hyper Frame Index of Radio Standard Offset
7-0	BFRM_OFFSET	Basic Frame Index of Radio Standard Offset

8.6.34.7 AIL PD_CPRI_RADSTD2_CFG [Address = 0x2_89A0 + (*S* × 0x0004)]

Size (*S*) = 0:7

Defines the number of Basic Frames per radio standard

Figure 8-588. AIL PD_CPRI_RADSTD2_CFG

31	18	17	0
Reserved		BFRM_NUM	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-676. AIL PD_CPRI_RADSTD2_CFG Field Descriptions

Bits	Name	Description
31-18	Reserved	RESERVED
17-0	BFRM_NUM	Number of Basic Frames in a Radio frame. Set N-1

8.6.34.8 AIL PD_CPRI_RADSTD_STS [Address = 0x2_89C0 + (*S* × 0x0004)]

Size (*S*) = 0:7

Read Only status of each radio status reflecting enable and satisfying basic frame offset

Figure 8-589. AIL PD_CPRI_RADSTD_STS

31	1	0
Reserved		ON
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-677. AIL PD_CPRI_RADSTD_STS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ON	0x1: RADSTD_ON 0x0:RADSTD_OFF

8.6.35 AIL_PD_CPRI_AXC_TDM_LUT_CFG [Address = 0x2_8C00 + (*R* × 0x0004)]

Table 8-678. AIL_PD_CPRI_AXC_TDM_LUT_CFG

Offset	Acronym	Register Description	Section
0x2_8C00 + (*R* × 0x0004)	AIL PD_CPRI_AXC_TDM_LUT_CFG	TDM AxC LUT. Used to map streams of CPRI containers to appropriate AxC. AxC are listed in order that they are represented on the CPRI link, different portions of LUT allocated to different groups (radio standards)	Section 8.6.35.1

8.6.35.1 AIL PD_CPRI_AXC_TDM_LUT_CFG [Address = 0x2_8C00 + (*R* × 0x0004)]

Range (*R*) = 0:255

TDM AxC LUT. Used to map streams of CPRI containers to appropriate AxC. AxC are listed in order that they are represented on the CPRI link, different portions of LUT allocated to different groups (radio standards)

Figure 8-590. AIL PD_CPRI_AXC_TDM_LUT_CFG

31	8	7	6	5	0
Reserved		EN	Reserved	AXC	
NA-0		R/W-0	NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-679. AIL PD_CPRI_AXC_TDM_LUT_CFG Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7	EN	Enables each entry. Disabled entries will result in dropped CPRI containers. With this disable, SW is not required to maintain unique AxC value for unused containers.
6	Reserved	RESERVED
5-0	AXC	List of AxC indexes giving TDM AxC order over CPRI link

8.6.36 AIL_PD_CPRI_CW_CFG [Address = 0x2_9000]

Table 8-680. AIL_PD_CPRI_CW_CFG

Offset	Acronym	Register Description	Section
0x2_9000	AIL PD_CPRI_CW_CHAN_CFG	PD CPRI Codeword Configuration register	Section 8.6.36.1
0x2_9400	AIL PD_CPRI_CW_LUT_CFG	CPRI CW Channel LUT Register	Section 8.6.36.2
0x2_9800	AIL PD_CPRI_HYPFRM0_LUT_CFG	PD CPRI Hyperframe Enable Part0, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels	Section 8.6.36.3
0x2_9804	AIL PD_CPRI_HYPFRM1_LUT_CFG	PD CPRI Hyperframe Enable Part1, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels	Section 8.6.36.4
0x2_9808	AIL PD_CPRI_HYPFRM2_LUT_CFG	PD CPRI Hyperframe Enable Part2, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels	Section 8.6.36.5
0x2_980C	AIL PD_CPRI_HYPFRM3_LUT_CFG	PD CPRI Hyperframe Enable Part3, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels	Section 8.6.36.6
0x2_9810	AIL PD_CPRI_HYPFRM4_LUT_CFG	PD CPRI Hyperframe Enable Part4, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels	Section 8.6.36.7
0x2_9814	AIL PD_CPRI_NULL_CFG	PD CPRI NULL Delimiter control register	Section 8.6.36.8
0x2_9818	AIL PD_CPRI_CRC_CFG	PD CPRI CRC8 control register	Section 8.6.36.9
0x2_9820	AIL PD_CPRI_4B5B_CFG	PD CPRI Fast Ethernet control register	Section 8.6.36.10

8.6.36.1 AIL PD_CPRI_CW_CHAN_CFG [Address = 0x2_9000 + (*S* × 0x0004)]

Size (*S*) = 0:3

PD CPRI Codeword Configuration register

Figure 8-591. AIL PD_CPRI_CW_CHAN_CFG

31 16	15 14	13 12	11 10
BYTE_EN	HDLC_RVRS_CRC	QWD_OMUX	DLMT_OMUX
R/W-0xFFFF	R/W-0	R/W-0	R/W-0

9 8	7	6	5 4	3 2	1	0
DLMT_IMUX	Reserved	CRC_INIT	CRC_SEL	DELIN_SEL	HF_LUT_EN	CHAN_EN
R/W-0	NA-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-681. AIL PD_CPRI_CW_CHAN_CFG Field Descriptions

Bits	Name	Description
31-16	BYTE_EN	CW byte Enable, used to disable CW bytes for some low rate HDLC or 5x/10x RTWP. (normal use set 0xffff)
15-14	HDLC_RVRS_CRC	Controls bit swapping of the CRC for the HDLC only • RVRS_CRC_NONE (0) = No reversing of the CRC bits (Never Used) • RVRS_CRC_BIT (1) = Reverse bits of the CRC (Never Used) • RVRS_CRC_BYTE (2) = Reverse bytes of the CRC (Never Used) • RVRS_CRC_BOTH (3) = Reverse all bits and bytes in the CRC (Always Used)
13-12	QWD_OMUX	Final swapping after the CRC operation. • NO_SWAP (0) = No swapping (Use with HDLC, HYP_FRM, 4B5B and NULL) • SWAP_NIBBLES (1) = Swaps the two nibbles within each byte (Never Used) • SWAP_NIBBLE_BITS (2) = Reverses the bits within each nibble (Never Used) • SWAP_BOTH (3) = Reverses the order of the bits within each byte (AIF2 backward compatible use case)
11-10	DLMT_OMUX	Delim Circuit output swapper mux (Nibble or bits within each byte). After Delim operation, before CRC operation • NO_SWAP (0) = No swapping (Use with HDLC, HYP_FRM, and NULL) • SWAP_NIBBLES (1) = Swaps the two nibbles within each byte (Use with 4B5B) • SWAP_NIBBLE_BITS (2) = Reverses the bits within each nibble (Never Used) • SWAP_BOTH (3) = Reverses the order of the bits within each byte (Never Used)
9-8	DLMT_IMUX	Delim Circuit input swapper mux (Nibble or bits within each 8 bit aligned data). Before CRC and Delim operation. Only used for users who want to do AIF2 PD pre 4b5b bit swap like operation • NO_SWAP (0) = No swapping (Use with HDLC, HYP_FRM, and NULL) • SWAP_NIBBLES (1) = Swaps the two nibbles within each byte (Never Used) • SWAP_NIBBLE_BITS (2) = Reverses the bits within each nibble (Never Used) • SWAP_BOTH (3) = Reverses the order of the bits within each byte (AIF2 backward compatible use case)
7	Reserved	RESERVED
6	CRC_INIT	Selects if the CRC starts with a value of 0 or -1 at the start of a packet. • ZEROS (0) = CRC starts with a 0. May be used for CRC 8 depending on the polynomial used. • ONES (1) = CRC starts with all 1s. Used for CRC 32 and 16. May be used for CRC 8 depending on the polynomial used.
5-4	CRC_SEL	Select which form of CRC check to perform • NO_CRC (0) = no CRC is used. (Used for Hyperframe) • CRC32 (1) = CRC32 is used with fixed polynomial. (Used for 4B5B) • CRC16 (2) = CRC16 is used with fixed polynomial. (Used for HDLC. May be used for NULL) • CRC8 (3) = CRC8 is used with programmable polynomial (Typically used for NULL)

Table 8-681. AIL PD_CPRI_CW_CHAN_CFG Field Descriptions (continued)

Bits	Name	Description
3-2	DELIN_SEL	Select which form of delineation is to be used for this channel • NULL (0) = Null delineated, null character indicates lack of traffic, SOP: null-to-non_null EOP: non_null-to-null • FAST_ETH (1) = Fast Ethernet, 4B5B encoding • HYP_FRM (2) = hyper frame boundary delineated, capture all indictated CW for enabled hyperframes • HDLC (3) = HDLC
1	HF_LUT_EN	Enables use of hyperframe_lut (which limits usable hyperframes), intended use is RTWP • DISABLE (0) = When 0 the LUT is disabled • ENABLE (1) = When 1 the LUT is enabled
0	CHAN_EN	All possible CPRI sub-channels are are mapped to one of four CPRI CW staging areas. This allow CPRI CW to be split into 4 different streams. • DISABLE (0) = When 0 the channel is disabled • ENABLE (1) = When 1 the channel is enabled

8.6.36.2 AIL PD_CPRI_CW_LUT_CFG [Address = 0x2_9400 + (*S* × 0x0004)]

Size (*S*) = 0:255

CPRI CW Channel LUT Register

Figure 8-592. AIL PD_CPRI_CW_LUT_CFG

31	3	2	1	0
Reserved		CW_EN	CW_CHAN	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-682. AIL PD_CPRI_CW_LUT_CFG Field Descriptions

Bits	Name	Description
31-3	Reserved	RESERVED
2	CW_EN	All possible CPRI sub-channel. Dictates whether the control word should be captured or not • DISABLE (0) = When 0 this CW is ignored • ENABLE (1) = When 1 this CW is transferred
1-0	CW_CHAN	Selects which of the 4 channels to use for this basic frame if the enable bit is set.

8.6.36.3 AIL PD_CPRI_HYPFRM0_LUT_CFG [Address = 0x2_9800]

PD CPRI Hyperframe Enable Part0, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels

Figure 8-593. AIL PD_CPRI_HYPFRM0_LUT_CFG

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-683. AIL PD_CPRI_HYPFRM0_LUT_CFG Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.36.4 AIL PD_CPRI_HYPFRM1_LUT_CFG [Address = 0x2_9804]

PD CPRI Hyperframe Enable Part1, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels

Figure 8-594. AIL PD_CPRI_HYPFRM1_LUT_CFG

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-684. AIL PD_CPRI_HYPFRM1_LUT_CFG Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.36.5 AIL PD_CPRI_HYPFRM2_LUT_CFG [Address = 0x2_9808]

PD CPRI Hyperframe Enable Part2, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels

Figure 8-595. AIL PD_CPRI_HYPFRM2_LUT_CFG

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-685. AIL PD_CPRI_HYPFRM2_LUT_CFG Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.36.6 AIL PD_CPRI_HYPFRM3_LUT_CFG [Address = 0x2_980C]

PD CPRI Hyperframe Enable Part3, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels

Figure 8-596. AIL PD_CPRI_HYPFRM3_LUT_CFG

31	0
HF_EN	
R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-686. AIL PD_CPRI_HYPFRM3_LUT_CFG Field Descriptions

Bits	Name	Description
31-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.36.7 AIL PD_CPRI_HYPFRM4_LUT_CFG [Address = 0x2_9810]

PD CPRI Hyperframe Enable Part4, used to support RTWP, use enabled by cw_chan register, only one hyperframe_lut for all 4 channels

Figure 8-597. AIL PD_CPRI_HYPFRM4_LUT_CFG

31	22	21	0
Reserved		HF_EN	
NA-0		R/W-NaN	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-687. AIL PD_CPRI_HYPFRM4_LUT_CFG Field Descriptions

Bits	Name	Description
31-22	Reserved	RESERVED
21-0	HF_EN	Enable bit per Hyperframe, 1: hyperframe used, 0: hyperframe unused

8.6.36.8 AIL PD_CPRI_NULL_CFG [Address = 0x2_9814]

PD CPRI NULL Delimiter control register

Figure 8-598. AIL PD_CPRI_NULL_CFG

31	9	8	0
Reserved		NULL_CHAR	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-688. AIL PD_CPRI_NULL_CFG Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8-0	NULL_CHAR	Null Delineator Character: bit8 indicates bit0~7 is k_char. it is safe to use k_char which is not used for CPRI

8.6.36.9 AIL PD_CPRI_CRC_CFG [Address = 0x2_9818]

PD CPRI CRC8 control register

Figure 8-599. AIL PD_CPRI_CRC_CFG

31 16	15 8	7 0
Reserved	CRC8_COMP	CRC8_POLY
NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-689. AIL PD_CPRI_CRC_CFG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-8	CRC8_COMP	CRC8 compare value when init is choosen as 1's. Sometimes referred as the Magic Number. Depends on chosen polynomial.
7-0	CRC8_POLY	CRC8 programmable polynomial

8.6.36.10 AIL PD_CPRI_4B5B_CFG [Address = 0x2_9820 + (*S* × 0x0004)]

Size (*S*) = 0:3

PD CPRI Fast Ethernet control register

Figure 8-600. AIL PD_CPRI_4B5B_CFG

31	4	3	2	1	0
Reserved		SSD_ORDER	BIT_ORDER	HDR	
NA-0		R/W-0	R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-690. AIL PD_CPRI_4B5B_CFG Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3	SSD_ORDER	Swaps the order of the 2 SSD and ESD 5 bit values when high. Should always be set low. • NORMAL (0) = The SSD1 or ESD1 is sent first followed by the SSD2 or ESD2. • REVERSE (1) = The SSD2 or ESD2 is sent first followed by the SSD1 or ESD1.
2	BIT_ORDER	Reverses the bit order of the 5 bit 4b5b data when high. this reversion includes HDR and SSD. Normally, should be set high. • NORMAL (0) = No bit reversal. For example a hex 0 which is decoded as 11110 will have the bits transferred out from left to right. • REVERSE (1) = Reverse bits. For example a hex 0 which is decoded as 11110 will have the bits transferred out from right to left.
1-0	HDR	Header stripping control selects how many bytes if any to ignore at the start of the packet. • NO_STRIP (0) = No stripping of the header • STRIP_7 (1) = Strip 7 bytes of header. Typically used) • STRIP_8 (2) = Strip 8 bytes of header. (AIF2 backward compatibility) • NO_CRC (3) = No stripping and ignore the CRC.

8.6.37 AIL_PD_OBSAI_CFG [Address = 0x2_A000]

Table 8-691. AIL_PD_OBSAI_CFG

Offset	Acronym	Register Description	Section
0x2_A000	AIL PD_OBSAI_GSM_BBHOP_CFG	chan-by-chan strobe signal: OBSAI GSM base band hopping control. Indicates to PD that next timeslot will not have PHY data. pd_gsm_bbhop_cfg[1]: chan 63-to-32 pd_gsm_bbhop_cfg[0]: chan 31-to-0. Value is cleared once used or if channel is OFF and not enabled.	Section 8.6.37.1
0x2_A010	AIL PD_OBSAI_RP3_01_STS	RP3_01 FCB capture from received OBSAI msg. Capture is OBSAI Type triggered, Type LUT has capture control. Whole OBSAI qwd payload is captured to 4 MMRs	Section 8.6.37.2
0x2_A020	AIL PD_OBSAI_RADSTD_CFG	OBSAI timing control, RadT usage	Section 8.6.37.3
0x2_A040	AIL PD_OBSAI_RADT_CFG	OBSAI timing control, RadT usage	Section 8.6.37.4
0x2_A060	AIL PD_OBSAI_FRM_TC_CFG	For framing state machine, supplies terminal counts of some of the state counters and some start counts. Eight different versions of this register are used to support 8 different radio standard variants simultaneously	Section 8.6.37.5

8.6.37.1 AIL PD_OBSAI_GSM_BBHOP_CFG [Address = 0x2_A000 + (*S* × 0x0004)]

Size (*S*) = 0:1

chan-by-chan strobe signal: OBSAI GSM base band hopping control. Indicates to PD that next timeslot will not have PHY data. pd_gsm_bbhop_cfg[1]: chan 63-to-32 pd_gsm_bbhop_cfg[0]: chan 31-to-0. Value is cleared once used or if channel is OFF and not enabled.

Figure 8-601. AIL PD_OBSAI_GSM_BBHOP_CFG

31	0
OFF_STB	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-692. AIL PD_OBSAI_GSM_BBHOP_CFG Field Descriptions

Bits	Name	Description
31-0	OFF_STB	1: next GSM time slot is OFF for this chan 0: normal, expect data to arrive on Phy (This register only used if pd_chan_cfg.gsm_bbhop=1)

8.6.37.2 AIL PD_OBSAI_RP3_01_STS [Address = 0x2_A010 + (*S* × 0x0004)]

Size (*S*) = 0:3

RP3_01 FCB capture from received OBSAI msg. Capture is OBSAI Type triggered, Type LUT has capture control. Whole OBSAI qwd payload is captured to 4 MMRs

Figure 8-602. AIL PD_OBSAI_RP3_01_STS

31	0
CAPTURE	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-693. AIL PD_OBSAI_RP3_01_STS Field Descriptions

Bits	Name	Description
31-0	CAPTURE	one of four payload word

8.6.37.3 AIL PD_OBSAI_RADSTD_CFG [Address = 0x2_A020 + (*S* × 0x0004)]

Size (*S*) = 0:7

OBSAI timing control, RadT usage

Figure 8-603. AIL PD_OBSAI_RADSTD_CFG

31 28	27 16	15 12	11 0
Reserved	AXCOFFSET_WIN	Reserved	WDOG_TC
NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-694. AIL PD_OBSAI_RADSTD_CFG Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-16	AXCOFFSET_WIN	OBSAI reception timing window width parameter. Indicates the window size for searching the radio frame boundary identified by TS=0. Minimum WCDMA value is (320/2 + 80)
15-12	Reserved	RESERVED
11-0	WDOG_TC	watch dog timer terminal count (sys_clks)

8.6.37.4 AIL PD_OBSAI_RADT_CFG [Address = 0x2_A040 + (*S* × 0x0004)]

Size (*S*) = 0:7

OBSAI timing control, RadT usage

Figure 8-604. AIL PD_OBSAI_RADT_CFG

31	25	24	0
Reserved		TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-695. AIL PD_OBSAI_RADT_CFG Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	TC	Max expected value for the RadT timer value. Used for creating an expected timing window (for which TS=0 marks a Radio Frame Boundary)

8.6.37.5 AIL PD_OBSAI_FRM_TC_CFG [Address = 0x2_A060 + (*S* × 0x0004)]

Size (*S*) = 0:7

For framing state machine, supplies terminal counts of some of the state counters and some start counts. Eight different versions of this register are used to support 8 different radio standard variants simultaneously

Figure 8-605. AIL PD_OBSAI_FRM_TC_CFG

31 24	23 16	15 8	7 0
Reserved	SYM_TC	INDEX_SC	INDEX_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-696. AIL PD_OBSAI_FRM_TC_CFG Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	SYM_TC	Radio framing counter. Symbol terminal count.
15-8	INDEX_SC	Radio framing counter. Index Start count.
7-0	INDEX_TC	Radio framing counter. Index Terminal count.

8.6.38 AIL_PD_OBSAI_LUT_CFG [Address = 0x2_A100]

Table 8-697. AIL_PD_OBSAI_LUT_CFG

Offset	Acronym	Register Description	Section
0x2_A100	AIL PD_OBSAI_CHAN_CFG	PD Channel Control Register	Section 8.6.38.1
0x2_A200	AIL PD_OBSAI_ROUTE_CFG	Information used to decode OBSAI header information for routing into PD channels.	Section 8.6.38.2
0x2_A300	AIL PD_OBSAI_TYPE_LUT_CFG	OBSAI Type Look Up Table. Allows for new OBSAI types to be defined (and reconfiguation of exisiting Types)	Section 8.6.38.3

8.6.38.1 AIL PD_OBSAI_CHAN_CFG [Address = 0x2_A100 + (*S* × 0x0004)]

Size (*S*) = 0:63

PD Channel Control Register

Figure 8-606. AIL PD_OBSAI_CHAN_CFG

31	5	4	3	1	0
Reserved		GSM_UL	Reserved		WDOG_EN
NA-0		R/W-0	NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-698. AIL PD_OBSAI_CHAN_CFG Field Descriptions

Bits	Name	Description
31-5	Reserved	RESERVED
4	GSM_UL	Data Format Selection • OTHER (0) = Not GSM UL • GSM_UL (1) = GSM UL, has special OBSAI Time Stamp implications. UL time stamp format msb=1 first four msg
3-1	Reserved	RESERVED
0	WDOG_EN	Enable WDog timer. Used for missing traffic handling and GSM BB_Hop missing EOP. WDog is configured per radio standard

8.6.38.2 AIL PD_OBSAI_ROUTE_CFG [Address = 0x2_A200 + (*S* × 0x0004)]

Size (*S*) = 0:63

Information used to decode OBSAI header information for routing into PD channels.

Figure 8-607. AIL PD_OBSAI_ROUTE_CFG

31	30	29 28	27 24	23 11	10 6	5 0
CHAN_EN	Reserved	CHAN_MASK	Reserved	CHAN_ADR	CHAN_TYPE	CHAN_TS
R/W-0	NA-0	R/W-0	NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-699. AIL PD_OBSAI_ROUTE_CFG Field Descriptions

Bits	Name	Description
31	CHAN_EN	0: this channel is always OFF(assumes other fields are junk) 1: channel is enabled
30	Reserved	RESERVED
29-28	CHAN_MASK	Reception Routing: controls how many OBSAI time stamp bits to use in the reception routing • NONE (0) = none. Do not use the TS field for routing • 4LSB (1) = 4 lsb bits: Use TS(3:0) • ALL (2) = all Use TS(5:0) • RESERVED (3) = Reserved
27-24	Reserved	RESERVED
23-11	CHAN_ADR	Reception Routing: OBSAI address
10-6	CHAN_TYPE	Reception Routing: OBSAI type
5-0	CHAN_TS	Reception Routing: OBSAI time stamp. Used to extend addressing by using the TS field. (Only known use is for OBSAI Generic Packet type and Control Packet type) The number of bits of TS to compare is controlled via the CHAN_MASK field.

8.6.38.3 AIL PD_OBSAI_TYPE_LUT_CFG [Address = 0x2_A300 + (*S* × 0x0004)]

Size (*S*) = 0:31

OBSAI Type Look Up Table. Allows for new OBSAI types to be defined (and reconfiguation of exisiting Types)

Figure 8-608. AIL PD_OBSAI_TYPE_LUT_CFG

31 18	17	16	15 12	11
Reserved	RP3_01_RST	RP3_01	Reserved	ENET_STRIP
NA-0	R/W-0	R/W-0	NA-0	R/W-0

10 9	8	7	6	5	4	3	2 0
Reserved	OBSAI_PKT_EN	Reserved	CRC_HDR	CRC_EN	CRC_TYPE	Reserved	TS _FORMAT
NA-0	R/W-0	NA-0	R/W-0	R/W-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-700. AIL PD_OBSAI_TYPE_LUT_CFG Field Descriptions

Bits	Name	Description
31-18	Reserved	RESERVED
17	RP3_01_RST	Used for RP3-01 Reset reception. If message type is received with correct address, causing an SoC reset, if enabled.
16	RP3_01	Used for RP3-01 FCB reception (slave timing sync via OBSAI link). Capture the OBSAI payload to an MMR, Fire off a strobe to uAT for BCN capture, fire off an EE for purposes of alerting processors of FCB arival
15-12	Reserved	RESERVED
11	ENET_STRIP	0x0: No Strip 0x1: Strip off the first 8 bytes of each packet. Purpose is to strip the ethernet preamble and SOP. PD blindly strips without checking content of 8 bytes. CRC is not calculated over stripped bytes.
10-9	Reserved	RESERVED
8	OBSAI_PKT_EN	determines if channel is packet type channel or axc type channel. AxC types align to Radio Frame Boundary while pkt alignment is a don't care. AXC channels are expected to stream where packet channels are on-demand. AXC channels use OBSAI Time Stamp and AXC Offset while packet traffic does not. Intended to be programmed consistantly with other TS format fields • OBSAI_AXC (0) = OBSAI_AXC • OBSAI_PKT (1) = OBSAI_PKT
7	Reserved	RESERVED
6	CRC_HDR	CRC16 is calculated over OBSAI header as well as payload (only valid for OBSAI TYPES CONTROL (0x0) & MEASUREMENT (0x1) • CRC_HDR_ON (1) = CRC16 is calculated over 3 byte OBSAI header and 14 bytes of 16 byte payload. Only valid for 19 byte OBSAI messages utilizing CRC16 • CRC_HDR_OFF (0) = do not perform CRC over OBSAI Header (program to OFF for CPRI and for most OBSAI types)
5	CRC_EN	CRC: enable CRC check on type-by-type basis.
4	CRC_TYPE	CRC: length of CRC. • 32BIT_CRC (0) = 32BIT_CRC • 16BIT_CRC (1) = 16BIT_CRC
3	Reserved	RESERVED

Table 8-700. AIL PD_OBSAI_TYPE_LUT_CFG Field Descriptions (continued)

Bits	Name	Description
2-0	TS_FORMAT	TS: OBSAI time stamp check • NO_TS (0) = No time stamp check, might be useful for some future radio standard or debug • NORM_TS (1) = normal time stamp format • GSM (2) = GSM OBSAI Time Stamp, UL time stamp format msb=1 first four msg. DL time stamp format msb=1 first msg • GEN_PKT (3) = Generic Packet (SOP=10, MOP=00, EOP=11) • ETHERNET (4) = Ethernet Type where last TS indicates number of valid bytes in last transfer • CTR_PKT (5) = TS checked by PD_Route, one message packet with inferred SOP & EOP in same OBSAI message. Accepts TS=6'b000000 or TS=6'b000001. (Use chan_mask and chan_ts for more exact checking)

8.6.39 AIL_PD_OBSAI_FRM_MSG_TC_CFG [Address = 0x2_A400 + (R × 0x0004)]

Table 8-701. AIL_PD_OBSAI_FRM_MSG_TC_CFG

Offset	Acronym	Register Description	Section
0x2_A400 + (*R* × 0x0004)	AIL PD_OBSAI_FRM_MSG_TC_CFG	PD Frame Message Terminal Count Register. This table is shared between all 8 radio standards. The index values control the mapping of different portions of this table to the different radio standards	Section 8.6.39.1

8.6.39.1 AIL PD_OBSAI_FRM_MSG_TC_CFG [Address = 0x2_A400 + (R × 0x0004)]

Range (*R*) = 0:255

PD Frame Message Terminal Count Register. This table is shared between all 8 radio standards. The index values control the mapping of different portions of this table to the different radio standards

Figure 8-609. AIL PD_OBSAI_FRM_MSG_TC_CFG

31	16	15	0
Reserved		TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-702. AIL PD_OBSAI_FRM_MSG_TC_CFG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	TC	Radio AxC framing counter. nx4 sample count (equal to OBSAI message count). Note this differs from similar registers in the SI_ING and SI_EGR which is programmed in units of samples vs. nx4 samples. For nornal TimeStamp prediction, RadStd FSM does not need to predict SYM bounaries, only Frame boundaries. For LTE1.4 and LTE3.0 use program for only 1 sym per sub-frame (0.5 ms)

8.6.40 AIL_phy_glb [Address = 0x3_0000]

Table 8-703. AIL_phy_glb

Offset	Acronym	Register Description	Section
0x3_0000	AIL PHY GLOBAL CONFIGURATION REGISTER	The AIL PHY Global Configuration Register defines the global operation of the AIL PHY	Section 8.6.40.1

8.6.40.1 AIL PHY GLOBAL CONFIGURATION REGISTER [Address = 0x3_0000]

The AIL PHY Global Configuration Register defines the global operation of the AIL PHY

Figure 8-610. AIL PHY GLOBAL CONFIGURATION REGISTER

31 8	7	6 4	3	2 0
Reserved	SHORT_FRM_EN	Reserved	OBSAI_CPRI	LINK_RATE
NA-0	R/W-0	NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-704. AIL PHY GLOBAL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	SHORT_FRM_EN	Short Frame Enable - Short frame enable mode is only used for TI internal verification purposes (never set this bit in an actual BTS)
6-4	Reserved	Reserved
3	OBSAI_CPRI	The OBSAI/CPRI bit defines the mode of operation for the link. This field may only be modified while the AIL is idle and may not be updated on-the-fly • CPRI (0) = CPRI Mode - The AIL Phy is configured for CPRI Operation • OBSAI (1) = OBSAI Mode - The AIL Phy is configured for OBSAI Operation
2-0	LINK_RATE	The link rate field defines the rate of the link. The field should only be updated if the TM Enable and RM Enable bits are 0. These link rates control the protocol layer as well (PD and PE). The field can be programmed for the following rates • 8X (0) = 8x Rate • 4X (1) = 4x Rate • 2X (2) = 2x Rate • 5X (3) = 5x Rate (CPRI Only) • 10X (4) = 10x Rate (CPRI Only) • 16X (5) = 16x Rate (CPRI Only)

8.6.41 AIL_phy_rt [Address = 0x3_0040]

Table 8-705. AIL_phy_rt

Offset	Acronym	Register Description	Section
0x3_0040	AIL PHY RT CONFIGURATION REGISTER	The AIL PHY RT Configuration Register defines the basic operation of the RT block	Section 8.6.41.1
0x3_0044	AIL PHY RT DEPTH STATUS REGISTER	The AIL PHY RT Depth Status Register displays the real time depth of the Link Buffer in the RT Block	Section 8.6.41.2
0x3_0048	AIL PHY RT HEADER ERROR STATUS REGISTER	The AIL PHY RT Header Error Status Register displays the status of the last header error determined during aggregation operations while the RT block is in OBSAI Mode	Section 8.6.41.3

8.6.41.1 AIL PHY RT CONFIGURATION REGISTER [Address = 0x3_0040]

The AIL PHY RT Configuration Register defines the basic operation of the RT block

Figure 8-611. AIL PHY RT CONFIGURATION REGISTER

31 16	15 8	7 5	4 3	2	1 0
Reserved	BF_DELAY	CI_LINK	Reserved	EM_EN	CONFIG
NA-0	R/W-0	R/W-0	NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-706. AIL PHY RT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved
15-8	BF_DELAY	(CPRI Only) Indicates repositioning of ingress AxC traffic into egress link due to Uplink RE Chaining. This value is the basic frame number on the egress link corresponding to basic frame 0 on the ingress link. normally set to zero
7-5	CI_LINK	Selects which Ingress AIL link is used (forwarding or aggregation) into egress link. • SEL_LINK0 (0) = Select CI AIL 0 • SEL_LINK1 (1) = Select CI AIL 1 • SEL_LINK2 (2) = Select CI AIL 2 • SEL_LINK3 (3) = Select CI AIL 3 • SEL_LINK4 (4) = Not Used • SEL_LINK5 (5) = Not Used • SEL_LINK6 (6) = Not Used • SEL_LINK7 (7) = Not Used
4-3	Reserved	Reserved
2	EM_EN	(OBSAI Only) Ingress messages are converted to OBSAI Empty Msg when an LCV error is detected in the header. (recommended) • DISABLE (0) = Empty Message Insertion Disabled • ENABLE (1) = Empty Message Insertion Enabled
1-0	CONFIG	The RT Config field defines the operation mode of the RT Block • FWDG_MODE (0) = Forwading Mode - The AIL Phy only transmits data that it receives from an external link • AGGR_MODE (1) = Aggregate Mode - Used to combine local SOC generated traffic with traffic recieved from remote device. In this mode, Protocol Layer (PE) controls the aggregation on a stream-by-stream basis. (use PE registers to control the operation) • TRANS_MODE (2) = Transmit Mode - Protocol Layyer (PE) data is transmitted. RT does not aggregate any RM data into the TM path. • CPRI_ULNK_MODE (3) = CPRI Uplink RE Chaining Mode - (CPRI Only), AxC: Aggregation mode where RM data has offset into the egress CPRI link by n basic frames. CW: CPRI control words are delayed such that they are re-transmitted into the next hyperframe (i.e ingress hyperframe0 maps to egress hyperframe1).

8.6.41.2 AIL PHY RT DEPTH STATUS REGISTER [Address = 0x3_0044]

The AIL PHY RT Depth Status Register displays the real time depth of the Link Buffer in the RT Block

Figure 8-612. AIL PHY RT DEPTH STATUS REGISTER

31	9	8	0
Reserved		VALUE	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-707. AIL PHY RT DEPTH STATUS REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	Reserved
8-0	VALUE	The RT Depth status displays the operating depth of the RT link buffer

8.6.41.3 AIL PHY RT HEADER ERROR STATUS REGISTER [Address = 0x3_0048]

The AIL PHY RT Header Error Status Register displays the status of the last header error determined during aggregation operations while the RT block is in OBSAI Mode

Figure 8-613. AIL PHY RT HEADER ERROR STATUS REGISTER

31	6	5	0
Reserved		CHAN	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-708. AIL PHY RT HEADER ERROR STATUS REGISTER Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved
5-0	CHAN	The RT Header Error status indicates the DMA channel number of the message that the header error occurred

8.6.42 AIL_phy_ci_lut [Address = 0x3_0080]

Table 8-709. AIL_phy_ci_lut

Offset	Acronym	Register Description	Section
0x3_0080	AIL PHY CI LUT SELECT CONFIGURATION REGISTER	The AIL PHY CI LUT Select Register selects between the LUT A table and the LUT B table for CI CPRI Conversion control. Used for dynamic modification of CI effectively giving the user a Ping Pong buffer. Select takes effect on next PHY frame boundary.	Section 8.6.42.1

8.6.42.1 AIL PHY CI LUT SELECT CONFIGURATION REGISTER [Address = 0x3_0080]

The AIL PHY CI LUT Select Register selects between the LUT A table and the LUT B table for CI CPRI Conversion control. Used for dynamic modification of CI effectively giving the user a Ping Pong buffer. Select takes effect on next PHY frame boundary.

Figure 8-614. AIL PHY CI LUT SELECT CONFIGURATION REGISTER

31	1	0
Reserved		SEL
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-710. AIL PHY CI LUT SELECT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	Reserved
0	SEL	0 Selects Table A, 1 Selects Table B

8.6.43 AIL_phy_co_lut [Address = 0x3_00C0]

Table 8-711. AIL_phy_co_lut

Offset	Acronym	Register Description	Section
0x3_00C0	AIL PHY CO LUT SELECT CONFIGURATION REGISTER	The AIL PHY CO LUT Select Register selects between the LUT A table and the LUT B table for CO CPRI Conversion control Used for dynamic modification of CO effectively giving the user a Ping Pong buffer. Select takes effect on next PHY frame boundary.	Section 8.6.43.1

8.6.43.1 AIL PHY CO LUT SELECT CONFIGURATION REGISTER [Address = 0x3_00C0]

The AIL PHY CO LUT Select Register selects between the LUT A table and the LUT B table for CO CPRI Conversion control Used for dynamic modification of CO effectively giving the user a Ping Pong buffer. Select takes effect on next PHY frame boundary.

Figure 8-615. AIL PHY CO LUT SELECT CONFIGURATION REGISTER

31	1	0
Reserved		SEL
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-712. AIL PHY CO LUT SELECT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	Reserved
0	SEL	0 Selects Table A, 1 Selects Table B

8.6.44 AIL_phy_ci_lut_a [Address = 0x3_0100 + (*R* × 0x0004)]

Table 8-713. AIL_phy_ci_lut_a

Offset	Acronym	Register Description	Section
0x3_0100 + (*R* × 0x0004)	AIL PHY CI LUT A CONFIGURATION REGISTER	The AIL PHY CI Look-up Table A Registers control up to eight groups of AxC containers for every given CPRI basic frame.	Section 8.6.44.1

8.6.44.1 AIL PHY CI LUT A CONFIGURATION REGISTER [Address = 0x3_0100 + (*R* × 0x0004)]

Range (*R*) = 0:7

The AIL PHY CI Look-up Table A Registers control up to eight groups of AxC containers for every given CPRI basic frame.

Figure 8-616. AIL PHY CI LUT A CONFIGURATION REGISTER

31 14	13	12 11	10 6	5 0
Reserved	SMPL_LAST	SMPL_TYPE	SMPL_OFFSET	SMPL_COUNT
NA-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-714. AIL PHY CI LUT A CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-14	Reserved	Reserved
13	SMPL_LAST	Indicates this is the last AXC Contgainer Group to be used when set. All group entries after this one are ignored.
12-11	SMPL_TYPE	Defines the sample type for AxC Container Group • 7Bit (0) = 7 Bit Samples • 8Bit (1) = 8 Bit Samples • 15Bit (2) = 15 Bit Samples • 16Bit (3) = 16 Bit Samples
10-6	SMPL_OFFSET	Defines the number of unused bits (gap) preceeding this container group. This value must be an even number from 0x0 to 0x1e
5-0	SMPL_COUNT	Defines the number of consecutive AxC Containers in the AxC Container Group. if SMPL_LAST bit is set for the group, this count should include all remaining containers in basic frame. Set N-1

8.6.45 AIL_phy_ci_lut_b [Address = 0x3_0140 + (R × 0x0004)]

Table 8-715. AIL_phy_ci_lut_b

Offset	Acronym	Register Description	Section
0x3_0140 + (*R* × 0x0004)	AIL PHY CI LUT B CONFIGURATION REGISTER	The AIL PHY CI Look-up Table B Registers control up to eight groups of AxC containers for every given CPRI basic frame.	Section 8.6.45.1

8.6.45.1 AIL PHY CI LUT B CONFIGURATION REGISTER [Address = 0x3_0140 + (R × 0x0004)]

Range (*R*) = 0:7

The AIL PHY CI Look-up Table B Registers control up to eight groups of AxC containers for every given CPRI basic frame.

Figure 8-617. AIL PHY CI LUT B CONFIGURATION REGISTER

31 14	13	12 11	10 6	5 0
Reserved	SMPL_LAST	SMPL_TYPE	SMPL_OFFSET	SMPL_COUNT
NA-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-716. AIL PHY CI LUT B CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-14	Reserved	Reserved
13	SMPL_LAST	Indicates this is the last AXC Contgainer Group to be used when set. All group entries after this one are ignored.
12-11	SMPL_TYPE	Defines the sample type for AxC Container Group • 7Bit (0) = 7 Bit Samples • 8Bit (1) = 8 Bit Samples • 15Bit (2) = 15 Bit Samples • 16Bit (3) = 16 Bit Samples
10-6	SMPL_OFFSET	Defines the number of unused bits (gap) preceeding this container group. This value must be an even number from 0x0 to 0x1e
5-0	SMPL_COUNT	Defines the number of consecutive AxC Containers in the AxC Container Group. if SMPL_LAST bit is set for the group, this count should include all remaining containers in basic frame. Set N-1

8.6.46 AIL_phy_co_lut_a [Address = 0x3_0180 + (R × 0x0004)]

Table 8-717. AIL_phy_co_lut_a

Offset	Acronym	Register Description	Section
0x3_0180 + (*R* × 0x0004)	AIL PHY CO LUT A CONFIGURATION REGISTER	The AIL PHY CO Look-up Table A Registers control up to eight groups of AxC containers for every given CPRI basic frame.	Section 8.6.46.1

8.6.46.1 AIL PHY CO LUT A CONFIGURATION REGISTER [Address = 0x3_0180 + (R × 0x0004)]

Range (*R*) = 0:7

The AIL PHY CO Look-up Table A Registers control up to eight groups of AxC containers for every given CPRI basic frame.

Figure 8-618. AIL PHY CO LUT A CONFIGURATION REGISTER

31 14	13	12 11	10 6	5 0
Reserved	SMPL_LAST	SMPL_TYPE	SMPL_OFFSET	SMPL_COUNT
NA-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-718. AIL PHY CO LUT A CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-14	Reserved	Reserved
13	SMPL_LAST	Indicates this is the last AXC Contgainer Group to be used when set. All group entries after this one are ignored.
12-11	SMPL_TYPE	Defines the sample type for AxC Container Group • 7Bit (0) = 7 Bit Samples • 8Bit (1) = 8 Bit Samples • 15Bit (2) = 15 Bit Samples • 16Bit (3) = 16 Bit Samples
10-6	SMPL_OFFSET	Defines the number of unused bits (gap) preceeding this container group. This value must be an even number from 0x0 to 0x1e
5-0	SMPL_COUNT	Defines the number of consecutive AxC Containers in the AxC Container Group. if SMPL_LAST bit is set for the group, this count should include all remaining containers in basic frame. Set N-1

8.6.47 AIL_phy_co_lut_b [Address = 0x3_01C0 + (R × 0x0004)]

Table 8-719. AIL_phy_co_lut_b

Offset	Acronym	Register Description	Section
0x3_01C0 + (*R* × 0x0004)	AIL PHY CO LUT B CONFIGURATION REGISTER	The AIL PHY CO Look-up Table B Registers control up to eight groups of AxC containers for every given CPRI basic frame.	Section 8.6.47.1

8.6.47.1 AIL PHY CO LUT B CONFIGURATION REGISTER [Address = 0x3_01C0 + (R × 0x0004)]

Range (*R*) = 0:7

The AIL PHY CO Look-up Table B Registers control up to eight groups of AxC containers for every given CPRI basic frame.

Figure 8-619. AIL PHY CO LUT B CONFIGURATION REGISTER

31 14	13	12 11	10 6	5 0
Reserved	SMPL_LAST	SMPL_TYPE	SMPL_OFFSET	SMPL_COUNT
NA-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-720. AIL PHY CO LUT B CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-14	Reserved	Reserved
13	SMPL_LAST	Indicates this is the last AXC Contgainer Group to be used when set. All group entries after this one are ignored.
12-11	SMPL_TYPE	Defines the sample type for AxC Container Group • 7Bit (0) = 7 Bit Samples • 8Bit (1) = 8 Bit Samples • 15Bit (2) = 15 Bit Samples • 16Bit (3) = 16 Bit Samples
10-6	SMPL_OFFSET	Defines the number of unused bits (gap) preceeding this container group. This value must be an even number from 0x0 to 0x1e
5-0	SMPL_COUNT	Defines the number of consecutive AxC Containers in the AxC Container Group. if SMPL_LAST bit is set for the group, this count should include all remaining containers in basic frame. Set N-1

8.6.48 AIL_phy_tm [Address = 0x3_0200]

Table 8-721. AIL_phy_tm

Offset	Acronym	Register Description	Section
0x3_0200	AIL PHY TM CONFIGURATION REGISTER	The TM Configuration Register is used to program basic functionality of the Tx Mac Block. Bit 0 can be updated at any time to turn on or off the link	Section 8.6.48.1
0x3_0204	AIL PHY TM STATE MACHINE CONTROL REGISTER	TM State Machine Control Register	Section 8.6.48.2
0x3_0208	AIL PHY TM SCRAMBLER CONFIGURATION REGISTER	The Scrambler Configuration Register contains the seed initialization vector for the LFSR scrambler utilized when scrambling is enabled in OBSAI 8x mode or CPRI 8x,10x,16x mode (for CPRI, it is optional), and the scrambler enable bit is set. This configuration register should only be updated when the Frame Sync state machine is disabled.	Section 8.6.48.3
0x3_020C	AIL PHY TM L1 INBAND CONFIGURATION REGISTER	(CPRI Only) SW supplied L1 inband alarm signals for for insertion into Egres CPRI link.	Section 8.6.48.4
0x3_0210	AIL PHY TM L1 INBAND ENABLE REGISTER	(CPRI Only)The L1 Inband Enable Register allows hardware control of the L1 inband alarm signals. A 1 for each bit indicates the hardware control is enabled. Each enable bit is a gate on an input condition that could affect an output condition. The nomenclature is defined as TXSIGNAL_RXCOND_EN. The term ERR indicates the error had been determined by the RM, while the term RX refers to the actual L1 inband signal received by the RM.	Section 8.6.48.5
0x3_0214	AIL PHY TM LOS ERROR REGISTER	Selects which RM link is used to drive the LOSERR condition to determine transmit L1 Inband signaling	Section 8.6.48.6
0x3_0218	AIL PHY TM LOF ERROR REGISTER	Selects which RM link is used to drive the LORERR condition to determine transmit L1 Inband signaling	Section 8.6.48.7
0x3_021C	AIL PHY TM LOS RX REGISTER	Selects which RM link is used to drive the LOSRx condition to determine transmit L1 Inband signaling	Section 8.6.48.8
0x3_0220	AIL PHY TM LOF RX REGISTER	Selects which RM link is used to drive the LOFRx condition to determine transmit L1 Inband signaling	Section 8.6.48.9
0x3_0224	AIL PHY TM RAI RX REGISTER	Selects which RM link is used to drive the RAIRx condition to determine transmit L1 Inband signaling	Section 8.6.48.10
0x3_0228	AIL PHY TM RST RX REGISTER	Selects which RM link is used to drive the RSTRx condition to determine transmit L1 Inband signaling	Section 8.6.48.11
0x3_022C	AIL PHY TM CPRI HFN STATUS REGISTER	TM CPRI HFN Status	Section 8.6.48.12
0x3_0230	AIL PHY TM CPRI POINTER P CONFIGURATION REGISTER		Section 8.6.48.13
0x3_0234	AIL PHY TM CPRI STARTUP CONFIGURTAION REGISTER	Contains Startup value	Section 8.6.48.14
0x3_0238	AIL PHY TM CPRI VERSION CONFIGURATION REGISTER	Contains Protocol Version value	Section 8.6.48.15
0x3_023C	AIL PHY TM STATUS REGISTER	The TM Status Register contains status of the TM block	Section 8.6.48.16
0x3_0240	AIL PHY TM CPRI PORT ID REGISTER A	TM CPRI PORT ID bits 31 to 0 which are inserted into the CPRI Egress Link at specific CPRI CW	Section 8.6.48.17
0x3_0244	AIL PHY TM CPRI PORT ID REGISTER B	TM CPRI PORT ID bits 63 to 32 which are inserted into the CPRI Egress Link at specific CPRI CW	Section 8.6.48.18

Table 8-721. AIL_phy_tm (continued)

Offset	Acronym	Register Description	Section
0x3_0248	AIL PHY TM CPRI SCRAMBLER CONFIGURATION REGISTER	(CPRI only) The Scrambler Configuration Register contains the seed initialization vector for the CPRI LFSR scrambler utilized in CPRI 8x,10x,16x mode. This configuration register should only be updated when the TM Frame Sync state machine is disabled.	Section 8.6.48.19

8.6.48.1 AIL PHY TM CONFIGURATION REGISTER [Address = 0x3_0200]

The TM Configuration Register is used to program basic functionality of the Tx Mac Block. Bit 0 can be updated at any time to turn on or off the link

Figure 8-620. AIL PHY TM CONFIGURATION REGISTER

31	1	0
Reserved		EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-722. AIL PHY TM CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	Reserved
0	EN	The Transmit Enable Bit allows the TM block transmit state machine to operate • DISABLE (0) = TM Block Disabled • ENABLE (1) = TM Block Enabled

8.6.48.2 AIL PHY TM STATE MACHINE CONTROL REGISTER [Address = 0x3_0204]

TM State Machine Control Register

Figure 8-621. AIL PHY TM STATE MACHINE CONTROL REGISTER

31	4	3	2	1	0
Reserved		LOS_EN	RESYNC	IDLE	FLUSH
NA-0		R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-723. AIL PHY TM STATE MACHINE CONTROL REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved
3	LOS_EN	When set, Loss of Signal from the RM to cause the TM state machine to transition to the OFF state. • DISABLE (0) = Loss of Signal Disabled • ENABLE (1) = Loss of Signal Enabled
2	RESYNC	Forces the Frame Sync state machine to transition from the FRAME_SYNC state to the RESYNC state and remain in the RESYNC state until the bit is cleared. If the state machine is in either the OFF state or the IDLE state, this bit is ignored until the state machine reaches the RESYNC state • No_Action (0) = No Action • RESYNC (1) = Forces the Frame Sync state machine to transition from the FRAME_SYNC state to the RESYNC state and remain in the RESYNC state until the bit is cleared
1	IDLE	Forces the Frame Sync state machine to transition from either the FRAME_SYNC or RESYNC states to the IDLE state and remain in the IDLE state until the bit is cleared. If the state machine is in the OFF state, this bit is ignored until the state machine reaches the IDLE state • No_Action (0) = No Action • Idle (1) = Force to Idle state and remain until cleared
0	FLUSH	Instructs the TM link to flush the FIFO and force a TM Fail condition on the link. When set high, the State machine is forced into the RE_SYNC state • No_Action (0) = No Action • FLUSH_FIFO (1) = Flush FIFO and force TM Fail condition

8.6.48.3 AIL PHY TM SCRAMBLER CONFIGURATION REGISTER [Address = 0x3_0208]

The Scrambler Configuration Register contains the seed initialization vector for the LFSR scrambler utilized when scrambling is enabled in OBSAI 8x mode or CPRI 8x,10x,16x mode (for CPRI, it is optional), and the scrambler enable bit is set. This configuration register should only be updated when the Frame Sync state machine is disabled.

Figure 8-622. AIL PHY TM SCRAMBLER CONFIGURATION REGISTER

31	8	7	6	0
Reserved		SCR_EN	SEED_VALUE	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-724. AIL PHY TM SCRAMBLER CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	SCR_EN	(OBSAI only) Enables the scrambler for operation in the transmit data path. • DISABLE (0) = Scrambler Disabled • ENABLE (1) = Scrambler Enabled
6-0	SEED_VALUE	(OBSAI only) The seed value is used to initialize the transmit scrambler circuit

8.6.48.4 AIL PHY TM L1 INBAND CONFIGURATION REGISTER [Address = 0x3_020C]

(CPRI Only) SW supplied L1 inband alarm signals for for insertion into Egres CPRI link.

Figure 8-623. AIL PHY TM L1 INBAND CONFIGURATION REGISTER

31	5	4	3
Reserved		L1_INBAND_LOF	L1_INBAND_LOS
NA-0		R/W-0	R/W-0

2	1	0
L1_INBAND_SDI	L1_INBAND_RAI	L1_INBAND_RST
R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-725. AIL PHY TM L1 INBAND CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved
4	L1_INBAND_LOF	LOF (see CPRI spec for usage)
3	L1_INBAND_LOS	LOS (see CPRI spec for usage)
2	L1_INBAND_SDI	SDI (see CPRI spec for usage)
1	L1_INBAND_RAI	RAI (see CPRI spec for usage)
0	L1_INBAND_RST	RST (see CPRI spec for usage)

8.6.48.5 AIL PHY TM L1 INBAND ENABLE REGISTER [Address = 0x3_0210]

(CPRI Only)The L1 Inband Enable Register allows hardware control of the L1 inband alarm signals. A 1 for each bit indicates the hardware control is enabled. Each enable bit is a gate on an input condition that could affect an output condition. The nomenclature is defined as TXSIGNAL_RXCOND_EN. The term ERR indicates the error had been determined by the RM, while the term RX refers to the actual L1 inband signal received by the RM.

Figure 8-624. AIL PHY TM L1 INBAND ENABLE REGISTER

31 10	9	8	7	6
Reserved	SDI_RSTRX_EN	LOS_LOSERR_EN	LOS_LOSRX_EN	LOF_LOFERR_EN
NA-0	R/W-0	R/W-0	R/W-0	R/W-0

5	4	3	2	1	0
LOF_LOFRX_EN	RAI_LOSERR_EN	RAI_LOSRX_EN	RAI_LOFERR_EN	RAI_LOFRX_EN	RAI_RAIRX_EN
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-726. AIL PHY TM L1 INBAND ENABLE REGISTER Field Descriptions

Bits	Name	Description
31-10	Reserved	Reserved
9	SDI_RSTRX_EN	Enables l1_inband SDI active upon rstrx signal from RM
8	LOS_LOSERR_EN	Enables l1_inband LOS active upon loserr signal from RM
7	LOS_LOSRX_EN	Enables l1_inband LOS active upon losrx signal from RM
6	LOF_LOFERR_EN	Enables l1_inband LOF active upon loferr signal from RM
5	LOF_LOFRX_EN	Enables l1_inband LOF active upon lofrx signal from RM
4	RAI_LOSERR_EN	Enables l1_inband RAI active upon loserr signal from RM
3	RAI_LOSRX_EN	Enables l1_inband RAI active upon losrx signal from RM
2	RAI_LOFERR_EN	Enables l1_inband RAI active upon loferr signal from RM
1	RAI_LOFRX_EN	Enables l1_inband RAI active upon lofrx signal from RM
0	RAI_RAIRX_EN	Enables l1_inband RAI active upon rairx signal from RM

8.6.48.6 AIL PHY TM LOS ERROR REGISTER [Address = 0x3_0214]

Selects which RM link is used to drive the LOSERR condition to determine transmit L1 Inband signaling

Figure 8-625. AIL PHY TM LOS ERROR REGISTER

31	3	2	0
Reserved		LINK_LOSERR	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-727. AIL PHY TM LOS ERROR REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	LINK_LOSERR	RM Link LOSERR Select • LOSERR0 (0) = RM Link LOSERR 0 • LOSERR1 (1) = RM Link LOSERR 1 • LOSERR2 (2) = RM Link LOSERR 2 • LOSERR3 (3) = RM Link LOSERR 3 • LOSERR4 (4) = RM Link LOSERR 4 • LOSERR5 (5) = RM Link LOSERR 5 • LOSERR6 (6) = RM Link LOSERR 6 • LOSERR7 (7) = RM Link LOSERR 7

8.6.48.7 AIL PHY TM LOF ERROR REGISTER [Address = 0x3_0218]

Selects which RM link is used to drive the LORERR condition to determine transmit L1 Inband signaling

Figure 8-626. AIL PHY TM LOF ERROR REGISTER

31	3	2	0
Reserved		LINK_LOFERR	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-728. AIL PHY TM LOF ERROR REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	LINK_LOFERR	RM Link LOFERR Select • LOFERR0 (0) = RM Link 0 • LOFERR1 (1) = RM Link 1 • LOFERR2 (2) = RM Link 2 • LOFERR3 (3) = RM Link 3 • LOFERR4 (4) = RM Link 4 • LOFERR5 (5) = RM Link 5 • LOFERR6 (6) = RM Link 6 • LOFERR7 (7) = RM Link 7

8.6.48.8 AIL PHY TM LOS RX REGISTER [Address = 0x3_021C]

Selects which RM link is used to drive the LOSRx condition to determine transmit L1 Inband signaling

Figure 8-627. AIL PHY TM LOS RX REGISTER

31	3	2	0
Reserved		LINK_LOSRX	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-729. AIL PHY TM LOS RX REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	LINK_LOSRX	RM Link LOSRx Select • LOSRx0 (0) = RM Link LOSRx 0 • LOSRx1 (1) = RM Link LOSRx 1 • LOSRx2 (2) = RM Link LOSRx 2 • LOSRx3 (3) = RM Link LOSRx 3 • LOSRx4 (4) = RM Link LOSRx 4 • LOSRx5 (5) = RM Link LOSRx 5 • LOSRx6 (6) = RM Link LOSRx 6 • LOSRx7 (7) = RM Link LOSRx 7

8.6.48.9 AIL PHY TM LOF RX REGISTER [Address = 0x3_0220]

Selects which RM link is used to drive the LOFRx condition to determine transmit L1 Inband signaling

Figure 8-628. AIL PHY TM LOF RX REGISTER

31	3	2	0
Reserved		LINK_LOFRX	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-730. AIL PHY TM LOF RX REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	LINK_LOFRX	RM Link LOFRx Select • LOFRx0 (0) = RM Link LOFRx 0 • LOFRx1 (1) = RM Link LOFRx 1 • LOFRx2 (2) = RM Link LOFRx 2 • LOFRx3 (3) = RM Link LOFRx 3 • LOFRx4 (4) = RM Link LOFRx 4 • LOFRx5 (5) = RM Link LOFRx 5 • LOFRx6 (6) = RM Link LOFRx 6 • LOFRx7 (7) = RM Link LOFRx 7

8.6.48.10 AIL PHY TM RAI RX REGISTER [Address = 0x3_0224]

Selects which RM link is used to drive the RAIRx condition to determine transmit L1 Inband signaling

Figure 8-629. AIL PHY TM RAI RX REGISTER

31	3	2	0
Reserved		LINK_RAIRX	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-731. AIL PHY TM RAI RX REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	LINK_RAIRX	RM Link RAIRx Select • RAIRx0 (0) = RM Link RAIRx 0 • RAIRx1 (1) = RM Link RAIRx 1 • RAIRx2 (2) = RM Link RAIRx 2 • RAIRx3 (3) = RM Link RAIRx 3 • RAIRx4 (4) = RM Link RAIRx 4 • RAIRx5 (5) = RM Link RAIRx 5 • RAIRx6 (6) = RM Link RAIRx 6 • RAIRx7 (7) = RM Link RAIRx 7

8.6.48.11 AIL PHY TM RST RX REGISTER [Address = 0x3_0228]

Selects which RM link is used to drive the RSTRx condition to determine transmit L1 Inband signaling

Figure 8-630. AIL PHY TM RST RX REGISTER

31	3	2	0
Reserved		LINK_RSTRX	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-732. AIL PHY TM RST RX REGISTER Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	LINK_RSTRX	RM Link RSTRx Select • RSTRx0 (0) = RM Link RSTRx 0 • RSTRx1 (1) = RM Link RSTRx 1 • RSTRx2 (2) = RM Link RSTRx 2 • RSTRx3 (3) = RM Link RSTRx 3 • RSTRx4 (4) = RM Link RSTRx 4 • RSTRx5 (5) = RM Link RSTRx 5 • RSTRx6 (6) = RM Link RSTRx 6 • RSTRx7 (7) = RM Link RSTRx 7

8.6.48.12 AIL PHY TM CPRI HFN STATUS REGISTER [Address = 0x3_022C]

TM CPRI HFN Status

Figure 8-631. AIL PHY TM CPRI HFN STATUS REGISTER

31	8	7	0
Reserved		HFN	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-733. AIL PHY TM CPRI HFN STATUS REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7-0	HFN	Synchronization field. The Hyperframe number of the currently transmitting frame

8.6.48.13 AIL PHY TM CPRI POINTER P CONFIGURATION REGISTER [Address = 0x3_0230]

Figure 8-632. AIL PHY TM CPRI POINTER P CONFIGURATION REGISTER

31	8	7	0
Reserved		PTR_P	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-734. AIL PHY TM CPRI POINTER P CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7-0	PTR_P	L1 inband field. Pointer P value which is inserted into the CPRI Egress link.

8.6.48.14 AIL PHY TM CPRI STARTUP CONFIGURTAION REGISTER [Address = 0x3_0234]

Contains Startup value

Figure 8-633. AIL PHY TM CPRI STARTUP CONFIGURTAION REGISTER

31	8	7	0
Reserved		STARTUP	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-735. AIL PHY TM CPRI STARTUP CONFIGURTAION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7-0	STARTUP	L1 inband field. Startup value which is inserted into the CPRI Egress link.

8.6.48.15 AIL PHY TM CPRI VERSION CONFIGURATION REGISTER [Address = 0x3_0238]

Contains Protocol Version value

Figure 8-634. AIL PHY TM CPRI VERSION CONFIGURATION REGISTER

31	8	7	0
Reserved		PROT_VERS	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-736. AIL PHY TM CPRI VERSION CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7-0	PROT_VERS	L1 inband field. Protocol version value which is inserted into the CPRI Egress link.

8.6.48.16 AIL PHY TM STATUS REGISTER [Address = 0x3_023C]

The TM Status Register contains status of the TM block

Figure 8-635. AIL PHY TM STATUS REGISTER

31	9	8	5	4	0
Reserved		FRM_STATE		Reserved	
NA-0		R-0x0001		NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-737. AIL PHY TM STATUS REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	Reserved
8-5	FRM_STATE	Indicates that status of the Frame Sync state machine • OFF (1) = FSM in OFF state • IDLE (2) = FSM in IDLE state • RE_SYNC (4) = FSM in RE_SYNC state • FRAME_SYNC (8) = FSM in FRAME_SYNC state
4-0	Reserved	Reserved

8.6.48.17 AIL PHY TM CPRI PORT ID REGISTER A [Address = 0x3_0240]

TM CPRI PORT ID bits 31 to 0 which are inserted into the CPRI Egress Link at specific CPRI CW

Figure 8-636. AIL PHY TM CPRI PORT ID REGISTER A

31 24	23 16	15 8	7 0
Z116_1	Z116_0	Z52_1	Z52_0
R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-738. AIL PHY TM CPRI PORT ID REGISTER A Field Descriptions

Bits	Name	Description
31-24	Z116_1	Contains the Z.116.1 byte transmitted CPRI Port ID value
23-16	Z116_0	Contains the Z.116.0 byte transmitted CPRI Port ID value
15-8	Z52_1	Contains the Z.52.1 byte transmitted CPRI Port ID value
7-0	Z52_0	Contains the Z.52.0 byte transmitted CPRI Port ID value

8.6.48.18 AIL PHY TM CPRI PORT ID REGISTER B [Address = 0x3_0244]

TM CPRI PORT ID bits 63 to 32 which are inserted into the CPRI Egress Link at specific CPRI CW

Figure 8-637. AIL PHY TM CPRI PORT ID REGISTER B

31 24	23 16	15 8	7 0
Z244_1	Z244_0	Z180_1	Z180_0
R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-739. AIL PHY TM CPRI PORT ID REGISTER B Field Descriptions

Bits	Name	Description
31-24	Z244_1	Contains the Z.244.1 byte transmitted CPRI Port ID value
23-16	Z244_0	Contains the Z.244.0 byte transmitted CPRI Port ID value
15-8	Z180_1	Contains the Z.180.1 byte transmitted CPRI Port ID value
7-0	Z180_0	Contains the Z.180.0 byte transmitted CPRI Port ID value

8.6.48.19 AIL PHY TM CPRI SCRAMBLER CONFIGURATION REGISTER [Address = 0x3_0248]

(CPRI only) The Scrambler Configuration Register contains the seed initialization vector for the CPRI LFSR scrambler utilized in CPRI 8x,10x,16x mode. This configuration register should only be updated when the TM Frame Sync state machine is disabled.

Figure 8-638. AIL PHY TM CPRI SCRAMBLER CONFIGURATION REGISTER

31	30	0
Reserved	SEED_VALUE	
NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-740. AIL PHY TM CPRI SCRAMBLER CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31	Reserved	Reserved
30-0	SEED_VALUE	The seed value is used to initialize the transmit scrambler circuit. setting zero will turn off CPRI scramber

8.6.49 AIL_phy_rm [Address = 0x3_0280]

Table 8-741. AIL_phy_rm

Offset	Acronym	Register Description	Section
0x3_0280	AIL PHY RM CONFIGURATION REGISTER	RM Configuration Register	Section 8.6.49.1
0x3_0284	AIL PHY RM DATA PATH CONFIGURATION REGISTER	Controls the RM Data Path Configuration	Section 8.6.49.2
0x3_0288	AIL PHY RM LCV CONTROL REGISTER	Controls the counting of LCV Errors in the RM	Section 8.6.49.3
0x3_028C	AIL PHY RM FSM SYNC COUNT CONFIGURATION REGISTER	RM FSM Sync Count Configuration Register	Section 8.6.49.4
0x3_0290	AIL PHY RM FSM UNSYNC COUNT CONFIGURATION REGISTER	RM FSM Unsync Count Configuration Register	Section 8.6.49.5
0x3_0294	AIL PHY RM DESCRAMBLING CONTROL REGISTER	Controls the descrambling operation of the RM	Section 8.6.49.6
0x3_0298	AIL PHY RM CLOCK DETECTION CONFIGURATION REGISTER	RM Clock Detection Configuration	Section 8.6.49.7
0x3_029C	AIL PHY RM CPRI HYPERFRAME STATUS REGISTER	Contains the last received CPRI HFN value	Section 8.6.49.8
0x3_02A0	AIL PHY RM CPRI BFN STATUS REGISTER	Contains the last received CPRI BFN value	Section 8.6.49.9
0x3_02A4	AIL PHY RM CPRI STATE STATUS REGISTER	Defines the RM CPRI State Status	Section 8.6.49.10
0x3_02A8	AIL PHY RM CPRI VERSION STATUS REGISTER	Contains the last received CPRI Version Value	Section 8.6.49.11
0x3_02AC	AIL PHY RM CPRI STARTUP STATUS REGISTER	Contains the last received CPRI Startup Value	Section 8.6.49.12
0x3_02B0	AIL PHY RM CPRI L1 INBAND STATUS REGISTER	Contains the last received CPRI L1 Inband Signals	Section 8.6.49.13
0x3_02B4	AIL PHY RM CPRI POINTER P STATUS REGISTER	Contains the last received CPRI PtrP Value	Section 8.6.49.14
0x3_02B8	AIL PHY RM CPRI DE-SCRAMBLER SEED STATUS REGISTER	RM CPRI De-scrambler Seed	Section 8.6.49.15
0x3_02C0	AIL PHY RM STATUS REGISTER	RM Status Register	Section 8.6.49.16
0x3_02C4	AIL PHY RM LCV LOS COUNT STATUS REGISTER	RM LCV LOS Count	Section 8.6.49.17
0x3_02C8	AIL PHY RM LCV COUNT STATUS REGISTER	RM LCV Count	Section 8.6.49.18
0x3_02CC	AIL PHY RM CLOCK QUALITY STATUS REGISTER	RM Clock Quality	Section 8.6.49.19
0x3_02D0	AIL PHY RM OBSAI DE-SCRAMBLER SEED STATUS REGISTER	RM OBSAI De-scrambler Seed	Section 8.6.49.20
0x3_02D4	AIL PHY RM CPRI PORT ID STATUS REGISTER A	RM CPRI PORT ID Z53 and Z116	Section 8.6.49.21
0x3_02D8	AIL PHY RM CPRI PORT ID STATUS REGISTER B	RM CPRI PORT ID Z180 and Z244	Section 8.6.49.22

8.6.49.1 AIL PHY RM CONFIGURATION REGISTER [Address = 0x3_0280]

RM Configuration Register

Figure 8-639. AIL PHY RM CONFIGURATION REGISTER

31	8	7	6	2	1	0
Reserved		RST_EN	Reserved		DATA_TRC_SEL	RX_EN
NA-0		R/W-0	NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-742. AIL PHY RM CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	RST_EN	Enable CPRI SOC Reset Signal operation. 5 consecutive recieved active L1_Inband_rst will fire a signal to SOC core which can be enabled with an LPSC to perform HW reset of entire SOC • Disable (0) = CPRI SOC Reset Disable • Enable (1) = CPRI SOC Reset Enable
6-2	Reserved	Reserved
1	DATA_TRC_SEL	Data Trace Select. Selects between the raw data after 8b/10b decoding and framed data after the frame sync state machine and de-scrambling. for Data Trace data • Raw_data_sel (0) = Selects raw data after 8b/10b for data trace • Frm_data_sel (1) = Selects framed data after de-scrambling for data trace, data is not available unless the Rx fsm in in Frame Sync
0	RX_EN	Enable RM Link FSM to activate on next recieved PHY frame boundary • Disable (0) = RM link disable • Enable (1) = RM link enable

8.6.49.2 AIL PHY RM DATA PATH CONFIGURATION REGISTER [Address = 0x3_0284]

Controls the RM Data Path Configuration

Figure 8-640. AIL PHY RM DATA PATH CONFIGURATION REGISTER

31 8	7	6	5	4 2	1 0
Reserved	LCV_UNSYNC_EN	SD_AUTO_ALIGN_EN	ERROR_SUPPRESS	FORCE_RX_STATE	Reserved
NA-0	R/W-0	R/W-0	R/W-0	R/W-0	NA-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-743. AIL PHY RM DATA PATH CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	LCV_UNSYNC_EN	Enables a state transition from the ST3 to the ST0 state when lcv_det_thold is met • No_effect (0) = lcv_det_thold has no effect on the RX FSM • Enable_transition (1) = The RX FSM transitions from ST3 to ST0 when lcv_det_thold is met
6	SD_AUTO_ALIGN_EN	Enables the RM to automatically disable Serdes symbol alignment when the receiver state machine reaches state ST3. normally set to Disable and this can be directly controlled by SerDes • Disable (0) = Disable auto alignment • Enable (1) = Enable auto alignment
5	ERROR_SUPPRESS	Suppress error reporting when the receiver state machine is not in state ST3 • Allow (0) = Allow all RM error reporting when not in ST3 • Suppress (1) = Suppress all RM error reporting when not in ST3
4-2	FORCE_RX_STATE	Force RM receiver state machine state • ST4 (2) = Force ST4 state • ST5 (3) = Force ST5 state • ST0 (4) = Force ST0 state • ST1 (5) = Force ST1 state • ST2 (6) = Force ST2 state • ST3 (7) = Force ST3 state • OFF (0) = Force state OFF
1-0	Reserved	Reserved

8.6.49.3 AIL PHY RM LCV CONTROL REGISTER [Address = 0x3_0288]

Controls the counting of LCV Errors in the RM

Figure 8-641. AIL PHY RM LCV CONTROL REGISTER

31	16	15	1	0
LOS_DET_THOLD		Reserved		EN
R/W-0		NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-744. AIL PHY RM LCV CONTROL REGISTER Field Descriptions

Bits	Name	Description
31-16	LOS_DET_THOLD	Sets 8b10b los detect threshold values in number of Line Code Violations received during a master frame, OBSAI, or during a Hyperframe, CPRI. Writing to this location will automatically clear the num_los counter and num_los_det status bit. Range 0 to 65,535
15-1	Reserved	RESERVED
0	EN	Writing a 1 to the bit will enable the Line Code Violation counter. This 16 bit counter will saturate when it reaches a value of 0xffff. Writing a 0 to this bit will clear and disable the counter. The current counter value is available as status, lcv_cntr_value • Disabled_Cleared (0) = lcv_cntr disabled adn cleared to a value of 0x0000. • Enabled (1) = lcv_cntr enabled, counts each LCV to a max of 0xffff

8.6.49.4 AIL PHY RM FSM SYNC COUNT CONFIGURATION REGISTER [Address = 0x3_028C]

RM FSM Sync Count Configuration Register

Figure 8-642. AIL PHY RM FSM SYNC COUNT CONFIGURATION REGISTER

31	16	15	0
FRAME_SYNC_T		SYNC_T	
R/W-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-745. AIL PHY RM FSM SYNC COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-16	FRAME_SYNC_T	Threshold value for consecutive valid message groups which result in state ST3. Range 0 to 65,535
15-0	SYNC_T	Threshold value for consecutive valid blocks of bytes which result in state ST1. Range 0 to 65,535

8.6.49.5 AIL PHY RM FSM UNSYNC COUNT CONFIGURATION REGISTER [Address = 0x3_0290]

RM FSM Unsync Count Configuration Register

Figure 8-643. AIL PHY RM FSM UNSYNC COUNT CONFIGURATION REGISTER

31	16	15	0
FRAME_UNSYNC_T		UNSYNC_T	
R/W-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-746. AIL PHY RM FSM UNSYNC COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-16	FRAME_UNSYNC_T	Threshold value for consecutive invalid message groups which result in state ST1. Range 0 to 65,535
15-0	UNSYNC_T	Threshold value for consecutive invalid blocks of bytes which result in state ST0. Range 0 to 65,535

8.6.49.6 AIL PHY RM DESCRAMBLING CONTROL REGISTER [Address = 0x3_0294]

Controls the descrambling operation of the RM

Figure 8-644. AIL PHY RM DESCRAMBLING CONTROL REGISTER

31	8	7	6	0
Reserved		SCR_EN	Reserved	
NA-0		R/W-0	NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-747. AIL PHY RM DESCRAMBLING CONTROL REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	SCR_EN	Enables the scrambler for operation in the receiver data path • Disable (0) = RM scrambler Disabled • Enable (1) = RM scrambler Enabled
6-0	Reserved	Reserved

8.6.49.7 AIL PHY RM CLOCK DETECTION CONFIGURATION REGISTER [Address = 0x3_0298]

RM Clock Detection Configuration

Figure 8-645. AIL PHY RM CLOCK DETECTION CONFIGURATION REGISTER

31 16	15 8	7 2	1	0
MON_WRAP	WD_WRAP	Reserved	CQ_EN	WD_EN
R/W-0	R/W-0	NA-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-748. AIL PHY RM CLOCK DETECTION CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-16	MON_WRAP	Defines the wrap value of the clock monitor used to define clock quality. A value of zero disables the clock monitor, Range 0 to 65,535
15-8	WD_WRAP	Defines the wrap value of the clock detection watchdog circuit. A value of zero disables the clock watchdog timer, Range 0 to 255
7-2	Reserved	RESERVED
1	CQ_EN	Enables the clock quality circuit. • Disabled_Cleared (0) = Clock qulity circuit Disabled. • Enabled (1) = Clock qulity circuit Enabled.
0	WD_EN	Enables the clock detect watch dog timer. • Disabled_Cleared (0) = Clock detect watch dog timer Disabled. • Enabled (1) = Clock detect watch dog timer Enabled.

8.6.49.8 AIL PHY RM CPRI HYPERFRAME STATUS REGISTER [Address = 0x3_029C]

Contains the last received CPRI HFN value

Figure 8-646. AIL PHY RM CPRI HYPERFRAME STATUS REGISTER

31	8	7	0
Reserved		HFN	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-749. AIL PHY RM CPRI HYPERFRAME STATUS REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7-0	HFN	Received hyperframe number, Z.64.0. Range 0 to 149 basic frames

8.6.49.9 AIL PHY RM CPRI BFN STATUS REGISTER [Address = 0x3_02A0]

Contains the last received CPRI BFN value

Figure 8-647. AIL PHY RM CPRI BFN STATUS REGISTER

31 16	15 8	7 0
Reserved	HIGH	LOW
NA-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-750. AIL PHY RM CPRI BFN STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved
15-8	HIGH	Received Node B Frame number high byte, Z.130.0
7-0	LOW	Received Node B Frame number low byte, Z.128.0

8.6.49.10 AIL PHY RM CPRI STATE STATUS REGISTER [Address = 0x3_02A4]

Defines the RM CPRI State Status

Figure 8-648. AIL PHY RM CPRI STATE STATUS REGISTER

31	2	1	0
Reserved		LOF	HFSYNC
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-751. AIL PHY RM CPRI STATE STATUS REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	RESERVED
1	LOF	Active high status indicates Loss Of Frame when the receiver FSM is in state ST0 or ST1. NOTE.. The value of this bit will be 0 after reset but will change to a value of 1 if CPRI mode is enabled.
0	HFSYNC	Active high status indicates when the receiber FSM is in the HFSYNC state ST3

8.6.49.11 AIL PHY RM CPRI VERSION STATUS REGISTER [Address = 0x3_02A8]

Contains the last received CPRI Version Value

Figure 8-649. AIL PHY RM CPRI VERSION STATUS REGISTER

31	8	7	0
Reserved		VALUE	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-752. AIL PHY RM CPRI VERSION STATUS REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	VALUE	Received protocol version, Z.2.0

8.6.49.12 AIL PHY RM CPRI STARTUP STATUS REGISTER [Address = 0x3_02AC]

Contains the last received CPRI Startup Value

Figure 8-650. AIL PHY RM CPRI STARTUP STATUS REGISTER

31	8	7	0
Reserved		VALUE	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-753. AIL PHY RM CPRI STARTUP STATUS REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	VALUE	Received start up information, Z.66.0

8.6.49.13 AIL PHY RM CPRI L1 INBAND STATUS REGISTER [Address = 0x3_02B0]

Contains the last received CPRI L1 Inband Signals

Figure 8-651. AIL PHY RM CPRI L1 INBAND STATUS REGISTER

31	5	4	3	2	1	0
Reserved		LOF	LOS	SDI	RAI	RST
NA-0		R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-754. AIL PHY RM CPRI L1 INBAND STATUS REGISTER Field Descriptions

Bits	Name	Description
31-5	Reserved	RESERVED
4	LOF	Received sdi, Z.130.0, b4
3	LOS	Received sdi, Z.130.0, b3
2	SDI	Received sdi, Z.130.0, b2
1	RAI	Received rai, Z.130.0, b1
0	RST	Received reset, Z.130.0, b0

8.6.49.14 AIL PHY RM CPRI POINTER P STATUS REGISTER [Address = 0x3_02B4]

Contains the last received CPRI PtrP Value

Figure 8-652. AIL PHY RM CPRI POINTER P STATUS REGISTER

31	8	7	0
Reserved		PNTR_P	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-755. AIL PHY RM CPRI POINTER P STATUS REGISTER Field Descriptions

Bits	Name	Description
31-8	Reserved	RESERVED
7-0	PNTR_P	Received Pointer P

8.6.49.15 AIL PHY RM CPRI DE-SCRAMBLER SEED STATUS REGISTER [Address = 0x3_02B8]

RM CPRI De-scrambler Seed

Figure 8-653. AIL PHY RM CPRI DE-SCRAMBLER SEED STATUS REGISTER

31	30 0
Reserved	VALUE
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-756. AIL PHY RM CPRI DE-SCRAMBLER SEED STATUS REGISTER Field Descriptions

Bits	Name	Description
31	Reserved	RESERVED
30-0	VALUE	Indicates the captured scrambling code, only when configuration bit scr_en = 1 in CPRI mode.

8.6.49.16 AIL PHY RM STATUS REGISTER [Address = 0x3_02C0]

RM Status Register

Figure 8-654. AIL PHY RM STATUS REGISTER

31 16	15 10	9 0
Reserved	RX_SYNC	Reserved
NA-0	R-0x0008	NA-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-757. AIL PHY RM STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-10	RX_SYNC	Indicates the current status of the RX state machine • ST0 (8) = ST0 State UNSYNC • ST1 (4) = ST1 State WAIT_FOR_K28p7_IDLES • ST2 (2) = ST2 State WAIT_FOR_FRAME_SYNC_T • ST3 (1) = ST3 State FRAME_SYNC • ST4 (16) = ST4 State WAIT_FOR_SEED • ST5 (32) = ST5 State WAIT_FOR_ACK
9-0	Reserved	RESERVED

8.6.49.17 AIL PHY RM LCV LOS COUNT STATUS REGISTER [Address = 0x3_02C4]

RM LCV LOS Count

Figure 8-655. AIL PHY RM LCV LOS COUNT STATUS REGISTER

31	16	15	0
Reserved		NUM	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-758. AIL PHY RM LCV LOS COUNT STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	NUM	Represents the number of los_det, 8b10b code violation, occurrences in a mater frame, in OBSAI, or hyperframe, in CPRI. This counter will saturate and hold its value until either cleared by writing the configuration value los_det_thold = 0 or after a master frame, in OBSAI, or hyperframe, in CPRI of no 8b10b errors. Range 0 to 65,535

8.6.49.18 AIL PHY RM LCV COUNT STATUS REGISTER [Address = 0x3_02C8]

RM LCV Count

Figure 8-656. AIL PHY RM LCV COUNT STATUS REGISTER

31	16	15	0
Reserved		VALUE	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-759. AIL PHY RM LCV COUNT STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	VALUE	Number of Line Code Violations counted since last cleared and enabled. Range 0 to 65,535

8.6.49.19 AIL PHY RM CLOCK QUALITY STATUS REGISTER [Address = 0x3_02CC]

RM Clock Quality

Figure 8-657. AIL PHY RM CLOCK QUALITY STATUS REGISTER

31	16	15	0
Reserved		VALUE	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-760. AIL PHY RM CLOCK QUALITY STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	VALUE	The clock quality status register reflects the result of comparing the number of received byte clock edges with that of the known, good quality system clock. The frequency of the received SERDES byte clock can be confirmed. At the wrap of the receiver clock count (mon_wrap field in the AIL_PHY_RM_CLK_DET_CFG register) the system clock count is captured in this register. Range 0 to 65,535

8.6.49.20 AIL PHY RM OBSAI DE-SCRAMBLER SEED STATUS REGISTER [Address = 0x3_02D0]

RM OBSAI De-scrambler Seed

Figure 8-658. AIL PHY RM OBSAI DE-SCRAMBLER SEED STATUS REGISTER

31	7	6	0
Reserved		VALUE	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-761. AIL PHY RM OBSAI DE-SCRAMBLER SEED STATUS REGISTER Field Descriptions

Bits	Name	Description
31-7	Reserved	RESERVED
6-0	VALUE	Indicates the captured scrambling code, only when configuration bit scr_en = 1.

8.6.49.21 AIL PHY RM CPRI PORT ID STATUS REGISTER A [Address = 0x3_02D4]

RM CPRI PORT ID Z53 and Z116

Figure 8-659. AIL PHY RM CPRI PORT ID STATUS REGISTER A

31 24	23 16	15 8	7 0
Z116_1	Z116_0	Z52_1	Z52_0
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-762. AIL PHY RM CPRI PORT ID STATUS REGISTER A Field Descriptions

Bits	Name	Description
31-24	Z116_1	Contains the Z.116.1 byte received CPRI Port ID value
23-16	Z116_0	Contains the Z.116.0 byte received CPRI Port ID value
15-8	Z52_1	Contains the Z.52.1 byte received CPRI Port ID value
7-0	Z52_0	Contains the Z.52.0 byte received CPRI Port ID value

8.6.49.22 AIL PHY RM CPRI PORT ID STATUS REGISTER B [Address = 0x3_02D8]

RM CPRI PORT ID Z180 and Z244

Figure 8-660. AIL PHY RM CPRI PORT ID STATUS REGISTER B

31 24	23 16	15 8	7 0
Z244_1	Z244_0	Z180_1	Z180_0
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-763. AIL PHY RM CPRI PORT ID STATUS REGISTER B Field Descriptions

Bits	Name	Description
31-24	Z244_1	Contains the Z.244.1 byte received CPRI Port ID value
23-16	Z244_0	Contains the Z.244.0 byte received CPRI Port ID value
15-8	Z180_1	Contains the Z.180.1 byte received CPRI Port ID value
7-0	Z180_0	Contains the Z.180.0 byte received CPRI Port ID value

8.6.50 AIL_IQN_AIL_EE_VBUSCLK_EE [Address = 0x3_2000]

Table 8-764. AIL_IQN_AIL_EE_VBUSCLK_EE

Offset	Acronym	Register Description	Section
0x3_2000	AIL EE_SII_E RAW INTERRUPT STATUS	SI si_i IQ info.	Section 8.6.50.1
0x3_2004	AIL EE_SII_E RAW SET	Raw Set	Section 8.6.50.2
0x3_2008	AIL EE_SII_E RAW CLEAR	Raw Clear	Section 8.6.50.3
0x3_200C	AIL EE_SII_E EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.4
0x3_2010	AIL EE_SII_E EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.5
0x3_2014	AIL EE_SII_E EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.6
0x3_2018	AIL EE_SII_E EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.7
0x3_201C	AIL EE_SII_E EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.8
0x3_2020	AIL EE_SII_E EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.9
0x3_2024	AIL EE_SII_E EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.10
0x3_2028	AIL EE_SII_E EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.11
0x3_202C	AIL EE_SII_F RAW INTERRUPT STATUS	SI si_i CTL info.	Section 8.6.50.12
0x3_2030	AIL EE_SII_F RAW SET	Raw Set	Section 8.6.50.13
0x3_2034	AIL EE_SII_F RAW CLEAR	Raw Clear	Section 8.6.50.14
0x3_2038	AIL EE_SII_F EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.15
0x3_203C	AIL EE_SII_F EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.16
0x3_2040	AIL EE_SII_F EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.17
0x3_2044	AIL EE_SII_F EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.18
0x3_2048	AIL EE_SII_F EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.19
0x3_204C	AIL EE_SII_F EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.20
0x3_2050	AIL EE_SII_F EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.21
0x3_2054	AIL EE_SII_F EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.22

Table 8-764. AIL_IQN_AIL_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_2058	AIL EE_SII_G_0 RAW INTERRUPT STATUS	SI si_i IQ per-channel SOP transmitted to PSI info	Section 8.6.50.23
0x3_205C	AIL EE_SII_G_0 RAW SET	Raw Set	Section 8.6.50.24
0x3_2060	AIL EE_SII_G_0 RAW CLEAR	Raw Clear	Section 8.6.50.25
0x3_2064	AIL EE_SII_G_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.26
0x3_2068	AIL EE_SII_G_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.27
0x3_206C	AIL EE_SII_G_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.28
0x3_2070	AIL EE_SII_G_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.29
0x3_2074	AIL EE_SII_G_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.30
0x3_2078	AIL EE_SII_G_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.31
0x3_207C	AIL EE_SII_G_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.32
0x3_2080	AIL EE_SII_G_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.33
0x3_2084	AIL EE_SII_G_1 RAW INTERRUPT STATUS	SI si_i IQ per-channel SOP transmitted to PSI info	Section 8.6.50.34
0x3_2088	AIL EE_SII_G_1 RAW SET	Raw Set	Section 8.6.50.35
0x3_208C	AIL EE_SII_G_1 RAW CLEAR	Raw Clear	Section 8.6.50.36
0x3_2090	AIL EE_SII_G_1 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.37
0x3_2094	AIL EE_SII_G_1 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.38
0x3_2098	AIL EE_SII_G_1 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.39
0x3_209C	AIL EE_SII_G_1 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.40
0x3_20A0	AIL EE_SII_G_1 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.41
0x3_20A4	AIL EE_SII_G_1 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.42

Table 8-764. AIL_IQN_AIL_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_20A8	AIL EE_SII_G_1 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.43
0x3_20AC	AIL EE_SII_G_1 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.44
0x3_2108	AIL EE_SII_H RAW INTERRUPT STATUS	SI si_i CTL per-channel SOP transmitted to PSI info	Section 8.6.50.45
0x3_210C	AIL EE_SII_H RAW SET	Raw Set	Section 8.6.50.46
0x3_2110	AIL EE_SII_H RAW CLEAR	Raw Clear	Section 8.6.50.47
0x3_2114	AIL EE_SII_H EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.48
0x3_2118	AIL EE_SII_H EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.49
0x3_211C	AIL EE_SII_H EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.50
0x3_2120	AIL EE_SII_H EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.51
0x3_2124	AIL EE_SII_H EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.52
0x3_2128	AIL EE_SII_H EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.53
0x3_212C	AIL EE_SII_H EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.54
0x3_2130	AIL EE_SII_H EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.55
0x3_21B8	AIL EE_SIE_D RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.6.50.56
0x3_21BC	AIL EE_SIE_D RAW SET	Raw Set	Section 8.6.50.57
0x3_21C0	AIL EE_SIE_D RAW CLEAR	Raw Clear	Section 8.6.50.58
0x3_21C4	AIL EE_SIE_D EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.59
0x3_21C8	AIL EE_SIE_D EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.60
0x3_21CC	AIL EE_SIE_D EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.61
0x3_21D0	AIL EE_SIE_D EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.62

Table 8-764. AIL_IQN_AIL_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_21D4	AIL EE_SIE_D EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.63
0x3_21D8	AIL EE_SIE_D EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.64
0x3_21DC	AIL EE_SIE_D EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.65
0x3_21E0	AIL EE_SIE_D EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.66
0x3_21E4	AIL EE_SIE_E RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.6.50.67
0x3_21E8	AIL EE_SIE_E RAW SET	Raw Set	Section 8.6.50.68
0x3_21EC	AIL EE_SIE_E RAW CLEAR	Raw Clear	Section 8.6.50.69
0x3_21F0	AIL EE_SIE_E EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.70
0x3_21F4	AIL EE_SIE_E EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.71
0x3_21F8	AIL EE_SIE_E EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.72
0x3_21FC	AIL EE_SIE_E EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.73
0x3_2200	AIL EE_SIE_E EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.74
0x3_2204	AIL EE_SIE_E EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.75
0x3_2208	AIL EE_SIE_E EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.76
0x3_220C	AIL EE_SIE_E EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.77
0x3_2210	AIL EE_SIE_F_0 RAW INTERRUPT STATUS	SI si_e IQ per-channel SOP received from PSI info	Section 8.6.50.78
0x3_2214	AIL EE_SIE_F_0 RAW SET	Raw Set	Section 8.6.50.79
0x3_2218	AIL EE_SIE_F_0 RAW CLEAR	Raw Clear	Section 8.6.50.80
0x3_221C	AIL EE_SIE_F_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.81
0x3_2220	AIL EE_SIE_F_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.82

Table 8-764. AIL_IQN_AIL_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_2224	AIL EE_SIE_F_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.83
0x3_2228	AIL EE_SIE_F_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.84
0x3_222C	AIL EE_SIE_F_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.85
0x3_2230	AIL EE_SIE_F_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.86
0x3_2234	AIL EE_SIE_F_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.87
0x3_2238	AIL EE_SIE_F_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.88
0x3_223C	AIL EE_SIE_F_1 RAW INTERRUPT STATUS	SI si_e IQ per-channel SOP received from PSI info	Section 8.6.50.89
0x3_2240	AIL EE_SIE_F_1 RAW SET	Raw Set	Section 8.6.50.90
0x3_2244	AIL EE_SIE_F_1 RAW CLEAR	Raw Clear	Section 8.6.50.91
0x3_2248	AIL EE_SIE_F_1 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.92
0x3_224C	AIL EE_SIE_F_1 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.93
0x3_2250	AIL EE_SIE_F_1 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.94
0x3_2254	AIL EE_SIE_F_1 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.95
0x3_2258	AIL EE_SIE_F_1 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.96
0x3_225C	AIL EE_SIE_F_1 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.97
0x3_2260	AIL EE_SIE_F_1 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.98
0x3_2264	AIL EE_SIE_F_1 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.99
0x3_22C0	AIL EE_SIE_G RAW INTERRUPT STATUS	SI si_e CTL per-channel SOP received from PSI info	Section 8.6.50.100
0x3_22C4	AIL EE_SIE_G RAW SET	Raw Set	Section 8.6.50.101
0x3_22C8	AIL EE_SIE_G RAW CLEAR	Raw Clear	Section 8.6.50.102

Table 8-764. AIL_IQN_AIL_EE_VBUSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_22CC	AIL EE_SIE_G EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.50.103
0x3_22D0	AIL EE_SIE_G EV0 ENABLE SET	EV0 Enable Set	Section 8.6.50.104
0x3_22D4	AIL EE_SIE_G EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.50.105
0x3_22D8	AIL EE_SIE_G EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.50.106
0x3_22DC	AIL EE_SIE_G EV1 ENABLE SET	EV1 Enable Set	Section 8.6.50.107
0x3_22E0	AIL EE_SIE_G EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.50.108
0x3_22E4	AIL EE_SIE_G EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.50.109
0x3_22E8	AIL EE_SIE_G EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.50.110
0x3_2370	AIL VBUSCLK_ORIG_REG	This is the vbusclk origination register indicating which interrupt register group caused the interrupt.	Section 8.6.50.111

8.6.50.1 AIL EE_SII_E RAW INTERRUPT STATUS [Address = 0x3_2000]

SI si_i IQ info.

Figure 8-661. AIL EE_SII_E RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-765. AIL EE_SII_E RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	SI Ingress IQ data transmitted to PSI
0	SI_ING_IQ_PSI_EOP_INFO	SI Ingress IQ EOP transmitted to PSI

8.6.50.2 AIL EE_SII_E RAW SET [Address = 0x3_2004]

Raw Set

Figure 8-662. AIL EE_SII_E RAW SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-766. AIL EE_SII_E RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.3 AIL EE_SII_E RAW CLEAR [Address = 0x3_2008]

Raw Clear

Figure 8-663. AIL EE_SII_E RAW CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-767. AIL EE_SII_E RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.4 AIL EE_SII_E EV0 ENABLE STATUS [Address = 0x3_200C]

EV0 Enable Status

Figure 8-664. AIL EE_SII_E EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-768. AIL EE_SII_E EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.5 AIL EE_SII_E EV0 ENABLE SET [Address = 0x3_2010]

EV0 Enable Set

Figure 8-665. AIL EE_SII_E EV0 ENABLE SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-769. AIL EE_SII_E EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.6 AIL EE_SII_E EV0 ENABLE CLEAR [Address = 0x3_2014]

EV0 Enable Clear

Figure 8-666. AIL EE_SII_E EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-770. AIL EE_SII_E EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.7 AIL EE_SII_E EV1 ENABLE STATUS [Address = 0x3_2018]

EV1 Enable Status

Figure 8-667. AIL EE_SII_E EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-771. AIL EE_SII_E EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.8 AIL EE_SII_E EV1 ENABLE SET [Address = 0x3_201C]

EV1 Enable Set

Figure 8-668. AIL EE_SII_E EV1 ENABLE SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-772. AIL EE_SII_E EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.9 AIL EE_SII_E EV1 ENABLE CLEAR [Address = 0x3_2020]

EV1 Enable Clear

Figure 8-669. AIL EE_SII_E EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-773. AIL EE_SII_E EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.10 AIL EE_SII_E EV0 ENABLED STATUS [Address = 0x3_2024]

EV0 Enabled Status

Figure 8-670. AIL EE_SII_E EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-774. AIL EE_SII_E EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.11 AIL EE_SII_E EV1 ENABLED STATUS [Address = 0x3_2028]

EV1 Enabled Status

Figure 8-671. AIL EE_SII_E EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-775. AIL EE_SII_E EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.12 AIL EE_SII_F RAW INTERRUPT STATUS [Address = 0x3_202C]

SI si_i CTL info.

Figure 8-672. AIL EE_SII_F RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-776. AIL EE_SII_F RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	SI Ingress CTL data transmitted to PSI
0	SI_ING_CTL_PSI_EOP_INFO	SI Ingress CTL EOP transmitted to PSI

8.6.50.13 AIL EE_SII_F RAW SET [Address = 0x3_2030]

Raw Set

Figure 8-673. AIL EE_SII_F RAW SET

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-777. AIL EE_SII_F RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.14 AIL EE_SII_F RAW CLEAR [Address = 0x3_2034]

Raw Clear

Figure 8-674. AIL EE_SII_F RAW CLEAR

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-778. AIL EE_SII_F RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.15 AIL EE_SII_F EV0 ENABLE STATUS [Address = 0x3_2038]

EV0 Enable Status

Figure 8-675. AIL EE_SII_F EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-779. AIL EE_SII_F EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.16 AIL EE_SII_F EV0 ENABLE SET [Address = 0x3_203C]

EV0 Enable Set

Figure 8-676. AIL EE_SII_F EV0 ENABLE SET

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-780. AIL EE_SII_F EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.17 AIL EE_SII_F EV0 ENABLE CLEAR [Address = 0x3_2040]

EV0 Enable Clear

Figure 8-677. AIL EE_SII_F EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-781. AIL EE_SII_F EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.18 AIL EE_SII_F EV1 ENABLE STATUS [Address = 0x3_2044]

EV1 Enable Status

Figure 8-678. AIL EE_SII_F EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-782. AIL EE_SII_F EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.19 AIL EE_SII_F EV1 ENABLE SET [Address = 0x3_2048]

EV1 Enable Set

Figure 8-679. AIL EE_SII_F EV1 ENABLE SET

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-783. AIL EE_SII_F EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.20 AIL EE_SII_F EV1 ENABLE CLEAR [Address = 0x3_204C]

EV1 Enable Clear

Figure 8-680. AIL EE_SII_F EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-784. AIL EE_SII_F EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.21 AIL EE_SII_F EV0 ENABLED STATUS [Address = 0x3_2050]

EV0 Enabled Status

Figure 8-681. AIL EE_SII_F EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-785. AIL EE_SII_F EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.22 AIL EE_SII_F EV1 ENABLED STATUS [Address = 0x3_2054]

EV1 Enabled Status

Figure 8-682. AIL EE_SII_F EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_CTL_PSI_DAT_INFO	SI_ING_CTL_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-786. AIL EE_SII_F EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.23 AIL EE_SII_G_0 RAW INTERRUPT STATUS [Address = 0x3_2058]

SI si_i IQ per-channel SOP transmitted to PSI info

Figure 8-683. AIL EE_SII_G_0 RAW INTERRUPT STATUS

31	0
SI_ING_IQ_PSI_SOP_INFO	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-787. AIL EE_SII_G_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	SI Ingress IQ SOP transmitted to PSI

8.6.50.24 AIL EE_SII_G_0 RAW SET [Address = 0x3_205C]

Raw Set

Figure 8-684. AIL EE_SII_G_0 RAW SET

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-788. AIL EE_SII_G_0 RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.25 AIL EE_SII_G_0 RAW CLEAR [Address = 0x3_2060]

Raw Clear

Figure 8-685. AIL EE_SII_G_0 RAW CLEAR

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

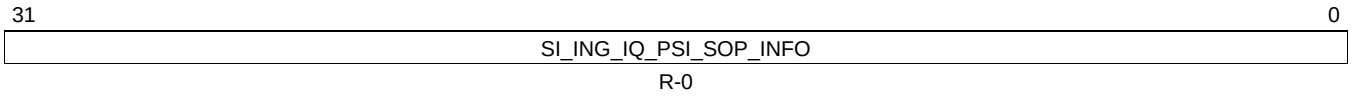
Table 8-789. AIL EE_SII_G_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.26 AIL EE_SII_G_0 EV0 ENABLE STATUS [Address = 0x3_2064]

EV0 Enable Status

Figure 8-686. AIL EE_SII_G_0 EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-790. AIL EE_SII_G_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.27 AIL EE_SII_G_0 EV0 ENABLE SET [Address = 0x3_2068]

EV0 Enable Set

Figure 8-687. AIL EE_SII_G_0 EV0 ENABLE SET

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

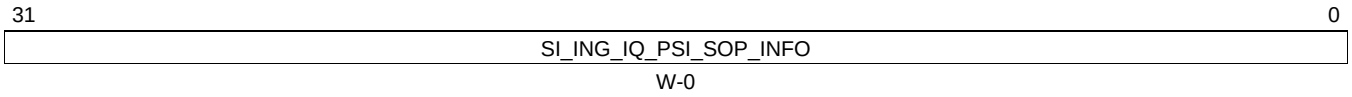
Table 8-791. AIL EE_SII_G_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.28 AIL EE_SII_G_0 EV0 ENABLE CLEAR [Address = 0x3_206C]

EV0 Enable Clear

Figure 8-688. AIL EE_SII_G_0 EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

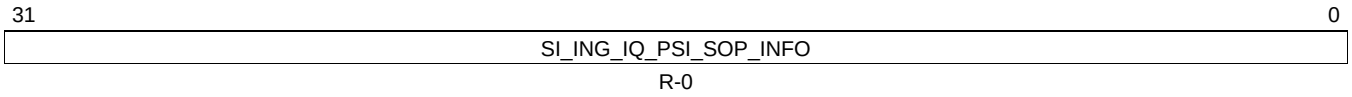
Table 8-792. AIL EE_SII_G_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.29 AIL EE_SII_G_0 EV1 ENABLE STATUS [Address = 0x3_2070]

EV1 Enable Status

Figure 8-689. AIL EE_SII_G_0 EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-793. AIL EE_SII_G_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.30 AIL EE_SII_G_0 EV1 ENABLE SET [Address = 0x3_2074]

EV1 Enable Set

Figure 8-690. AIL EE_SII_G_0 EV1 ENABLE SET

31	0
SI_ING_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

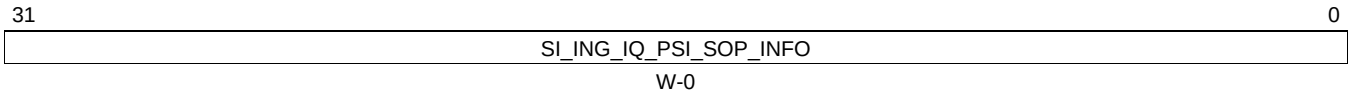
Table 8-794. AIL EE_SII_G_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.31 AIL EE_SII_G_0 EV1 ENABLE CLEAR [Address = 0x3_2078]

EV1 Enable Clear

Figure 8-691. AIL EE_SII_G_0 EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-795. AIL EE_SII_G_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.32 AIL EE_SII_G_0 EV0 ENABLED STATUS [Address = 0x3_207C]

EV0 Enabled Status

Figure 8-692. AIL EE_SII_G_0 EV0 ENABLED STATUS

31	0
SI_ING_IQ_PSI_SOP_INFO	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

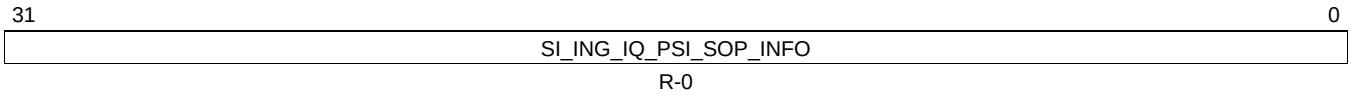
Table 8-796. AIL EE_SII_G_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.33 AIL EE_SII_G_0 EV1 ENABLED STATUS [Address = 0x3_2080]

EV1 Enabled Status

Figure 8-693. AIL EE_SII_G_0 EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

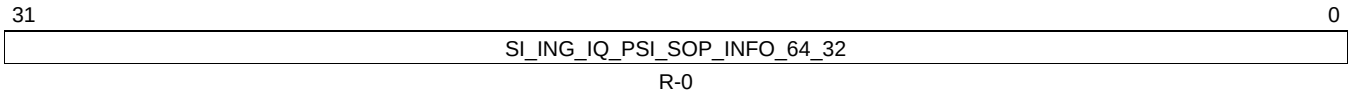
Table 8-797. AIL EE_SII_G_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.34 AIL EE_SII_G_1 RAW INTERRUPT STATUS [Address = 0x3_2084]

SI si_i IQ per-channel SOP transmitted to PSI info

Figure 8-694. AIL EE_SII_G_1 RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-798. AIL EE_SII_G_1 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	SI Ingress IQ SOP transmitted to PSI

8.6.50.35 AIL EE_SII_G_1 RAW SET [Address = 0x3_2088]

Raw Set

Figure 8-695. AIL EE_SII_G_1 RAW SET

31	0
SI_ING_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-799. AIL EE_SII_G_1 RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.36 AIL EE_SII_G_1 RAW CLEAR [Address = 0x3_208C]

Raw Clear

Figure 8-696. AIL EE_SII_G_1 RAW CLEAR

31	0
SI_ING_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

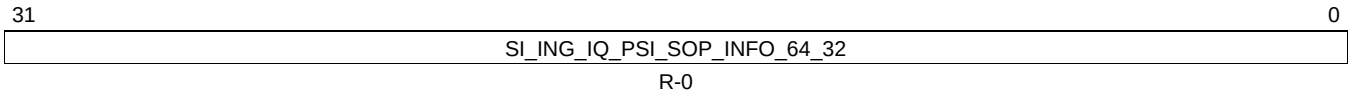
Table 8-800. AIL EE_SII_G_1 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.37 AIL EE_SII_G_1 EV0 ENABLE STATUS [Address = 0x3_2090]

EV0 Enable Status

Figure 8-697. AIL EE_SII_G_1 EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-801. AIL EE_SII_G_1 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.38 AIL EE_SII_G_1 EV0 ENABLE SET [Address = 0x3_2094]

EV0 Enable Set

Figure 8-698. AIL EE_SII_G_1 EV0 ENABLE SET

31	0
SI_ING_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-802. AIL EE_SII_G_1 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.39 AIL EE_SII_G_1 EV0 ENABLE CLEAR [Address = 0x3_2098]

EV0 Enable Clear

Figure 8-699. AIL EE_SII_G_1 EV0 ENABLE CLEAR

31	0
SI_ING_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

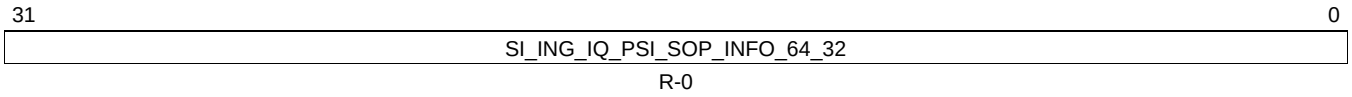
Table 8-803. AIL EE_SII_G_1 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.40 AIL EE_SII_G_1 EV1 ENABLE STATUS [Address = 0x3_209C]

EV1 Enable Status

Figure 8-700. AIL EE_SII_G_1 EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

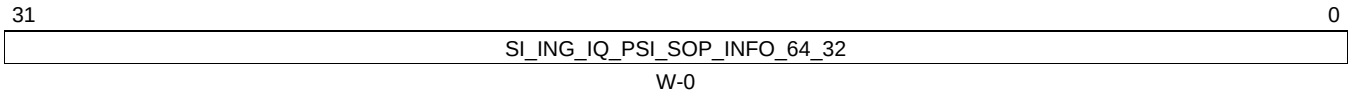
Table 8-804. AIL EE_SII_G_1 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.41 AIL EE_SII_G_1 EV1 ENABLE SET [Address = 0x3_20A0]

EV1 Enable Set

Figure 8-701. AIL EE_SII_G_1 EV1 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

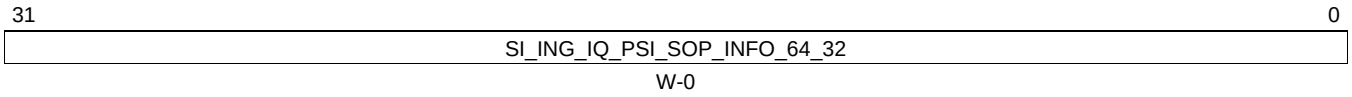
Table 8-805. AIL EE_SII_G_1 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.42 AIL EE_SII_G_1 EV1 ENABLE CLEAR [Address = 0x3_20A4]

EV1 Enable Clear

Figure 8-702. AIL EE_SII_G_1 EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

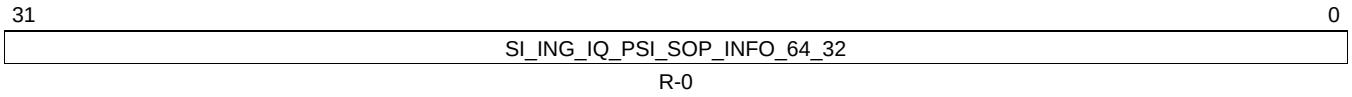
Table 8-806. AIL EE_SII_G_1 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.43 AIL EE_SII_G_1 EV0 ENABLED STATUS [Address = 0x3_20A8]

EV0 Enabled Status

Figure 8-703. AIL EE_SII_G_1 EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

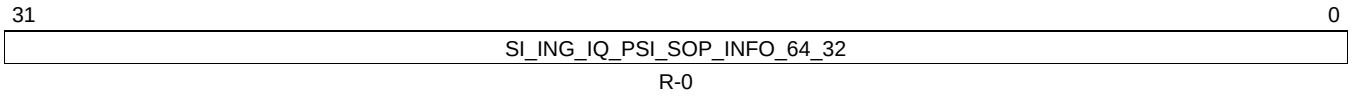
Table 8-807. AIL EE_SII_G_1 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.44 AIL EE_SII_G_1 EV1 ENABLED STATUS [Address = 0x3_20AC]

EV1 Enabled Status

Figure 8-704. AIL EE_SII_G_1 EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-808. AIL EE_SII_G_1 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_PSI_SOP_INFO_64_32	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.45 AIL EE_SII_H RAW INTERRUPT STATUS [Address = 0x3_2108]

SI si_i CTL per-channel SOP transmitted to PSI info

Figure 8-705. AIL EE_SII_H RAW INTERRUPT STATUS

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-809. AIL EE_SII_H RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	SI Ingress CTL per channel SOP transmitted to PSI

8.6.50.46 AIL EE_SII_H RAW SET [Address = 0x3_210C]

Raw Set

Figure 8-706. AIL EE_SII_H RAW SET

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-810. AIL EE_SII_H RAW SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.47 AIL EE_SII_H RAW CLEAR [Address = 0x3_2110]

Raw Clear

Figure 8-707. AIL EE_SII_H RAW CLEAR

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-811. AIL EE_SII_H RAW CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.48 AIL EE_SII_H EV0 ENABLE STATUS [Address = 0x3_2114]

EV0 Enable Status

Figure 8-708. AIL EE_SII_H EV0 ENABLE STATUS

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-812. AIL EE_SII_H EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.49 AIL EE_SII_H EV0 ENABLE SET [Address = 0x3_2118]

EV0 Enable Set

Figure 8-709. AIL EE_SII_H EV0 ENABLE SET

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-813. AIL EE_SII_H EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.50 AIL EE_SII_H EV0 ENABLE CLEAR [Address = 0x3_211C]

EV0 Enable Clear

Figure 8-710. AIL EE_SII_H EV0 ENABLE CLEAR

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-814. AIL EE_SII_H EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.51 AIL EE_SII_H EV1 ENABLE STATUS [Address = 0x3_2120]

EV1 Enable Status

Figure 8-711. AIL EE_SII_H EV1 ENABLE STATUS

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-815. AIL EE_SII_H EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.52 AIL EE_SII_H EV1 ENABLE SET [Address = 0x3_2124]

EV1 Enable Set

Figure 8-712. AIL EE_SII_H EV1 ENABLE SET

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-816. AIL EE_SII_H EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.53 AIL EE_SII_H EV1 ENABLE CLEAR [Address = 0x3_2128]

EV1 Enable Clear

Figure 8-713. AIL EE_SII_H EV1 ENABLE CLEAR

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-817. AIL EE_SII_H EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.54 AIL EE_SII_H EV0 ENABLED STATUS [Address = 0x3_212C]

EV0 Enabled Status

Figure 8-714. AIL EE_SII_H EV0 ENABLED STATUS

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-818. AIL EE_SII_H EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.55 AIL EE_SII_H EV1 ENABLED STATUS [Address = 0x3_2130]

EV1 Enabled Status

Figure 8-715. AIL EE_SII_H EV1 ENABLED STATUS

31	4	3	0
Reserved		SI_ING_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-819. AIL EE_SII_H EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.56 AIL EE_SIE_D RAW INTERRUPT STATUS [Address = 0x3_21B8]

SI si_e IQ errors and info.

Figure 8-716. AIL EE_SIE_D RAW INTERRUPT STATUS

31	3	2
Reserved		SI_EGR_IQ_PSI_DAT_INFO
NA-0		R-0

1	0
SI_EGR_IQ_PSI_EOP_INFO	SI_EGR_IQ_PSI_DATA_TYPE_ERR
R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-820. AIL EE_SIE_D RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	SI Egress IQ valid data received from PSI
1	SI_EGR_IQ_PSI_EOP_INFO	SI Egress IQ EOP received from PSI
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	SI Egress IQ PSI data type error

8.6.50.57 AIL EE_SIE_D RAW SET [Address = 0x3_21BC]

Raw Set

Figure 8-717. AIL EE_SIE_D RAW SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-821. AIL EE_SIE_D RAW SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.58 AIL EE_SIE_D RAW CLEAR [Address = 0x3_21C0]

Raw Clear

Figure 8-718. AIL EE_SIE_D RAW CLEAR

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-822. AIL EE_SIE_D RAW CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.59 AIL EE_SIE_D EV0 ENABLE STATUS [Address = 0x3_21C4]

EV0 Enable Status

Figure 8-719. AIL EE_SIE_D EV0 ENABLE STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-823. AIL EE_SIE_D EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.60 AIL EE_SIE_D EV0 ENABLE SET [Address = 0x3_21C8]

EV0 Enable Set

Figure 8-720. AIL EE_SIE_D EV0 ENABLE SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-824. AIL EE_SIE_D EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.61 AIL EE_SIE_D EV0 ENABLE CLEAR [Address = 0x3_21CC]

EV0 Enable Clear

Figure 8-721. AIL EE_SIE_D EV0 ENABLE CLEAR

31	3	2
Reserved		SI_EGR_IQ_PSI_DAT_INFO
NA-0		W-0

1	0
SI_EGR_IQ_PSI_EOP_INFO	SI_EGR_IQ_PSI_DATA_TYPE_ERR
W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-825. AIL EE_SIE_D EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.62 AIL EE_SIE_D EV1 ENABLE STATUS [Address = 0x3_21D0]

EV1 Enable Status

Figure 8-722. AIL EE_SIE_D EV1 ENABLE STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-826. AIL EE_SIE_D EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.63 AIL EE_SIE_D EV1 ENABLE SET [Address = 0x3_21D4]

EV1 Enable Set

Figure 8-723. AIL EE_SIE_D EV1 ENABLE SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-827. AIL EE_SIE_D EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.64 AIL EE_SIE_D EV1 ENABLE CLEAR [Address = 0x3_21D8]

EV1 Enable Clear

Figure 8-724. AIL EE_SIE_D EV1 ENABLE CLEAR

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-828. AIL EE_SIE_D EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.65 AIL EE_SIE_D EV0 ENABLED STATUS [Address = 0x3_21DC]

EV0 Enabled Status

Figure 8-725. AIL EE_SIE_D EV0 ENABLED STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-829. AIL EE_SIE_D EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.66 AIL EE_SIE_D EV1 ENABLED STATUS [Address = 0x3_21E0]

EV1 Enabled Status

Figure 8-726. AIL EE_SIE_D EV1 ENABLED STATUS

31	3	2	0
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1			0
SI_EGR_IQ_PSI_EOP_INFO			SI_EGR_IQ_PSI_DATA_TYPE_ERR
R-0			R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-830. AIL EE_SIE_D EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.67 AIL EE_SIE_E RAW INTERRUPT STATUS [Address = 0x3_21E4]

SI si_e IQ errors and info.

Figure 8-727. AIL EE_SIE_E RAW INTERRUPT STATUS

31	3	2	1	0
Reserved		SI_EGR_CTL_PSI_DAT_INFO	SI_EGR_CTL_PSI_EOP_INFO	SI_EGR_CTL_PSI_DATA_TYPE_ERR
NA-0		R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-831. AIL EE_SIE_E RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	SI Egress CTL valid data received from PSI
1	SI_EGR_CTL_PSI_EOP_INFO	SI Egress CTL EOP received from PSI
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	SI Egress CTL PSI data type error

8.6.50.68 AIL EE_SIE_E RAW SET [Address = 0x3_21E8]

Raw Set

Figure 8-728. AIL EE_SIE_E RAW SET

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-832. AIL EE_SIE_E RAW SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.69 AIL EE_SIE_E RAW CLEAR [Address = 0x3_21EC]

Raw Clear

Figure 8-729. AIL EE_SIE_E RAW CLEAR

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-833. AIL EE_SIE_E RAW CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.70 AIL EE_SIE_E EV0 ENABLE STATUS [Address = 0x3_21F0]

EV0 Enable Status

Figure 8-730. AIL EE_SIE_E EV0 ENABLE STATUS

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		R-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-834. AIL EE_SIE_E EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.71 AIL EE_SIE_E EV0 ENABLE SET [Address = 0x3_21F4]

EV0 Enable Set

Figure 8-731. AIL EE_SIE_E EV0 ENABLE SET

31	3	2
Reserved		SI_EGR_CTL_PSI_DAT_INFO
NA-0		W-0

1	0
SI_EGR_CTL_PSI_EOP_INFO	SI_EGR_CTL_PSI_DATA_TYPE_ERR
W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-835. AIL EE_SIE_E EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.72 AIL EE_SIE_E EV0 ENABLE CLEAR [Address = 0x3_21F8]

EV0 Enable Clear

Figure 8-732. AIL EE_SIE_E EV0 ENABLE CLEAR

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-836. AIL EE_SIE_E EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.73 AIL EE_SIE_E EV1 ENABLE STATUS [Address = 0x3_21FC]

EV1 Enable Status

Figure 8-733. AIL EE_SIE_E EV1 ENABLE STATUS

31	3	2	0
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		R-0	
	1		0
	SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR
	R-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-837. AIL EE_SIE_E EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.74 AIL EE_SIE_E EV1 ENABLE SET [Address = 0x3_2200]

EV1 Enable Set

Figure 8-734. AIL EE_SIE_E EV1 ENABLE SET

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO			SI_EGR_CTL_PSI_DATA_TYPE_ERR
W-0			W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-838. AIL EE_SIE_E EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.75 AIL EE_SIE_E EV1 ENABLE CLEAR [Address = 0x3_2204]

EV1 Enable Clear

Figure 8-735. AIL EE_SIE_E EV1 ENABLE CLEAR

31	3	2	0
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		W-0	
	1		0
	SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR
	W-0		W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-839. AIL EE_SIE_E EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_CTL_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.76 AIL EE_SIE_E EV0 ENABLED STATUS [Address = 0x3_2208]

EV0 Enabled Status

Figure 8-736. AIL EE_SIE_E EV0 ENABLED STATUS

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		R-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-840. AIL EE_SIE_E EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.77 AIL EE_SIE_E EV1 ENABLED STATUS [Address = 0x3_220C]

EV1 Enabled Status

Figure 8-737. AIL EE_SIE_E EV1 ENABLED STATUS

31	3	2	
Reserved		SI_EGR_CTL_PSI_DAT_INFO	
NA-0		R-0	
	1		0
SI_EGR_CTL_PSI_EOP_INFO		SI_EGR_CTL_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-841. AIL EE_SIE_E EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_CTL_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_CTL_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_CTL_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.78 AIL EE_SIE_F_0 RAW INTERRUPT STATUS [Address = 0x3_2210]

SI si_e IQ per-channel SOP received from PSI info

Figure 8-738. AIL EE_SIE_F_0 RAW INTERRUPT STATUS

31	0
SI_EGR_IQ_PSI_SOP_INFO	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-842. AIL EE_SIE_F_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	SI Ingress IQ per channel SOP received from PSI

8.6.50.79 AIL EE_SIE_F_0 RAW SET [Address = 0x3_2214]

Raw Set

Figure 8-739. AIL EE_SIE_F_0 RAW SET

31	0
SI_EGR_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-843. AIL EE_SIE_F_0 RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.80 AIL EE_SIE_F_0 RAW CLEAR [Address = 0x3_2218]

Raw Clear

Figure 8-740. AIL EE_SIE_F_0 RAW CLEAR

31	0
SI_EGR_IQ_PSI_SOP_INFO	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

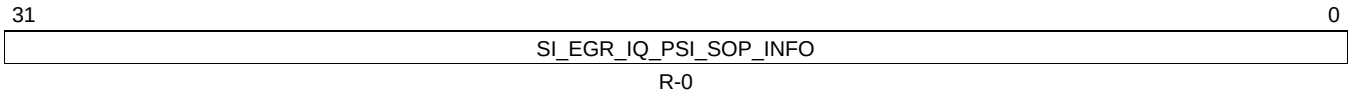
Table 8-844. AIL EE_SIE_F_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.81 AIL EE_SIE_F_0 EV0 ENABLE STATUS [Address = 0x3_221C]

EV0 Enable Status

Figure 8-741. AIL EE_SIE_F_0 EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

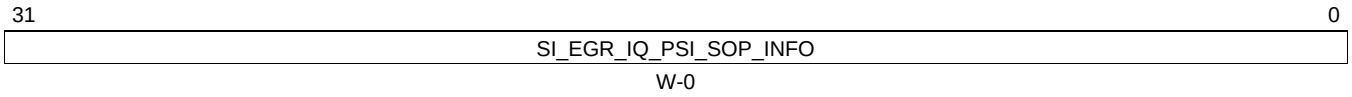
Table 8-845. AIL EE_SIE_F_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.82 AIL EE_SIE_F_0 EV0 ENABLE SET [Address = 0x3_2220]

EV0 Enable Set

Figure 8-742. AIL EE_SIE_F_0 EV0 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

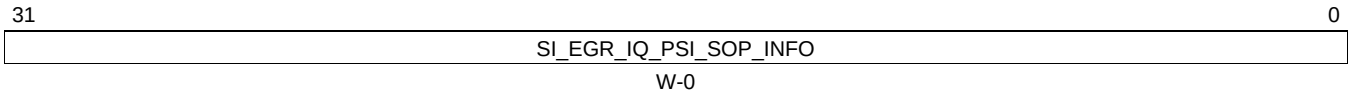
Table 8-846. AIL EE_SIE_F_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.83 AIL EE_SIE_F_0 EV0 ENABLE CLEAR [Address = 0x3_2224]

EV0 Enable Clear

Figure 8-743. AIL EE_SIE_F_0 EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

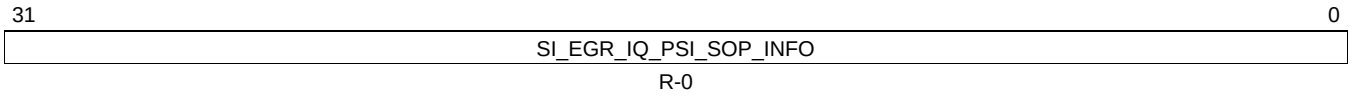
Table 8-847. AIL EE_SIE_F_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.84 AIL EE_SIE_F_0 EV1 ENABLE STATUS [Address = 0x3_2228]

EV1 Enable Status

Figure 8-744. AIL EE_SIE_F_0 EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

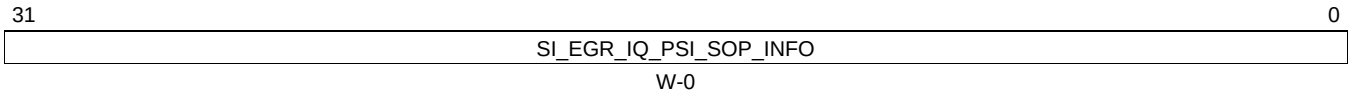
Table 8-848. AIL EE_SIE_F_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.85 AIL EE_SIE_F_0 EV1 ENABLE SET [Address = 0x3_222C]

EV1 Enable Set

Figure 8-745. AIL EE_SIE_F_0 EV1 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

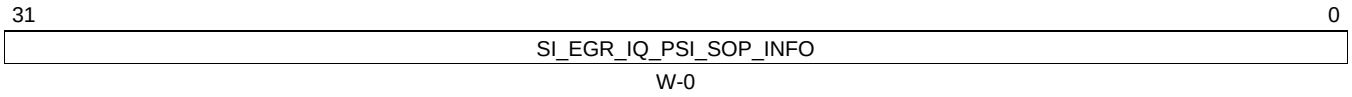
Table 8-849. AIL EE_SIE_F_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.86 AIL EE_SIE_F_0 EV1 ENABLE CLEAR [Address = 0x3_2230]

EV1 Enable Clear

Figure 8-746. AIL EE_SIE_F_0 EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

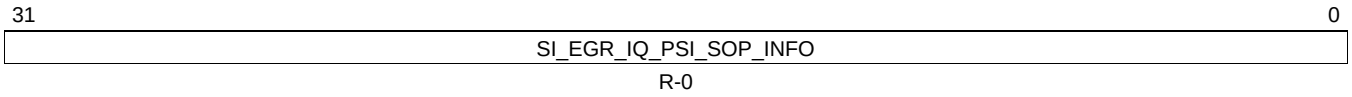
Table 8-850. AIL EE_SIE_F_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.87 AIL EE_SIE_F_0 EV0 ENABLED STATUS [Address = 0x3_2234]

EV0 Enabled Status

Figure 8-747. AIL EE_SIE_F_0 EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

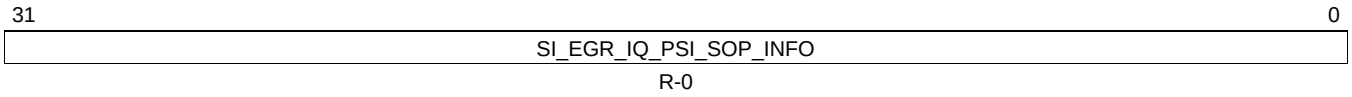
Table 8-851. AIL EE_SIE_F_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.88 AIL EE_SIE_F_0 EV1 ENABLED STATUS [Address = 0x3_2238]

EV1 Enabled Status

Figure 8-748. AIL EE_SIE_F_0 EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-852. AIL EE_SIE_F_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.89 AIL EE_SIE_F_1 RAW INTERRUPT STATUS [Address = 0x3_223C]

SI si_e IQ per-channel SOP received from PSI info

Figure 8-749. AIL EE_SIE_F_1 RAW INTERRUPT STATUS

31	0
SI_EGR_IQ_PSI_SOP_INFO_64_32	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-853. AIL EE_SIE_F_1 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	SI Ingress IQ per channel SOP received from PSI

8.6.50.90 AIL EE_SIE_F_1 RAW SET [Address = 0x3_2240]

Raw Set

Figure 8-750. AIL EE_SIE_F_1 RAW SET

31	0
SI_EGR_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-854. AIL EE_SIE_F_1 RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.91 AIL EE_SIE_F_1 RAW CLEAR [Address = 0x3_2244]

Raw Clear

Figure 8-751. AIL EE_SIE_F_1 RAW CLEAR

31	0
SI_EGR_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

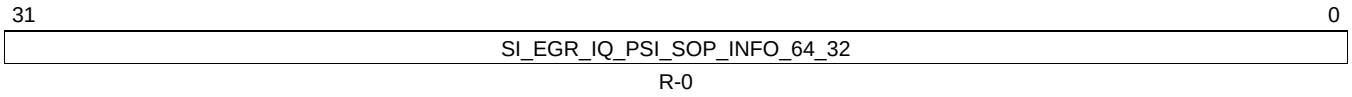
Table 8-855. AIL EE_SIE_F_1 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.92 AIL EE_SIE_F_1 EV0 ENABLE STATUS [Address = 0x3_2248]

EV0 Enable Status

Figure 8-752. AIL EE_SIE_F_1 EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

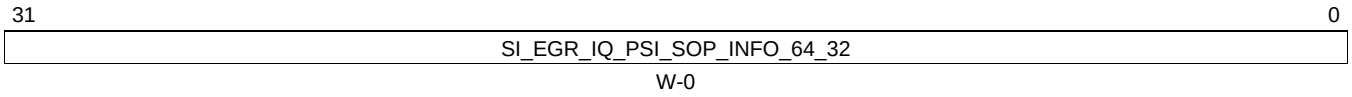
Table 8-856. AIL EE_SIE_F_1 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.93 AIL EE_SIE_F_1 EV0 ENABLE SET [Address = 0x3_224C]

EV0 Enable Set

Figure 8-753. AIL EE_SIE_F_1 EV0 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-857. AIL EE_SIE_F_1 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.94 AIL EE_SIE_F_1 EV0 ENABLE CLEAR [Address = 0x3_2250]

EV0 Enable Clear

Figure 8-754. AIL EE_SIE_F_1 EV0 ENABLE CLEAR

31	0
SI_EGR_IQ_PSI_SOP_INFO_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-858. AIL EE_SIE_F_1 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.95 AIL EE_SIE_F_1 EV1 ENABLE STATUS [Address = 0x3_2254]

EV1 Enable Status

Figure 8-755. AIL EE_SIE_F_1 EV1 ENABLE STATUS

31	0
SI_EGR_IQ_PSI_SOP_INFO_64_32	
R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

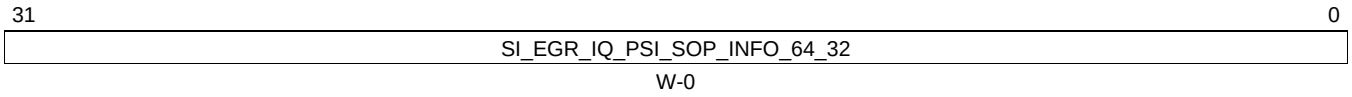
Table 8-859. AIL EE_SIE_F_1 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.96 AIL EE_SIE_F_1 EV1 ENABLE SET [Address = 0x3_2258]

EV1 Enable Set

Figure 8-756. AIL EE_SIE_F_1 EV1 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

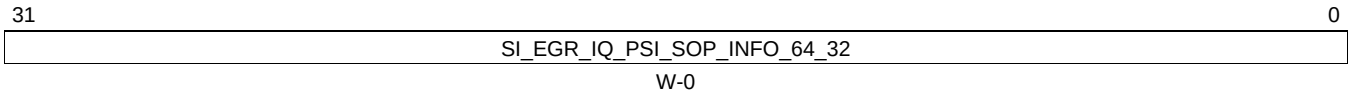
Table 8-860. AIL EE_SIE_F_1 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.97 AIL EE_SIE_F_1 EV1 ENABLE CLEAR [Address = 0x3_225C]

EV1 Enable Clear

Figure 8-757. AIL EE_SIE_F_1 EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

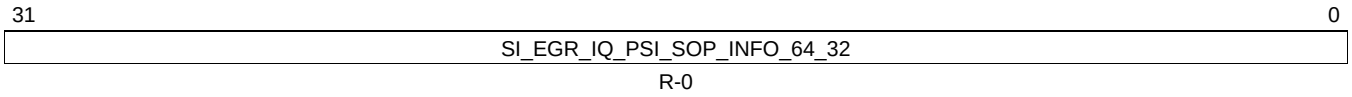
Table 8-861. AIL EE_SIE_F_1 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.98 AIL EE_SIE_F_1 EV0 ENABLED STATUS [Address = 0x3_2260]

EV0 Enabled Status

Figure 8-758. AIL EE_SIE_F_1 EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

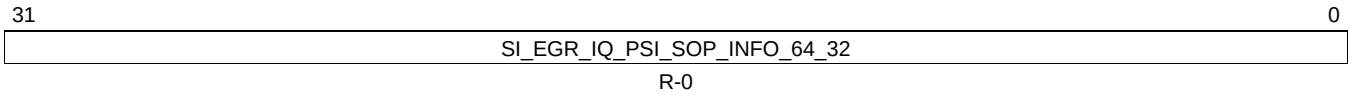
Table 8-862. AIL EE_SIE_F_1 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.99 AIL EE_SIE_F_1 EV1 ENABLED STATUS [Address = 0x3_2264]

EV1 Enabled Status

Figure 8-759. AIL EE_SIE_F_1 EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-863. AIL EE_SIE_F_1 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_EGR_IQ_PSI_SOP_INFO_64_32	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.100 AIL EE_SIE_G RAW INTERRUPT STATUS [Address = 0x3_22C0]

SI si_e CTL per-channel SOP received from PSI info

Figure 8-760. AIL EE_SIE_G RAW INTERRUPT STATUS

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-864. AIL EE_SIE_G RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	SI Egress CTL per channel SOP received from PSI

8.6.50.101 AIL EE_SIE_G RAW SET [Address = 0x3_22C4]

Raw Set

Figure 8-761. AIL EE_SIE_G RAW SET

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-865. AIL EE_SIE_G RAW SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.102 AIL EE_SIE_G RAW CLEAR [Address = 0x3_22C8]

Raw Clear

Figure 8-762. AIL EE_SIE_G RAW CLEAR

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-866. AIL EE_SIE_G RAW CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.50.103 AIL EE_SIE_G EV0 ENABLE STATUS [Address = 0x3_22CC]

EV0 Enable Status

Figure 8-763. AIL EE_SIE_G EV0 ENABLE STATUS

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-867. AIL EE_SIE_G EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.50.104 AIL EE_SIE_G EV0 ENABLE SET [Address = 0x3_22D0]

EV0 Enable Set

Figure 8-764. AIL EE_SIE_G EV0 ENABLE SET

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-868. AIL EE_SIE_G EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.105 AIL EE_SIE_G EV0 ENABLE CLEAR [Address = 0x3_22D4]

EV0 Enable Clear

Figure 8-765. AIL EE_SIE_G EV0 ENABLE CLEAR

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

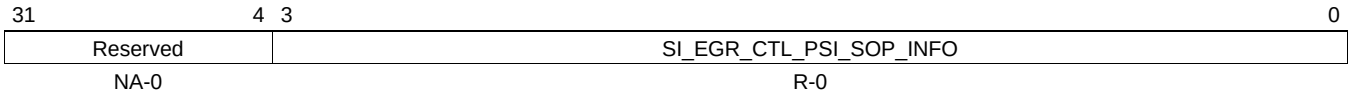
Table 8-869. AIL EE_SIE_G EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.50.106 AIL EE_SIE_G EV1 ENABLE STATUS [Address = 0x3_22D8]

EV1 Enable Status

Figure 8-766. AIL EE_SIE_G EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-870. AIL EE_SIE_G EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.50.107 AIL EE_SIE_G EV1 ENABLE SET [Address = 0x3_22DC]

EV1 Enable Set

Figure 8-767. AIL EE_SIE_G EV1 ENABLE SET

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-871. AIL EE_SIE_G EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.108 AIL EE_SIE_G EV1 ENABLE CLEAR [Address = 0x3_22E0]

EV1 Enable Clear

Figure 8-768. AIL EE_SIE_G EV1 ENABLE CLEAR

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-872. AIL EE_SIE_G EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.50.109 AIL EE_SIE_G EV0 ENABLED STATUS [Address = 0x3_22E4]

EV0 Enabled Status

Figure 8-769. AIL EE_SIE_G EV0 ENABLED STATUS

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-873. AIL EE_SIE_G EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.50.110 AIL EE_SIE_G EV1 ENABLED STATUS [Address = 0x3_22E8]

EV1 Enabled Status

Figure 8-770. AIL EE_SIE_G EV1 ENABLED STATUS

31	4	3	0
Reserved		SI_EGR_CTL_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-874. AIL EE_SIE_G EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.50.111 AIL VBUSCLK_ORIG_REG [Address = 0x3_2370]

This is the vbusclk origination register indicating which interrupt register group caused the interrupt.

Figure 8-771. AIL VBUSCLK_ORIG_REG

31	20	19	18	17	16
Reserved		ORIG_EE_19	ORIG_EE_18	ORIG_EE_17	ORIG_EE_16
NA-0		R-0	R-0	R-0	R-0

15	14	13	12	11	10
ORIG_EE_15	ORIG_EE_14	ORIG_EE_13	ORIG_EE_12	ORIG_EE_11	ORIG_EE_10
R-0	R-0	R-0	R-0	R-0	R-0

9	8	7	6	5	4	3	2	1	0
ORIG_EE_9	ORIG_EE_8	ORIG_EE_7	ORIG_EE_6	ORIG_EE_5	ORIG_EE_4	ORIG_EE_3	ORIG_EE_2	ORIG_EE_1	ORIG_EE_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-875. AIL VBUSCLK_ORIG_REG Field Descriptions

Bits	Name	Description
31-20	Reserved	Reserved
19	ORIG_EE_19	Reserved.
18	ORIG_EE_18	Reserved.
17	ORIG_EE_17	Reserved.
16	ORIG_EE_16	If set a bit is set in the ee_sie_g register.
15	ORIG_EE_15	Reserved.
14	ORIG_EE_14	Reserved.
13	ORIG_EE_13	If set a bit is set in the ee_sie_f_1 register.
12	ORIG_EE_12	If set a bit is set in the ee_sie_f_0 register.
11	ORIG_EE_11	If set a bit is set in the ee_sie_e register.
10	ORIG_EE_10	If set a bit is set in the ee_sie_d register.
9	ORIG_EE_9	Reserved.
8	ORIG_EE_8	Reserved.
7	ORIG_EE_7	Reserved.
6	ORIG_EE_6	If set a bit is set in the ee_sii_h_d register.
5	ORIG_EE_5	Reserved.
4	ORIG_EE_4	Reserved.
3	ORIG_EE_3	If set a bit is set in the ee_sii_g_1 register.
2	ORIG_EE_2	If set a bit is set in the ee_sii_g_0 register.
1	ORIG_EE_1	If set a bit is set in the ee_sii_f register.
0	ORIG_EE_0	If set a bit is set in the ee_sii_e register.

8.6.51 AIL_IQN_AIL_EE_SYSCLK_PHY_EE [Address = 0x3_4000]

Table 8-876. AIL_IQN_AIL_EE_SYSCLK_PHY_EE

Offset	Acronym	Register Description	Section
0x3_4000	AIL RM_0 RAW INTERRUPT STATUS	AIL RM error register.	Section 8.6.51.1
0x3_4004	AIL RM_0 RAW SET	Raw Set	Section 8.6.51.2
0x3_4008	AIL RM_0 RAW CLEAR	Raw Clear	Section 8.6.51.3
0x3_400C	AIL RM_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.51.4
0x3_4010	AIL RM_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.51.5
0x3_4014	AIL RM_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.51.6
0x3_4018	AIL RM_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.51.7
0x3_401C	AIL RM_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.51.8
0x3_4020	AIL RM_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.51.9
0x3_4024	AIL RM_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.51.10
0x3_4028	AIL RM_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.51.11
0x3_402C	AIL RT_TM_0 RAW INTERRUPT STATUS	AIL RT and TM error register.	Section 8.6.51.12
0x3_4030	AIL RT_TM_0 RAW SET	Raw Set	Section 8.6.51.13
0x3_4034	AIL RT_TM_0 RAW CLEAR	Raw Clear	Section 8.6.51.14
0x3_4038	AIL RT_TM_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.51.15
0x3_403C	AIL RT_TM_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.51.16
0x3_4040	AIL RT_TM_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.51.17
0x3_4044	AIL RT_TM_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.51.18
0x3_4048	AIL RT_TM_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.51.19
0x3_404C	AIL RT_TM_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.51.20
0x3_4050	AIL RT_TM_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.51.21
0x3_4054	AIL RT_TM_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.51.22

Table 8-876. AIL_IQN_AIL_EE_SYSCLK_PHY_EE (continued)

Offset	Acronym	Register Description	Section
0x3_4058	AIL CI_CO_0 RAW INTERRUPT STATUS	AIL CI and CO error register.	Section 8.6.51.23
0x3_405C	AIL CI_CO_0 RAW SET	Raw Set	Section 8.6.51.24
0x3_4060	AIL CI_CO_0 RAW CLEAR	Raw Clear	Section 8.6.51.25
0x3_4064	AIL CI_CO_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.51.26
0x3_4068	AIL CI_CO_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.51.27
0x3_406C	AIL CI_CO_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.51.28
0x3_4070	AIL CI_CO_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.51.29
0x3_4074	AIL CI_CO_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.51.30
0x3_4078	AIL CI_CO_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.51.31
0x3_407C	AIL CI_CO_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.51.32
0x3_4080	AIL CI_CO_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.51.33
0x3_4084	AIL SYSCLK_PHY_ORIG_REG	This is the sysclk origination register indicating which interrupt register group caused the interrupt.	Section 8.6.51.34

8.6.51.1 AIL RM_0 RAW INTERRUPT STATUS [Address = 0x3_4000]

AIL RM error register.

Figure 8-772. AIL RM_0 RAW INTERRUPT STATUS

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		R-0	R-0	R-0	R-0	R-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
R-0	R-0	R-0	R-0	R-0	R-0	R-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
R-0	R-0	R-0	R-0	R-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
R-0	R-0	R-0	R-0	R-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-877. AIL RM_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	RM reset is an SOC reset generated when the L1inband rst signal is valid high for 5 consecutive frames.
24	LOF_STATE	lof state indicates the Rx state machine lost frame.
23	HFNSYNC_STATE	hfnsync state indicates that the Rx state has recognized the hfn value in CPRI mode.
22	LOF_ERR	An lof error has occurred in the Rx state machine, indicating that a valid frame format is no longer received from the ser-des interface.
21	LOS_ERR	An los error has occurred in the Rx state machine, indicating that a valid signal is no longer received from the ser-des interface.
20	RCVD_RST	Recevied a rst set high in the CPRI L1inband signal while in CPRI mode.
19	RCVD_SDI	Recevied an sdi (Signal Defect Indicator) in the CPRI L1inband signal while in CPRI mode.
18	RCVD_RAI	Recieved an rai (Remote Alarm Indicator) in the CPRI L1inband signal while in CPRI mode.
17	RCVD_LOF	Recieved an lof in the CPRI L1inband signal while in CPRI mode.
16	RCVD_LOS	Recieved an los in the CPRI L1inband signal while in CPRI mode.
15	RX_FIFO_OVF	RX Fifo has overflowed, indicating the rx clock is faster than the system clock.
14	LOC_DET	Loc was detected in the RM block as determined by the clock monitor circuit.
13	K30P7_DET	A k30p7 was detected in the RM received byte data.
12	MISSING_K28P7	An expected k28p7 was missed by the Rx state machine.
11	MISSING_K28P5	An expected k28p5 was missed by the Rx state machine.
10	BLOCK_BNDRY_DET	The RM has detected a valid block boundary.
9	FRAME_BNDRY_DET	The RM has detected Frame boundary.
8	LCV_DET	lcv error detected.
7	NUM_LOS_DET	Number of los detected over los_thold number.
6	RM_STATUS_STATE5	The Rx state machine of the RM is in state5, indicating the link is in OBSAI scramberl received state.

Table 8-877. AIL RM_0 RAW INTERRUPT STATUS Field Descriptions (continued)

Bits	Name	Description
5	RM_STATUS_STATE4	The Rx state machine of the RM is in state4, indicating the link is in OBSAI scrambler detect state.
4	RM_STATUS_STATE3	The Rx state machine of the RM is in state3, indicating the link is in sync state.
3	RM_STATUS_STATE2	The Rx state machine of the RM is in state2, indicating the link is in pre-sync state.
2	RM_STATUS_STATE1	The Rx state machine of the RM is in state1, indicating the link is in K character recieved state.
1	RM_STATUS_STATE0	The Rx state machine of the RM is in state0, indicating the link is idle.
0	SYNC_STATUS_CHANGE	Sync status has changed in the Rx state machine.

8.6.51.2 AIL RM_0 RAW SET [Address = 0x3_4004]

Raw Set

Figure 8-773. AIL RM_0 RAW SET

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		W-0	W-0	W-0	W-0	W-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
W-0	W-0	W-0	W-0	W-0	W-0	W-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
W-0	W-0	W-0	W-0	W-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
W-0	W-0	W-0	W-0	W-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-878. AIL RM_0 RAW SET Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
24	LOF_STATE	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
23	HFNSYNC_STATE	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
22	LOF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
21	LOS_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
20	RCVD_RST	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
19	RCVD_SDI	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
18	RCVD_RAI	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
17	RCVD_LOF	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
16	RCVD_LOS	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
15	RX_FIFO_OVF	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
14	LOC_DET	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
13	K30P7_DET	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
12	MISSING_K28P7	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
11	MISSING_K28P5	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

Table 8-878. AIL RM_0 RAW SET Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
9	FRAME_BNDRY_DET	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
8	LCV_DET	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
7	NUM_LOS_DET	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
6	RM_STATUS_STATE5	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
5	RM_STATUS_STATE4	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	RM_STATUS_STATE3	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	RM_STATUS_STATE2	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	RM_STATUS_STATE1	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	RM_STATUS_STATE0	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SYNC_STATUS_CHANGE	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.51.3 AIL RM_0 RAW CLEAR [Address = 0x3_4008]

Raw Clear

Figure 8-774. AIL RM_0 RAW CLEAR

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		W-0	W-0	W-0	W-0	W-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
W-0	W-0	W-0	W-0	W-0	W-0	W-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
W-0	W-0	W-0	W-0	W-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
W-0	W-0	W-0	W-0	W-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-879. AIL RM_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
24	LOF_STATE	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
23	HFNSYNC_STATE	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
22	LOF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
21	LOS_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
20	RCVD_RST	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
19	RCVD_SDI	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
18	RCVD_RAI	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
17	RCVD_LOF	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
16	RCVD_LOS	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
15	RX_FIFO_OVF	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
14	LOC_DET	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
13	K30P7_DET	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
12	MISSING_K28P7	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
11	MISSING_K28P5	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

Table 8-879. AIL RM_0 RAW CLEAR Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
9	FRAME_BNDRY_DET	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
8	LCV_DET	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
7	NUM_LOS_DET	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
6	RM_STATUS_STATE5	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
5	RM_STATUS_STATE4	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	RM_STATUS_STATE3	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	RM_STATUS_STATE2	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	RM_STATUS_STATE1	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	RM_STATUS_STATE0	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SYNC_STATUS_CHANGE	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.51.4 AIL RM_0 EV0 ENABLE STATUS [Address = 0x3_400C]

EV0 Enable Status

Figure 8-775. AIL RM_0 EV0 ENABLE STATUS

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		R-0	R-0	R-0	R-0	R-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
R-0	R-0	R-0	R-0	R-0	R-0	R-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
R-0	R-0	R-0	R-0	R-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
R-0	R-0	R-0	R-0	R-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-880. AIL RM_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
24	LOF_STATE	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
23	HFNSYNC_STATE	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
22	LOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
21	LOS_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
20	RCVD_RST	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
19	RCVD_SDI	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
18	RCVD_RAI	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
17	RCVD_LOF	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
16	RCVD_LOS	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
15	RX_FIFO_OVF	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
14	LOC_DET	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
13	K30P7_DET	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
12	MISSING_K28P7	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
11	MISSING_K28P5	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

Table 8-880. AIL RM_0 EV0 ENABLE STATUS Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
9	FRAME_BNDRY_DET	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
8	LCV_DET	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
7	NUM_LOS_DET	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
6	RM_STATUS_STATE5	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
5	RM_STATUS_STATE4	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	RM_STATUS_STATE3	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	RM_STATUS_STATE2	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	RM_STATUS_STATE1	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	RM_STATUS_STATE0	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SYNC_STATUS_CHANGE	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.51.5 AIL RM_0 EV0 ENABLE SET [Address = 0x3_4010]

EV0 Enable Set

Figure 8-776. AIL RM_0 EV0 ENABLE SET

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		W-0	W-0	W-0	W-0	W-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
W-0	W-0	W-0	W-0	W-0	W-0	W-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
W-0	W-0	W-0	W-0	W-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
W-0	W-0	W-0	W-0	W-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-881. AIL RM_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	Sets the corresponding bit in the enable register when set. Write only, self-clears.
24	LOF_STATE	Sets the corresponding bit in the enable register when set. Write only, self-clears.
23	HFNSYNC_STATE	Sets the corresponding bit in the enable register when set. Write only, self-clears.
22	LOF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
21	LOS_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
20	RCVD_RST	Sets the corresponding bit in the enable register when set. Write only, self-clears.
19	RCVD_SDI	Sets the corresponding bit in the enable register when set. Write only, self-clears.
18	RCVD_RAI	Sets the corresponding bit in the enable register when set. Write only, self-clears.
17	RCVD_LOF	Sets the corresponding bit in the enable register when set. Write only, self-clears.
16	RCVD_LOS	Sets the corresponding bit in the enable register when set. Write only, self-clears.
15	RX_FIFO_OVF	Sets the corresponding bit in the enable register when set. Write only, self-clears.
14	LOC_DET	Sets the corresponding bit in the enable register when set. Write only, self-clears.
13	K30P7_DET	Sets the corresponding bit in the enable register when set. Write only, self-clears.
12	MISSING_K28P7	Sets the corresponding bit in the enable register when set. Write only, self-clears.
11	MISSING_K28P5	Sets the corresponding bit in the enable register when set. Write only, self-clears.
10	BLOCK_BNDRY_DET	Sets the corresponding bit in the enable register when set. Write only, self-clears.
9	FRAME_BNDRY_DET	Sets the corresponding bit in the enable register when set. Write only, self-clears.
8	LCV_DET	Sets the corresponding bit in the enable register when set. Write only, self-clears.
7	NUM_LOS_DET	Sets the corresponding bit in the enable register when set. Write only, self-clears.
6	RM_STATUS_STATE5	Sets the corresponding bit in the enable register when set. Write only, self-clears.
5	RM_STATUS_STATE4	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	RM_STATUS_STATE3	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	RM_STATUS_STATE2	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	RM_STATUS_STATE1	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	RM_STATUS_STATE0	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SYNC_STATUS_CHANGE	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.51.6 AIL RM_0 EV0 ENABLE CLEAR [Address = 0x3_4014]

EV0 Enable Clear

Figure 8-777. AIL RM_0 EV0 ENABLE CLEAR

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		W-0	W-0	W-0	W-0	W-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
W-0	W-0	W-0	W-0	W-0	W-0	W-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
W-0	W-0	W-0	W-0	W-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
W-0	W-0	W-0	W-0	W-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-882. AIL RM_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	Clears the corresponding bit in the enable register when set. Write only, self-clears.
24	LOF_STATE	Clears the corresponding bit in the enable register when set. Write only, self-clears.
23	HFNSYNC_STATE	Clears the corresponding bit in the enable register when set. Write only, self-clears.
22	LOF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
21	LOS_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
20	RCVD_RST	Clears the corresponding bit in the enable register when set. Write only, self-clears.
19	RCVD_SDI	Clears the corresponding bit in the enable register when set. Write only, self-clears.
18	RCVD_RAI	Clears the corresponding bit in the enable register when set. Write only, self-clears.
17	RCVD_LOF	Clears the corresponding bit in the enable register when set. Write only, self-clears.
16	RCVD_LOS	Clears the corresponding bit in the enable register when set. Write only, self-clears.
15	RX_FIFO_OVF	Clears the corresponding bit in the enable register when set. Write only, self-clears.
14	LOC_DET	Clears the corresponding bit in the enable register when set. Write only, self-clears.
13	K30P7_DET	Clears the corresponding bit in the enable register when set. Write only, self-clears.
12	MISSING_K28P7	Clears the corresponding bit in the enable register when set. Write only, self-clears.
11	MISSING_K28P5	Clears the corresponding bit in the enable register when set. Write only, self-clears.
10	BLOCK_BNDRY_DET	Clears the corresponding bit in the enable register when set. Write only, self-clears.
9	FRAME_BNDRY_DET	Clears the corresponding bit in the enable register when set. Write only, self-clears.
8	LCV_DET	Clears the corresponding bit in the enable register when set. Write only, self-clears.
7	NUM_LOS_DET	Clears the corresponding bit in the enable register when set. Write only, self-clears.
6	RM_STATUS_STATE5	Clears the corresponding bit in the enable register when set. Write only, self-clears.
5	RM_STATUS_STATE4	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	RM_STATUS_STATE3	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	RM_STATUS_STATE2	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	RM_STATUS_STATE1	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	RM_STATUS_STATE0	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SYNC_STATUS_CHANGE	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.51.7 AIL RM_0 EV1 ENABLE STATUS [Address = 0x3_4018]

EV1 Enable Status

Figure 8-778. AIL RM_0 EV1 ENABLE STATUS

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		R-0	R-0	R-0	R-0	R-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
R-0	R-0	R-0	R-0	R-0	R-0	R-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
R-0	R-0	R-0	R-0	R-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
R-0	R-0	R-0	R-0	R-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-883. AIL RM_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
24	LOF_STATE	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
23	HFNSYNC_STATE	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
22	LOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
21	LOS_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
20	RCVD_RST	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
19	RCVD_SDI	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
18	RCVD_RAI	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
17	RCVD_LOF	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
16	RCVD_LOS	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
15	RX_FIFO_OVF	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
14	LOC_DET	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
13	K30P7_DET	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
12	MISSING_K28P7	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
11	MISSING_K28P5	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

Table 8-883. AIL RM_0 EV1 ENABLE STATUS Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
9	FRAME_BNDRY_DET	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
8	LCV_DET	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
7	NUM_LOS_DET	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
6	RM_STATUS_STATE5	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
5	RM_STATUS_STATE4	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	RM_STATUS_STATE3	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	RM_STATUS_STATE2	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	RM_STATUS_STATE1	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	RM_STATUS_STATE0	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SYNC_STATUS_CHANGE	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.51.8 AIL RM_0 EV1 ENABLE SET [Address = 0x3_401C]

EV1 Enable Set

Figure 8-779. AIL RM_0 EV1 ENABLE SET

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		W-0	W-0	W-0	W-0	W-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
W-0	W-0	W-0	W-0	W-0	W-0	W-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
W-0	W-0	W-0	W-0	W-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
W-0	W-0	W-0	W-0	W-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-884. AIL RM_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
24	LOF_STATE	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
23	HFNSYNC_STATE	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
22	LOF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
21	LOS_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	RCVD_RST	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
19	RCVD_SDI	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
18	RCVD_RAI	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
17	RCVD_LOF	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
16	RCVD_LOS	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
15	RX_FIFO_OVF	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
14	LOC_DET	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
13	K30P7_DET	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
12	MISSING_K28P7	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
11	MISSING_K28P5	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

Table 8-884. AIL RM_0 EV1 ENABLE SET Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
9	FRAME_BNDRY_DET	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
8	LCV_DET	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	NUM_LOS_DET	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
6	RM_STATUS_STATE5	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
5	RM_STATUS_STATE4	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	RM_STATUS_STATE3	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	RM_STATUS_STATE2	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	RM_STATUS_STATE1	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	RM_STATUS_STATE0	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SYNC_STATUS_CHANGE	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.51.9 AIL RM_0 EV1 ENABLE CLEAR [Address = 0x3_4020]

EV1 Enable Clear

Figure 8-780. AIL RM_0 EV1 ENABLE CLEAR

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		W-0	W-0	W-0	W-0	W-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
W-0	W-0	W-0	W-0	W-0	W-0	W-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
W-0	W-0	W-0	W-0	W-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
W-0	W-0	W-0	W-0	W-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-885. AIL RM_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
24	LOF_STATE	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
23	HFNSYNC_STATE	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
22	LOF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
21	LOS_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	RCVD_RST	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
19	RCVD_SDI	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
18	RCVD_RAI	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
17	RCVD_LOF	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
16	RCVD_LOS	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
15	RX_FIFO_OVF	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
14	LOC_DET	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
13	K30P7_DET	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
12	MISSING_K28P7	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
11	MISSING_K28P5	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

Table 8-885. AIL RM_0 EV1 ENABLE CLEAR Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
9	FRAME_BNDRY_DET	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
8	LCV_DET	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	NUM_LOS_DET	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
6	RM_STATUS_STATE5	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
5	RM_STATUS_STATE4	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	RM_STATUS_STATE3	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	RM_STATUS_STATE2	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	RM_STATUS_STATE1	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	RM_STATUS_STATE0	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SYNC_STATUS_CHANGE	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.51.10 AIL RM_0 EV0 ENABLED STATUS [Address = 0x3_4024]

EV0 Enabled Status

Figure 8-781. AIL RM_0 EV0 ENABLED STATUS

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		R-0	R-0	R-0	R-0	R-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
R-0	R-0	R-0	R-0	R-0	R-0	R-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
R-0	R-0	R-0	R-0	R-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
R-0	R-0	R-0	R-0	R-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-886. AIL RM_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
24	LOF_STATE	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
23	HFNSYNC_STATE	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
22	LOF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
21	LOS_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
20	RCVD_RST	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
19	RCVD_SDI	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
18	RCVD_RAI	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
17	RCVD_LOF	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
16	RCVD_LOS	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
15	RX_FIFO_OVF	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
14	LOC_DET	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
13	K30P7_DET	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
12	MISSING_K28P7	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
11	MISSING_K28P5	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

Table 8-886. AIL RM_0 EV0 ENABLED STATUS Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
9	FRAME_BNDRY_DET	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
8	LCV_DET	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
7	NUM_LOS_DET	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
6	RM_STATUS_STATE5	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
5	RM_STATUS_STATE4	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	RM_STATUS_STATE3	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	RM_STATUS_STATE2	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	RM_STATUS_STATE1	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	RM_STATUS_STATE0	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SYNC_STATUS_CHANGE	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.51.11 AIL RM_0 EV1 ENABLED STATUS [Address = 0x3_4028]

EV1 Enabled Status

Figure 8-782. AIL RM_0 EV1 ENABLED STATUS

31	26	25	24	23	22	21
Reserved		RM_RST	LOF_STATE	HFNSYNC_STATE	LOF_ERR	LOS_ERR
NA-0		R-0	R-0	R-0	R-0	R-0

20	19	18	17	16	15	14
RCVD_RST	RCVD_SDI	RCVD_RAI	RCVD_LOF	RCVD_LOS	RX_FIFO_OVF	LOC_DET
R-0	R-0	R-0	R-0	R-0	R-0	R-0

13	12	11	10	9
K30P7_DET	MISSING_K28P7	MISSING_K28P5	BLOCK_BNDRY_DET	FRAME_BNDRY_DET
R-0	R-0	R-0	R-0	R-0

8	7	6	5	4
LCV_DET	NUM_LOS_DET	RM_STATUS_STATE5	RM_STATUS_STATE4	RM_STATUS_STATE3
R-0	R-0	R-0	R-0	R-0

3	2	1	0
RM_STATUS_STATE2	RM_STATUS_STATE1	RM_STATUS_STATE0	SYNC_STATUS_CHANGE
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-887. AIL RM_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-26	Reserved	Reserved.
25	RM_RST	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
24	LOF_STATE	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
23	HFNSYNC_STATE	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
22	LOF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
21	LOS_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
20	RCVD_RST	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
19	RCVD_SDI	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
18	RCVD_RAI	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
17	RCVD_LOF	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
16	RCVD_LOS	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
15	RX_FIFO_OVF	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
14	LOC_DET	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
13	K30P7_DET	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
12	MISSING_K28P7	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
11	MISSING_K28P5	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

Table 8-887. AIL RM_0 EV1 ENABLED STATUS Field Descriptions (continued)

Bits	Name	Description
10	BLOCK_BNDRY_DET	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
9	FRAME_BNDRY_DET	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
8	LCV_DET	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
7	NUM_LOS_DET	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
6	RM_STATUS_STATE5	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
5	RM_STATUS_STATE4	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	RM_STATUS_STATE3	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	RM_STATUS_STATE2	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	RM_STATUS_STATE1	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	RM_STATUS_STATE0	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SYNC_STATUS_CHANGE	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.51.12 AIL RT_TM_0 RAW INTERRUPT STATUS [Address = 0x3_402C]

AIL RT and TM error register.

Figure 8-783. AIL RT_TM_0 RAW INTERRUPT STATUS

31–22	21	20	19	18
Reserved	TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0	R-0	R-0	R-0	R-0

17	16	15–10	9–6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved	RT_AGGR_STATE_INFO
R-0	R-0	NA-0	R-0

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-888. AIL RT_TM_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	TM Failure indicates that the tm has forced the upstream logic to flush data buffers and resynchronize to a new frame boundary.
20	FIFO_UNDEFLOW	TM Fifo underflowed.
19	FRAME_MISALIGN	TM detected a frame misalignment in the signal it receives from the CO.
18	DELTA_MODIFIED	TM detected that the frame strobe from the micro-at was received earlier than expected.
17	DELTA_INACTIVE	TM detected that the frame strobe from the micro-at seems inactive compared to the Tx state machine and link configuration.
16	SYNC_STATUS_CHANGE	TM detected a change in sync status. The actual frame status can be found in the TM status register
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	RT aggregation state info bit 0 = aggr_init, bit 1 = aggr_pe, bit 2 = aggr_rm, bit 3 = aggr_pe_rm.
5	RT_UNALIGN_ERR	RT detected the alignment window is too large in RE ULNK mode.
4	RT_FRM_ERR	RT detected a framing error from either the CI input or the PE input.
3	RT_OVFL	RT FIFO Overflow.
2	RT_UNFL	RT FIFO Underflow.
1	RT_EM_INSERT	RT inserted an empty message.
0	RT_HDR_ERROR	RT detected an error in the header.

8.6.51.13 AIL RT_TM_0 RAW SET [Address = 0x3_4030]

Raw Set

Figure 8-784. AIL RT_TM_0 RAW SET

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		W-0	W-0	W-0	W-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
W-0	W-0	NA-0		W-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
W-0	W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-889. AIL RT_TM_0 RAW SET Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
20	FIFO_UNDEFLOW	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
19	FRAME_MISALIGN	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
18	DELTA_MODIFIED	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
17	DELTA_INACTIVE	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
16	SYNC_STATUS_CHANGE	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
5	RT_UNALIGN_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	RT_FRM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	RT_OVFL	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	RT_UNFL	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	RT_EM_INSERT	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	RT_HDR_ERROR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.51.14 AIL RT_TM_0 RAW CLEAR [Address = 0x3_4034]

Raw Clear

Figure 8-785. AIL RT_TM_0 RAW CLEAR

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		W-0	W-0	W-0	W-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
W-0	W-0	NA-0		W-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
W-0	W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-890. AIL RT_TM_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
20	FIFO_UNDEFLOW	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
19	FRAME_MISALIGN	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
18	DELTA_MODIFIED	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
17	DELTA_INACTIVE	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
16	SYNC_STATUS_CHANGE	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
5	RT_UNALIGN_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	RT_FRM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	RT_OVFL	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	RT_UNFL	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	RT_EM_INSERT	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	RT_HDR_ERROR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.51.15 AIL RT_TM_0 EV0 ENABLE STATUS [Address = 0x3_4038]

EV0 Enable Status

Figure 8-786. AIL RT_TM_0 EV0 ENABLE STATUS

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		R-0	R-0	R-0	R-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
R-0	R-0	NA-0		R-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-891. AIL RT_TM_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
20	FIFO_UNDEFLOW	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
19	FRAME_MISALIGN	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
18	DELTA_MODIFIED	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
17	DELTA_INACTIVE	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
16	SYNC_STATUS_CHANGE	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
5	RT_UNALIGN_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	RT_FRM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	RT_OVFL	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	RT_UNFL	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	RT_EM_INSERT	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	RT_HDR_ERROR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.51.16 AIL RT_TM_0 EV0 ENABLE SET [Address = 0x3_403C]

EV0 Enable Set

Figure 8-787. AIL RT_TM_0 EV0 ENABLE SET

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		W-0	W-0	W-0	W-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
W-0	W-0	NA-0		W-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
W-0	W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-892. AIL RT_TM_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	Sets the corresponding bit in the enable register when set. Write only, self-clears.
20	FIFO_UNDEFLOW	Sets the corresponding bit in the enable register when set. Write only, self-clears.
19	FRAME_MISALIGN	Sets the corresponding bit in the enable register when set. Write only, self-clears.
18	DELTA_MODIFIED	Sets the corresponding bit in the enable register when set. Write only, self-clears.
17	DELTA_INACTIVE	Sets the corresponding bit in the enable register when set. Write only, self-clears.
16	SYNC_STATUS_CHANGE	Sets the corresponding bit in the enable register when set. Write only, self-clears.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
5	RT_UNALIGN_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	RT_FRM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	RT_OVFL	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	RT_UNFL	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	RT_EM_INSERT	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	RT_HDR_ERROR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.51.17 AIL RT_TM_0 EV0 ENABLE CLEAR [Address = 0x3_4040]

EV0 Enable Clear

Figure 8-788. AIL RT_TM_0 EV0 ENABLE CLEAR

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		W-0	W-0	W-0	W-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
W-0	W-0	NA-0		W-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
W-0	W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-893. AIL RT_TM_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	Clears the corresponding bit in the enable register when set. Write only, self-clears.
20	FIFO_UNDEFLOW	Clears the corresponding bit in the enable register when set. Write only, self-clears.
19	FRAME_MISALIGN	Clears the corresponding bit in the enable register when set. Write only, self-clears.
18	DELTA_MODIFIED	Clears the corresponding bit in the enable register when set. Write only, self-clears.
17	DELTA_INACTIVE	Clears the corresponding bit in the enable register when set. Write only, self-clears.
16	SYNC_STATUS_CHANGE	Clears the corresponding bit in the enable register when set. Write only, self-clears.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
5	RT_UNALIGN_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	RT_FRM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	RT_OVFL	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	RT_UNFL	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	RT_EM_INSERT	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	RT_HDR_ERROR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.51.18 AIL RT_TM_0 EV1 ENABLE STATUS [Address = 0x3_4044]

EV1 Enable Status

Figure 8-789. AIL RT_TM_0 EV1 ENABLE STATUS

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		R-0	R-0	R-0	R-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
R-0	R-0	NA-0		R-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-894. AIL RT_TM_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
20	FIFO_UNDEFLOW	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
19	FRAME_MISALIGN	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
18	DELTA_MODIFIED	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
17	DELTA_INACTIVE	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
16	SYNC_STATUS_CHANGE	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
5	RT_UNALIGN_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	RT_FRM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	RT_OVFL	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	RT_UNFL	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	RT_EM_INSERT	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	RT_HDR_ERROR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.51.19 AIL RT_TM_0 EV1 ENABLE SET [Address = 0x3_4048]

EV1 Enable Set

Figure 8-790. AIL RT_TM_0 EV1 ENABLE SET

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		W-0	W-0	W-0	W-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
W-0	W-0	NA-0		W-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
W-0	W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-895. AIL RT_TM_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	FIFO_UNDEFLOW	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
19	FRAME_MISALIGN	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
18	DELTA_MODIFIED	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
17	DELTA_INACTIVE	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
16	SYNC_STATUS_CHANGE	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
5	RT_UNALIGN_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	RT_FRM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	RT_OVFL	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	RT_UNFL	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	RT_EM_INSERT	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	RT_HDR_ERROR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.51.20 AIL RT_TM_0 EV1 ENABLE CLEAR [Address = 0x3_404C]

EV1 Enable Clear

Figure 8-791. AIL RT_TM_0 EV1 ENABLE CLEAR

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		W-0	W-0	W-0	W-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
W-0	W-0	NA-0		W-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
W-0	W-0	W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-896. AIL RT_TM_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	FIFO_UNDEFLOW	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
19	FRAME_MISALIGN	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
18	DELTA_MODIFIED	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
17	DELTA_INACTIVE	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
16	SYNC_STATUS_CHANGE	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
5	RT_UNALIGN_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	RT_FRM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	RT_OVFL	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	RT_UNFL	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	RT_EM_INSERT	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	RT_HDR_ERROR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.51.21 AIL RT_TM_0 EV0 ENABLED STATUS [Address = 0x3_4050]

EV0 Enabled Status

Figure 8-792. AIL RT_TM_0 EV0 ENABLED STATUS

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		R-0	R-0	R-0	R-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
R-0	R-0	NA-0		R-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-897. AIL RT_TM_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
20	FIFO_UNDEFLOW	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
19	FRAME_MISALIGN	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
18	DELTA_MODIFIED	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
17	DELTA_INACTIVE	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
16	SYNC_STATUS_CHANGE	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
5	RT_UNALIGN_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	RT_FRM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	RT_OVFL	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	RT_UNFL	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	RT_EM_INSERT	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	RT_HDR_ERROR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.51.22 AIL RT_TM_0 EV1 ENABLED STATUS [Address = 0x3_4054]

EV1 Enabled Status

Figure 8-793. AIL RT_TM_0 EV1 ENABLED STATUS

31	22	21	20	19	18
Reserved		TM_FAIL	FIFO_UNDEFLOW	FRAME_MISALIGN	DELTA_MODIFIED
NA-0		R-0	R-0	R-0	R-0

17	16	15	10	9	6
DELTA_INACTIVE	SYNC_STATUS_CHANGE	Reserved		RT_AGGR_STATE_INFO	
R-0	R-0	NA-0		R-0	

5	4	3	2	1	0
RT_UNALIGN_ERR	RT_FRM_ERR	RT_OVFL	RT_UNFL	RT_EM_INSERT	RT_HDR_ERROR
R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-898. AIL RT_TM_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	TM_FAIL	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
20	FIFO_UNDEFLOW	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
19	FRAME_MISALIGN	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
18	DELTA_MODIFIED	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
17	DELTA_INACTIVE	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
16	SYNC_STATUS_CHANGE	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
15-10	Reserved	Reserved.
9-6	RT_AGGR_STATE_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
5	RT_UNALIGN_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	RT_FRM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	RT_OVFL	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	RT_UNFL	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	RT_EM_INSERT	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	RT_HDR_ERROR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.51.23 AIL CI_CO_0 RAW INTERRUPT STATUS [Address = 0x3_4058]

AIL CI and CO error register.

Figure 8-794. AIL CI_CO_0 RAW INTERRUPT STATUS

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-899. AIL CI_CO_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	CO AXC Group LUT requested more containers transferred in a basic frame than can fit.
0	CI_TBLTOOLONG	CI AXC Group LUT requested more containers transferred in a basic frame than can fit.

8.6.51.24 AIL CI_CO_0 RAW SET [Address = 0x3_405C]

Raw Set

Figure 8-795. AIL CI_CO_0 RAW SET

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-900. AIL CI_CO_0 RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	CI_TBLTOOLONG	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.51.25 AIL CI_CO_0 RAW CLEAR [Address = 0x3_4060]

Raw Clear

Figure 8-796. AIL CI_CO_0 RAW CLEAR

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-901. AIL CI_CO_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	CI_TBLTOOLONG	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.51.26 AIL CI_CO_0 EV0 ENABLE STATUS [Address = 0x3_4064]

EV0 Enable Status

Figure 8-797. AIL CI_CO_0 EV0 ENABLE STATUS

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-902. AIL CI_CO_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	CI_TBLTOOLONG	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.51.27 AIL CI_CO_0 EV0 ENABLE SET [Address = 0x3_4068]

EV0 Enable Set

Figure 8-798. AIL CI_CO_0 EV0 ENABLE SET

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-903. AIL CI_CO_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	CI_TBLTOOLONG	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.51.28 AIL CI_CO_0 EV0 ENABLE CLEAR [Address = 0x3_406C]

EV0 Enable Clear

Figure 8-799. AIL CI_CO_0 EV0 ENABLE CLEAR

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-904. AIL CI_CO_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	CI_TBLTOOLONG	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.51.29 AIL CI_CO_0 EV1 ENABLE STATUS [Address = 0x3_4070]

EV1 Enable Status

Figure 8-800. AIL CI_CO_0 EV1 ENABLE STATUS

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-905. AIL CI_CO_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	CI_TBLTOOLONG	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.51.30 AIL CI_CO_0 EV1 ENABLE SET [Address = 0x3_4074]

EV1 Enable Set

Figure 8-801. AIL CI_CO_0 EV1 ENABLE SET

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-906. AIL CI_CO_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	CI_TBLTOOLONG	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.51.31 AIL CI_CO_0 EV1 ENABLE CLEAR [Address = 0x3_4078]

EV1 Enable Clear

Figure 8-802. AIL CI_CO_0 EV1 ENABLE CLEAR

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-907. AIL CI_CO_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	CI_TBLTOOLONG	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.51.32 AIL CI_CO_0 EV0 ENABLED STATUS [Address = 0x3_407C]

EV0 Enabled Status

Figure 8-803. AIL CI_CO_0 EV0 ENABLED STATUS

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-908. AIL CI_CO_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	CI_TBLTOOLONG	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.51.33 AIL CI_CO_0 EV1 ENABLED STATUS [Address = 0x3_4080]

EV1 Enabled Status

Figure 8-804. AIL CI_CO_0 EV1 ENABLED STATUS

31	2	1	0
Reserved		CO_TBLTOOLONG	CI_TBLTOOLONG
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-909. AIL CI_CO_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	CO_TBLTOOLONG	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	CI_TBLTOOLONG	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.51.34 AIL SYSCLK_PHY_ORIG_REG [Address = 0x3_4084]

This is the sysclk origination register indicating which interrupt register group caused the interrupt.

Figure 8-805. AIL SYSCLK_PHY_ORIG_REG

31	3	2	1	0
Reserved		ORIG_EE_2	ORIG_EE_1	ORIG_EE_0
NA-0		R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-910. AIL SYSCLK_PHY_ORIG_REG Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2	ORIG_EE_2	If set a bit is set in the ci_co_0 register.
1	ORIG_EE_1	If set a bit is set in the rt_tm_0 register.
0	ORIG_EE_0	If set a bit is set in the rm_0 register.

8.6.52 AIL_IQN_AIL_EE_SYSCLK_EE [Address = 0x3_4800]

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE

Offset	Acronym	Register Description	Section
0x3_4800	AIL PD_0 RAW INTERRUPT STATUS	AIL PD error register.	Section 8.6.52.1
0x3_4804	AIL PD_0 RAW SET	Raw Set	Section 8.6.52.2
0x3_4808	AIL PD_0 RAW CLEAR	Raw Clear	Section 8.6.52.3
0x3_480C	AIL PD_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.4
0x3_4810	AIL PD_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.5
0x3_4814	AIL PD_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.6
0x3_4818	AIL PD_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.7
0x3_481C	AIL PD_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.8
0x3_4820	AIL PD_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.9
0x3_4824	AIL PD_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.10
0x3_4828	AIL PD_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.11
0x3_482C	AIL PD_1 RAW INTERRUPT STATUS	AIL PD error register.	Section 8.6.52.12
0x3_4830	AIL PD_1 RAW SET	Raw Set	Section 8.6.52.13
0x3_4834	AIL PD_1 RAW CLEAR	Raw Clear	Section 8.6.52.14
0x3_4838	AIL PD_1 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.15
0x3_483C	AIL PD_1 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.16
0x3_4840	AIL PD_1 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.17
0x3_4844	AIL PD_1 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.18
0x3_4848	AIL PD_1 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.19
0x3_484C	AIL PD_1 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.20
0x3_4850	AIL PD_1 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.21
0x3_4854	AIL PD_1 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.22

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_4858	AIL PD_2_0 RAW INTERRUPT STATUS	AIL PD error register.	Section 8.6.52.23
0x3_485C	AIL PD_2_0 RAW SET	Raw Set	Section 8.6.52.24
0x3_4860	AIL PD_2_0 RAW CLEAR	Raw Clear	Section 8.6.52.25
0x3_4864	AIL PD_2_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.26
0x3_4868	AIL PD_2_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.27
0x3_486C	AIL PD_2_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.28
0x3_4870	AIL PD_2_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.29
0x3_4874	AIL PD_2_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.30
0x3_4878	AIL PD_2_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.31
0x3_487C	AIL PD_2_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.32
0x3_4880	AIL PD_2_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.33
0x3_4884	AIL PD_2_1 RAW INTERRUPT STATUS	AIL PD error register.	Section 8.6.52.34
0x3_4888	AIL PD_2_1 RAW SET	Raw Set	Section 8.6.52.35
0x3_488C	AIL PD_2_1 RAW CLEAR	Raw Clear	Section 8.6.52.36
0x3_4890	AIL PD_2_1 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.37
0x3_4894	AIL PD_2_1 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.38
0x3_4898	AIL PD_2_1 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.39
0x3_489C	AIL PD_2_1 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.40
0x3_48A0	AIL PD_2_1 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.41
0x3_48A4	AIL PD_2_1 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.42

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_48A8	AIL PD_2_1 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.43
0x3_48AC	AIL PD_2_1 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.44
0x3_4908	AIL PE_0 RAW INTERRUPT STATUS	AIL PE error register.	Section 8.6.52.45
0x3_490C	AIL PE_0 RAW SET	Raw Set	Section 8.6.52.46
0x3_4910	AIL PE_0 RAW CLEAR	Raw Clear	Section 8.6.52.47
0x3_4914	AIL PE_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.48
0x3_4918	AIL PE_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.49
0x3_491C	AIL PE_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.50
0x3_4920	AIL PE_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.51
0x3_4924	AIL PE_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.52
0x3_4928	AIL PE_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.53
0x3_492C	AIL PE_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.54
0x3_4930	AIL PE_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.55
0x3_4934	AIL AIL_SI_0 RAW INTERRUPT STATUS	AIL uAT and SI_AIL_PE_SCH error register.	Section 8.6.52.56
0x3_4938	AIL AIL_SI_0 RAW SET	Raw Set	Section 8.6.52.57
0x3_493C	AIL AIL_SI_0 RAW CLEAR	Raw Clear	Section 8.6.52.58
0x3_4940	AIL AIL_SI_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.59
0x3_4944	AIL AIL_SI_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.60
0x3_4948	AIL AIL_SI_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.61
0x3_494C	AIL AIL_SI_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.62

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_4950	AIL AIL_SI_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.63
0x3_4954	AIL AIL_SI_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.64
0x3_4958	AIL AIL_SI_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.65
0x3_495C	AIL AIL_SI_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.66
0x3_4960	AIL EE_SII_A RAW INTERRUPT STATUS	SI si_i IQ errors and info.	Section 8.6.52.67
0x3_4964	AIL EE_SII_A RAW SET	Raw Set	Section 8.6.52.68
0x3_4968	AIL EE_SII_A RAW CLEAR	Raw Clear	Section 8.6.52.69
0x3_496C	AIL EE_SII_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.70
0x3_4970	AIL EE_SII_A EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.71
0x3_4974	AIL EE_SII_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.72
0x3_4978	AIL EE_SII_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.73
0x3_497C	AIL EE_SII_A EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.74
0x3_4980	AIL EE_SII_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.75
0x3_4984	AIL EE_SII_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.76
0x3_4988	AIL EE_SII_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.77
0x3_498C	AIL EE_SII_B RAW INTERRUPT STATUS	SI si_i CTL errors and info.	Section 8.6.52.78
0x3_4990	AIL EE_SII_B RAW SET	Raw Set	Section 8.6.52.79
0x3_4994	AIL EE_SII_B RAW CLEAR	Raw Clear	Section 8.6.52.80
0x3_4998	AIL EE_SII_B EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.81
0x3_499C	AIL EE_SII_B EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.82

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_49A0	AIL EE_SII_B EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.83
0x3_49A4	AIL EE_SII_B EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.84
0x3_49A8	AIL EE_SII_B EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.85
0x3_49AC	AIL EE_SII_B EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.86
0x3_49B0	AIL EE_SII_B EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.87
0x3_49B4	AIL EE_SII_B EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.88
0x3_49B8	AIL EE_SII_C_0 RAW INTERRUPT STATUS	SI si_i IQ per-channel start of frame errors	Section 8.6.52.89
0x3_49BC	AIL EE_SII_C_0 RAW SET	Raw Set	Section 8.6.52.90
0x3_49C0	AIL EE_SII_C_0 RAW CLEAR	Raw Clear	Section 8.6.52.91
0x3_49C4	AIL EE_SII_C_0 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.92
0x3_49C8	AIL EE_SII_C_0 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.93
0x3_49CC	AIL EE_SII_C_0 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.94
0x3_49D0	AIL EE_SII_C_0 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.95
0x3_49D4	AIL EE_SII_C_0 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.96
0x3_49D8	AIL EE_SII_C_0 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.97
0x3_49DC	AIL EE_SII_C_0 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.98
0x3_49E0	AIL EE_SII_C_0 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.99
0x3_49E4	AIL EE_SII_C_1 RAW INTERRUPT STATUS	SI si_i IQ per-channel start of frame errors	Section 8.6.52.100
0x3_49E8	AIL EE_SII_C_1 RAW SET	Raw Set	Section 8.6.52.101
0x3_49EC	AIL EE_SII_C_1 RAW CLEAR	Raw Clear	Section 8.6.52.102

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_49F0	AIL EE_SII_C_1 EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.103
0x3_49F4	AIL EE_SII_C_1 EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.104
0x3_49F8	AIL EE_SII_C_1 EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.105
0x3_49FC	AIL EE_SII_C_1 EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.106
0x3_4A00	AIL EE_SII_C_1 EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.107
0x3_4A04	AIL EE_SII_C_1 EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.108
0x3_4A08	AIL EE_SII_C_1 EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.109
0x3_4A0C	AIL EE_SII_C_1 EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.110
0x3_4A68	AIL EE_SII_D RAW INTERRUPT STATUS	SI si_i CTL per-channel SOP received from ICC info	Section 8.6.52.111
0x3_4A6C	AIL EE_SII_D RAW SET	Raw Set	Section 8.6.52.112
0x3_4A70	AIL EE_SII_D RAW CLEAR	Raw Clear	Section 8.6.52.113
0x3_4A74	AIL EE_SII_D EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.114
0x3_4A78	AIL EE_SII_D EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.115
0x3_4A7C	AIL EE_SII_D EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.116
0x3_4A80	AIL EE_SII_D EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.117
0x3_4A84	AIL EE_SII_D EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.118
0x3_4A88	AIL EE_SII_D EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.119
0x3_4A8C	AIL EE_SII_D EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.120
0x3_4A90	AIL EE_SII_D EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.121
0x3_4B18	AIL EE_SIE_A RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.6.52.122

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_4B1C	AIL EE_SIE_A RAW SET	Raw Set	Section 8.6.52.123
0x3_4B20	AIL EE_SIE_A RAW CLEAR	Raw Clear	Section 8.6.52.124
0x3_4B24	AIL EE_SIE_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.125
0x3_4B28	AIL EE_SIE_A EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.126
0x3_4B2C	AIL EE_SIE_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.127
0x3_4B30	AIL EE_SIE_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.128
0x3_4B34	AIL EE_SIE_A EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.129
0x3_4B38	AIL EE_SIE_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.130
0x3_4B3C	AIL EE_SIE_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.131
0x3_4B40	AIL EE_SIE_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.132
0x3_4B44	AIL EE_SIE_B RAW INTERRUPT STATUS	SI si_e CTL info.	Section 8.6.52.133
0x3_4B48	AIL EE_SIE_B RAW SET	Raw Set	Section 8.6.52.134
0x3_4B4C	AIL EE_SIE_B RAW CLEAR	Raw Clear	Section 8.6.52.135
0x3_4B50	AIL EE_SIE_B EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.136
0x3_4B54	AIL EE_SIE_B EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.137
0x3_4B58	AIL EE_SIE_B EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.138
0x3_4B5C	AIL EE_SIE_B EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.139
0x3_4B60	AIL EE_SIE_B EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.140
0x3_4B64	AIL EE_SIE_B EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.141
0x3_4B68	AIL EE_SIE_B EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.142

Table 8-911. AIL_IQN_AIL_EE_SYSCLK_EE (continued)

Offset	Acronym	Register Description	Section
0x3_4B6C	AIL EE_SIE_B EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.143
0x3_4B70	AIL EE_SIE_C RAW INTERRUPT STATUS	SI si_e CTL per-channel SOP transmitted to ICC	Section 8.6.52.144
0x3_4B74	AIL EE_SIE_C RAW SET	Raw Set	Section 8.6.52.145
0x3_4B78	AIL EE_SIE_C RAW CLEAR	Raw Clear	Section 8.6.52.146
0x3_4B7C	AIL EE_SIE_C EV0 ENABLE STATUS	EV0 Enable Status	Section 8.6.52.147
0x3_4B80	AIL EE_SIE_C EV0 ENABLE SET	EV0 Enable Set	Section 8.6.52.148
0x3_4B84	AIL EE_SIE_C EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.6.52.149
0x3_4B88	AIL EE_SIE_C EV1 ENABLE STATUS	EV1 Enable Status	Section 8.6.52.150
0x3_4B8C	AIL EE_SIE_C EV1 ENABLE SET	EV1 Enable Set	Section 8.6.52.151
0x3_4B90	AIL EE_SIE_C EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.6.52.152
0x3_4B94	AIL EE_SIE_C EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.6.52.153
0x3_4B98	AIL EE_SIE_C EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.6.52.154
0x3_4C20	AIL SYSCLK_ORIG_REG	This is the sysclk origination register indicating which interrupt register group caused the interrupt.	Section 8.6.52.155

8.6.52.1 AIL PD_0 RAW INTERRUPT STATUS [Address = 0x3_4800]

AIL PD error register.

Figure 8-806. AIL PD_0 RAW INTERRUPT STATUS

31	28	27	26
Reserved		PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0		R-0	R-0

25	24	23	22
PD_EE_OBSAI_SOP_INFO		Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
R-0		NA-0	R-0

21	20	19	16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR	
R-0	R-0	R-0	

15	11	10	9
Reserved		PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0		R-0	R-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
R-0	R-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
R-0	R-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
R-0	R-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-912. AIL PD_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	OBSAI, on any channel, an sof occurred from the PD.
26	PD_EE_OBSAI_EOP_INFO	OBSAI, on any channel, an eop occurred from the PD.
25	PD_EE_OBSAI_SOP_INFO	OBSAI, on any channel, an sop occurred from the PD.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	The CPRI CW 4B5B logic detected an illegal bit pattern. It could not determine what the correct character was.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	The CPRI CW 4B5B logic detected an EOP while not currently processing a packet.
20	PD_EE_CPRI_CW_OVFL_ERR	The CPRI CW Fifo for the channel has overflowed, indicating that it was not serviced fast enough.
19-16	PD_EE_CPRI_CW_CRC_ERR	When CPRI CW CRC checks are enabled, a CRC was received which did not match the calculated CRC. CRC failure could be caused by SERDES bit error -or- bad programming at either sender or receiver.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	OBSAI, a gsm off strobe was received for a channel.
9	PD_EE_RP3_01_CRC_FAIL_ERR	OBSAI, a remote rp3-01 message was recieved but the CRC failed for the message.
8	PD_EE_RP3_01_CAPTURE_INFO	OBSAI, a remote rp3-01 message was received as determined by the lut table.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	OBSAI, a received message failed to match entries for addr and type in the lut table.

Table 8-912. AIL PD_0 RAW INTERRUPT STATUS Field Descriptions (continued)

Bits	Name	Description
6	PD_EE_RP3_01_SOC_RST_INFO	OBSAI, received a remote RP3-01 message controlling the entire SOC to perform a HW reset. AIL port will strobe, Must be enabled at higher layers of SOC to perform actual RESET (similar function exists for CPRI, but controlled via PHY_RM)
5	PD_EE_OBSAI_CRC_ERR	OBSAI, ctrl packet crc failure, pkt marked as bad
4	PD_EE_OBSAI_AXC_FAIL_ERR	OBSAI, unrecoverable ts or wdog error, chan restart. Caused by missing or extra OBSAI messages. (OBSAI time stamp prediction failure)
3	PD_EE_OBSAI_TS_WDOG_ERR	OBSAI, watch dog timed out before chan received OBSAI msg.
2	PD_EE_OBSAI_TS_MISS_ERR	OBSAI, estra, single missing or double missing timestamp. (If this is the only failure, AxC will recover. If no recovery, pd_ee_obsai_axc_fail_err will fire next)
1	PD_EE_SOP_ERR	CPRI Received a second SOP without an EOP in between for 4B/5B. OBSAI Was in middle of packet but recieved TS violated protocol. Packet forced to EOP and ERROR (PD_Frame)
0	PD_EE_OBSAI_FRM_WIN_ERR	OBSAI timestamp failed timing window test. Wrap of the PD_Frame Counters did not predict a Radio Frame Boundary consistent with TS=0 falling within the reception timing window.

8.6.52.2 AIL PD_0 RAW SET [Address = 0x3_4804]

Raw Set

Figure 8-807. AIL PD_0 RAW SET

31–28	27	26
Reserved	PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0	W-0	W-0

25	24–23	22
PD_EE_OBSAI_SOP_INFO	Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
W-0	NA-0	W-0

21	20	19–16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR
W-0	W-0	W-0

15–11	10	9
Reserved	PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0	W-0	W-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
W-0	W-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
W-0	W-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
W-0	W-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-913. AIL PD_0 RAW SET Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
26	PD_EE_OBSAI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
25	PD_EE_OBSAI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
20	PD_EE_CPRI_CW_OVFL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
19-16	PD_EE_CPRI_CW_CRC_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
9	PD_EE_RP3_01_CRC_FAIL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

Table 8-913. AIL PD_0 RAW SET Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
6	PD_EE_RP3_01_SOC_RST_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
5	PD_EE_OBSAI_CRC_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	PD_EE_OBSAI_AXC_FAIL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	PD_EE_OBSAI_TS_WDOG_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	PD_EE_OBSAI_TS_MISS_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	PD_EE_SOP_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	PD_EE_OBSAI_FRM_WIN_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.3 AIL PD_0 RAW CLEAR [Address = 0x3_4808]

Raw Clear

Figure 8-808. AIL PD_0 RAW CLEAR

31–28	27	26
Reserved	PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0	W-0	W-0

25	24	23–22
PD_EE_OBSAI_SOP_INFO	Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
W-0	NA-0	W-0

21	20	19–16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR
W-0	W-0	W-0

15–11	10	9
Reserved	PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0	W-0	W-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
W-0	W-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
W-0	W-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
W-0	W-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-914. AIL PD_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
26	PD_EE_OBSAI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
25	PD_EE_OBSAI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
20	PD_EE_CPRI_CW_OVFL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
19-16	PD_EE_CPRI_CW_CRC_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
9	PD_EE_RP3_01_CRC_FAIL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

Table 8-914. AIL PD_0 RAW CLEAR Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
6	PD_EE_RP3_01_SOC_RST_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
5	PD_EE_OBSAI_CRC_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	PD_EE_OBSAI_AXC_FAIL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	PD_EE_OBSAI_TS_WDOG_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	PD_EE_OBSAI_TS_MISS_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	PD_EE_SOP_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	PD_EE_OBSAI_FRM_WIN_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.4 AIL PD_0 EV0 ENABLE STATUS [Address = 0x3_480C]

EV0 Enable Status

Figure 8-809. AIL PD_0 EV0 ENABLE STATUS

31–28	27	26
Reserved	PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0	R-0	R-0

25	24	23–22
PD_EE_OBSAI_SOP_INFO	Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
R-0	NA-0	R-0

21	20	19–16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR
R-0	R-0	R-0

15–11	10	9
Reserved	PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0	R-0	R-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
R-0	R-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
R-0	R-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
R-0	R-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-915. AIL PD_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
26	PD_EE_OBSAI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
25	PD_EE_OBSAI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
20	PD_EE_CPRI_CW_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
19-16	PD_EE_CPRI_CW_CRC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
9	PD_EE_RP3_01_CRC_FAIL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

Table 8-915. AIL PD_0 EV0 ENABLE STATUS Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
6	PD_EE_RP3_01_SOC_RST_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
5	PD_EE_OBSAI_CRC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	PD_EE_OBSAI_AXC_FAIL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	PD_EE_OBSAI_TS_WDOG_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	PD_EE_OBSAI_TS_MISS_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	PD_EE_SOP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	PD_EE_OBSAI_FRM_WIN_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.5 AIL PD_0 EV0 ENABLE SET [Address = 0x3_4810]

EV0 Enable Set

Figure 8-810. AIL PD_0 EV0 ENABLE SET

31–28	27	26
Reserved	PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0	W-0	W-0

25	24–23	22
PD_EE_OBSAI_SOP_INFO	Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
W-0	NA-0	W-0

21	20	19–16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR
W-0	W-0	W-0

15–11	10	9
Reserved	PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0	W-0	W-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
W-0	W-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
W-0	W-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
W-0	W-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-916. AIL PD_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
26	PD_EE_OBSAI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
25	PD_EE_OBSAI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
20	PD_EE_CPRI_CW_OVFL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
19-16	PD_EE_CPRI_CW_CRC_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
9	PD_EE_RP3_01_CRC_FAIL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
8	PD_EE_RP3_01_CAPTURE_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
6	PD_EE_RP3_01_SOC_RST_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
5	PD_EE_OBSAI_CRC_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	PD_EE_OBSAI_AXC_FAIL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	PD_EE_OBSAI_TS_WDOG_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	PD_EE_OBSAI_TS_MISS_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

Table 8-916. AIL PD_0 EV0 ENABLE SET Field Descriptions (continued)

Bits	Name	Description
1	PD_EE_SOP_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	PD_EE_OBSAI_FRM_WIN_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.6 AIL PD_0 EV0 ENABLE CLEAR [Address = 0x3_4814]

EV0 Enable Clear

Figure 8-811. AIL PD_0 EV0 ENABLE CLEAR

31	28	27	26
Reserved		PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0		W-0	W-0

25	24	23	22
PD_EE_OBSAI_SOP_INFO		Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
W-0		NA-0	W-0

21	20	19	16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR	
W-0	W-0	W-0	

15	11	10	9
Reserved		PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0		W-0	W-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
W-0	W-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
W-0	W-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
W-0	W-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-917. AIL PD_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
26	PD_EE_OBSAI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
25	PD_EE_OBSAI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
20	PD_EE_CPRI_CW_OVFL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
19-16	PD_EE_CPRI_CW_CRC_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
9	PD_EE_RP3_01_CRC_FAIL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
8	PD_EE_RP3_01_CAPTURE_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
6	PD_EE_RP3_01_SOC_RST_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
5	PD_EE_OBSAI_CRC_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	PD_EE_OBSAI_AXC_FAIL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	PD_EE_OBSAI_TS_WDOG_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	PD_EE_OBSAI_TS_MISS_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

Table 8-917. AIL PD_0 EV0 ENABLE CLEAR Field Descriptions (continued)

Bits	Name	Description
1	PD_EE_SOP_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	PD_EE_OBSAI_FRM_WIN_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.7 AIL PD_0 EV1 ENABLE STATUS [Address = 0x3_4818]

EV1 Enable Status

Figure 8-812. AIL PD_0 EV1 ENABLE STATUS

31	28	27	26
Reserved		PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0		R-0	R-0

25	24	23	22
PD_EE_OBSAI_SOP_INFO		Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
R-0		NA-0	R-0

21	20	19	16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR	
R-0	R-0	R-0	

15	11	10	9
Reserved		PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0		R-0	R-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
R-0	R-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
R-0	R-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
R-0	R-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-918. AIL PD_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
26	PD_EE_OBSAI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
25	PD_EE_OBSAI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
20	PD_EE_CPRI_CW_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
19-16	PD_EE_CPRI_CW_CRC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
9	PD_EE_RP3_01_CRC_FAIL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

Table 8-918. AIL PD_0 EV1 ENABLE STATUS Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
6	PD_EE_RP3_01_SOC_RST_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
5	PD_EE_OBSAI_CRC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	PD_EE_OBSAI_AXC_FAIL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	PD_EE_OBSAI_TS_WDOG_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	PD_EE_OBSAI_TS_MISS_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	PD_EE_SOP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	PD_EE_OBSAI_FRM_WIN_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.8 AIL PD_0 EV1 ENABLE SET [Address = 0x3_481C]

EV1 Enable Set

Figure 8-813. AIL PD_0 EV1 ENABLE SET

31	28	27	26
Reserved		PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0		W-0	W-0

25	24	23	22
PD_EE_OBSAI_SOP_INFO		Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
W-0		NA-0	W-0

21	20	19	16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR	
W-0	W-0	W-0	

15	11	10	9
Reserved		PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0		W-0	W-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
W-0	W-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
W-0	W-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
W-0	W-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-919. AIL PD_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
26	PD_EE_OBSAI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
25	PD_EE_OBSAI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	PD_EE_CPRI_CW_OVFL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
19-16	PD_EE_CPRI_CW_CRC_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
9	PD_EE_RP3_01_CRC_FAIL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

Table 8-919. AIL PD_0 EV1 ENABLE SET Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
6	PD_EE_RP3_01_SOC_RST_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
5	PD_EE_OBSAI_CRC_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	PD_EE_OBSAI_AXC_FAIL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	PD_EE_OBSAI_TS_WDOG_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	PD_EE_OBSAI_TS_MISS_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	PD_EE_SOP_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	PD_EE_OBSAI_FRM_WIN_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.9 AIL PD_0 EV1 ENABLE CLEAR [Address = 0x3_4820]

EV1 Enable Clear

Figure 8-814. AIL PD_0 EV1 ENABLE CLEAR

31	28	27	26
Reserved		PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0		W-0	W-0

25	24	23	22
PD_EE_OBSAI_SOP_INFO		Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
W-0		NA-0	W-0

21	20	19	16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR	
W-0	W-0	W-0	

15	11	10	9
Reserved		PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0		W-0	W-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
W-0	W-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
W-0	W-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
W-0	W-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-920. AIL PD_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
26	PD_EE_OBSAI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
25	PD_EE_OBSAI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	PD_EE_CPRI_CW_OVFL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
19-16	PD_EE_CPRI_CW_CRC_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
9	PD_EE_RP3_01_CRC_FAIL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

Table 8-920. AIL PD_0 EV1 ENABLE CLEAR Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
6	PD_EE_RP3_01_SOC_RST_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
5	PD_EE_OBSAI_CRC_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	PD_EE_OBSAI_AXC_FAIL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	PD_EE_OBSAI_TS_WDOG_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	PD_EE_OBSAI_TS_MISS_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	PD_EE_SOP_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	PD_EE_OBSAI_FRM_WIN_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.10 AIL PD_0 EV0 ENABLED STATUS [Address = 0x3_4824]

EV0 Enabled Status

Figure 8-815. AIL PD_0 EV0 ENABLED STATUS

31–28	27	26
Reserved	PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0	R-0	R-0

25	24–23	22
PD_EE_OBSAI_SOP_INFO	Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
R-0	NA-0	R-0

21	20	19–16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR
R-0	R-0	R-0

15–11	10	9
Reserved	PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0	R-0	R-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
R-0	R-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
R-0	R-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
R-0	R-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-921. AIL PD_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
26	PD_EE_OBSAI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
25	PD_EE_OBSAI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
20	PD_EE_CPRI_CW_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
19-16	PD_EE_CPRI_CW_CRC_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
9	PD_EE_RP3_01_CRC_FAIL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

Table 8-921. AIL PD_0 EV0 ENABLED STATUS Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
6	PD_EE_RP3_01_SOC_RST_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
5	PD_EE_OBSAI_CRC_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	PD_EE_OBSAI_AXC_FAIL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	PD_EE_OBSAI_TS_WDOG_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	PD_EE_OBSAI_TS_MISS_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	PD_EE_SOP_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	PD_EE_OBSAI_FRM_WIN_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.11 AIL PD_0 EV1 ENABLED STATUS [Address = 0x3_4828]

EV1 Enabled Status

Figure 8-816. AIL PD_0 EV1 ENABLED STATUS

31–28	27	26
Reserved	PD_EE_OBSAI_SOF_INFO	PD_EE_OBSAI_EOP_INFO
NA-0	R-0	R-0

25	24–23	22
PD_EE_OBSAI_SOP_INFO	Reserved	PD_EE_CPRI_CW_4B5B_CHAR_ERR
R-0	NA-0	R-0

21	20	19–16
PD_EE_CPRI_CW_4B5B_EOP_ERR	PD_EE_CPRI_CW_OVFL_ERR	PD_EE_CPRI_CW_CRC_ERR
R-0	R-0	R-0

15–11	10	9
Reserved	PD_EE_OBSAI_GSM_OFF_STB_INFO	PD_EE_RP3_01_CRC_FAIL_ERR
NA-0	R-0	R-0

8	7
PD_EE_RP3_01_CAPTURE_INFO	PD_EE_OBSAI_ROUTE_FAIL_INFO
R-0	R-0

6	5
PD_EE_RP3_01_SOC_RST_INFO	PD_EE_OBSAI_CRC_ERR
R-0	R-0

4	3
PD_EE_OBSAI_AXC_FAIL_ERR	PD_EE_OBSAI_TS_WDOG_ERR
R-0	R-0

2	1	0
PD_EE_OBSAI_TS_MISS_ERR	PD_EE_SOP_ERR	PD_EE_OBSAI_FRM_WIN_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-922. AIL PD_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved.
27	PD_EE_OBSAI_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
26	PD_EE_OBSAI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
25	PD_EE_OBSAI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
24-23	Reserved	Reserved.
22	PD_EE_CPRI_CW_4B5B_CHAR_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
21	PD_EE_CPRI_CW_4B5B_EOP_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
20	PD_EE_CPRI_CW_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
19-16	PD_EE_CPRI_CW_CRC_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
15-11	Reserved	Reserved.
10	PD_EE_OBSAI_GSM_OFF_STB_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
9	PD_EE_RP3_01_CRC_FAIL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

Table 8-922. AIL PD_0 EV1 ENABLED STATUS Field Descriptions (continued)

Bits	Name	Description
8	PD_EE_RP3_01_CAPTURE_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
7	PD_EE_OBSAI_ROUTE_FAIL_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
6	PD_EE_RP3_01_SOC_RST_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
5	PD_EE_OBSAI_CRC_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	PD_EE_OBSAI_AXC_FAIL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	PD_EE_OBSAI_TS_WDOG_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	PD_EE_OBSAI_TS_MISS_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	PD_EE_SOP_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	PD_EE_OBSAI_FRM_WIN_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.12 AIL PD_1 RAW INTERRUPT STATUS [Address = 0x3_482C]

AIL PD error register.

Figure 8-817. AIL PD_1 RAW INTERRUPT STATUS

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		R-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-923. AIL PD_1 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	The radio standard framing FSM did not wrap naturally back to zero on a 10ms boundary (indicated by hyperframe and basic frame offset relative to PHY frame boundary). For GSM or some WiMax radio standards without 10ms framing, this error should be ignored.
15-8	PD_EE_CPRI_TDM_FSM_ERR	CPRI Channel TDM did not wrap back to start position prior to end of a radio frame boundary. Mostly likely cause is incorrect programming of TDM and Bubble insertion parameters.
7-0	PD_EE_CPRI_BUB_FSM_ERR	The bubble FSM did not wrap back to zero on a radio frame boundary. This is likely a programming error resulting from programming a KNC_CFG value which doesn't evenly fit in the radio frame. In GSM, a radio frame boundary is 60ms. Even if the bubble FSM is disabled, this may still fire.

8.6.52.13 AIL PD_1 RAW SET [Address = 0x3_4830]

Raw Set

Figure 8-818. AIL PD_1 RAW SET

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		W-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-924. AIL PD_1 RAW SET Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
15-8	PD_EE_CPRI_TDM_FSM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
7-0	PD_EE_CPRI_BUB_FSM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.14 AIL PD_1 RAW CLEAR [Address = 0x3_4834]

Raw Clear

Figure 8-819. AIL PD_1 RAW CLEAR

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		W-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-925. AIL PD_1 RAW CLEAR Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
15-8	PD_EE_CPRI_TDM_FSM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
7-0	PD_EE_CPRI_BUB_FSM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.15 AIL PD_1 EV0 ENABLE STATUS [Address = 0x3_4838]

EV0 Enable Status

Figure 8-820. AIL PD_1 EV0 ENABLE STATUS

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		R-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-926. AIL PD_1 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
15-8	PD_EE_CPRI_TDM_FSM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
7-0	PD_EE_CPRI_BUB_FSM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.16 AIL PD_1 EV0 ENABLE SET [Address = 0x3_483C]

EV0 Enable Set

Figure 8-821. AIL PD_1 EV0 ENABLE SET

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		W-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-927. AIL PD_1 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
15-8	PD_EE_CPRI_TDM_FSM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
7-0	PD_EE_CPRI_BUB_FSM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.17 AIL PD_1 EV0 ENABLE CLEAR [Address = 0x3_4840]

EV0 Enable Clear

Figure 8-822. AIL PD_1 EV0 ENABLE CLEAR

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		W-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-928. AIL PD_1 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
15-8	PD_EE_CPRI_TDM_FSM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
7-0	PD_EE_CPRI_BUB_FSM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.18 AIL PD_1 EV1 ENABLE STATUS [Address = 0x3_4844]

EV1 Enable Status

Figure 8-823. AIL PD_1 EV1 ENABLE STATUS

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		R-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-929. AIL PD_1 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
15-8	PD_EE_CPRI_TDM_FSM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
7-0	PD_EE_CPRI_BUB_FSM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.19 AIL PD_1 EV1 ENABLE SET [Address = 0x3_4848]

EV1 Enable Set

Figure 8-824. AIL PD_1 EV1 ENABLE SET

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		W-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-930. AIL PD_1 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-8	PD_EE_CPRI_TDM_FSM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
7-0	PD_EE_CPRI_BUB_FSM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.20 AIL PD_1 EV1 ENABLE CLEAR [Address = 0x3_484C]

EV1 Enable Clear

Figure 8-825. AIL PD_1 EV1 ENABLE CLEAR

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		W-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-931. AIL PD_1 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-8	PD_EE_CPRI_TDM_FSM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
7-0	PD_EE_CPRI_BUB_FSM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.21 AIL PD_1 EV0 ENABLED STATUS [Address = 0x3_4850]

EV0 Enabled Status

Figure 8-826. AIL PD_1 EV0 ENABLED STATUS

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		R-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-932. AIL PD_1 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
15-8	PD_EE_CPRI_TDM_FSM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
7-0	PD_EE_CPRI_BUB_FSM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.22 AIL PD_1 EV1 ENABLED STATUS [Address = 0x3_4854]

EV1 Enabled Status

Figure 8-827. AIL PD_1 EV1 ENABLED STATUS

31	24	23	16
Reserved		PD_EE_CPRI_RADSTD_ERR	
NA-0		R-0	

15	8	7	0
PD_EE_CPRI_TDM_FSM_ERR		PD_EE_CPRI_BUB_FSM_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-933. AIL PD_1 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved.
23-16	PD_EE_CPRI_RADSTD_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
15-8	PD_EE_CPRI_TDM_FSM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
7-0	PD_EE_CPRI_BUB_FSM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.23 AIL PD_2_0 RAW INTERRUPT STATUS [Address = 0x3_4858]

AIL PD error register.

Figure 8-828. AIL PD_2_0 RAW INTERRUPT STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-934. AIL PD_2_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.24 AIL PD_2_0 RAW SET [Address = 0x3_485C]

Raw Set

Figure 8-829. AIL PD_2_0 RAW SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-935. AIL PD_2_0 RAW SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.25 AIL PD_2_0 RAW CLEAR [Address = 0x3_4860]

Raw Clear

Figure 8-830. AIL PD_2_0 RAW CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-936. AIL PD_2_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.26 AIL PD_2_0 EV0 ENABLE STATUS [Address = 0x3_4864]

EV0 Enable Status

Figure 8-831. AIL PD_2_0 EV0 ENABLE STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-937. AIL PD_2_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.27 AIL PD_2_0 EV0 ENABLE SET [Address = 0x3_4868]

EV0 Enable Set

Figure 8-832. AIL PD_2_0 EV0 ENABLE SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-938. AIL PD_2_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.28 AIL PD_2_0 EV0 ENABLE CLEAR [Address = 0x3_486C]

EV0 Enable Clear

Figure 8-833. AIL PD_2_0 EV0 ENABLE CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-939. AIL PD_2_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.29 AIL PD_2_0 EV1 ENABLE STATUS [Address = 0x3_4870]

EV1 Enable Status

Figure 8-834. AIL PD_2_0 EV1 ENABLE STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-940. AIL PD_2_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.30 AIL PD_2_0 EV1 ENABLE SET [Address = 0x3_4874]

EV1 Enable Set

Figure 8-835. AIL PD_2_0 EV1 ENABLE SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-941. AIL PD_2_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.31 AIL PD_2_0 EV1 ENABLE CLEAR [Address = 0x3_4878]

EV1 Enable Clear

Figure 8-836. AIL PD_2_0 EV1 ENABLE CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-942. AIL PD_2_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.32 AIL PD_2_0 EV0 ENABLED STATUS [Address = 0x3_487C]

EV0 Enabled Status

Figure 8-837. AIL PD_2_0 EV0 ENABLED STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-943. AIL PD_2_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.33 AIL PD_2_0 EV1 ENABLED STATUS [Address = 0x3_4880]

EV1 Enabled Status

Figure 8-838. AIL PD_2_0 EV1 ENABLED STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-944. AIL PD_2_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.34 AIL PD_2_1 RAW INTERRUPT STATUS [Address = 0x3_4884]

AIL PD error register.

Figure 8-839. AIL PD_2_1 RAW INTERRUPT STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-945. AIL PD_2_1 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.35 AIL PD_2_1 RAW SET [Address = 0x3_4888]

Raw Set

Figure 8-840. AIL PD_2_1 RAW SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-946. AIL PD_2_1 RAW SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.36 AIL PD_2_1 RAW CLEAR [Address = 0x3_488C]

Raw Clear

Figure 8-841. AIL PD_2_1 RAW CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-947. AIL PD_2_1 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.37 AIL PD_2_1 EV0 ENABLE STATUS [Address = 0x3_4890]

EV0 Enable Status

Figure 8-842. AIL PD_2_1 EV0 ENABLE STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-948. AIL PD_2_1 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.38 AIL PD_2_1 EV0 ENABLE SET [Address = 0x3_4894]

EV0 Enable Set

Figure 8-843. AIL PD_2_1 EV0 ENABLE SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-949. AIL PD_2_1 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.39 AIL PD_2_1 EV0 ENABLE CLEAR [Address = 0x3_4898]

EV0 Enable Clear

Figure 8-844. AIL PD_2_1 EV0 ENABLE CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-950. AIL PD_2_1 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.40 AIL PD_2_1 EV1 ENABLE STATUS [Address = 0x3_489C]

EV1 Enable Status

Figure 8-845. AIL PD_2_1 EV1 ENABLE STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-951. AIL PD_2_1 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.41 AIL PD_2_1 EV1 ENABLE SET [Address = 0x3_48A0]

EV1 Enable Set

Figure 8-846. AIL PD_2_1 EV1 ENABLE SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-952. AIL PD_2_1 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.42 AIL PD_2_1 EV1 ENABLE CLEAR [Address = 0x3_48A4]

EV1 Enable Clear

Figure 8-847. AIL PD_2_1 EV1 ENABLE CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-953. AIL PD_2_1 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.43 AIL PD_2_1 EV0 ENABLED STATUS [Address = 0x3_48A8]

EV0 Enabled Status

Figure 8-848. AIL PD_2_1 EV0 ENABLED STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-954. AIL PD_2_1 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.44 AIL PD_2_1 EV1 ENABLED STATUS [Address = 0x3_48AC]

EV1 Enabled Status

Figure 8-849. AIL PD_2_1 EV1 ENABLED STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-955. AIL PD_2_1 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.6.52.45 AIL PE_0 RAW INTERRUPT STATUS [Address = 0x3_4908]

AIL PE error register.

Figure 8-850. AIL PE_0 RAW INTERRUPT STATUS

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		R-0	NA-0	R-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
R-0		R-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-956. AIL PE_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	The PE-to-RT FIFO overflowed. Suspected cause is PE_STB from uAT is too early or RT has been programmed to disregard PE traffic.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Indicates a Hyperframe packet did not complete before the hyperframe boundary.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Indicates there was no data available for transfer while in an active packet state
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Indicates there was no data available for transfer while in an active packet state
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Indicates there was no data available for transfer while in an active packet state
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Indicates there was no data available for transfer while in an active packet state

8.6.52.46 AIL PE_0 RAW SET [Address = 0x3_490C]

Raw Set

Figure 8-851. AIL PE_0 RAW SET

31 22	21	20	19 16
Reserved	PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR
NA-0	W-0	NA-0	W-0

15 12	11 8
PE_EE_CPRI_CW_HDLC_STARVE_ERR	PE_EE_CPRI_CW_HYPFM_STARVE_ERR
W-0	W-0

7 4	3 0
PE_EE_CPRI_CW_4B5B_STARVE_ERR	PE_EE_CPRI_CW_NULL_STARVE_ERR
W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-957. AIL PE_0 RAW SET Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.47 AIL PE_0 RAW CLEAR [Address = 0x3_4910]

Raw Clear

Figure 8-852. AIL PE_0 RAW CLEAR

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		W-0	NA-0	W-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
W-0		W-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-958. AIL PE_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.48 AIL PE_0 EV0 ENABLE STATUS [Address = 0x3_4914]

EV0 Enable Status

Figure 8-853. AIL PE_0 EV0 ENABLE STATUS

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		R-0	NA-0	R-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
R-0		R-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-959. AIL PE_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.49 AIL PE_0 EV0 ENABLE SET [Address = 0x3_4918]

EV0 Enable Set

Figure 8-854. AIL PE_0 EV0 ENABLE SET

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		W-0	NA-0	W-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
W-0		W-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-960. AIL PE_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.50 AIL PE_0 EV0 ENABLE CLEAR [Address = 0x3_491C]

EV0 Enable Clear

Figure 8-855. AIL PE_0 EV0 ENABLE CLEAR

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		W-0	NA-0	W-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
W-0		W-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-961. AIL PE_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.51 AIL PE_0 EV1 ENABLE STATUS [Address = 0x3_4920]

EV1 Enable Status

Figure 8-856. AIL PE_0 EV1 ENABLE STATUS

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		R-0	NA-0	R-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
R-0		R-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-962. AIL PE_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.52 AIL PE_0 EV1 ENABLE SET [Address = 0x3_4924]

EV1 Enable Set

Figure 8-857. AIL PE_0 EV1 ENABLE SET

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		W-0	NA-0	W-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
W-0		W-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-963. AIL PE_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.53 AIL PE_0 EV1 ENABLE CLEAR [Address = 0x3_4928]

EV1 Enable Clear

Figure 8-858. AIL PE_0 EV1 ENABLE CLEAR

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		W-0	NA-0	W-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
W-0		W-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-964. AIL PE_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.54 AIL PE_0 EV0 ENABLED STATUS [Address = 0x3_492C]

EV0 Enabled Status

Figure 8-859. AIL PE_0 EV0 ENABLED STATUS

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		R-0	NA-0	R-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
R-0		R-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-965. AIL PE_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.55 AIL PE_0 EV1 ENABLED STATUS [Address = 0x3_4930]

EV1 Enabled Status

Figure 8-860. AIL PE_0 EV1 ENABLED STATUS

31	22	21	20	19	16
Reserved		PE_EE_OFIFO_OFLOW_ERR	Reserved	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	
NA-0		R-0	NA-0	R-0	

15	12	11	8
PE_EE_CPRI_CW_HDLC_STARVE_ERR		PE_EE_CPRI_CW_HYPFM_STARVE_ERR	
R-0		R-0	

7	4	3	0
PE_EE_CPRI_CW_4B5B_STARVE_ERR		PE_EE_CPRI_CW_NULL_STARVE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-966. AIL PE_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-22	Reserved	Reserved.
21	PE_EE_OFIFO_OFLOW_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
20	Reserved	Reserved.
19-16	PE_EE_CPRI_CW_HYPFM_OFLOW_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
15-12	PE_EE_CPRI_CW_HDLC_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
11-8	PE_EE_CPRI_CW_HYPFM_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
7-4	PE_EE_CPRI_CW_4B5B_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3-0	PE_EE_CPRI_CW_NULL_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.56 AIL AIL_SI_0 RAW INTERRUPT STATUS [Address = 0x3_4934]

AIL uAT and SI_AIL_PE_SCH error register.

Figure 8-861. AIL AIL_SI_0 RAW INTERRUPT STATUS

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		R-0	R-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-967. AIL AIL_SI_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	An OBSAI Transmission Rule (MOD or DBM) did not wrap back naturally on a PHY frame boundary. Likely a programming error of OBSAI rules, possibly rules rates which are incompatible with link rate
4	OBSAI_MULTRULEFIRE_ERR	Multiple OBSAI rules fired simultaniously. Indicates a programming error of OBSAI rules.
3	OBSAI_PHY_SYNC_ERR	The uAT indicated to the PE_SCH of an OBSAI PHY frame boundary, but OBSAI FSM did not predict a PHY frame boundary. Likely indicates a programming error of OBSAI PHY FSM. Also will trigger if uAT timing is changed while PE_SCH OBSAI PHY FSM is currently operational
2	CPRI_BUB_FSM_ERR	The bubble FSM did not wrap back to zero on a radio frame boundary. This is likely a programming error. In GSM, a radio frame boundary is 60ms.
1	CPRI_TDM_LUT_ERR	CPRI Channel TDM did not wrap back to start position prior to end of an iteration window (few GSM cases will legally cause this EE) Mostly likely cause is incorrect programming of TDM and Bubble insertion parameters.
0	UAT_PI_ERR	UAT OBSAI PI error. PHY_RM PHY frame boundary detected outside programmed window specified by uat_pimax_cfg_pi_max_cfg (OBSAI defines Pi as reception time of PHY FB)

8.6.52.57 AIL AIL_SI_0 RAW SET [Address = 0x3_4938]

Raw Set

Figure 8-862. AIL AIL_SI_0 RAW SET

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		W-0	W-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-968. AIL AIL_SI_0 RAW SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	OBSAI_MULTRULEFIRE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	OBSAI_PHY_SYNC_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	CPRI_BUB_FSM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	CPRI_TDM_LUT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	UAT_PI_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.58 AIL AIL_SI_0 RAW CLEAR [Address = 0x3_493C]

Raw Clear

Figure 8-863. AIL AIL_SI_0 RAW CLEAR

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		W-0	W-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-969. AIL AIL_SI_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	OBSAI_MULTRULEFIRE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	OBSAI_PHY_SYNC_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	CPRI_BUB_FSM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	CPRI_TDM_LUT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	UAT_PI_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.59 AIL AIL_SI_0 EV0 ENABLE STATUS [Address = 0x3_4940]

EV0 Enable Status

Figure 8-864. AIL AIL_SI_0 EV0 ENABLE STATUS

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		R-0	R-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-970. AIL AIL_SI_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	OBSAI_MULTRULEFIRE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	OBSAI_PHY_SYNC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	CPRI_BUB_FSM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	CPRI_TDM_LUT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	UAT_PI_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.60 AIL AIL_SI_0 EV0 ENABLE SET [Address = 0x3_4944]

EV0 Enable Set

Figure 8-865. AIL AIL_SI_0 EV0 ENABLE SET

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		W-0	W-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-971. AIL AIL_SI_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	OBSAI_MULTRULEFIRE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	OBSAI_PHY_SYNC_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	CPRI_BUB_FSM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	CPRI_TDM_LUT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	UAT_PI_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.61 AIL AIL_SI_0 EV0 ENABLE CLEAR [Address = 0x3_4948]

EV0 Enable Clear

Figure 8-866. AIL AIL_SI_0 EV0 ENABLE CLEAR

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		W-0	W-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-972. AIL AIL_SI_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	OBSAI_MULTRULEFIRE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	OBSAI_PHY_SYNC_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	CPRI_BUB_FSM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	CPRI_TDM_LUT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	UAT_PI_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.62 AIL AIL_SI_0 EV1 ENABLE STATUS [Address = 0x3_494C]

EV1 Enable Status

Figure 8-867. AIL AIL_SI_0 EV1 ENABLE STATUS

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		R-0	R-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-973. AIL AIL_SI_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	OBSAI_MULTRULEFIRE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	OBSAI_PHY_SYNC_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	CPRI_BUB_FSM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	CPRI_TDM_LUT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	UAT_PI_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.63 AIL AIL_SI_0 EV1 ENABLE SET [Address = 0x3_4950]

EV1 Enable Set

Figure 8-868. AIL AIL_SI_0 EV1 ENABLE SET

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		W-0	W-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-974. AIL AIL_SI_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	OBSAI_MULTRULEFIRE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	OBSAI_PHY_SYNC_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	CPRI_BUB_FSM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	CPRI_TDM_LUT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	UAT_PI_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.64 AIL AIL_SI_0 EV1 ENABLE CLEAR [Address = 0x3_4954]

EV1 Enable Clear

Figure 8-869. AIL AIL_SI_0 EV1 ENABLE CLEAR

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		W-0	W-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-975. AIL AIL_SI_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	OBSAI_MULTRULEFIRE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	OBSAI_PHY_SYNC_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	CPRI_BUB_FSM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	CPRI_TDM_LUT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	UAT_PI_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.65 AIL AIL_SI_0 EV0 ENABLED STATUS [Address = 0x3_4958]

EV0 Enabled Status

Figure 8-870. AIL AIL_SI_0 EV0 ENABLED STATUS

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		R-0	R-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-976. AIL AIL_SI_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	OBSAI_MULTRULEFIRE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	OBSAI_PHY_SYNC_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	CPRI_BUB_FSM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	CPRI_TDM_LUT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	UAT_PI_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.66 AIL AIL_SI_0 EV1 ENABLED STATUS [Address = 0x3_495C]

EV1 Enabled Status

Figure 8-871. AIL AIL_SI_0 EV1 ENABLED STATUS

31	6	5	4
Reserved		OBSAI_DBM_WRAP_ERR	OBSAI_MULTRULEFIRE_ERR
NA-0		R-0	R-0

3	2	1	0
OBSAI_PHY_SYNC_ERR	CPRI_BUB_FSM_ERR	CPRI_TDM_LUT_ERR	UAT_PI_ERR
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-977. AIL AIL_SI_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	OBSAI_DBM_WRAP_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	OBSAI_MULTRULEFIRE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	OBSAI_PHY_SYNC_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	CPRI_BUB_FSM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	CPRI_TDM_LUT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	UAT_PI_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.67 AIL EE_SII_A RAW INTERRUPT STATUS [Address = 0x3_4960]

SI si_i IQ errors and info.

Figure 8-872. AIL EE_SII_A RAW INTERRUPT STATUS

31	6	5	4	3
Reserved		SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-978. AIL EE_SII_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	SI Ingress IQ FIFO overflow error
4	SI_ING_IQ_IFE_DAT_INFO	SI Ingress IQ IFE transmitted valid data phase
3	SI_ING_IQ_IFE_EOP_INFO	SI Ingress IQ IFE transmitted EOP
2	SI_ING_IQ_IFE_SOP_INFO	SI Ingress IQ IFE transmitted SOP
1	SI_ING_IQ_ICC_DAT_INFO	SI Ingress IQ ICC data transfer received
0	SI_ING_IQ_ICC_SOF_INFO	SI Ingress IQ ICC Start of Frame received

8.6.52.68 AIL EE_SII_A RAW SET [Address = 0x3_4964]

Raw Set

Figure 8-873. AIL EE_SII_A RAW SET

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-979. AIL EE_SII_A RAW SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.69 AIL EE_SII_A RAW CLEAR [Address = 0x3_4968]

Raw Clear

Figure 8-874. AIL EE_SII_A RAW CLEAR

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-980. AIL EE_SII_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.70 AIL EE_SII_A EV0 ENABLE STATUS [Address = 0x3_496C]

EV0 Enable Status

Figure 8-875. AIL EE_SII_A EV0 ENABLE STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-981. AIL EE_SII_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.71 AIL EE_SII_A EV0 ENABLE SET [Address = 0x3_4970]

EV0 Enable Set

Figure 8-876. AIL EE_SII_A EV0 ENABLE SET

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-982. AIL EE_SII_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.72 AIL EE_SII_A EV0 ENABLE CLEAR [Address = 0x3_4974]

EV0 Enable Clear

Figure 8-877. AIL EE_SII_A EV0 ENABLE CLEAR

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-983. AIL EE_SII_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.73 AIL EE_SII_A EV1 ENABLE STATUS [Address = 0x3_4978]

EV1 Enable Status

Figure 8-878. AIL EE_SII_A EV1 ENABLE STATUS

31	6	5	4	3
Reserved		SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-984. AIL EE_SII_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.74 AIL EE_SII_A EV1 ENABLE SET [Address = 0x3_497C]

EV1 Enable Set

Figure 8-879. AIL EE_SII_A EV1 ENABLE SET

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-985. AIL EE_SII_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.75 AIL EE_SII_A EV1 ENABLE CLEAR [Address = 0x3_4980]

EV1 Enable Clear

Figure 8-880. AIL EE_SII_A EV1 ENABLE CLEAR

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	W-0	W-0	W-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
W-0	W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-986. AIL EE_SII_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.76 AIL EE_SII_A EV0 ENABLED STATUS [Address = 0x3_4984]

EV0 Enabled Status

Figure 8-881. AIL EE_SII_A EV0 ENABLED STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0
2	1	0	
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO	
R-0	R-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-987. AIL EE_SII_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.77 AIL EE_SII_A EV1 ENABLED STATUS [Address = 0x3_4988]

EV1 Enabled Status

Figure 8-882. AIL EE_SII_A EV1 ENABLED STATUS

31 6	5	4	3
Reserved	SI_ING_IQ_FIFO_OVFL_ERR	SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0	R-0	R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-988. AIL EE_SII_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-6	Reserved	Reserved.
5	SI_ING_IQ_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
4	SI_ING_IQ_IFE_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.78 AIL EE_SII_B RAW INTERRUPT STATUS [Address = 0x3_498C]

SI si_i CTL errors and info.

Figure 8-883. AIL EE_SII_B RAW INTERRUPT STATUS

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		R-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-989. AIL EE_SII_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	SI Ingress CTL FIFO overflow error
2	SI_ING_CTL_ICC_DAT_INFO	SI Ingress CTL received valid data phase from ICC
1	SI_ING_CTL_ICC_EOP_INFO	SI Ingress CTL received EOP from ICC
0	SI_ING_CTL_PKT_ERR	SI Ingress CTL Packet error occurred

8.6.52.79 AIL EE_SII_B RAW SET [Address = 0x3_4990]

Raw Set

Figure 8-884. AIL EE_SII_B RAW SET

31	4	3	2	1	0
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
NA-0		W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-990. AIL EE_SII_B RAW SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.80 AIL EE_SII_B RAW CLEAR [Address = 0x3_4994]

Raw Clear

Figure 8-885. AIL EE_SII_B RAW CLEAR

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		W-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-991. AIL EE_SII_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.81 AIL EE_SII_B EV0 ENABLE STATUS [Address = 0x3_4998]

EV0 Enable Status

Figure 8-886. AIL EE_SII_B EV0 ENABLE STATUS

31	4	3	
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	
NA-0		R-0	
2		1	0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-992. AIL EE_SII_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_CTL_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.82 AIL EE_SII_B EV0 ENABLE SET [Address = 0x3_499C]

EV0 Enable Set

Figure 8-887. AIL EE_SII_B EV0 ENABLE SET

31	4	3	
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	
NA-0		W-0	
2		1	0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-993. AIL EE_SII_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.83 AIL EE_SII_B EV0 ENABLE CLEAR [Address = 0x3_49A0]

EV0 Enable Clear

Figure 8-888. AIL EE_SII_B EV0 ENABLE CLEAR

31	4	3	2	1	0
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
NA-0		W-0	W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-994. AIL EE_SII_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.84 AIL EE_SII_B EV1 ENABLE STATUS [Address = 0x3_49A4]

EV1 Enable Status

Figure 8-889. AIL EE_SII_B EV1 ENABLE STATUS

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		R-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-995. AIL EE_SII_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_CTL_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.85 AIL EE_SII_B EV1 ENABLE SET [Address = 0x3_49A8]

EV1 Enable Set

Figure 8-890. AIL EE_SII_B EV1 ENABLE SET

31	4	3	
Reserved		SI_ING_CTL_FIFO_OVFL_ERR	
NA-0		W-0	
2		1	0
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-996. AIL EE_SII_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.86 AIL EE_SII_B EV1 ENABLE CLEAR [Address = 0x3_49AC]

EV1 Enable Clear

Figure 8-891. AIL EE_SII_B EV1 ENABLE CLEAR

31	4	3		
Reserved		SI_ING_CTL_FIFO_OVFL_ERR		
NA-0		W-0		
	2	1	0	
SI_ING_CTL_ICC_DAT_INFO		SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR	
W-0		W-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-997. AIL EE_SII_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_CTL_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_CTL_ICC_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_CTL_PKT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.87 AIL EE_SII_B EV0 ENABLED STATUS [Address = 0x3_49B0]

EV0 Enabled Status

Figure 8-892. AIL EE_SII_B EV0 ENABLED STATUS

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		R-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-998. AIL EE_SII_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_CTL_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.88 AIL EE_SII_B EV1 ENABLED STATUS [Address = 0x3_49B4]

EV1 Enabled Status

Figure 8-893. AIL EE_SII_B EV1 ENABLED STATUS

31	4	3
Reserved		SI_ING_CTL_FIFO_OVFL_ERR
NA-0		R-0

2	1	0
SI_ING_CTL_ICC_DAT_INFO	SI_ING_CTL_ICC_EOP_INFO	SI_ING_CTL_PKT_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

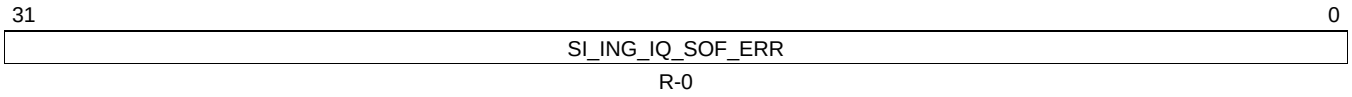
Table 8-999. AIL EE_SII_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3	SI_ING_CTL_FIFO_OVFL_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_ING_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_ING_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_CTL_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.89 AIL EE_SII_C_0 RAW INTERRUPT STATUS [Address = 0x3_49B8]

SI si_i IQ per-channel start of frame errors

Figure 8-894. AIL EE_SII_C_0 RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1000. AIL EE_SII_C_0 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	SI Ingress IQ per channel Start of Frame alignment error

8.6.52.90 AIL EE_SII_C_0 RAW SET [Address = 0x3_49BC]

Raw Set

Figure 8-895. AIL EE_SII_C_0 RAW SET

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1001. AIL EE_SII_C_0 RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.91 AIL EE_SII_C_0 RAW CLEAR [Address = 0x3_49C0]

Raw Clear

Figure 8-896. AIL EE_SII_C_0 RAW CLEAR

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

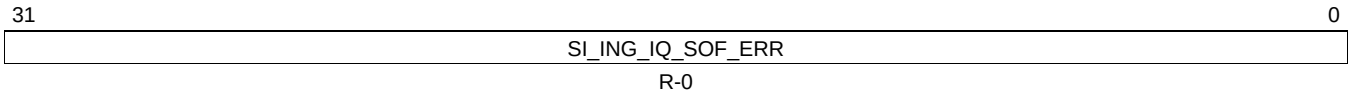
Table 8-1002. AIL EE_SII_C_0 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.92 AIL EE_SII_C_0 EV0 ENABLE STATUS [Address = 0x3_49C4]

EV0 Enable Status

Figure 8-897. AIL EE_SII_C_0 EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1003. AIL EE_SII_C_0 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.93 AIL EE_SII_C_0 EV0 ENABLE SET [Address = 0x3_49C8]

EV0 Enable Set

Figure 8-898. AIL EE_SII_C_0 EV0 ENABLE SET

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

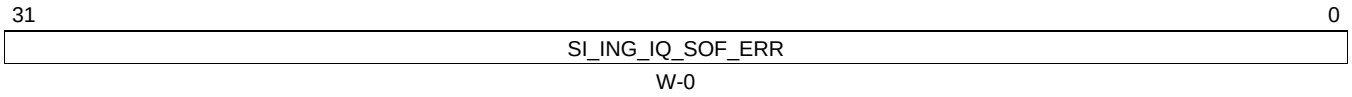
Table 8-1004. AIL EE_SII_C_0 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.94 AIL EE_SII_C_0 EV0 ENABLE CLEAR [Address = 0x3_49CC]

EV0 Enable Clear

Figure 8-899. AIL EE_SII_C_0 EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

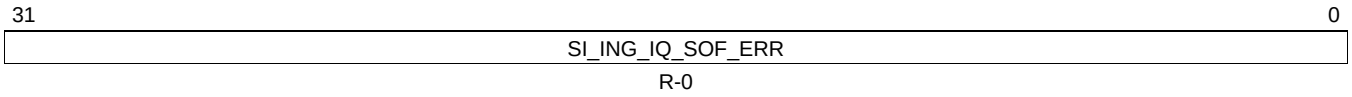
Table 8-1005. AIL EE_SII_C_0 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.95 AIL EE_SII_C_0 EV1 ENABLE STATUS [Address = 0x3_49D0]

EV1 Enable Status

Figure 8-900. AIL EE_SII_C_0 EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1006. AIL EE_SII_C_0 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.96 AIL EE_SII_C_0 EV1 ENABLE SET [Address = 0x3_49D4]

EV1 Enable Set

Figure 8-901. AIL EE_SII_C_0 EV1 ENABLE SET

31	0
SI_ING_IQ_SOF_ERR	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

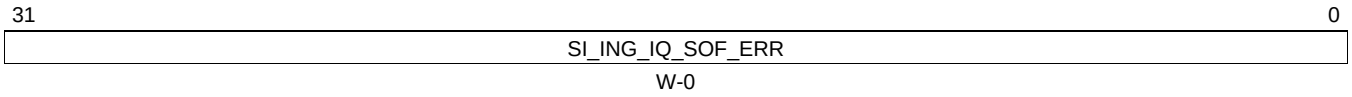
Table 8-1007. AIL EE_SII_C_0 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.97 AIL EE_SII_C_0 EV1 ENABLE CLEAR [Address = 0x3_49D8]

EV1 Enable Clear

Figure 8-902. AIL EE_SII_C_0 EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

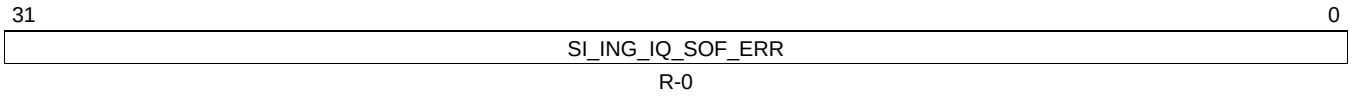
Table 8-1008. AIL EE_SII_C_0 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.98 AIL EE_SII_C_0 EV0 ENABLED STATUS [Address = 0x3_49DC]

EV0 Enabled Status

Figure 8-903. AIL EE_SII_C_0 EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

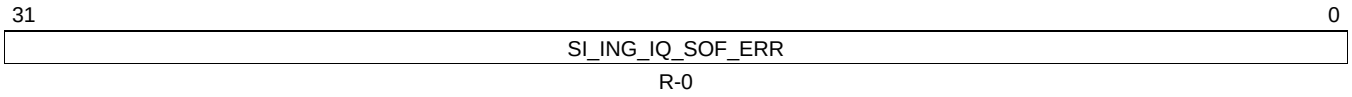
Table 8-1009. AIL EE_SII_C_0 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.99 AIL EE_SII_C_0 EV1 ENABLED STATUS [Address = 0x3_49E0]

EV1 Enabled Status

Figure 8-904. AIL EE_SII_C_0 EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

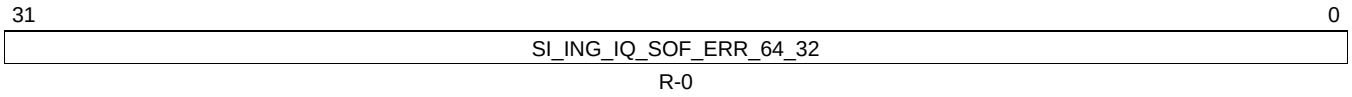
Table 8-1010. AIL EE_SII_C_0 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.100 AIL EE_SII_C_1 RAW INTERRUPT STATUS [Address = 0x3_49E4]

SI si_i IQ per-channel start of frame errors

Figure 8-905. AIL EE_SII_C_1 RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1011. AIL EE_SII_C_1 RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	SI Ingress IQ per channel Start of Frame alignment error

8.6.52.101 AIL EE_SII_C_1 RAW SET [Address = 0x3_49E8]

Raw Set

Figure 8-906. AIL EE_SII_C_1 RAW SET

31	0
SI_ING_IQ_SOF_ERR_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1012. AIL EE_SII_C_1 RAW SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.102 AIL EE_SII_C_1 RAW CLEAR [Address = 0x3_49EC]

Raw Clear

Figure 8-907. AIL EE_SII_C_1 RAW CLEAR

31	0
SI_ING_IQ_SOF_ERR_64_32	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

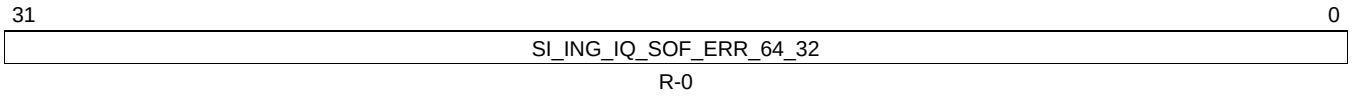
Table 8-1013. AIL EE_SII_C_1 RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.103 AIL EE_SII_C_1 EV0 ENABLE STATUS [Address = 0x3_49F0]

EV0 Enable Status

Figure 8-908. AIL EE_SII_C_1 EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

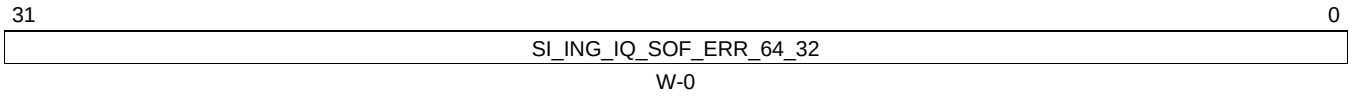
Table 8-1014. AIL EE_SII_C_1 EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.104 AIL EE_SII_C_1 EV0 ENABLE SET [Address = 0x3_49F4]

EV0 Enable Set

Figure 8-909. AIL EE_SII_C_1 EV0 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

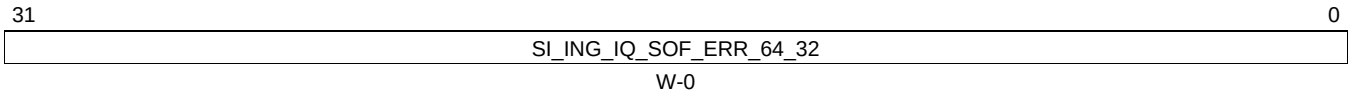
Table 8-1015. AIL EE_SII_C_1 EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.105 AIL EE_SII_C_1 EV0 ENABLE CLEAR [Address = 0x3_49F8]

EV0 Enable Clear

Figure 8-910. AIL EE_SII_C_1 EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

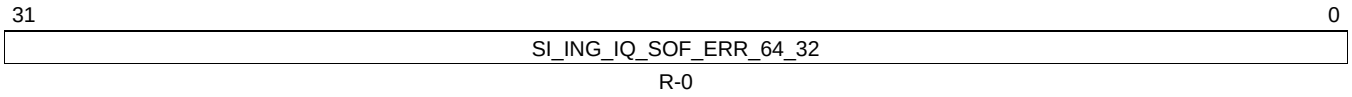
Table 8-1016. AIL EE_SII_C_1 EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.106 AIL EE_SII_C_1 EV1 ENABLE STATUS [Address = 0x3_49FC]

EV1 Enable Status

Figure 8-911. AIL EE_SII_C_1 EV1 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

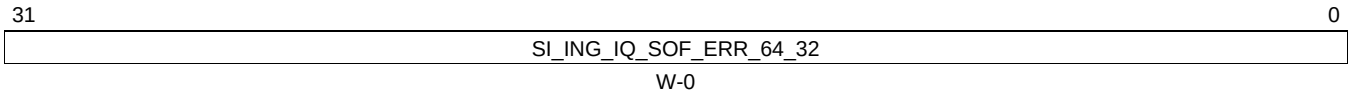
Table 8-1017. AIL EE_SII_C_1 EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.107 AIL EE_SII_C_1 EV1 ENABLE SET [Address = 0x3_4A00]

EV1 Enable Set

Figure 8-912. AIL EE_SII_C_1 EV1 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

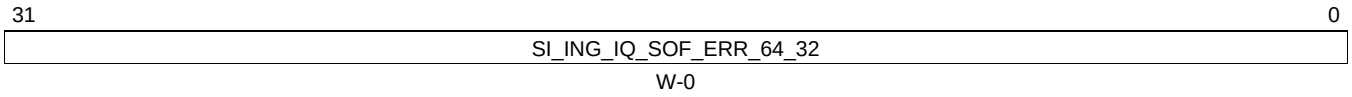
Table 8-1018. AIL EE_SII_C_1 EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.108 AIL EE_SII_C_1 EV1 ENABLE CLEAR [Address = 0x3_4A04]

EV1 Enable Clear

Figure 8-913. AIL EE_SII_C_1 EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

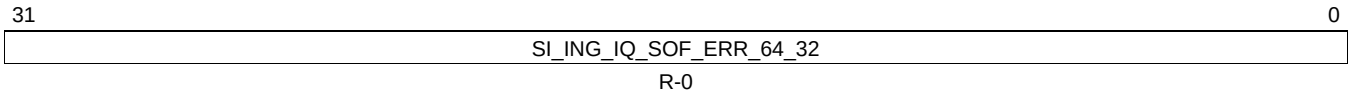
Table 8-1019. AIL EE_SII_C_1 EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.109 AIL EE_SII_C_1 EV0 ENABLED STATUS [Address = 0x3_4A08]

EV0 Enabled Status

Figure 8-914. AIL EE_SII_C_1 EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

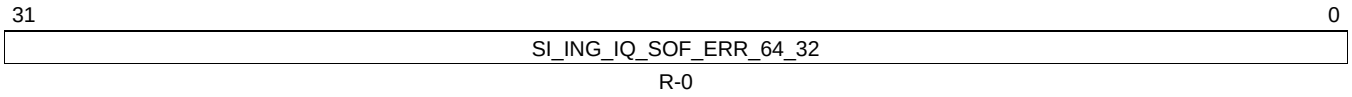
Table 8-1020. AIL EE_SII_C_1 EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.110 AIL EE_SII_C_1 EV1 ENABLED STATUS [Address = 0x3_4A0C]

EV1 Enabled Status

Figure 8-915. AIL EE_SII_C_1 EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1021. AIL EE_SII_C_1 EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	SI_ING_IQ_SOF_ERR_64_32	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.111 AIL EE_SII_D RAW INTERRUPT STATUS [Address = 0x3_4A68]

SI si_i CTL per-channel SOP received from ICC info

Figure 8-916. AIL EE_SII_D RAW INTERRUPT STATUS

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1022. AIL EE_SII_D RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	SI Ingress CTL per channel SOP received from ICC

8.6.52.112 AIL EE_SII_D RAW SET [Address = 0x3_4A6C]

Raw Set

Figure 8-917. AIL EE_SII_D RAW SET

31 4	3 0
Reserved	SI_ING_CTL_ICC_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1023. AIL EE_SII_D RAW SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.113 AIL EE_SII_D RAW CLEAR [Address = 0x3_4A70]

Raw Clear

Figure 8-918. AIL EE_SII_D RAW CLEAR

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1024. AIL EE_SII_D RAW CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.114 AIL EE_SII_D EV0 ENABLE STATUS [Address = 0x3_4A74]

EV0 Enable Status

Figure 8-919. AIL EE_SII_D EV0 ENABLE STATUS

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1025. AIL EE_SII_D EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.115 AIL EE_SII_D EV0 ENABLE SET [Address = 0x3_4A78]

EV0 Enable Set

Figure 8-920. AIL EE_SII_D EV0 ENABLE SET

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1026. AIL EE_SII_D EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.116 AIL EE_SII_D EV0 ENABLE CLEAR [Address = 0x3_4A7C]

EV0 Enable Clear

Figure 8-921. AIL EE_SII_D EV0 ENABLE CLEAR

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1027. AIL EE_SII_D EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.117 AIL EE_SII_D EV1 ENABLE STATUS [Address = 0x3_4A80]

EV1 Enable Status

Figure 8-922. AIL EE_SII_D EV1 ENABLE STATUS

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1028. AIL EE_SII_D EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.118 AIL EE_SII_D EV1 ENABLE SET [Address = 0x3_4A84]

EV1 Enable Set

Figure 8-923. AIL EE_SII_D EV1 ENABLE SET

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1029. AIL EE_SII_D EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.119 AIL EE_SII_D EV1 ENABLE CLEAR [Address = 0x3_4A88]

EV1 Enable Clear

Figure 8-924. AIL EE_SII_D EV1 ENABLE CLEAR

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1030. AIL EE_SII_D EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.120 AIL EE_SII_D EV0 ENABLED STATUS [Address = 0x3_4A8C]

EV0 Enabled Status

Figure 8-925. AIL EE_SII_D EV0 ENABLED STATUS

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1031. AIL EE_SII_D EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.121 AIL EE_SII_D EV1 ENABLED STATUS [Address = 0x3_4A90]

EV1 Enabled Status

Figure 8-926. AIL EE_SII_D EV1 ENABLED STATUS

31	4	3	0
Reserved		SI_ING_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1032. AIL EE_SII_D EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_ING_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.122 AIL EE_SIE_A RAW INTERRUPT STATUS [Address = 0x3_4B18]

SI si_e IQ errors and info.

Figure 8-927. AIL EE_SIE_A RAW INTERRUPT STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1033. AIL EE_SIE_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	SI Egress IQ transmitted data to ICC
3	SI_EGR_IQ_ICC_SOF_INFO	SI Egress IQ transmitted Start of Frame to ICC
2	SI_EGR_IQ_EFE_SYM_ERR	SI Egress IQ EFE symbol number error. (Packet boundary errors due to a missing, early, or late SOP disable the reporting of any symbol errors since the symbol number is only valid for SOPs)
1	SI_EGR_IQ_EFE_PKT_ERR	SI Egress IQ EFE packet boundary error
0	SI_EGR_IQ_EFE_STARVE_ERR	SI Egress IQ EFE data starvation error

8.6.52.123 AIL EE_SIE_A RAW SET [Address = 0x3_4B1C]

Raw Set

Figure 8-928. AIL EE_SIE_A RAW SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1034. AIL EE_SIE_A RAW SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.124 AIL EE_SIE_A RAW CLEAR [Address = 0x3_4B20]

Raw Clear

Figure 8-929. AIL EE_SIE_A RAW CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1035. AIL EE_SIE_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.125 AIL EE_SIE_A EV0 ENABLE STATUS [Address = 0x3_4B24]

EV0 Enable Status

Figure 8-930. AIL EE_SIE_A EV0 ENABLE STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1036. AIL EE_SIE_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.126 AIL EE_SIE_A EV0 ENABLE SET [Address = 0x3_4B28]

EV0 Enable Set

Figure 8-931. AIL EE_SIE_A EV0 ENABLE SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1037. AIL EE_SIE_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.127 AIL EE_SIE_A EV0 ENABLE CLEAR [Address = 0x3_4B2C]

EV0 Enable Clear

Figure 8-932. AIL EE_SIE_A EV0 ENABLE CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1038. AIL EE_SIE_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.128 AIL EE_SIE_A EV1 ENABLE STATUS [Address = 0x3_4B30]

EV1 Enable Status

Figure 8-933. AIL EE_SIE_A EV1 ENABLE STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1039. AIL EE_SIE_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.129 AIL EE_SIE_A EV1 ENABLE SET [Address = 0x3_4B34]

EV1 Enable Set

Figure 8-934. AIL EE_SIE_A EV1 ENABLE SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1040. AIL EE_SIE_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.130 AIL EE_SIE_A EV1 ENABLE CLEAR [Address = 0x3_4B38]

EV1 Enable Clear

Figure 8-935. AIL EE_SIE_A EV1 ENABLE CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1041. AIL EE_SIE_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.131 AIL EE_SIE_A EV0 ENABLED STATUS [Address = 0x3_4B3C]

EV0 Enabled Status

Figure 8-936. AIL EE_SIE_A EV0 ENABLED STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1042. AIL EE_SIE_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.132 AIL EE_SIE_A EV1 ENABLED STATUS [Address = 0x3_4B40]

EV1 Enabled Status

Figure 8-937. AIL EE_SIE_A EV1 ENABLED STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1043. AIL EE_SIE_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.133 AIL EE_SIE_B RAW INTERRUPT STATUS [Address = 0x3_4B44]

SI si_e CTL info.

Figure 8-938. AIL EE_SIE_B RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1044. AIL EE_SIE_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	SI Egress CTL transmitted data to ICC
0	SI_EGR_CTL_ICC_EOP_INFO	SI Egress CTL transmitted EOP to ICC

8.6.52.134 AIL EE_SIE_B RAW SET [Address = 0x3_4B48]

Raw Set

Figure 8-939. AIL EE_SIE_B RAW SET

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1045. AIL EE_SIE_B RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.135 AIL EE_SIE_B RAW CLEAR [Address = 0x3_4B4C]

Raw Clear

Figure 8-940. AIL EE_SIE_B RAW CLEAR

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1046. AIL EE_SIE_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.136 AIL EE_SIE_B EV0 ENABLE STATUS [Address = 0x3_4B50]

EV0 Enable Status

Figure 8-941. AIL EE_SIE_B EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1047. AIL EE_SIE_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.137 AIL EE_SIE_B EV0 ENABLE SET [Address = 0x3_4B54]

EV0 Enable Set

Figure 8-942. AIL EE_SIE_B EV0 ENABLE SET

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1048. AIL EE_SIE_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.138 AIL EE_SIE_B EV0 ENABLE CLEAR [Address = 0x3_4B58]

EV0 Enable Clear

Figure 8-943. AIL EE_SIE_B EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1049. AIL EE_SIE_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.139 AIL EE_SIE_B EV1 ENABLE STATUS [Address = 0x3_4B5C]

EV1 Enable Status

Figure 8-944. AIL EE_SIE_B EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1050. AIL EE_SIE_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.140 AIL EE_SIE_B EV1 ENABLE SET [Address = 0x3_4B60]

EV1 Enable Set

Figure 8-945. AIL EE_SIE_B EV1 ENABLE SET

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1051. AIL EE_SIE_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.141 AIL EE_SIE_B EV1 ENABLE CLEAR [Address = 0x3_4B64]

EV1 Enable Clear

Figure 8-946. AIL EE_SIE_B EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1052. AIL EE_SIE_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_CTL_ICC_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.142 AIL EE_SIE_B EV0 ENABLED STATUS [Address = 0x3_4B68]

EV0 Enabled Status

Figure 8-947. AIL EE_SIE_B EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1053. AIL EE_SIE_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.143 AIL EE_SIE_B EV1 ENABLED STATUS [Address = 0x3_4B6C]

EV1 Enabled Status

Figure 8-948. AIL EE_SIE_B EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_EGR_CTL_ICC_DAT_INFO	SI_EGR_CTL_ICC_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1054. AIL EE_SIE_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_EGR_CTL_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_CTL_ICC_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.144 AIL EE_SIE_C RAW INTERRUPT STATUS [Address = 0x3_4B70]

SI si_e CTL per-channel SOP transmitted to ICC

Figure 8-949. AIL EE_SIE_C RAW INTERRUPT STATUS

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1055. AIL EE_SIE_C RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	SI Egress CTL per channel SOP transmitted to ICC

8.6.52.145 AIL EE_SIE_C RAW SET [Address = 0x3_4B74]

Raw Set

Figure 8-950. AIL EE_SIE_C RAW SET

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1056. AIL EE_SIE_C RAW SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.146 AIL EE_SIE_C RAW CLEAR [Address = 0x3_4B78]

Raw Clear

Figure 8-951. AIL EE_SIE_C RAW CLEAR

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1057. AIL EE_SIE_C RAW CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.6.52.147 AIL EE_SIE_C EV0 ENABLE STATUS [Address = 0x3_4B7C]

EV0 Enable Status

Figure 8-952. AIL EE_SIE_C EV0 ENABLE STATUS

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1058. AIL EE_SIE_C EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.6.52.148 AIL EE_SIE_C EV0 ENABLE SET [Address = 0x3_4B80]

EV0 Enable Set

Figure 8-953. AIL EE_SIE_C EV0 ENABLE SET

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1059. AIL EE_SIE_C EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.149 AIL EE_SIE_C EV0 ENABLE CLEAR [Address = 0x3_4B84]

EV0 Enable Clear

Figure 8-954. AIL EE_SIE_C EV0 ENABLE CLEAR

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1060. AIL EE_SIE_C EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.6.52.150 AIL EE_SIE_C EV1 ENABLE STATUS [Address = 0x3_4B88]

EV1 Enable Status

Figure 8-955. AIL EE_SIE_C EV1 ENABLE STATUS

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1061. AIL EE_SIE_C EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.6.52.151 AIL EE_SIE_C EV1 ENABLE SET [Address = 0x3_4B8C]

EV1 Enable Set

Figure 8-956. AIL EE_SIE_C EV1 ENABLE SET

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1062. AIL EE_SIE_C EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.152 AIL EE_SIE_C EV1 ENABLE CLEAR [Address = 0x3_4B90]

EV1 Enable Clear

Figure 8-957. AIL EE_SIE_C EV1 ENABLE CLEAR

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1063. AIL EE_SIE_C EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.6.52.153 AIL EE_SIE_C EV0 ENABLED STATUS [Address = 0x3_4B94]

EV0 Enabled Status

Figure 8-958. AIL EE_SIE_C EV0 ENABLED STATUS

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1064. AIL EE_SIE_C EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.6.52.154 AIL EE_SIE_C EV1 ENABLED STATUS [Address = 0x3_4B98]

EV1 Enabled Status

Figure 8-959. AIL EE_SIE_C EV1 ENABLED STATUS

31	4	3	0
Reserved		SI_EGR_CTL_ICC_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1065. AIL EE_SIE_C EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-4	Reserved	Reserved.
3-0	SI_EGR_CTL_ICC_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.6.52.155 AIL SYSCLK_ORIG_REG [Address = 0x3_4C20]

This is the sysclk origination register indicating which interrupt register group caused the interrupt.

Figure 8-960. AIL SYSCLK_ORIG_REG

31	24	23	22	21	20
Reserved		ORIG_EE_23	ORIG_EE_22	ORIG_EE_21	ORIG_EE_20
NA-0		R-0	R-0	R-0	R-0
19		18	17	16	15
ORIG_EE_19		ORIG_EE_18	ORIG_EE_17	ORIG_EE_16	ORIG_EE_15
R-0		R-0	R-0	R-0	R-0
14		13	12	11	10
ORIG_EE_14		ORIG_EE_13	ORIG_EE_12	ORIG_EE_11	ORIG_EE_10
R-0		R-0	R-0	R-0	R-0

9	8	7	6	5	4	3	2	1	0
ORIG_EE_9	ORIG_EE_8	ORIG_EE_7	ORIG_EE_6	ORIG_EE_5	ORIG_EE_4	ORIG_EE_3	ORIG_EE_2	ORIG_EE_1	ORIG_EE_0
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1066. AIL SYSCLK_ORIG_REG Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23	ORIG_EE_23	Reserved.
22	ORIG_EE_22	Reserved.
21	ORIG_EE_21	Reserved.
20	ORIG_EE_20	If set a bit is set in the ee_sie_c register.
19	ORIG_EE_19	If set a bit is set in the ee_sie_b register.
18	ORIG_EE_18	If set a bit is set in the ee_sie_a register.
17	ORIG_EE_17	Reserved.
16	ORIG_EE_16	Reserved.
15	ORIG_EE_15	Reserved.
14	ORIG_EE_14	If set a bit is set in the ee_sii_d register.
13	ORIG_EE_13	Reserved.
12	ORIG_EE_12	Reserved.
11	ORIG_EE_11	If set a bit is set in the ee_sii_c_1 register.
10	ORIG_EE_10	If set a bit is set in the ee_sii_c_0 register.
9	ORIG_EE_9	If set a bit is set in the ee_sii_b register.
8	ORIG_EE_8	If set a bit is set in the ee_sii_a register.
7	ORIG_EE_7	If set a bit is set in the ail_si_0 register.
6	ORIG_EE_6	If set a bit is set in the pe_0 register.
5	ORIG_EE_5	Reserved.
4	ORIG_EE_4	Reserved.
3	ORIG_EE_3	If set a bit is set in the pd_2_1 register.
2	ORIG_EE_2	If set a bit is set in the pd_2_0 register.
1	ORIG_EE_1	If set a bit is set in the pd_1 register.
0	ORIG_EE_0	If set a bit is set in the pd_0 register.

8.7 DIO Registers

Table 8-1067. DIO Register Groups

Offset	Acronym	Description	Section
0x0000	DIO2_SI_IQ_EFE_CONFIG_GROUP	Group containing EFE Channel Configuration registers	Section 8.7.1
0x0400	DIO2_SI_IQ_EFE_RADIO _STANDARD_GROUP	Group of registers containing EFE configuration which is radio standard specific. Eight radio standards are supported, individual AxC channels are each assigned to one of these.	Section 8.7.2
0x0600	DIO2_IQ_EFE_CHAN_AXC_OFFSET	Group containing IQ_EFE_CHAN_AXC_OFFSET RAM	Section 8.7.3
0x0800	DIO2_IQ_EFE_FRM_SAMP_TC_MMR _RAM	Group containing Egress Sample Terminal Count Configuration registers	Section 8.7.4
0x0C00	DIO2_IQ_EFE_CHAN_TDM_LUT	Group containing IQ_EFE_CHAN_TDM_LUT RAM	Section 8.7.5
0x1000	DIO2_IQ_EFE_RADIO_STANDARD _SCHEDULER_GROUP	Group containing EFE Channel Scheduler Configuration registers	Section 8.7.6
0x2000	DIO2_IQ_IFE_CHANNEL _CONFIGURATION_GROUP	Group containing IFE Radio Stanadard registers	Section 8.7.7
0x2200	DIO2_IQ_IFE_RADIO _STANDARD_GROUP	Group containing IFE Radio Stanadard registers	Section 8.7.8
0x2340	DIO2_IQ_IFE_CONFIG_GROUP	Group containing IFE Configuration registers	Section 8.7.9
0x2384	DIO2_IQ_IDC_GENERAL_STATUS _GROUP	Group containing IDC Status registers	Section 8.7.10
0x23C0	DIO2_IQ_IDC_CONFIGURATION _GROUP	Group containing IFE Radio Stanadard registers	Section 8.7.11
0x2400	DIO2_IQ_IDC_CHANNEL_CONFIG _GROUP	Group containing IDC Channel Configuration registers	Section 8.7.12
0x2800	DIO2_IFE_FRM_SAMP_TC_MMR _RAM	Group containing Sample Terminal Count Configuration registers	Section 8.7.13
0x5000	DIO2_UAT_GEN_CTL	Run bit for all uAT timers and BCN registers	Section 8.7.14
0x5080	DIO2_UAT_EGR_RADT	Egress RADT registers	Section 8.7.15
0x5100	DIO2_UAT_ING_RADT	Ingress RADT registers	Section 8.7.16
0x5200	DIO2_UAT_RADT_EVT	(Unused for AIL) RADT event compare registers for Frame strobe and iteration strobe counter config for 4sample Iteration strobe. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress	Section 8.7.17
0x5300	DIO2_UAT_DIO_EGR_RADT	(DIO use only) DIO Egress RADT registers. These Radio Timers are used to Pace the DIO DMA start and iteration cycles	Section 8.7.18
0x5340	DIO2_UAT_DIO_ING_RADT	(DIO use only) DIO Ingress RADT registers. These Radio Timers are used to Pace the DIO DMA start and iteration cycles	Section 8.7.19
0x8000	DIO2_IQ_EDC_REGISTER_GROUP	Group containing EDC Configuration registers	Section 8.7.20
0xA000	DIO2_IQ_INGRESS_VBUS_MMR _GROUP	Group containing VBUS Ingress IQ MMR registers	Section 8.7.21
0x1_0000	DIO2_GLOBAL	Group containing GLOBAL configuration registers	Section 8.7.22
0x1_0100	DIO2_CORE_INGRESS	Group containing INGRESS configuration registers	Section 8.7.23
0x1_0200	DIO2_I_AXC_OFF_MMR	Group containing the Ingress AxC offset registers	Section 8.7.24

Table 8-1067. DIO Register Groups (continued)

Offset	Acronym	Description	Section
0x1_0300	DIO2_CORE_EGRESS	Group containing EGRESS configuration registers	Section 8.7.25
0x1_0400	DIO2_DT	Group containing Data Trace configuration registers	Section 8.7.26
0x1_0800	DIO2_I_DBCNT0_RAM_MMR	Group containing Ingress DBCNT0 registers. Table A addressed 0 to 15. Table B addressed 16 to 31	Section 8.7.27
0x1_1000	DIO2_I_DBCNT1_RAM_MMR	Group containing Ingress DBCNT1 registers. Table A addressed 0 to 15. Table B addressed 16 to 31	Section 8.7.28
0x1_1800	DIO2_I_DBCNT2_RAM_MMR	Group containing Ingress DBCNT2 registers. Table A addressed 0 to 15. Table B addressed 16 to 31	Section 8.7.29
0x1_2800	DIO2_E_AOG_RAM_MMR	Group containing the AxC offset registers	Section 8.7.30
0x1_3000	DIO2_E_DBCNT0_RAM_MMR	Group containing Egress DBCNT0 registers. Table A addressed 0 to 15. Table B addressed 16 to 31	Section 8.7.31
0x1_3800	DIO2_E_DBCNT1_RAM_MMR	Group containing Egress DBCNT1 registers. Table A addressed 0 to 15. Table B addressed 16 to 31	Section 8.7.32
0x1_4000	DIO2_E_DBCNT2_RAM_MMR	Group containing Egress DBCNT2 registers. Table A addressed 0 to 15. Table B addressed 16 to 31	Section 8.7.33
0x1_8000	DIO2_EE	IQN_DIO2_EE EE register group	Section 8.7.34

8.7.1 DIO2_SI_IQ_EFE_CONFIG_GROUP [Address = 0x0000]

Table 8-1068. DIO2_SI_IQ_EFE_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x0000	DIO2 IQ EFE CHANNEL CONFIGURATION REGISTER	IFE DMA Channel Configuration Register	Section 8.7.1.1
0x0200	DIO2 IQ EFE CONFIGURATION REGISTER	EFE Rx to Tx Loopback Configuration Register	Section 8.7.1.2
0x0240	DIO2 IQ EFE GLOBAL ENABLE SET REG	Set Global Enable for EFE	Section 8.7.1.3
0x0244	DIO2 IQ EFE GLOBAL ENABLE CLEAR REG	Clear Global Enable for EFE	Section 8.7.1.4
0x0248	DIO2 IQ EFE GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, EFE may still be closing out packets.	Section 8.7.1.5
0x0260	DIO2 IQ EFE CHANNEL ON STATUS REG	Gives current On/Off Status of every available AxC stream. One bit per channel (bit0:ch0 ~ bit31:ch31). Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.7.1.6
0x0280	DIO2 IQ EFE IN PACKET STATUS REGISTERS	Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP. Not used for DIO SI	Section 8.7.1.7
0x02A0	DIO2 IQ EFE DMA SYNC STATUS REGISTERS	Gives current DMA SYNC state of AxC channels only. Bits are always zero for OBSAI control channels. Bit is activated when symbol 0 (non-TDD configuation) or first TDD-ON symbol (TDD configuration) of a frame is read from the Residual Buffer and the channel is in the CHAN_ON state. Bit is deactivated on the next SYM/SLOT boundary when channel is disabled or EFE is shutdown. Bit is deactivated immediately when the channel experiences starvation or a protocol error.	Section 8.7.1.8

8.7.1.1 DIO2 IQ EFE CHANNEL CONFIGURATION REGISTER [Address = 0x0000 + (*S* × 0x0004)]

Size (*S*) = 0:15

IFE DMA Channel Configuration Register

Figure 8-961. DIO2 IQ EFE CHANNEL CONFIGURATION REGISTER

31 15	14 12	11 9	8	7 1	0
Reserved	CHAN_RADIO_SEL	Reserved	CHAN_TDD_FRC_OFF	Reserved	CHAN_EN
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1069. DIO2 IQ EFE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-15	Reserved	RESERVED
14-12	CHAN_RADIO_SEL	Assigns each channel to one of eight radio standard groups. i.e. radio standard 0 may be LTE 20MHz • RS0 (0) = Radio Standard 0 • RS1 (1) = Radio Standard 1 • RS2 (2) = Radio Standard 2 • RS3 (3) = Radio Standard 3 • RS4 (4) = Radio Standard 4 • RS5 (5) = Radio Standard 5 • RS6 (6) = Radio Standard 6 • RS7 (7) = Radio Standard 7
11-9	Reserved	RESERVED
8	CHAN_TDD_FRC_OFF	Alternate TDD mode for controlling TDD also used for GSM Base Band Hopping. APP SW controls updates this bit each symbol of time to control whether the next symbol will be TDD OFF. TDD OFF channels generate no Ingress DMA traffic and expect no Egress DMA traffic. Zeros are sent over the PHY. In BBHop mode, the same applies and in OBSAI, empty_msg is sent over the PHY instead of zeroed traffic • FRC_SYM_OFF (1) = Force symbols off • NO_FRC_OFF_SYM (0) = No forcing off of symbols
7-1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.7.1.2 DIO2 IQ EFE CONFIGURATION REGISTER [Address = 0x0200]

EFE Rx to Tx Loopback Configuration Register

Figure 8-962. DIO2 IQ EFE CONFIGURATION REGISTER

31	1	0
Reserved		LOOPBACK_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1070. DIO2 IQ EFE CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	LOOPBACK_EN	(TI use Only) 0x1: Ingress data from ICC is looped back to Egress data to ICC. DMA traffic is unused. (i.e. for purpose of DFE only testing)

8.7.1.3 DIO2 IQ EFE GLOBAL ENABLE SET REG [Address = 0x0240]

Set Global Enable for EFE

Figure 8-963. DIO2 IQ EFE GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1071. DIO2 IQ EFE GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.7.1.4 DIO2 IQ EFE GLOBAL ENABLE CLEAR REG [Address = 0x0244]

Clear Global Enable for EFE

Figure 8-964. DIO2 IQ EFE GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1072. DIO2 IQ EFE GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.7.1.5 DIO2 IQ EFE GLOBAL ENABLE STATUS [Address = 0x0248]

Read Only status of global enable state. Even if this register is OFF, EFE may still be closing out packets.

Figure 8-965. DIO2 IQ EFE GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1073. DIO2 IQ EFE GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: efe_ON 0x0:efe_OFF

8.7.1.6 DIO2 IQ EFE CHANNEL ON STATUS REG [Address = 0x0260]

Gives current On/Off Status of every available AxC stream. One bit per channel (bit0:ch0 ~ bit31:ch31). Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-966. DIO2 IQ EFE CHANNEL ON STATUS REG

31	16	15	0
Reserved		CHAN_ON	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1074. DIO2 IQ EFE CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.7.1.7 DIO2 IQ EFE IN PACKET STATUS REGISTERS [Address = 0x0280]

Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP. Not used for DIO SI

Figure 8-967. DIO2 IQ EFE IN PACKET STATUS REGISTERS

31	16	15	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1075. DIO2 IQ EFE IN PACKET STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	IN_PKT	0x1: IN_PKT 0x0:OUT_PKT

8.7.1.8 DIO2 IQ EFE DMA SYNC STATUS REGISTERS [Address = 0x02A0]

Gives current DMA SYNC state of AxC channels only. Bits are always zero for OBSAI control channels. Bit is activated when symbol 0 (non-TDD configuation) or first TDD-ON symbol (TDD configuration) of a frame is read from the Residual Buffer and the channel is in the CHAN_ON state. Bit is deactivated on the next SYM/SLOT boundary when channel is disabled or EFE is shutdown. Bit is deactivated immediately when the channel experiences starvation or a protocol error.

Figure 8-968. DIO2 IQ EFE DMA SYNC STATUS REGISTERS

31	16	15	0
Reserved		DMA_SYNC	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1076. DIO2 IQ EFE DMA SYNC STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	DMA_SYNC	0x1: DMA synchronized to radio timing for this channel 0x0:DMA not synchronized to radio timing for this channel. Channel is in in re-sync mode.

8.7.2 DIO2_SI_IQ_EFE_RADIO_STANDARD_GROUP [Address = 0x0400]

Table 8-1077. DIO2_SI_IQ_EFE_RADIO_STANDARD_GROUP

Offset	Acronym	Register Description	Section
0x0400	DIO2 IQ EFE FRAME COUNT REGISTER	EFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants	Section 8.7.2.1
0x0420	DIO2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER	EFE Radio Standard Configuration Register	Section 8.7.2.2
0x0440	DIO2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.3
0x0460	DIO2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.4
0x0480	DIO2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.5
0x04A0	DIO2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.6
0x04C0	DIO2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.7
0x04E0	DIO2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.8
0x0500	DIO2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.9
0x0520	DIO2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.2.10

8.7.2.1 DIO2 IQ EFE FRAME COUNT REGISTER [Address = 0x0400 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants

Figure 8-969. DIO2 IQ EFE FRAME COUNT REGISTER

31 24	23 16	15 8	7 0
Reserved	INDEX_TC	INDEX_SC	SYM_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1078. DIO2 IQ EFE FRAME COUNT REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	INDEX_TC	Radio Framing Counter. Index Counter Terminal Count. Index counter terminal count which is the last value of the Index Counter before it wraps. For simple use case, program same as frm_sym_tc.
15-8	INDEX_SC	Radio Framing Counter. Index Counter Starting Location. Starting location of the Sample Terminal Count LUT loaded into the Index Counter when it first starts and each time it wraps. Depending on the radio standard, the index will wrap once per radio frame such as WCDMA or multiple times per frame as in LTE. Index is the address for XXX_IQ_EFE_FRM_SAMP_TC
7-0	SYM_TC	Radio Framing Counter. Symbol Count. Number of symbols per frame programmed as a terminal count.

8.7.2.2 DIO2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER [Address = 0x0420 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Radio Standard Configuration Register

Figure 8-970. DIO2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER

31	9	8	7	0
Reserved		TDD_LUT_EN	TDD_FIRST_SYM	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1079. DIO2 SI IQ EFE RADIO STANDARD CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	TDD_LUT_EN	Enable use of iq_efe_tdd_en_cfg and use of TDD_FIRST_SYM. Does not impact CHAN_TDD_FRC_OFF operation (which does not use TDD_FIRST_SYM) • ENABLED (1) = TDD enabled for this radio standard • DISABLED (0) = TDD disabled for this radio standard
7-0	TDD_FIRST_SYM	Selects first symbol to start TDD

8.7.2.3 DIO2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT [Address = 0x0440 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-971. DIO2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1080. DIO2 IQ EFE RADIO STANDARD 0 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.4 DIO2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT [Address = 0x0460 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-972. DIO2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1081. DIO2 IQ EFE RADIO STANDARD 1 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.5 DIO2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT [Address = 0x0480 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-973. DIO2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1082. DIO2 IQ EFE RADIO STANDARD 2 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.6 DIO2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT [Address = 0x04A0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-974. DIO2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1083. DIO2 IQ EFE RADIO STANDARD 3 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.7 DIO2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT [Address = 0x04C0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-975. DIO2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1084. DIO2 IQ EFE RADIO STANDARD 4 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.8 DIO2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT [Address = 0x04E0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-976. DIO2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1085. DIO2 IQ EFE RADIO STANDARD 5 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.9 DIO2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT [Address = 0x0500 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-977. DIO2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1086. DIO2 IQ EFE RADIO STANDARD 6 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.2.10 DIO2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT [Address = 0x0520 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-978. DIO2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1087. DIO2 IQ EFE RADIO STANDARD 7 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffffffff for most applications, disabling TDD operation. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.3 DIO2_IQ_EFE_CHAN_AXC_OFFSET [Address = 0x0600 + (R × 0x0004)]

Table 8-1088. DIO2_IQ_EFE_CHAN_AXC_OFFSET

Offset	Acronym	Register Description	Section
0x0600 + (*R* × 0x0004)	DIO2 IQ EFE CHANNEL AXC OFFSET REG	Sets the AXC offset for each channel.	Section 8.7.3.1

8.7.3.1 DIO2 IQ EFE CHANNEL AXC OFFSET REG [Address = 0x0600 + (*R* × 0x0004)]

Range (*R*) = 0:15

Sets the AXC offset for each channel.

Figure 8-979. DIO2 IQ EFE CHANNEL AXC OFFSET REG

31	20	19	0
Reserved		AXC_OFFSET	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1089. DIO2 IQ EFE CHANNEL AXC OFFSET REG Field Descriptions

Bits	Name	Description
31-20	Reserved	RESERVED
19-0	AXC_OFFSET	AxC-by-AxC delay control. Allows different timing alignments for each AxC. DIO & AID: this is a 4 sample offset relative to the group or TDM of AxC. AIL CPRI: this is a sample offset relative to the CPRI AxC Group. AIL OBSAI: this is a Radio Timer compare value (unit is sys_clk). Other than OBSAI, for most customer applications, these fields are programmed as zero.

8.7.4 DIO2_IQ_EFE_FRM_SAMP_TC_MMR_RAM [Address = 0x0800 + (*R* × 0x0004)]

Table 8-1090. DIO2_IQ_EFE_FRM_SAMP_TC_MMR_RAM

Offset	Acronym	Register Description	Section
0x0800 + (*R* × 0x0004)	DIO2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER	EFE AxC Radio Framing Sample Terminal Count Configuration Register	Section 8.7.4.1

8.7.4.1 DIO2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER [Address = 0x0800 + (*R* × 0x0004)]

Range (*R*) = 0:255

EFE AxC Radio Framing Sample Terminal Count Configuration Register

Figure 8-980. DIO2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER

31	18	17	0
Reserved		SAMP_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1091. DIO2 IQ EFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-18	Reserved	Reserved
17-0	SAMP_TC	Radio Framing Counter. Number of samples (4 Bytes) per radio symbol programmed as a terminal count

8.7.5 DIO2_IQ_EFE_CHAN_TDM_LUT [Address = 0x0C00 + (R × 0x0004)]

Table 8-1092. DIO2_IQ_EFE_CHAN_TDM_LUT

Offset	Acronym	Register Description	Section
0x0C00 + (*R* × 0x0004)	DIO2 IQ EFE CHANNEL TDM LUT REG	EFE Channel TDM LUT configuration register	Section 8.7.5.1

8.7.5.1 DIO2 IQ EFE CHANNEL TDM LUT REG [Address = 0x0C00 + (R × 0x0004)]

Range (*R*) = 0:255

EFE Channel TDM LUT configuration register

Figure 8-981. DIO2 IQ EFE CHANNEL TDM LUT REG

31	9	8	7	6	0
Reserved		CHAN_INDEX_EN_CFG	Reserved	CHAN_INDEX_CFG	
NA-0		R/W-0	NA-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1093. DIO2 IQ EFE CHANNEL TDM LUT REG Field Descriptions

Bits	Name	Description
31-9	Reserved	Reserved
8	CHAN_INDEX_EN_CFG	TDM Channel Index LUT Enable
7	Reserved	Reserved
6-0	CHAN_INDEX_CFG	TDM Channel Index

8.7.6 DIO2_IQ_EFE_RADIO_STANDARD_SCHEDULER_GROUP [Address = 0x1000]

Table 8-1094. DIO2_IQ_EFE_RADIO_STANDARD_SCHEDULER_GROUP

Offset	Acronym	Register Description	Section
0x1000	DIO2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER	EFE Radio Standard Scheduler Configuration Register	Section 8.7.6.1

8.7.6.1 DIO2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER [Address = 0x1000 + (*S* × 0x0004)]

Size (*S*) = 0:7

EFE Radio Standard Scheduler Configuration Register

Figure 8-982. DIO2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER

31	17	16	15	8	7	0
Reserved		TDM_EN	TDM_LEN		TDM_START	
NA-0		R/W-0	R/W-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1095. DIO2 IQ EFE RADIO STANDARD SCHEDULER CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-17	Reserved	RESERVED
16	TDM_EN	EFE Scheduler Enable TDM • ENABLED (1) = TDM enabled for this radio standard • DISABLED (0) = TDM disabled for this radio standard
15-8	TDM_LEN	EFE Scheduler TDM Length
7-0	TDM_START	EFE Scheduler TDM Starting address in LUT

8.7.7 DIO2_IQ_IFE_CHANNEL_CONFIGURATION_GROUP [Address = 0x2000]

Table 8-1096. DIO2_IQ_IFE_CHANNEL_CONFIGURATION_GROUP

Offset	Acronym	Register Description	Section
0x2000	DIO2 IQ IFE CHANNEL CONFIGURATION REGISTER	IFE DMA Channel Configuration Register	Section 8.7.7.1

8.7.7.1 DIO2 IQ IFE CHANNEL CONFIGURATION REGISTER [Address = 0x2000 + (*S* × 0x0004)]

Size (*S*) = 0:15

IFE DMA Channel Configuration Register

Figure 8-983. DIO2 IQ IFE CHANNEL CONFIGURATION REGISTER

31 9	8	7	6 4	3 2	1	0
Reserved	CHAN_TDD_FRC_OFF	Reserved	CHAN_RADIO_SEL	CHAN_AXC_OFFSET	Reserved	CHAN_EN
NA-0	R/W-0	NA-0	R/W-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1097. DIO2 IQ IFE CHANNEL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	CHAN_TDD_FRC_OFF	Forces a channel into the TDD OFF state on the next symbol after it is set to a 1 regardless of the TDD configuration of the radio standard variant the channel is assigned to. • FRC_SYM_OFF (1) = Force symbols off • NO_FRC_OFF_SYM (0) = No forcing off of symbols
7	Reserved	RESERVED
6-4	CHAN_RADIO_SEL	Radio Standard Select for channel • RS0 (0) = Radio Standard 0 • RS1 (1) = Radio Standard 1 • RS2 (2) = Radio Standard 2 • RS3 (3) = Radio Standard 3 • RS4 (4) = Radio Standard 4 • RS5 (5) = Radio Standard 5 • RS6 (6) = Radio Standard 6 • RS7 (7) = Radio Standard 7
3-2	CHAN_AXC_OFFSET	Fine AxC Offset within Quad Word • NONE (0) = No offset • ONE (1) = One sample offset • TWO (2) = Two sample offset • THREE (3) = Three sample offset
1	Reserved	RESERVED
0	CHAN_EN	Enable channel • ENABLED (1) = Enable channel • DISABLED (0) = Disable channel

8.7.8 DIO2_IQ_IFE_RADIO_STANDARD_GROUP [Address = 0x2200]

Table 8-1098. DIO2_IQ_IFE_RADIO_STANDARD_GROUP

Offset	Acronym	Register Description	Section
0x2200	DIO2 IQ IFE FRAME COUNT REGISTER	IFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants	Section 8.7.8.1
0x2220	DIO2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER	IFE Radio Standard Configuration Register	Section 8.7.8.2
0x2240	DIO2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.3
0x2260	DIO2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.4
0x2280	DIO2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.5
0x22A0	DIO2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.6
0x22C0	DIO2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.7
0x22E0	DIO2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.8
0x2300	DIO2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.9
0x2320	DIO2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT	Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR	Section 8.7.8.10

8.7.8.1 DIO2 IQ IFE FRAME COUNT REGISTER [Address = 0x2200 + (*S* × 0x0004)]

Size (*S*) = 0:7

IFE Frame Count Register. There are 8 sets of these values in order to support 6 simultaneous radio standard variants

Figure 8-984. DIO2 IQ IFE FRAME COUNT REGISTER

31 24	23 16	15 8	7 0
Reserved	INDEX_TC	INDEX_SC	SYM_TC
NA-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1099. DIO2 IQ IFE FRAME COUNT REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-16	INDEX_TC	Radio Framing Counter. Index Counter Terminal Count. Index counter terminal count which is the last value of the Index Counter before it wraps. For simple use case, program same as frm_sym_tc.
15-8	INDEX_SC	Radio Framing Counter. Index Counter Starting Location. Starting location of the Sample Terminal Count LUT loaded into the Index Counter when it first starts and each time it wraps.
7-0	SYM_TC	Radio Framing Counter. Symbol Count. Number of symbols per frame programmed as a terminal count.

8.7.8.2 DIO2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER [Address = 0x2220 + (*S* × 0x0004)]

Size (*S*) = 0:7

IFE Radio Standard Configuration Register

Figure 8-985. DIO2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER

31	1	0
Reserved		TDD_LUT_EN
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1100. DIO2 IQ IFE RADIO STANDARD CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	TDD_LUT_EN	Enable TDD • ENABLED (1) = TDD enabled for this radio standard • DISABLED (0) = TDD disabled for this radio standard

8.7.8.3 DIO2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT [Address = 0x2240 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 0. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-986. DIO2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1101. DIO2 IQ IFE RADIO STANDARD 0 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.4 DIO2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT [Address = 0x2260 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 1. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-987. DIO2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1102. DIO2 IQ IFE RADIO STANDARD 1 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.5 DIO2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT [Address = 0x2280 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 2. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-988. DIO2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1103. DIO2 IQ IFE RADIO STANDARD 2 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.6 DIO2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT [Address = 0x22A0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 3. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-989. DIO2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1104. DIO2 IQ IFE RADIO STANDARD 3 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.7 DIO2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT [Address = 0x22C0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 4. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-990. DIO2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1105. DIO2 IQ IFE RADIO STANDARD 4 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.8 DIO2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT [Address = 0x22E0 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 5. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-991. DIO2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1106. DIO2 IQ IFE RADIO STANDARD 5 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.9 DIO2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT [Address = 0x2300 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 6. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-992. DIO2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1107. DIO2 IQ IFE RADIO STANDARD 6 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.8.10 DIO2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT [Address = 0x2320 + (*S* × 0x0004)]

Size (*S*) = 0:4

Per symbol enables for TDD operation for Radio Standard 7. 5 MMRs of 32 bits each can accommodate 160 symbols. Enable for symbol 0 in bit 0 of first MMR and enable for symbol 159 in bit 31 of last MMR

Figure 8-993. DIO2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT

31	0
TDD_EN	
R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1108. DIO2 IQ IFE RADIO STANDARD 7 TDD ENABLE LUT Field Descriptions

Bits	Name	Description
31-0	TDD_EN	enables/disables DMA of whole symbols (PktDMA packets). Program as 0xffff for most applications. • SYM_ON (1) = symbol dma enabled • SYM_OFF (0) = symbol dma disabled

8.7.9 DIO2_IQ_IFE_CONFIG_GROUP [Address = 0x2340]

Table 8-1109. DIO2_IQ_IFE_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x2340	DIO2 IQ IFE GLOBAL ENABLE SET REG	Set Global Enable for IFE	Section 8.7.9.1
0x2344	DIO2 IQ IFE GLOBAL ENABLE CLEAR REG	Clear Global Enable for IFE	Section 8.7.9.2
0x2348	DIO2 IQ IFE GLOBAL ENABLE STATUS	Read Only status of global enable state. Even if this register is OFF, IFE may still be closing out packets.	Section 8.7.9.3
0x2350	DIO2 IQ IFE CHANNEL ON STATUS REG	Gives current On/Off Status of every available AxC stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.	Section 8.7.9.4
0x2360	DIO2 IQ IFE IN PACKET STATUS REGISTERS	Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP.	Section 8.7.9.5

8.7.9.1 DIO2 IQ IFE GLOBAL ENABLE SET REG [Address = 0x2340]

Set Global Enable for IFE

Figure 8-994. DIO2 IQ IFE GLOBAL ENABLE SET REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1110. DIO2 IQ IFE GLOBAL ENABLE SET REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which sets (enables) global enable

8.7.9.2 DIO2 IQ IFE GLOBAL ENABLE CLEAR REG [Address = 0x2344]

Clear Global Enable for IFE

Figure 8-995. DIO2 IQ IFE GLOBAL ENABLE CLEAR REG

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1111. DIO2 IQ IFE GLOBAL ENABLE CLEAR REG Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register which clears (enables) global enable

8.7.9.3 DIO2 IQ IFE GLOBAL ENABLE STATUS [Address = 0x2348]

Read Only status of global enable state. Even if this register is OFF, IFE may still be closing out packets.

Figure 8-996. DIO2 IQ IFE GLOBAL ENABLE STATUS

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1112. DIO2 IQ IFE GLOBAL ENABLE STATUS Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: ife_ON 0x0:ife_OFF

8.7.9.4 DIO2 IQ IFE CHANNEL ON STATUS REG [Address = 0x2350]

Gives current On/Off Status of every available AxC stream. One bit per channel. Required because channels only turn on/off on radio frame so the chan_en alone does not give channel status. Chan on/off is not tracked for packet channels; These bits are 0 for packet channels.

Figure 8-997. DIO2 IQ IFE CHANNEL ON STATUS REG

31	16	15	0
Reserved		CHAN_ON	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1113. DIO2 IQ IFE CHANNEL ON STATUS REG Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	CHAN_ON	0x1: CHAN_ON 0x0:CHAN_OFF

8.7.9.5 DIO2 IQ IFE IN PACKET STATUS REGISTERS [Address = 0x2360]

Gives current In/Out packet state of packet channels only. Bits are always zero for AxC channels. Bit is activated at SOP, holds high mid packet, deactivates at EOP.

Figure 8-998. DIO2 IQ IFE IN PACKET STATUS REGISTERS

31	16	15	0
Reserved		IN_PKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1114. DIO2 IQ IFE IN PACKET STATUS REGISTERS Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	IN_PKT	0x1: IN_PKT 0x0:OUT_PKT

8.7.10 DIO2_IQ_IDC_GENERAL_STATUS_GROUP [Address = 0x2384]

Table 8-1115. DIO2_IQ_IDC_GENERAL_STATUS_GROUP

Offset	Acronym	Register Description	Section
0x2384	DIO2 IQ IDC STATUS REGISTER	IDC Status register.	Section 8.7.10.1
0x2390	DIO2 IQ IDC IN PACKET STATUS REGISTER	Indicates when a channel is actively receiving a packet from the IFE	Section 8.7.10.2

8.7.10.1 DIO2 IQ IDC STATUS REGISTER [Address = 0x2384]

IDC Status register.

Figure 8-999. DIO2 IQ IDC STATUS REGISTER

31	1	0
Reserved		EMPTY
NA-0		R-0x0001

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1116. DIO2 IQ IDC STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	EMPTY	Empty indicator for IDC internal FIFOs • FIFO_NOT_EMPTY (0) = FIFOs are not empty • FIFO_EMPTY (1) = FIFOs are empty

8.7.10.2 DIO2 IQ IDC IN PACKET STATUS REGISTER [Address = 0x2390]

Indicates when a channel is actively receiving a packet from the IFE

Figure 8-1000. DIO2 IQ IDC IN PACKET STATUS REGISTER

31	16	15	0
Reserved		INPKT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1117. DIO2 IQ IDC IN PACKET STATUS REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	INPKT	Per-channel in packet status bits where a 0 indicates that the channel is not actively processing a packet and a 1 indicates that it is actively processing a packet. The inpkt to channel assignment is such that inpkt[0] is associated with channel 0 and inpkt[15] is associated with channel 15

8.7.11 DIO2_IQ_IDC_CONFIGURATION_GROUP [Address = 0x23C0]

Table 8-1118. DIO2_IQ_IDC_CONFIGURATION_GROUP

Offset	Acronym	Register Description	Section
0x23C0	DIO2 IQ IDC CONFIGURATION REGISTER	IDC Configuration Register	Section 8.7.11.1

8.7.11.1 DIO2 IQ IDC CONFIGURATION REGISTER [Address = 0x23C0]

IDC Configuration Register

Figure 8-1001. DIO2 IQ IDC CONFIGURATION REGISTER

31	2	1	0
Reserved		FRC_OFF_ALL	FAIL_MARK_ONLY
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1119. DIO2 IQ IDC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved
1	FRC_OFF_ALL	Forces off all Ingress channels without waiting for an end of symbol or time slot. All open packets are automatically closed by creating an EOP for each open packet • FRC_OFF (1) = Force all channels off and close all open packets • NOP (0) = No effect
0	FAIL_MARK_ONLY	Controls how the IDC handles packet errors detected by IFE • DROP (0) = Drop Error packets • MARK (1) = Only Mark Packets With Errors

8.7.12 DIO2_IQ_IDC_CHANNEL_CONFIG_GROUP [Address = 0x2400]

Table 8-1120. DIO2_IQ_IDC_CHANNEL_CONFIG_GROUP

Offset	Acronym	Register Description	Section
0x2400	DIO2 IQ IDC CHANNEL CONFIGURATION REGISTERS	IDC Channel configuration registers.	Section 8.7.12.1

8.7.12.1 DIO2 IQ IDC CHANNEL CONFIGURATION REGISTERS [Address = 0x2400 + (*S* × 0x0004)]

Size (*S*) = 0:15

IDC Channel configuration registers.

Figure 8-1002. DIO2 IQ IDC CHANNEL CONFIGURATION REGISTERS

31 25	24	23 21	20 16	15 6	5 4	3 2	1 0
Reserved	CHAN_FRC_OFF	Reserved	PKT_TYPE	Reserved	IQ_ORDER	Reserved	DAT_SWAP
NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1121. DIO2 IQ IDC CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24	CHAN_FRC_OFF	Forces off all channel without waiting for an end of symbol or time slot. If channel has an open packet it is automatically closed by creating an EOP • FRC_OFF (0) = Force off channel and close an existing open packet • NOP (1) = No effect
23-21	Reserved	RESERVED
20-16	PKT_TYPE	Programmable packet type that is inserted into pkt_type field of PKTDMA Info Word 0.
15-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.7.13 DIO2_IFE_FRM_SAMP_TC_MMR_RAM [Address = 0x2800 + (R × 0x0004)]

Table 8-1122. DIO2_IFE_FRM_SAMP_TC_MMR_RAM

Offset	Acronym	Register Description	Section
0x2800 + (*R* × 0x0004)	DIO2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER	IFE AxC Framing Sample Terminal Count Configuration Register	Section 8.7.13.1

8.7.13.1 DIO2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER [Address = 0x2800 + (R × 0x0004)]

Range (*R*) = 0:255

IFE AxC Framing Sample Terminal Count Configuration Register

Figure 8-1003. DIO2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER

31	18	17	0
Reserved		SAMP_TC	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1123. DIO2 IQ IFE AXC FRAMING SAMPLE TERMINAL COUNT CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-18	Reserved	Reserved
17-0	SAMP_TC	Radio Framing Counter. Number of samples (4 Bytes) per radio symbol programmed as a terminal count

8.7.14 DIO2_UAT_GEN_CTL [Address = 0x5000]

Table 8-1124. DIO2_UAT_GEN_CTL

Offset	Acronym	Register Description	Section
0x5000	DIO2 UAT CONFIG REGISTER	This register simply starts the uAT timers running. It is implied that SW is unable to precisely time the start of timers. The intent is for the SW to correct the timers by later writting to the offset register of each timer.	Section 8.7.14.1
0x5004	DIO2 UAT BCN TERMINAL COUNT REGISTER	UAT BCN terminal count Register	Section 8.7.14.2
0x5008	DIO2 UAT BCN OFFSET REGISTER	UAT BCN offset Register	Section 8.7.14.3
0x500C	DIO2 UAT SYNC BCN CAPTURE REGISTER	UAT SYNC BCN capture Register	Section 8.7.14.4

8.7.14.1 DIO2 UAT CONFIG REGISTER [Address = 0x5000]

This register simply starts the uAT timers running. It is implied that SW is unable to precisely time the start of timers. The intent is for the SW to correct the timers by later writting to the offset register of each timer.

Figure 8-1004. DIO2 UAT CONFIG REGISTER

31	2	1	0
Reserved		DIAG_SYNC	UAT_RUN
NA-0		R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1125. DIO2 UAT CONFIG REGISTER Field Descriptions

Bits	Name	Description
31-2	Reserved	RESERVED
1	DIAG_SYNC	diag_sync = 1 starts the BCN and RAD counters if uat_run is set and an AT sync is received. This is only used in simulation and for diagnostics
0	UAT_RUN	UAT run starts the BCN and RAD counters free running

8.7.14.2 DIO2 UAT BCN TERMINAL COUNT REGISTER [Address = 0x5004]

UAT BCN terminal count Register

Figure 8-1005. DIO2 UAT BCN TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1126. DIO2 UAT BCN TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT BCN terminal count. BCN counts from zero to this limit and wraps to zero. Program as 2,457,599 for sys_clk=245.76MHz and 3,071,999 for sys_clk=307.2MHz

8.7.14.3 DIO2 UAT BCN OFFSET REGISTER [Address = 0x5008]

UAT BCN offset Register

Figure 8-1006. DIO2 UAT BCN OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1127. DIO2 UAT BCN OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	Offset correction to the raw uAT BCN counter. Used to correct the alignment of the local uAT BCN to the master AT2 BCN. BCN is initially randomly started. SW uses uat_sync_bcn_capture_sts rd_val to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.7.14.4 DIO2 UAT SYNC BCN CAPTURE REGISTER [Address = 0x500C]

UAT SYNC BCN capture Register

Figure 8-1007. DIO2 UAT SYNC BCN CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1128. DIO2 UAT SYNC BCN CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	uAT raw BCN value captured each frame boundary of AT2 master BCN. Used to calculate uAT BCN offset value for the purpose of aligning uAT to AT2 BCN.

8.7.15 DIO2_UAT_EGR_RADT [Address = 0x5080 + (R × 0x0010)]

Table 8-1129. DIO2_UAT_EGR_RADT

Offset	Acronym	Register Description	Section
0x5080 + (*R* × 0x0010)	DIO2 UAT RADT TERMINAL COUNT REGISTER	UAT RADT terminal count Register	Section 8.7.15.1
0x5084 + (*R* × 0x0010)	DIO2 UAT RADT OFFSET REGISTER	UAT RADT offset Register	Section 8.7.15.2
0x5088 + (*R* × 0x0010)	DIO2 UAT SYNC RADT CAPTURE REGISTER	UAT SYNC RADT capture Register	Section 8.7.15.3

8.7.15.1 DIO2 UAT RADT TERMINAL COUNT REGISTER [Address = 0x5080 + (R × 0x0010)]

Range (*R*) = 0:7

UAT RADT terminal count Register

Figure 8-1008. DIO2 UAT RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1130. DIO2 UAT RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.7.15.2 DIO2 UAT RADT OFFSET REGISTER [Address = 0x5084 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT offset Register

Figure 8-1009. DIO2 UAT RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1131. DIO2 UAT RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.7.15.3 DIO2 UAT SYNC RADT CAPTURE REGISTER [Address = 0x5088 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT SYNC RADT capture Register

Figure 8-1010. DIO2 UAT SYNC RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1132. DIO2 UAT SYNC RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	UAT RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.7.16 DIO2_UAT_ING_RADT [Address = 0x5100 + (*R* × 0x0010)]

Table 8-1133. DIO2_UAT_ING_RADT

Offset	Acronym	Register Description	Section
0x5100 + (*R* × 0x0010)	DIO2 UAT RADT TERMINAL COUNT REGISTER	UAT RADT terminal count Register	Section 8.7.16.1
0x5104 + (*R* × 0x0010)	DIO2 UAT RADT OFFSET REGISTER	UAT RADT offset Register	Section 8.7.16.2
0x5108 + (*R* × 0x0010)	DIO2 UAT SYNC RADT CAPTURE REGISTER	UAT SYNC RADT capture Register	Section 8.7.16.3

8.7.16.1 DIO2 UAT RADT TERMINAL COUNT REGISTER [Address = 0x5100 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT terminal count Register

Figure 8-1011. DIO2 UAT RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1134. DIO2 UAT RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.7.16.2 DIO2 UAT RADT OFFSET REGISTER [Address = 0x5104 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT RADT offset Register

Figure 8-1012. DIO2 UAT RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1135. DIO2 UAT RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.7.16.3 DIO2 UAT SYNC RADT CAPTURE REGISTER [Address = 0x5108 + (*R* × 0x0010)]

Range (*R*) = 0:7

UAT SYNC RADT capture Register

Figure 8-1013. DIO2 UAT SYNC RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1136. DIO2 UAT SYNC RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	UAT RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.7.17 DIO2_UAT_RADT_EVT [Address = 0x5200 + (R × 0x0008)]

Table 8-1137. DIO2_UAT_RADT_EVT

Offset	Acronym	Register Description	Section
0x5200 + (*R* × 0x0008)	DIO2 UAT RADT EVENT COMPARE REGISTER	UAT RADT event compare Register per RADT. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress	Section 8.7.17.1
0x5204 + (*R* × 0x0008)	DIO2 UAT RADT EVENT CLOCK COUNT TC REGISTER	UAT RADT event clock counter terminal count Register per RADT	Section 8.7.17.2

8.7.17.1 DIO2 UAT RADT EVENT COMPARE REGISTER [Address = 0x5200 + (R × 0x0008)]

Range (*R*) = 0:21

UAT RADT event compare Register per RADT. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

Figure 8-1014. DIO2 UAT RADT EVENT COMPARE REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1138. DIO2 UAT RADT EVENT COMPARE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	UAT RADT event compare per RADT. When compare value equals RADT count, frame rate event is generated. Also periodic event (i.e. 4SAMP) is started. The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

8.7.17.2 DIO2 UAT RADT EVENT CLOCK COUNT TC REGISTER [Address = 0x5204 + (*R* × 0x0008)]

Range (*R*) = 0:21

UAT RADT event clock counter terminal count Register per RADT

Figure 8-1015. DIO2 UAT RADT EVENT CLOCK COUNT TC REGISTER

31	16	15	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1139. DIO2 UAT RADT EVENT CLOCK COUNT TC REGISTER Field Descriptions

Bits	Name	Description
31-16	Reserved	RESERVED
15-0	VAL	UAT RADT event clock counter terminal count controls spacing of the periodic strobe (i.e. 4SAMP). Once the uat_evt_radt_cmp_cfg equals the RADT, the period strobe will fire and re-fire every time a clock counter reaches this terminal count. The The 0 to 7 are for si egress, 8 to 15 for si ingress, 16 to 18 for dio egress, 19 to 21 for dio ingress

8.7.18 DIO2_UAT_DIO_EGR_RADT [Address = 0x5300 + (R × 0x0010)]

Table 8-1140. DIO2_UAT_DIO_EGR_RADT

Offset	Acronym	Register Description	Section
0x5300 + (*R* × 0x0010)	DIO2 UAT DIO EGRESS RADT TERMINAL COUNT REGISTER	UAT DIO egress RADT terminal count Register	Section 8.7.18.1
0x5304 + (*R* × 0x0010)	DIO2 UAT DIO EGRESS RADT OFFSET REGISTER	UAT DIO egress RADT offset Register	Section 8.7.18.2
0x5308 + (*R* × 0x0010)	DIO2 UAT SYNC DIO EGRESS RADT CAPTURE REGISTER	UAT SYNC DIO egress RADT capture Register. RADT timer value is sampled and held in this Register each time the AT2 Master BCN wraps. Used for calculating timing correction offsetRADT count when a uat_mst_slv_sync from the AT occurs. Used by SW to determine correct RADT offset to apply.	Section 8.7.18.3

8.7.18.1 DIO2 UAT DIO EGRESS RADT TERMINAL COUNT REGISTER [Address = 0x5300 + (R × 0x0010)]

Range (*R*) = 0:2

UAT DIO egress RADT terminal count Register

Figure 8-1016. DIO2 UAT DIO EGRESS RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1141. DIO2 UAT DIO EGRESS RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(DIO use only) UAT DIO egress RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.7.18.2 DIO2 UAT DIO EGRESS RADT OFFSET REGISTER [Address = 0x5304 + (*R* × 0x0010)]

Range (*R*) = 0:2

UAT DIO egress RADT offset Register

Figure 8-1017. DIO2 UAT DIO EGRESS RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1142. DIO2 UAT DIO EGRESS RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(DIO use only) UAT DIO egress RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.7.18.3 DIO2 UAT SYNC DIO EGRESS RADT CAPTURE REGISTER [Address = 0x5308 + (*R* × 0x0010)]

Range (*R*) = 0:2

UAT SYNC DIO egress RADT capture Register. RADT timer value is sampled and held in this Register each time the AT2 Master BCN wraps. Used for calculating timing correction offsetRADT count when a uat_mst_slv_sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

Figure 8-1018. DIO2 UAT SYNC DIO EGRESS RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1143. DIO2 UAT SYNC DIO EGRESS RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	(DIO use only)UAT DIO egress RADT sync capture captures the offset RADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

8.7.19 DIO2_UAT_DIO_ING_RADT [Address = 0x5340 + (*R* × 0x0010)]

Table 8-1144. DIO2_UAT_DIO_ING_RADT

Offset	Acronym	Register Description	Section
0x5340 + (*R* × 0x0010)	DIO2 UAT DIO INGRESS RADT TERMINAL COUNT REGISTER	UAT DIO ingress RADT terminal count Register	Section 8.7.19.1
0x5344 + (*R* × 0x0010)	DIO2 UAT DIO INGRESS RADT OFFSET REGISTER	UAT DIO ingress RADT offset Register	Section 8.7.19.2
0x5348 + (*R* × 0x0010)	DIO2 UAT SYNC DIO INGRESS RADT CAPTURE REGISTER	UAT SYNC DIO ingress RADT capture Register. RADT timer value is sampled and held in this Register each time the AT2 Master BCN wraps. Used for calculating timing correction offsetRADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.	Section 8.7.19.3

8.7.19.1 DIO2 UAT DIO INGRESS RADT TERMINAL COUNT REGISTER [Address = 0x5340 + (*R* × 0x0010)]

Range (*R*) = 0:2

UAT DIO ingress RADT terminal count Register

Figure 8-1019. DIO2 UAT DIO INGRESS RADT TERMINAL COUNT REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1145. DIO2 UAT DIO INGRESS RADT TERMINAL COUNT REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(DIO use only) UAT DIO ingress RADT terminal count. (i.e. 2,457,599 for WCDMA with sys_clk=245.76MHz)

8.7.19.2 DIO2 UAT DIO INGRESS RADT OFFSET REGISTER [Address = 0x5344 + (*R* × 0x0010)]

Range (*R*) = 0:2

UAT DIO ingress RADT offset Register

Figure 8-1020. DIO2 UAT DIO INGRESS RADT OFFSET REGISTER

31	25	24	0
Reserved		VAL	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1146. DIO2 UAT DIO INGRESS RADT OFFSET REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	VAL	(DIO use only) UAT DIO ingress RADT offset. Value which is added to the raw RADT as a timing correction. RadT is initially randomly started, SW uses radt_capture value to calculate offset correction factor. This correction factor will be Frame size - captured value.

8.7.19.3 DIO2 UAT SYNC DIO INGRESS RADT CAPTURE REGISTER [Address = 0x5348 + (*R* × 0x0010)]

Range (*R*) = 0:2

UAT SYNC DIO ingress RADT capture Register. RADT timer value is sampled and held in this Register each time the AT2 Master BCN wraps. Used for calculating timing correction offsetRADT count when a master sync from the AT occurs. Used by SW to determine correct RADT offset to apply.

Figure 8-1021. DIO2 UAT SYNC DIO INGRESS RADT CAPTURE REGISTER

31	25	24	0
Reserved		RD_VAL	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1147. DIO2 UAT SYNC DIO INGRESS RADT CAPTURE REGISTER Field Descriptions

Bits	Name	Description
31-25	Reserved	RESERVED
24-0	RD_VAL	(DIO use only) UAT DIO ingress RADT sync capture captures the offset.

8.7.20 DIO2_IQ_EDC_REGISTER_GROUP [Address = 0x8000]

Table 8-1148. DIO2_IQ_EDC_REGISTER_GROUP

Offset	Acronym	Register Description	Section
0x8000	DIO2 IQ EDC CONFIGURATION REGISTER	EDC Configuration Register	Section 8.7.20.1
0x8004	DIO2 IQ EDC SOP COUNTER STATUS REGISTER	Counts the number of SOPs seen by the IQ EDC	Section 8.7.20.2
0x8008	DIO2 IQ EDC EOP COUNTER STATUS REGISTER	Counts the number of EOPs seen by the IQ EDC	Section 8.7.20.3
0x8080	DIO2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER	EDC Status Occupancy counter for each channel register. User can ignore this (TI debug only)	Section 8.7.20.4
0x8200	DIO2 IQ EDC CHANNEL CONFIGURATION REGISTERS	Per-channel configuration registers.	Section 8.7.20.5

8.7.20.1 DIO2 IQ EDC CONFIGURATION REGISTER [Address = 0x8000]

EDC Configuration Register

Figure 8-1022. DIO2 IQ EDC CONFIGURATION REGISTER

31	1	0
Reserved		PSI_ERR_CHK_DISABLE
NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1149. DIO2 IQ EDC CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	Reserved
0	PSI_ERR_CHK_DISABLE	Controls how the EDC handles packet errors detected by efe • DROP (0) = Drop the rest of the packet on errors • NO_DROP (1) = Do not drop packet on errors

8.7.20.2 DIO2 IQ EDC SOP COUNTER STATUS REGISTER [Address = 0x8004]

Counts the number of SOPs seen by the IQ EDC

Figure 8-1023. DIO2 IQ EDC SOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1150. DIO2 IQ EDC SOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	SOP_CNT	Count of the number of SOPs seen by the IQ EDC

8.7.20.3 DIO2 IQ EDC EOP COUNTER STATUS REGISTER [Address = 0x8008]

Counts the number of EOPs seen by the IQ EDC

Figure 8-1024. DIO2 IQ EDC EOP COUNTER STATUS REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1151. DIO2 IQ EDC EOP COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	Reserved
23-0	EOP_CNT	Count of the number of EOPs seen by the IQ EDC

8.7.20.4 DIO2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER [Address = 0x8080 + (*S* × 0x0004)]

Size (*S*) = 0:3

EDC Status Occupancy counter for each channel register. User can ignore this (TI debug only)

Figure 8-1025. DIO2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER

31 24	23 16	15 8	7 0
OCC_CNTR_D	OCC_CNTR_C	OCC_CNTR_B	OCC_CNTR_A
R-0	R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1152. DIO2 IQ EDC OCCUPANCY COUNTER STATUS REGISTER Field Descriptions

Bits	Name	Description
31-24	OCC_CNTR_D	Occupancy Counter for register D for this address
23-16	OCC_CNTR_C	Occupancy Counter for register C for this address
15-8	OCC_CNTR_B	Occupancy Counter for register B for this address
7-0	OCC_CNTR_A	Occupancy Counter for register A for this address

8.7.20.5 DIO2 IQ EDC CHANNEL CONFIGURATION REGISTERS [Address = 0x8200 + (*S* × 0x0004)]

Size (*S*) = 0:15

Per-channel configuration registers.

Figure 8-1026. DIO2 IQ EDC CHANNEL CONFIGURATION REGISTERS

31	6	5	4	3	2	1	0
Reserved		IQ_ORDER		Reserved		DAT_SWAP	
NA-0		R/W-0		NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1153. DIO2 IQ EDC CHANNEL CONFIGURATION REGISTERS Field Descriptions

Bits	Name	Description
31-6	Reserved	RESERVED
5-4	IQ_ORDER	IQ swapping control. • NONE1 (0) = no swap • NONE2 (1) = no swap • BYTE (2) = byte swap • HALF (3) = 16-bit swap
3-2	Reserved	RESERVED
1-0	DAT_SWAP	Byte swapping control. • NONE (0) = no swap • BYTE (1) = byte swap • HALF (2) = half word swap. 16-bit swap • WORD (3) = word swap. 32-bits

8.7.21 DIO2_IQ_INGRESS_VBUS_MMR_GROUP [Address = 0xA000]

Table 8-1154. DIO2_IQ_INGRESS_VBUS_MMR_GROUP

Offset	Acronym	Register Description	Section
0xA000	DIO2 IQ IDC RATE CONTROL CONFIGURATION REGISTER	IDC Rate Control Configuration register. Programmable rate control for OBSAI control word and generic packet mode	Section 8.7.21.1
0xA004	DIO2 IQ IDC SOP COUNTER REGISTER	This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.7.21.2
0xA008	DIO2 IQ IDC EOP COUNTER REGISTER	This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.	Section 8.7.21.3

8.7.21.1 DIO2 IQ IDC RATE CONTROL CONFIGURATION REGISTER [Address = 0xA000]

IDC Rate Control Configuration register. Programmable rate control for OBSAI control word and generic packet mode

Figure 8-1027. DIO2 IQ IDC RATE CONTROL CONFIGURATION REGISTER

31	4	3	0
Reserved		RATE	
NA-0		R/W-0x000F	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1155. DIO2 IQ IDC RATE CONTROL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3-0	RATE	Rate Controller will allow the IDC to create RATE+1 active requests on the PSI bus within a 16 clock cycle window. As an example, a value of 7 will allow the IDC to create 8 active requests within a 16-clock cycle window which uses 50% of the PSI bus.

8.7.21.2 DIO2 IQ IDC SOP COUNTER REGISTER [Address = 0xA004]

This register provides a count of the Ingress SOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-1028. DIO2 IQ IDC SOP COUNTER REGISTER

31	24	23	0
Reserved		SOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1156. DIO2 IQ IDC SOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	SOP_CNT	Wrapping count of SOPs sent on PSI.

8.7.21.3 DIO2 IQ IDC EOP COUNTER REGISTER [Address = 0xA008]

This register provides a count of the Ingress EOPs sent on the PSI to the IQN2 buffer or switch for activity monitoring.

Figure 8-1029. DIO2 IQ IDC EOP COUNTER REGISTER

31	24	23	0
Reserved		EOP_CNT	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1157. DIO2 IQ IDC EOP COUNTER REGISTER Field Descriptions

Bits	Name	Description
31-24	Reserved	RESERVED
23-0	EOP_CNT	Wrapping count of EOPs sent on PSI.

8.7.22 DIO2_GLOBAL [Address = 0x1_0000]

Table 8-1158. DIO2_GLOBAL

Offset	Acronym	Register Description	Section
0x1_0000	DIO2 DIO INGRESS GLOBAL ENABLE SET REGISTER	The Set Global Enable for Ingress DIO. A write of any value to this register sets the global enable for the Ingress DIO.	Section 8.7.22.1
0x1_0004	DIO2 DIO INGRESS GLOBAL ENABLE CLEAR REGISTER	Clear Global Enable for Ingress DIO. A write of any value to this register clears the global enable for the Ingress DIO.	Section 8.7.22.2
0x1_0008	DIO2 DIO INGRESS GLOBAL ENABLE STATUS REGISTER	This register is Read Only and provides the status of the Ingress DIO global enable state.	Section 8.7.22.3
0x1_0010	DIO2 DIO EGRESS GLOBAL ENABLE SET REGISTER	Set Global Enable for Egress DIO. A write of any value to this register sets the global enable for the Egress DIO..	Section 8.7.22.4
0x1_0014	DIO2 DIO EGRESS GLOBAL ENABLE CLEAR REGISTER	Clear Global Enable for Egress DIO. A write of any value to this register clears the global enable for the Egress DIO.	Section 8.7.22.5
0x1_0018	DIO2 DIO EGRESS GLOBAL ENABLE STATUS REGISTER	This register is Read Only and provides the status of the Egress DIO global enable state.	Section 8.7.22.6
0x1_0020	DIO2 DIO DATA TRACE GLOBAL ENABLE SET REGISTER	Set Global Enable for Data Trace DIO. A write of any value to this register sets the global enable for the Data Trace DIO.	Section 8.7.22.7
0x1_0024	DIO2 DIO DATA TRACE GLOBAL ENABLE CLEAR REGISTER	Clear Global Enable for Data Trace DIO. A write of any value to this register clears the global enable for the Data Trace DIO.	Section 8.7.22.8
0x1_0028	DIO2 DIO DATA TRACE GLOBAL ENABLE STATUS REGISTER	This register is Read Only and provides the status of the Data Trace DIO global enable state.	Section 8.7.22.9
0x1_0040	DIO2 DIO GLOBAL CONFIGURATION REGISTER	The DIO Global Configuration Register allows the user to select priority on the VBUSM as well as control the Endianess of RSA Data Format Conversian	Section 8.7.22.10

8.7.22.1 DIO2 DIO INGRESS GLOBAL ENABLE SET REGISTER [Address = 0x1_0000]

The Set Global Enable for Ingress DIO. A write of any value to this register sets the global enable for the Ingress DIO.

Figure 8-1030. DIO2 DIO INGRESS GLOBAL ENABLE SET REGISTER

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1159. DIO2 DIO INGRESS GLOBAL ENABLE SET REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register sets the global enable for the Ingress DIO

8.7.22.2 DIO2 DIO INGRESS GLOBAL ENABLE CLEAR REGISTER [Address = 0x1_0004]

Clear Global Enable for Ingress DIO. A write of any value to this register clears the global enable for the Ingress DIO.

Figure 8-1031. DIO2 DIO INGRESS GLOBAL ENABLE CLEAR REGISTER

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1160. DIO2 DIO INGRESS GLOBAL ENABLE CLEAR REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register clears the global enable for the Ingress DIO

8.7.22.3 DIO2 DIO INGRESS GLOBAL ENABLE STATUS REGISTER [Address = 0x1_0008]

This register is Read Only and provides the status of the Ingress DIO global enable state.

Figure 8-1032. DIO2 DIO INGRESS GLOBAL ENABLE STATUS REGISTER

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1161. DIO2 DIO INGRESS GLOBAL ENABLE STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: Ingress DIO ON 0x0:Ingress DIO OFF

8.7.22.4 DIO2 DIO EGRESS GLOBAL ENABLE SET REGISTER [Address = 0x1_0010]

Set Global Enable for Egress DIO. A write of any value to this register sets the global enable for the Egress DIO..

Figure 8-1033. DIO2 DIO EGRESS GLOBAL ENABLE SET REGISTER

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1162. DIO2 DIO EGRESS GLOBAL ENABLE SET REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register sets the global enable for the Egress DIO

8.7.22.5 DIO2 DIO EGRESS GLOBAL ENABLE CLEAR REGISTER [Address = 0x1_0014]

Clear Global Enable for Egress DIO. A write of any value to this register clears the global enable for the Egress DIO.

Figure 8-1034. DIO2 DIO EGRESS GLOBAL ENABLE CLEAR REGISTER

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1163. DIO2 DIO EGRESS GLOBAL ENABLE CLEAR REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register clears the global enable for the Egress DIO

8.7.22.6 DIO2 DIO EGRESS GLOBAL ENABLE STATUS REGISTER [Address = 0x1_0018]

This register is Read Only and provides the status of the Egress DIO global enable state.

Figure 8-1035. DIO2 DIO EGRESS GLOBAL ENABLE STATUS REGISTER

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1164. DIO2 DIO EGRESS GLOBAL ENABLE STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: Egress DIO ON 0x0:Egress DIO OFF

8.7.22.7 DIO2 DIO DATA TRACE GLOBAL ENABLE SET REGISTER [Address = 0x1_0020]

Set Global Enable for Data Trace DIO. A write of any value to this register sets the global enable for the Data Trace DIO.

Figure 8-1036. DIO2 DIO DATA TRACE GLOBAL ENABLE SET REGISTER

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

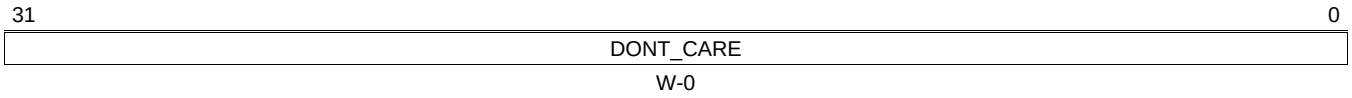
Table 8-1165. DIO2 DIO DATA TRACE GLOBAL ENABLE SET REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register sets the global enable for the Data Trace DIO

8.7.22.8 DIO2 DIO DATA TRACE GLOBAL ENABLE CLEAR REGISTER [Address = 0x1_0024]

Clear Global Enable for Data Trace DIO. A write of any value to this register clears the global enable for the Data Trace DIO.

Figure 8-1037. DIO2 DIO DATA TRACE GLOBAL ENABLE CLEAR REGISTER



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1166. DIO2 DIO DATA TRACE GLOBAL ENABLE CLEAR REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register clears the global enable for the Data Trace DIO

8.7.22.9 DIO2 DIO DATA TRACE GLOBAL ENABLE STATUS REGISTER [Address = 0x1_0028]

This register is Read Only and provides the status of the Data Trace DIO global enable state.

Figure 8-1038. DIO2 DIO DATA TRACE GLOBAL ENABLE STATUS REGISTER

31	1	0
Reserved		ENABLE
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1167. DIO2 DIO DATA TRACE GLOBAL ENABLE STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	ENABLE	0x1: Data Trace DIO ON 0x0:Data Trace DIO OFF

8.7.22.10 DIO2 DIO GLOBAL CONFIGURATION REGISTER [Address = 0x1_0040]

The DIO Global Configuration Register allows the user to select priority on the VBUSM as well as control the Endianess of RSA Data Format Conversian

Figure 8-1039. DIO2 DIO GLOBAL CONFIGURATION REGISTER

31	9	8	7	3	2	0
Reserved		RSA_BIG_ENDIAN	Reserved		VBUSM_PRIORITY	
NA-0		R/W-0	NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1168. DIO2 DIO GLOBAL CONFIGURATION REGISTER Field Descriptions

Bits	Name	Description
31-9	Reserved	RESERVED
8	RSA_BIG_ENDIAN	Sets RSA Data Format Conversian Endianess • RSALTL (0) = Selects little endian • RSABIG (1) = Selects big endian
7-3	Reserved	RESERVED
2-0	VBUSM_PRIORITY	Sets vbusm priority for both reads and writes (priority 0 = highest,7 = lowest, reset value = 0 (highest priority))

8.7.23 DIO2_CORE_INGRESS [Address = 0x1_0100 + (*R* × 0x0040)]

Table 8-1169. DIO2_CORE_INGRESS

Offset	Acronym	Register Description	Section
0x1_0100 + (*R* × 0x0040)	DIO2 DIO INGRESS TABLE SELECT REGISTER	This register selects which table to use so that channels may be added or deleted for Ingress.Programmed at the same time is the number of AxCs referenced in the table. The user indicates to the DMA engine, which table is to be active during the next frame. When bcn_table_sel =0, Table A is selected and when bcn_table_sel=1, Table B is selected.The non-selected table may be written any time between frame boundary strobes from the uAT. Switching tables, must be done in the middle, between frame boundary strobes in order to assure that the new table takes effect in the next frame	Section 8.7.23.1
0x1_0104 + (*R* × 0x0040)	DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 0	This register alows the user to program the number of quad words in a burst,the number of quad words per AxC and the number of data blocks to transfer before wrapping back to dma_base_addr for Ingress. This register also allows the user to enable RSA mode and the DMA engine itself.	Section 8.7.23.2
0x1_0108 + (*R* × 0x0040)	DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 1	This register enables the user to set the DMA block address stride between block transfers for Ingress.	Section 8.7.23.3

8.7.23.1 DIO2 DIO INGRESS TABLE SELECT REGISTER [Address = 0x1_0100 + (*R* × 0x0040)]

Range (*R*) = 0:2

This register selects which table to use so that channels may be added or deleted for Ingress.Programmed at the same time is the number of AxCs referenced in the table.

The user indicates to the DMA engine, which table is to be active during the next frame.

When bcn_table_sel =0, Table A is selected and when bcn_table_sel=1, Table B is selected.The non-selected table may be written any time between frame boundary strobes from the uAT. Switching tables, must be done in the middle, between frame boundary strobes in order to assure that the new table takes effect in the next frame

Figure 8-1040. DIO2 DIO INGRESS TABLE SELECT REGISTER

31	12	11	8	7	1	0
Reserved		DMA_NUM_AXC		Reserved		BCN_TABLE_SEL
NA-0		R/W-0		NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1170. DIO2 DIO INGRESS TABLE SELECT REGISTER Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-8	DMA_NUM_AXC	Sets the number of AxCs (Set N-1).
7-1	Reserved	RESERVED
0	BCN_TABLE_SEL	Selects which buffer channel number table for the DMA engine to use • TABLE_A (0) = Selects buffer channel number table A (addressed from 0 to N/2-1) • TABLE_B (1) = Selects buffer channel number table B (addressed from N/2 to N-1)

8.7.23.2 DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 0 [Address = 0x1_0104 + (*R* × 0x0040)]

Range (*R*) = 0:2

This register alows the user to program the number of quad words in a burst,the number of quad words per AxC and the number of data blocks to transfer before wrapping back to dma_base_addr for Ingress.

This register also allows the user to enable RSA mode and the DMA engine itself.

Figure 8-1041. DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 0

31 29	28 16	15 10	9
Reserved	DMA_NUM_BLKS	Reserved	DMA_ENG_EN
NA-0	R/W-0	NA-0	R/W-0

8	7 6	5 4	3 2	1 0
RSA_CNVRT_EN	Reserved	DMA_NUM_QWD	Reserved	DMA_BRST_LN
R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1171. DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 0 Field Descriptions

Bits	Name	Description
31-29	Reserved	RESERVED
28-16	DMA_NUM_BLKS	Set the number of data blocks to transfer before wrapping back to dma_base_addr(Set N-1). Note: (num_blks + 1) must be an even number.
15-10	Reserved	RESERVED
9	DMA_ENG_EN	Enable DMA engine. • DMACLR (0) = DMA engine disabled i.e. cleared state • DMAEN (1) = DMA engine enabled
8	RSA_CNVRT_EN	Ingress RSA data conversion enable per DMA engine. • NORSA (0) = RSA Data Format Conversion Disabled • RSAEN (1) = RSA Data Format Conversion Enabled
7-6	Reserved	RESERVED
5-4	DMA_NUM_QWD	Sets the number of quad words per AxC. • 1QUAD (0) = 1 quad word per AxC • 2QUAD (1) = 2 quad word per AxC • 4QUAD (2) = 4 quad word per AxC
3-2	Reserved	RESERVED
1-0	DMA_BRST_LN	Sets the maximum DMA burst length. • 1QUAD (0) = 1 quad word transferred per burst • 2QUAD (1) = 2 quad words transferred per burst • 4QUAD (2) = 4 quad words transferred per burst

8.7.23.3 DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 1 [Address = 0x1_0108 + (*R* × 0x0040)]

Range (*R*) = 0:2

This register enables the user to set the DMA block address stride between block transfers for Ingress.

Figure 8-1042. DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 1

31	12	11	0
Reserved		DMA_BLK_ADDR_STRIDE	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1172. DIO2 DIO INGRESS DMA CONFIGURATION REGISTER 1 Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	DMA_BLK_ADDR_STRIDE	Sets the DMA block address stride (in multiples of 0x10).

8.7.24 DIO2_I_AXC_OFF_MMR [Address = 0x1_0200 + (R × 0x0004)]

Table 8-1173. DIO2_I_AXC_OFF_MMR

Offset	Acronym	Register Description	Section
0x1_0200 + (*R* × 0x0004)	DIO2 DIO INGRESS AXC OFFSET REG	A per-channel, Modulo 8 AxC offset in 4 sample (like DIO offset in AIF2) i.e. 1 QW increments that determine the starting address within a circular data buffer. e.g. a value of 0 would cause zero offset. A value of 1 would cause a 4 sample offset. A value of 0 would also represent an offset of 8, 16, etc.	Section 8.7.24.1

8.7.24.1 DIO2 DIO INGRESS AXC OFFSET REG [Address = 0x1_0200 + (R × 0x0004)]

Range (*R*) = 0:15

A per-channel, Modulo 8 AxC offset in 4 sample (like DIO offset in AIF2)

i.e. 1 QW increments that determine the starting address within a circular data buffer.

e.g. a value of 0 would cause zero offset. A value of 1 would cause a 4 sample offset. A value of 0 would also represent an offset of 8, 16, etc.

Figure 8-1043. DIO2 DIO INGRESS AXC OFFSET REG

31	3	2	0
Reserved		DIO_I_AXC_4SAMP_OFFSET	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1174. DIO2 DIO INGRESS AXC OFFSET REG Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved
2-0	DIO_I_AXC_4SAMP_OFFSET	DIO Ingress AxC offset within a circular buffer.

8.7.25 DIO2_CORE_EGRESS [Address = 0x1_0300 + (*R* × 0x0040)]

Table 8-1175. DIO2_CORE_EGRESS

Offset	Acronym	Register Description	Section
0x1_0300 + (*R* × 0x0040)	DIO2 DIO EGRESS TABLE SELECT REGISTER	This register selects which table to use so that channels may be added or deleted for Egress. Programmed at the same time is the number of AxCs referenced in the table. The user indicates to the DMA engine, which table is to be active during the next frame. When bcn_table_sel =0, Table A is selected and when bcn_table_sel=1, Table B is selected. The non-selected table may be written any time between frame boundary strobes from the uAT. Switching tables, must be done in the middle, between frame boundary strobes in order to assure that the new table takes effect in the next frame.	Section 8.7.25.1
0x1_0304 + (*R* × 0x0040)	DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 0	This register alows the user to program the number of quad words in a burst, the number of quad words per AxC and the number of data blocks to transfer before wrapping back to dma_base_addr for Egress. This register also allows the user to enable RSA mode and the DMA engine itself.	Section 8.7.25.2
0x1_0308 + (*R* × 0x0040)	DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 1	This register enables the user to set the DMA block address stride between block transfers for Egress.	Section 8.7.25.3

8.7.25.1 DIO2 DIO EGRESS TABLE SELECT REGISTER [Address = 0x1_0300 + (*R* × 0x0040)]

Range (*R*) = 0:2

This register selects which table to use so that channels may be added or deleted for Egress. Programmed at the same time is the number of AxCs referenced in the table.

The user indicates to the DMA engine, which table is to be active during the next frame.

When bcn_table_sel =0, Table A is selected and when bcn_table_sel=1, Table B is selected. The non-selected table may be written any time between frame boundary strobes from the uAT. Switching tables, must be done in the middle, between frame boundary strobes in order to assure that the new table takes effect in the next frame.

Figure 8-1044. DIO2 DIO EGRESS TABLE SELECT REGISTER

31	12	11	8	7	1	0
Reserved		DMA_NUM_AXC		Reserved		BCN_TABLE_SEL
NA-0		R/W-0		NA-0		R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1176. DIO2 DIO EGRESS TABLE SELECT REGISTER Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-8	DMA_NUM_AXC	Sets the number of AxCs (Set N-1).
7-1	Reserved	RESERVED
0	BCN_TABLE_SEL	Selects which buffer channel number table for the DMA engine to use • TABLE_A (0) = Selects buffer channel number table A (addressed from 0 to N/2-1) • TABLE_B (1) = Selects buffer channel number table B (addressed from N/2 to N-1)

8.7.25.2 DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 0 [Address = 0x1_0304 + (*R* × 0x0040)]

Range (*R*) = 0:2

This register alows the user to program the number of quad words in a burst, the number of quad words per AxC and the number of data blocks to transfer before wrapping back to dma_base_addr for Egress.

This register also allows the user to enable RSA mode and the DMA engine itself.

Figure 8-1045. DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 0

31 29	28 16	15 10	9
Reserved	DMA_NUM_BLKS	Reserved	DMA_ENG_EN
NA-0	R/W-0	NA-0	R/W-0

8	7 6	5 4	3 2	1 0
RSA_CNVRT_EN	Reserved	DMA_NUM_QWD	Reserved	DMA_BRST_LN
R/W-0	NA-0	R/W-0	NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1177. DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 0 Field Descriptions

Bits	Name	Description
31-29	Reserved	RESERVED
28-16	DMA_NUM_BLKS	Set the number of data blocks to transfer before wrapping back to dma_base_addr. (Set N-1). Note: (num_blks + 1) must be an even number.
15-10	Reserved	RESERVED
9	DMA_ENG_EN	Enable DMA engine. • DMACLR (0) = DMA engine disabled i.e. cleared state • DMAEN (1) = DMA engine enabled
8	RSA_CNVRT_EN	Egress RSA data conversion enable per channel. • NORSA (0) = RSA Data Format Conversion Disabled • RSAEN (1) = RSA Data Format Conversion Enabled
7-6	Reserved	RESERVED
5-4	DMA_NUM_QWD	Sets the number of quad words per AxC. • 1QUAD (0) = 1 quad word per AxC • 2QUAD (1) = 2 quad word per AxC • 4QUAD (2) = 4 quad word per AxC
3-2	Reserved	RESERVED
1-0	DMA_BRST_LN	Sets the maximum DMA burst length. • 1QUAD (0) = 1 quad word transferred per burst • 2QUAD (1) = 2 quad words transferred per burst • 4QUAD (2) = 4 quad words transferred per burst

8.7.25.3 DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 1 [Address = 0x1_0308 + (*R* × 0x0040)]

Range (*R*) = 0:2

This register enables the user to set the DMA block address stride between block transfers for Egress.

Figure 8-1046. DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 1

31	12	11	0
Reserved		DMA_BLK_ADDR_STRIDE	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1178. DIO2 DIO EGRESS DMA CONFIGURATION REGISTER 1 Field Descriptions

Bits	Name	Description
31-12	Reserved	RESERVED
11-0	DMA_BLK_ADDR_STRIDE	Sets the DMA block address stride (in multiples of 0x10).

8.7.26 DIO2_DT [Address = 0x1_0400]

Table 8-1179. DIO2_DT

Offset	Acronym	Register Description	Section
0x1_0400	DIO2 DIO DATA TRACE CONFIGURATION REGISTER 0	This register allows the user to program the various mode of Data Trace operation	Section 8.7.26.1
0x1_0404	DIO2 DIO DATA TRACE CONFIGURATION REGISTER 1	This register allows the user to program the destination VBUS base address for Data Trace.	Section 8.7.26.2
0x1_0408	DIO2 DIO DATA TRACE CONFIGURATION REGISTER 2	This register allows the user to program the number of burst transfers before the destination address wraps back to the base address for Data Trace	Section 8.7.26.3
0x1_040C	DIO2 DIO DATA TRACE START REGISTER	A write of any value to this register will start Data Trace operation if dt_en = 1.	Section 8.7.26.4
0x1_0410	DIO2 DIO DATA TRACE OPERATIONAL STATUS REGISTER	Read Only status of Data Trace operational state.	Section 8.7.26.5

8.7.26.1 DIO2 DIO DATA TRACE CONFIGURATION REGISTER 0 [Address = 0x1_0400]

This register allows the user to program the various mode of Data Trace operation

Figure 8-1047. DIO2 DIO DATA TRACE CONFIGURATION REGISTER 0

31	4	3	2	1	0
Reserved		DT_ENDIAN_SEL	DT_STOP_MODE	DT_START_MODE	DT_EN
NA-0		R/W-0	R/W-0	R/W-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1180. DIO2 DIO DATA TRACE CONFIGURATION REGISTER 0 Field Descriptions

Bits	Name	Description
31-4	Reserved	RESERVED
3	DT_ENDIAN_SEL	Selects Data Trace Endian mode. • BIG (0) = Data Trace data in Big Endian format (default) • LITTLE (1) = Data Trace data in Little Endian format.
2	DT_STOP_MODE	Selects Data Trace stopping mode. • CIRCULAR (0) = Writes data in a circular fashion and overwriting previously written data until Data Trace is disabled • ONESHOT (1) = Data is captured until the end of the external buffer (dio_dt_cfg2.dt_dma_wrap) is reached, then stops capturing data. The EE event dio_ee_dt_done_info may be used to signal to software when Data Trace has finished capturing data.
1	DT_START_MODE	Selects Data Trace start operating mode. • CAPRAW (0) = Raw Data (i.e. unframed) is captured starting when Data Trace is Enable • CAPSOF (1) = Data is captured when Start Of Frame is received
0	DT_EN	Enables Data Trace DMA • NODT (0) = Data Trace DMA disabled (cleared state) • DTEN (1) = Data Trace DMA enabled (and wait dt start strobe)

8.7.26.2 DIO2 DIO DATA TRACE CONFIGURATION REGISTER 1 [Address = 0x1_0404]

This register allows the user to program the destination VBUS base address for Data Trace.

Figure 8-1048. DIO2 DIO DATA TRACE CONFIGURATION REGISTER 1

31	28	27	0
Reserved		DT_DMA_BASE_ADDR	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1181. DIO2 DIO DATA TRACE CONFIGURATION REGISTER 1 Field Descriptions

Bits	Name	Description
31-28	Reserved	RESERVED
27-0	DT_DMA_BASE_ADDR	Sets the destination VBUS base address (upper 28 bits of 32 bit data bus) for data trace receive data. The base address must be programmed BEFORE dt_en is set.

8.7.26.3 DIO2 DIO DATA TRACE CONFIGURATION REGISTER 2 [Address = 0x1_0408]

This register allows the user to program the number of burst transfers before the destination address wraps back to the base address for Data Trace

Figure 8-1049. DIO2 DIO DATA TRACE CONFIGURATION REGISTER 2

31	18	17	0
Reserved		DT_DMA_WRAP	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1182. DIO2 DIO DATA TRACE CONFIGURATION REGISTER 2 Field Descriptions

Bits	Name	Description
31-18	Reserved	RESERVED
17-0	DT_DMA_WRAP	Sets the number of burst transfers before the destination address wraps back to the base address. Each burst transfer is 4 Quad Words.

8.7.26.4 DIO2 DIO DATA TRACE START REGISTER [Address = 0x1_040C]

A write of any value to this register will start Data Trace operation if dt_en = 1.

Figure 8-1050. DIO2 DIO DATA TRACE START REGISTER

31	0
DONT_CARE	
W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1183. DIO2 DIO DATA TRACE START REGISTER Field Descriptions

Bits	Name	Description
31-0	DONT_CARE	A write of any value to this register will start Data Trace operation if dt_en = 1.

8.7.26.5 DIO2 DIO DATA TRACE OPERATIONAL STATUS REGISTER [Address = 0x1_0410]

Read Only status of Data Trace operational state.

Figure 8-1051. DIO2 DIO DATA TRACE OPERATIONAL STATUS REGISTER

31	1	0
Reserved		DT_IN_PROGRESS
NA-0		R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1184. DIO2 DIO DATA TRACE OPERATIONAL STATUS REGISTER Field Descriptions

Bits	Name	Description
31-1	Reserved	RESERVED
0	DT_IN_PROGRESS	0x0:Data Trace DIO Idle 0x1: Data Trace DIO data capture in progress

8.7.27 DIO2_I_DBCNT0_RAM_MMR [Address = 0x1_0800 + (*R* × 0x0008)]

Table 8-1185. DIO2_I_DBCNT0_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_0800 + (*R* × 0x0008)	DIO2 DIO INGRESS DBCNT0 BASE ADDRESS REG	A per AxC register that is a field in the DIO Ingress DBCNT 0 LUT that enables the user to program the associated AxC's destination VBUS base address. This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.	Section 8.7.27.1
0x1_0804 + (*R* × 0x0008)	DIO2 DIO INGRESS DBCNT0 CONTROL REG	A per AxC register that is a field in the DIO Ingress DBCNT 0 LUT that enables the user to program the associated AxC's channel ID and channel enable.	Section 8.7.27.2

8.7.27.1 DIO2 DIO INGRESS DBCNT0 BASE ADDRESS REG [Address = 0x1_0800 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Ingress DBCNT 0 LUT that enables the user to program the associated AxC's destination VBUS base address.

This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.

Figure 8-1052. DIO2 DIO INGRESS DBCNT0 BASE ADDRESS REG

31 28	27 0
Reserved	DMA_VBUS_BASE_ADDR_AXC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1186. DIO2 DIO INGRESS DBCNT0 BASE ADDRESS REG Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved
27-0	DMA_VBUS_BASE_ADDR_AXC	DIO Ingress DBCNT 0 - Per AxC VBUS Base address Register

8.7.27.2 DIO2 DIO INGRESS DBCNT0 CONTROL REG [Address = 0x1_0804 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Ingress DBCNT 0 LUT that enables the user to program the associated AxC's channel ID and channel enable.

Figure 8-1053. DIO2 DIO INGRESS DBCNT0 CONTROL REG

31	8	7	6	0
Reserved		CH_EN	CH_ID	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1187. DIO2 DIO INGRESS DBCNT0 CONTROL REG Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	CH_EN	DIO Ingress DBCNT 0 - Channel Enable Register
6-0	CH_ID	DIO Ingress DBCNT 0 - Channel ID Register

8.7.28 DIO2_I_DBCNT1_RAM_MMR [Address = 0x1_1000 + (R × 0x0008)]

Table 8-1188. DIO2_I_DBCNT1_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_1000 + (*R* × 0x0008)	DIO2 DIO INGRESS DBCNT1 BASE ADDRESS REG	A per AxC register that is a field in the DIO Ingress DBCNT 1 LUT that enables the user to program the associated AxC's destination VBUS base address. This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.	Section 8.7.28.1
0x1_1004 + (*R* × 0x0008)	DIO2 DIO INGRESS DBCNT1 CONTROL REG	A per AxC register that is a field in the DIO Ingress DBCNT 1 LUT that enables the user to program the associated AxC's channel ID and channel enable.	Section 8.7.28.2

8.7.28.1 DIO2 DIO INGRESS DBCNT1 BASE ADDRESS REG [Address = 0x1_1000 + (R × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Ingress DBCNT 1 LUT that enables the user to program the associated AxC's destination VBUS base address.

This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.

Figure 8-1054. DIO2 DIO INGRESS DBCNT1 BASE ADDRESS REG

31 28	27 0
Reserved	DMA_VBUS_BASE_ADDR_AXC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1189. DIO2 DIO INGRESS DBCNT1 BASE ADDRESS REG Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved
27-0	DMA_VBUS_BASE_ADDR_AXC	DIO Ingress DBCNT 1 - Per AxC VBUS Base address Register

8.7.28.2 DIO2 DIO INGRESS DBCNT1 CONTROL REG [Address = 0x1_1004 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Ingress DBCNT 1 LUT that enables the user to program the associated AxC's channel ID and channel enable.

Figure 8-1055. DIO2 DIO INGRESS DBCNT1 CONTROL REG

31	8	7	6	0
Reserved		CH_EN	CH_ID	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1190. DIO2 DIO INGRESS DBCNT1 CONTROL REG Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	CH_EN	DIO Ingress DBCNT 1 - Channel Enable Register
6-0	CH_ID	DIO Ingress DBCNT 1 - Channel ID Register

8.7.29 DIO2_I_DBCNT2_RAM_MMR [Address = 0x1_1800 + (*R* × 0x0008)]

Table 8-1191. DIO2_I_DBCNT2_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_1800 + (*R* × 0x0008)	DIO2 DIO INGRESS DBCNT2 BASE ADDRESS REG	A per AxC register that is a field in the DIO Ingress DBCNT 2 LUT that enables the user to program the associated AxC's destination VBUS base address. This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.	Section 8.7.29.1
0x1_1804 + (*R* × 0x0008)	DIO2 DIO INGRESS DBCNT2 CONTROL REG	A per AxC register that is a field in the DIO Ingress DBCNT 2 LUT that enables the user to program the associated AxC's channel ID and channel enable.	Section 8.7.29.2

8.7.29.1 DIO2 DIO INGRESS DBCNT2 BASE ADDRESS REG [Address = 0x1_1800 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Ingress DBCNT 2 LUT that enables the user to program the associated AxC's destination VBUS base address.

This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.

Figure 8-1056. DIO2 DIO INGRESS DBCNT2 BASE ADDRESS REG

31 28	27 0
Reserved	DMA_VBUS_BASE_ADDR_AXC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1192. DIO2 DIO INGRESS DBCNT2 BASE ADDRESS REG Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved
27-0	DMA_VBUS_BASE_ADDR_AXC	DIO Ingress DBCNT 2 - Per AxC VBUS Base address Register

8.7.29.2 DIO2 DIO INGRESS DBCNT2 CONTROL REG [Address = 0x1_1804 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Ingress DBCNT 2 LUT that enables the user to program the associated AxC's channel ID and channel enable.

Figure 8-1057. DIO2 DIO INGRESS DBCNT2 CONTROL REG

31	8	7	6	0
Reserved		CH_EN	CH_ID	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1193. DIO2 DIO INGRESS DBCNT2 CONTROL REG Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	CH_EN	DIO Ingress DBCNT 2 - Channel Enable Register
6-0	CH_ID	DIO Ingress DBCNT 2 - Channel ID Register

8.7.30 DIO2_E_AOG_RAM_MMR [Address = 0x1_2800 + (R × 0x0004)]

Table 8-1194. DIO2_E_AOG_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_2800 + (*R* × 0x0004)	DIO2 DIO EGRESS AXC OFFSET REG	These registers are per channel and allow the user the ability to program the Egress AxC offset from the Frame Boundary in 4 sample (1 QW) increments. e.g. a value of 0 would cause zero offset from frame boundary. A value of 1 would cause a 4 sample offset from frame boundary.	Section 8.7.30.1

8.7.30.1 DIO2 DIO EGRESS AXC OFFSET REG [Address = 0x1_2800 + (R × 0x0004)]

Range (*R*) = 0:15

These registers are per channel and allow the user the ability to program the Egress AxC offset from the Frame Boundary in 4 sample (1 QW) increments.

e.g. a value of 0 would cause zero offset from frame boundary. A value of 1 would cause a 4 sample offset from frame boundary.

Figure 8-1058. DIO2 DIO EGRESS AXC OFFSET REG

31	17	16	0
Reserved		DIO_E_AXC_4SAMP_OFFSET	
NA-0		R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1195. DIO2 DIO EGRESS AXC OFFSET REG Field Descriptions

Bits	Name	Description
31-17	Reserved	Reserved
16-0	DIO_E_AXC_4SAMP_OFFSET	DIO Egress AxC offset from Frame Boundary in 4 sample (1 QW) increments

8.7.31 DIO2_E_DBCNT0_RAM_MMR [Address = 0x1_3000 + (*R* × 0x0008)]

Table 8-1196. DIO2_E_DBCNT0_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_3000 + (*R* × 0x0008)	DIO2 DIO EGRESS DBCNT0 BASE ADDRESS REG	A per AxC register that is a field in the DIO Egress DBCNT 0 LUT that enables the user to program the associated AxC's destination VBUS base address. This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.	Section 8.7.31.1
0x1_3004 + (*R* × 0x0008)	DIO2 DIO EGRESS DBCNT0 CONTROL REG	A per AxC register that is a field in the DIO Egress DBCNT 0 LUT that enables the user to program the associated AxC's channel ID and channel enable.	Section 8.7.31.2

8.7.31.1 DIO2 DIO EGRESS DBCNT0 BASE ADDRESS REG [Address = 0x1_3000 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Egress DBCNT 0 LUT that enables the user to program the associated AxC's destination VBUS base address.

This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.

Figure 8-1059. DIO2 DIO EGRESS DBCNT0 BASE ADDRESS REG

31 28	27 0
Reserved	DMA_VBUS_BASE_ADDR_AXC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1197. DIO2 DIO EGRESS DBCNT0 BASE ADDRESS REG Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved
27-0	DMA_VBUS_BASE_ADDR_AXC	DIO Egress DBCNT 0 - Per AxC VBUS Base address Register

8.7.31.2 DIO2 DIO EGRESS DBCNT0 CONTROL REG [Address = 0x1_3004 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Egress DBCNT 0 LUT that enables the user to program the associated AxC's channel ID and channel enable.

Figure 8-1060. DIO2 DIO EGRESS DBCNT0 CONTROL REG

31	8	7	6	0
Reserved		CH_EN	CH_ID	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1198. DIO2 DIO EGRESS DBCNT0 CONTROL REG Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	CH_EN	DIO Egress DBCNT 0 - Channel Enable Register
6-0	CH_ID	DIO Egress DBCNT 0 - Channel ID Register

8.7.32 DIO2_E_DBCNT1_RAM_MMR [Address = 0x1_3800 + (R × 0x0008)]

Table 8-1199. DIO2_E_DBCNT1_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_3800 + (*R* × 0x0008)	DIO2 DIO EGRESS DBCNT1 BASE ADDRESS REG	A per AxC register that is a field in the DIO Egress DBCNT 1 LUT that enables the user to program the associated AxC's destination VBUS base address. This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.	Section 8.7.32.1
0x1_3804 + (*R* × 0x0008)	DIO2 DIO EGRESS DBCNT1 CONTROL REG	A per AxC register that is a field in the DIO Egress DBCNT 1 LUT that enables the user to program the associated AxC's channel ID and channel enable.	Section 8.7.32.2

8.7.32.1 DIO2 DIO EGRESS DBCNT1 BASE ADDRESS REG [Address = 0x1_3800 + (R × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Egress DBCNT 1 LUT that enables the user to program the associated AxC's destination VBUS base address.

This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.

Figure 8-1061. DIO2 DIO EGRESS DBCNT1 BASE ADDRESS REG

31 28	27 0
Reserved	DMA_VBUS_BASE_ADDR_AXC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1200. DIO2 DIO EGRESS DBCNT1 BASE ADDRESS REG Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved
27-0	DMA_VBUS_BASE_ADDR_AXC	DIO Egress DBCNT 1 - Per AxC VBUS Base address Register

8.7.32.2 DIO2 DIO EGRESS DBCNT1 CONTROL REG [Address = 0x1_3804 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Egress DBCNT 1 LUT that enables the user to program the associated AxC's channel ID and channel enable.

Figure 8-1062. DIO2 DIO EGRESS DBCNT1 CONTROL REG

31	8	7	6	0
Reserved		CH_EN	CH_ID	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1201. DIO2 DIO EGRESS DBCNT1 CONTROL REG Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	CH_EN	DIO Egress DBCNT 1 - Channel Enable Register
6-0	CH_ID	DIO Egress DBCNT 1 - Channel ID Register

8.7.33 DIO2_E_DBCNT2_RAM_MMR [Address = 0x1_4000 + (*R* × 0x0008)]

Table 8-1202. DIO2_E_DBCNT2_RAM_MMR

Offset	Acronym	Register Description	Section
0x1_4000 + (*R* × 0x0008)	DIO2 DIO EGRESS DBCNT2 BASE ADDRESS REG	A per AxC register that is a field in the DIO Egress DBCNT 2 LUT that enables the user to program the associated AxC's destination VBUS base address. This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.	Section 8.7.33.1
0x1_4004 + (*R* × 0x0008)	DIO2 DIO EGRESS DBCNT2 CONTROL REG	A per AxC register that is a field in the DIO Egress DBCNT 2 LUT that enables the user to program the associated AxC's channel ID and channel enable.	Section 8.7.33.2

8.7.33.1 DIO2 DIO EGRESS DBCNT2 BASE ADDRESS REG [Address = 0x1_4000 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Egress DBCNT 2 LUT that enables the user to program the associated AxC's destination VBUS base address.

This LUT is comprised of two parts. Table A is the lower half of the LUT's address and Table B which is the upper half of the LUT's address.

Figure 8-1063. DIO2 DIO EGRESS DBCNT2 BASE ADDRESS REG

31 28	27 0
Reserved	DMA_VBUS_BASE_ADDR_AXC
NA-0	R/W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1203. DIO2 DIO EGRESS DBCNT2 BASE ADDRESS REG Field Descriptions

Bits	Name	Description
31-28	Reserved	Reserved
27-0	DMA_VBUS_BASE_ADDR_AXC	DIO Egress DBCNT 2 - Per AxC VBUS Base address Register

8.7.33.2 DIO2 DIO EGRESS DBCNT2 CONTROL REG [Address = 0x1_4004 + (*R* × 0x0008)]

Range (*R*) = 0:31

A per AxC register that is a field in the DIO Egress DBCNT 2 LUT that enables the user to program the associated AxC's channel ID and channel enable.

Figure 8-1064. DIO2 DIO EGRESS DBCNT2 CONTROL REG

31	8	7	6	0
Reserved		CH_EN	CH_ID	
NA-0		R/W-0	R/W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1204. DIO2 DIO EGRESS DBCNT2 CONTROL REG Field Descriptions

Bits	Name	Description
31-8	Reserved	Reserved
7	CH_EN	DIO Egress DBCNT 2 - Channel Enable Register
6-0	CH_ID	DIO Egress DBCNT 2 - Channel ID Register

8.7.34 DIO2_EE [Address = 0x1_8000]

Table 8-1205. DIO2_EE

Offset	Acronym	Register Description	Section
0x1_8000	DIO2 EE_DMA_ING_A RAW INTERRUPT STATUS	DIO Ingress Interrupt Raw Status Register A	Section 8.7.34.1
0x1_8004	DIO2 EE_DMA_ING_A RAW SET	Raw Set	Section 8.7.34.2
0x1_8008	DIO2 EE_DMA_ING_A RAW CLEAR	Raw Clear	Section 8.7.34.3
0x1_800C	DIO2 EE_DMA_ING_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.4
0x1_8010	DIO2 EE_DMA_ING_A EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.5
0x1_8014	DIO2 EE_DMA_ING_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.6
0x1_8018	DIO2 EE_DMA_ING_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.7
0x1_801C	DIO2 EE_DMA_ING_A EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.8
0x1_8020	DIO2 EE_DMA_ING_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.9
0x1_8024	DIO2 EE_DMA_ING_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.10
0x1_8028	DIO2 EE_DMA_ING_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.11
0x1_802C	DIO2 EE_DMA_ING_B RAW INTERRUPT STATUS	DIO Ingress Interrupt Raw Status Register B	Section 8.7.34.12
0x1_8030	DIO2 EE_DMA_ING_B RAW SET	Raw Set	Section 8.7.34.13
0x1_8034	DIO2 EE_DMA_ING_B RAW CLEAR	Raw Clear	Section 8.7.34.14
0x1_8038	DIO2 EE_DMA_ING_B EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.15
0x1_803C	DIO2 EE_DMA_ING_B EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.16
0x1_8040	DIO2 EE_DMA_ING_B EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.17
0x1_8044	DIO2 EE_DMA_ING_B EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.18
0x1_8048	DIO2 EE_DMA_ING_B EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.19
0x1_804C	DIO2 EE_DMA_ING_B EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.20
0x1_8050	DIO2 EE_DMA_ING_B EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.21
0x1_8054	DIO2 EE_DMA_ING_B EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.22

Table 8-1205. DIO2_EE (continued)

Offset	Acronym	Register Description	Section
0x1_80DC	DIO2 EE_DMA_EGR_A RAW INTERRUPT STATUS	DIO Egress Interrupt Raw Status Register A	Section 8.7.34.23
0x1_80E0	DIO2 EE_DMA_EGR_A RAW SET	Raw Set	Section 8.7.34.24
0x1_80E4	DIO2 EE_DMA_EGR_A RAW CLEAR	Raw Clear	Section 8.7.34.25
0x1_80E8	DIO2 EE_DMA_EGR_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.26
0x1_80EC	DIO2 EE_DMA_EGR_A EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.27
0x1_80F0	DIO2 EE_DMA_EGR_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.28
0x1_80F4	DIO2 EE_DMA_EGR_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.29
0x1_80F8	DIO2 EE_DMA_EGR_A EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.30
0x1_80FC	DIO2 EE_DMA_EGR_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.31
0x1_8100	DIO2 EE_DMA_EGR_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.32
0x1_8104	DIO2 EE_DMA_EGR_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.33
0x1_8108	DIO2 EE_DT_A RAW INTERRUPT STATUS	DIO DataTrace Interrupt Raw Status Register A	Section 8.7.34.34
0x1_810C	DIO2 EE_DT_A RAW SET	Raw Set	Section 8.7.34.35
0x1_8110	DIO2 EE_DT_A RAW CLEAR	Raw Clear	Section 8.7.34.36
0x1_8114	DIO2 EE_DT_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.37
0x1_8118	DIO2 EE_DT_A EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.38
0x1_811C	DIO2 EE_DT_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.39
0x1_8120	DIO2 EE_DT_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.40
0x1_8124	DIO2 EE_DT_A EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.41
0x1_8128	DIO2 EE_DT_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.42

Table 8-1205. DIO2_EE (continued)

Offset	Acronym	Register Description	Section
0x1_812C	DIO2 EE_DT_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.43
0x1_8130	DIO2 EE_DT_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.44
0x1_8134	DIO2 EE_SII_A RAW INTERRUPT STATUS	SI si_i IQ errors and info.	Section 8.7.34.45
0x1_8138	DIO2 EE_SII_A RAW SET	Raw Set	Section 8.7.34.46
0x1_813C	DIO2 EE_SII_A RAW CLEAR	Raw Clear	Section 8.7.34.47
0x1_8140	DIO2 EE_SII_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.48
0x1_8144	DIO2 EE_SII_A EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.49
0x1_8148	DIO2 EE_SII_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.50
0x1_814C	DIO2 EE_SII_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.51
0x1_8150	DIO2 EE_SII_A EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.52
0x1_8154	DIO2 EE_SII_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.53
0x1_8158	DIO2 EE_SII_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.54
0x1_815C	DIO2 EE_SII_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.55
0x1_8160	DIO2 EE_SII_C RAW INTERRUPT STATUS	SI si_i IQ per-channel start of frame errors	Section 8.7.34.56
0x1_8164	DIO2 EE_SII_C RAW SET	Raw Set	Section 8.7.34.57
0x1_8168	DIO2 EE_SII_C RAW CLEAR	Raw Clear	Section 8.7.34.58
0x1_816C	DIO2 EE_SII_C EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.59
0x1_8170	DIO2 EE_SII_C EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.60
0x1_8174	DIO2 EE_SII_C EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.61
0x1_8178	DIO2 EE_SII_C EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.62

Table 8-1205. DIO2_EE (continued)

Offset	Acronym	Register Description	Section
0x1_817C	DIO2 EE_SII_C EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.63
0x1_8180	DIO2 EE_SII_C EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.64
0x1_8184	DIO2 EE_SII_C EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.65
0x1_8188	DIO2 EE_SII_C EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.66
0x1_8210	DIO2 EE_SIE_A RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.7.34.67
0x1_8214	DIO2 EE_SIE_A RAW SET	Raw Set	Section 8.7.34.68
0x1_8218	DIO2 EE_SIE_A RAW CLEAR	Raw Clear	Section 8.7.34.69
0x1_821C	DIO2 EE_SIE_A EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.70
0x1_8220	DIO2 EE_SIE_A EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.71
0x1_8224	DIO2 EE_SIE_A EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.72
0x1_8228	DIO2 EE_SIE_A EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.73
0x1_822C	DIO2 EE_SIE_A EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.74
0x1_8230	DIO2 EE_SIE_A EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.75
0x1_8234	DIO2 EE_SIE_A EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.76
0x1_8238	DIO2 EE_SIE_A EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.77
0x1_823C	DIO2 EE_SII_E RAW INTERRUPT STATUS	SI si_i IQ info.	Section 8.7.34.78
0x1_8240	DIO2 EE_SII_E RAW SET	Raw Set	Section 8.7.34.79
0x1_8244	DIO2 EE_SII_E RAW CLEAR	Raw Clear	Section 8.7.34.80
0x1_8248	DIO2 EE_SII_E EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.81
0x1_824C	DIO2 EE_SII_E EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.82

Table 8-1205. DIO2_EE (continued)

Offset	Acronym	Register Description	Section
0x1_8250	DIO2 EE_SII_E EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.83
0x1_8254	DIO2 EE_SII_E EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.84
0x1_8258	DIO2 EE_SII_E EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.85
0x1_825C	DIO2 EE_SII_E EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.86
0x1_8260	DIO2 EE_SII_E EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.87
0x1_8264	DIO2 EE_SII_E EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.88
0x1_8268	DIO2 EE_SII_G RAW INTERRUPT STATUS	SI si_i IQ per-channel SOP transmitted to PSI info	Section 8.7.34.89
0x1_826C	DIO2 EE_SII_G RAW SET	Raw Set	Section 8.7.34.90
0x1_8270	DIO2 EE_SII_G RAW CLEAR	Raw Clear	Section 8.7.34.91
0x1_8274	DIO2 EE_SII_G EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.92
0x1_8278	DIO2 EE_SII_G EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.93
0x1_827C	DIO2 EE_SII_G EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.94
0x1_8280	DIO2 EE_SII_G EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.95
0x1_8284	DIO2 EE_SII_G EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.96
0x1_8288	DIO2 EE_SII_G EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.97
0x1_828C	DIO2 EE_SII_G EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.98
0x1_8290	DIO2 EE_SII_G EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.99
0x1_8318	DIO2 EE_SIE_D RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.7.34.100
0x1_831C	DIO2 EE_SIE_D RAW SET	Raw Set	Section 8.7.34.101
0x1_8320	DIO2 EE_SIE_D RAW CLEAR	Raw Clear	Section 8.7.34.102

Table 8-1205. DIO2_EE (continued)

Offset	Acronym	Register Description	Section
0x1_8324	DIO2 EE_SIE_D EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.103
0x1_8328	DIO2 EE_SIE_D EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.104
0x1_832C	DIO2 EE_SIE_D EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.105
0x1_8330	DIO2 EE_SIE_D EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.106
0x1_8334	DIO2 EE_SIE_D EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.107
0x1_8338	DIO2 EE_SIE_D EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.108
0x1_833C	DIO2 EE_SIE_D EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.109
0x1_8340	DIO2 EE_SIE_D EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.110
0x1_8344	DIO2 EE_SIE_E RAW INTERRUPT STATUS	SI si_e IQ errors and info.	Section 8.7.34.111
0x1_8348	DIO2 EE_SIE_E RAW SET	Raw Set	Section 8.7.34.112
0x1_834C	DIO2 EE_SIE_E RAW CLEAR	Raw Clear	Section 8.7.34.113
0x1_8350	DIO2 EE_SIE_E EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.114
0x1_8354	DIO2 EE_SIE_E EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.115
0x1_8358	DIO2 EE_SIE_E EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.116
0x1_835C	DIO2 EE_SIE_E EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.117
0x1_8360	DIO2 EE_SIE_E EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.118
0x1_8364	DIO2 EE_SIE_E EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.119
0x1_8368	DIO2 EE_SIE_E EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.120
0x1_836C	DIO2 EE_SIE_E EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.121
0x1_8370	DIO2 EE_SIE_F RAW INTERRUPT STATUS	SI si_e IQ per-channel SOP received from PSI info	Section 8.7.34.122

Table 8-1205. DIO2_EE (continued)

Offset	Acronym	Register Description	Section
0x1_8374	DIO2 EE_SIE_F RAW SET	Raw Set	Section 8.7.34.123
0x1_8378	DIO2 EE_SIE_F RAW CLEAR	Raw Clear	Section 8.7.34.124
0x1_837C	DIO2 EE_SIE_F EV0 ENABLE STATUS	EV0 Enable Status	Section 8.7.34.125
0x1_8380	DIO2 EE_SIE_F EV0 ENABLE SET	EV0 Enable Set	Section 8.7.34.126
0x1_8384	DIO2 EE_SIE_F EV0 ENABLE CLEAR	EV0 Enable Clear	Section 8.7.34.127
0x1_8388	DIO2 EE_SIE_F EV1 ENABLE STATUS	EV1 Enable Status	Section 8.7.34.128
0x1_838C	DIO2 EE_SIE_F EV1 ENABLE SET	EV1 Enable Set	Section 8.7.34.129
0x1_8390	DIO2 EE_SIE_F EV1 ENABLE CLEAR	EV1 Enable Clear	Section 8.7.34.130
0x1_8394	DIO2 EE_SIE_F EV0 ENABLED STATUS	EV0 Enabled Status	Section 8.7.34.131
0x1_8398	DIO2 EE_SIE_F EV1 ENABLED STATUS	EV1 Enabled Status	Section 8.7.34.132
0x1_8420	DIO2 DIO2_ORIG_REG	This is the DIO2 origination register provided as a shortcut way to determine where an interrupt originated.	Section 8.7.34.133

8.7.34.1 DIO2 EE_DMA_ING_A RAW INTERRUPT STATUS [Address = 0x1_8000]

DIO Ingress Interrupt Raw Status Register A

Figure 8-1065. DIO2 EE_DMA_ING_A RAW INTERRUPT STATUS

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		R-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1206. DIO2 EE_DMA_ING_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Ingress DMA block transfer complete detected per DMA engine
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Ingress DMA Programming error detected per DMA engine
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Ingress DMA engine(s) error i.e. the trigger pending queue overflowed.

8.7.34.2 DIO2 EE_DMA_ING_A RAW SET [Address = 0x1_8004]

Raw Set

Figure 8-1066. DIO2 EE_DMA_ING_A RAW SET

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		W-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1207. DIO2 EE_DMA_ING_A RAW SET Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.3 DIO2 EE_DMA_ING_A RAW CLEAR [Address = 0x1_8008]

Raw Clear

Figure 8-1067. DIO2 EE_DMA_ING_A RAW CLEAR

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		W-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1208. DIO2 EE_DMA_ING_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.4 DIO2 EE_DMA_ING_A EV0 ENABLE STATUS [Address = 0x1_800C]

EV0 Enable Status

Figure 8-1068. DIO2 EE_DMA_ING_A EV0 ENABLE STATUS

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		R-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1209. DIO2 EE_DMA_ING_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.5 DIO2 EE_DMA_ING_A EV0 ENABLE SET [Address = 0x1_8010]

EV0 Enable Set

Figure 8-1069. DIO2 EE_DMA_ING_A EV0 ENABLE SET

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		W-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1210. DIO2 EE_DMA_ING_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.6 DIO2 EE_DMA_ING_A EV0 ENABLE CLEAR [Address = 0x1_8014]

EV0 Enable Clear

Figure 8-1070. DIO2 EE_DMA_ING_A EV0 ENABLE CLEAR

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		W-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1211. DIO2 EE_DMA_ING_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.7 DIO2 EE_DMA_ING_A EV1 ENABLE STATUS [Address = 0x1_8018]

EV1 Enable Status

Figure 8-1071. DIO2 EE_DMA_ING_A EV1 ENABLE STATUS

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		R-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1212. DIO2 EE_DMA_ING_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.8 DIO2 EE_DMA_ING_A EV1 ENABLE SET [Address = 0x1_801C]

EV1 Enable Set

Figure 8-1072. DIO2 EE_DMA_ING_A EV1 ENABLE SET

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		W-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1213. DIO2 EE_DMA_ING_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.9 DIO2 EE_DMA_ING_A EV1 ENABLE CLEAR [Address = 0x1_8020]

EV1 Enable Clear

Figure 8-1073. DIO2 EE_DMA_ING_A EV1 ENABLE CLEAR

31	11	10	8	7
Reserved		DMA_ING_XFER_DONE_INFO		Reserved
NA-0		W-0		NA-0

6	4	3	2	0
DMA_ING_PROG_ERR		Reserved	DMA_ING_PEND_QUE_OVF_ERR	
W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

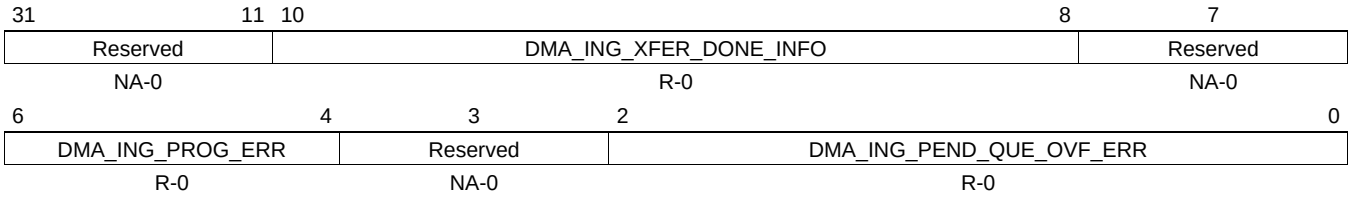
Table 8-1214. DIO2 EE_DMA_ING_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.10 DIO2 EE_DMA_ING_A EV0 ENABLED STATUS [Address = 0x1_8024]

EV0 Enabled Status

Figure 8-1074. DIO2 EE_DMA_ING_A EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

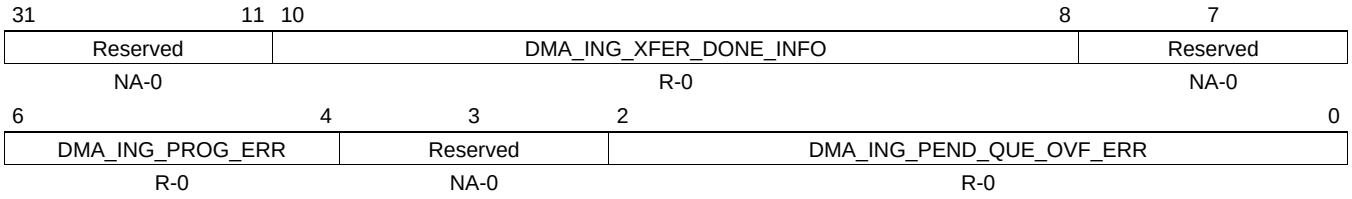
Table 8-1215. DIO2 EE_DMA_ING_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.11 DIO2 EE_DMA_ING_A EV1 ENABLED STATUS [Address = 0x1_8028]

EV1 Enabled Status

Figure 8-1075. DIO2 EE_DMA_ING_A EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1216. DIO2 EE_DMA_ING_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-11	Reserved	Reserved.
10-8	DMA_ING_XFER_DONE_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
7	Reserved	Reserved.
6-4	DMA_ING_PROG_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	Reserved	Reserved.
2-0	DMA_ING_PEND_QUE_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.12 DIO2 EE_DMA_ING_B RAW INTERRUPT STATUS [Address = 0x1_802C]

DIO Ingress Interrupt Raw Status Register B

Figure 8-1076. DIO2 EE_DMA_ING_B RAW INTERRUPT STATUS

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1217. DIO2 EE_DMA_ING_B RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Ingress Data Buffer overflow per channel

8.7.34.13 DIO2 EE_DMA_ING_B RAW SET [Address = 0x1_8030]

Raw Set

Figure 8-1077. DIO2 EE_DMA_ING_B RAW SET

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1218. DIO2 EE_DMA_ING_B RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.14 DIO2 EE_DMA_ING_B RAW CLEAR [Address = 0x1_8034]

Raw Clear

Figure 8-1078. DIO2 EE_DMA_ING_B RAW CLEAR

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1219. DIO2 EE_DMA_ING_B RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.15 DIO2 EE_DMA_ING_B EV0 ENABLE STATUS [Address = 0x1_8038]

EV0 Enable Status

Figure 8-1079. DIO2 EE_DMA_ING_B EV0 ENABLE STATUS

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1220. DIO2 EE_DMA_ING_B EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.16 DIO2 EE_DMA_ING_B EV0 ENABLE SET [Address = 0x1_803C]

EV0 Enable Set

Figure 8-1080. DIO2 EE_DMA_ING_B EV0 ENABLE SET

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1221. DIO2 EE_DMA_ING_B EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.17 DIO2 EE_DMA_ING_B EV0 ENABLE CLEAR [Address = 0x1_8040]

EV0 Enable Clear

Figure 8-1081. DIO2 EE_DMA_ING_B EV0 ENABLE CLEAR

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1222. DIO2 EE_DMA_ING_B EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.18 DIO2 EE_DMA_ING_B EV1 ENABLE STATUS [Address = 0x1_8044]

EV1 Enable Status

Figure 8-1082. DIO2 EE_DMA_ING_B EV1 ENABLE STATUS

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1223. DIO2 EE_DMA_ING_B EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.19 DIO2 EE_DMA_ING_B EV1 ENABLE SET [Address = 0x1_8048]

EV1 Enable Set

Figure 8-1083. DIO2 EE_DMA_ING_B EV1 ENABLE SET

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1224. DIO2 EE_DMA_ING_B EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.20 DIO2 EE_DMA_ING_B EV1 ENABLE CLEAR [Address = 0x1_804C]

EV1 Enable Clear

Figure 8-1084. DIO2 EE_DMA_ING_B EV1 ENABLE CLEAR

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1225. DIO2 EE_DMA_ING_B EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.21 DIO2 EE_DMA_ING_B EV0 ENABLED STATUS [Address = 0x1_8050]

EV0 Enabled Status

Figure 8-1085. DIO2 EE_DMA_ING_B EV0 ENABLED STATUS

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1226. DIO2 EE_DMA_ING_B EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.22 DIO2 EE_DMA_ING_B EV1 ENABLED STATUS [Address = 0x1_8054]

EV1 Enabled Status

Figure 8-1086. DIO2 EE_DMA_ING_B EV1 ENABLED STATUS

31	16	15	0
Reserved		DMA_ING_BUF_OVF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1227. DIO2 EE_DMA_ING_B EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	DMA_ING_BUF_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.23 DIO2 EE_DMA_EGR_A RAW INTERRUPT STATUS [Address = 0x1_80DC]

DIO Egress Interrupt Raw Status Register A

Figure 8-1087. DIO2 EE_DMA_EGR_A RAW INTERRUPT STATUS

31	13	12	11	10	8
Reserved		SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO	
NA-0		R-0	NA-0	R-0	

7	6	4	3	2	0
Reserved	DMA_EGR_PROG_ERR		Reserved	DMA_EGR_PEND_QUE_OVF_ERR	
NA-0	R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1228. DIO2 EE_DMA_EGR_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	PSI Staging FIFO Full i.e. back pressuring the egress data path including the VBUSM
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Egress DMA block transfer complete detected per DMA engine
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Egress DMA Programming error detected per DMA engine
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Egress DMA engine(s) error i.e. the trigger pending queue overflowed.

8.7.34.24 DIO2 EE_DMA_EGR_A RAW SET [Address = 0x1_80E0]

Raw Set

Figure 8-1088. DIO2 EE_DMA_EGR_A RAW SET

31 13	12	11	10 8
Reserved	SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO
NA-0	W-0	NA-0	W-0

7	6 4	3	2 0
Reserved	DMA_EGR_PROG_ERR	Reserved	DMA_EGR_PEND_QUE_OVF_ERR
NA-0	W-0	NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1229. DIO2 EE_DMA_EGR_A RAW SET Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.25 DIO2 EE_DMA_EGR_A RAW CLEAR [Address = 0x1_80E4]

Raw Clear

Figure 8-1089. DIO2 EE_DMA_EGR_A RAW CLEAR

31	13	12	11	10	8
Reserved		SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO	
NA-0		W-0	NA-0	W-0	

7	6	4	3	2	0
Reserved	DMA_EGR_PROG_ERR		Reserved	DMA_EGR_PEND_QUE_OVF_ERR	
NA-0	W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1230. DIO2 EE_DMA_EGR_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.26 DIO2 EE_DMA_EGR_A EV0 ENABLE STATUS [Address = 0x1_80E8]

EV0 Enable Status

Figure 8-1090. DIO2 EE_DMA_EGR_A EV0 ENABLE STATUS

31 13	12	11	10 8
Reserved	SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO
NA-0	R-0	NA-0	R-0

7	6 4	3	2 0
Reserved	DMA_EGR_PROG_ERR	Reserved	DMA_EGR_PEND_QUE_OVF_ERR
NA-0	R-0	NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1231. DIO2 EE_DMA_EGR_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.27 DIO2 EE_DMA_EGR_A EV0 ENABLE SET [Address = 0x1_80EC]

EV0 Enable Set

Figure 8-1091. DIO2 EE_DMA_EGR_A EV0 ENABLE SET

31 13	12	11	10 8
Reserved	SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO
NA-0	W-0	NA-0	W-0

7	6 4	3	2 0
Reserved	DMA_EGR_PROG_ERR	Reserved	DMA_EGR_PEND_QUE_OVF_ERR
NA-0	W-0	NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1232. DIO2 EE_DMA_EGR_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.28 DIO2 EE_DMA_EGR_A EV0 ENABLE CLEAR [Address = 0x1_80F0]

EV0 Enable Clear

Figure 8-1092. DIO2 EE_DMA_EGR_A EV0 ENABLE CLEAR

31 13	12	11	10 8
Reserved	SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO
NA-0	W-0	NA-0	W-0

7	6 4	3	2 0
Reserved	DMA_EGR_PROG_ERR	Reserved	DMA_EGR_PEND_QUE_OVF_ERR
NA-0	W-0	NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1233. DIO2 EE_DMA_EGR_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.29 DIO2 EE_DMA_EGR_A EV1 ENABLE STATUS [Address = 0x1_80F4]

EV1 Enable Status

Figure 8-1093. DIO2 EE_DMA_EGR_A EV1 ENABLE STATUS

31	13	12	11	10	8
Reserved		SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO	
NA-0		R-0	NA-0	R-0	

7	6	4	3	2	0
Reserved	DMA_EGR_PROG_ERR		Reserved	DMA_EGR_PEND_QUE_OVF_ERR	
NA-0	R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1234. DIO2 EE_DMA_EGR_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.30 DIO2 EE_DMA_EGR_A EV1 ENABLE SET [Address = 0x1_80F8]

EV1 Enable Set

Figure 8-1094. DIO2 EE_DMA_EGR_A EV1 ENABLE SET

31 13	12	11 10	8
Reserved	SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO
NA-0	W-0	NA-0	W-0

7	6 4	3	2 0
Reserved	DMA_EGR_PROG_ERR	Reserved	DMA_EGR_PEND_QUE_OVF_ERR
NA-0	W-0	NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1235. DIO2 EE_DMA_EGR_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.31 DIO2 EE_DMA_EGR_A EV1 ENABLE CLEAR [Address = 0x1_80FC]

EV1 Enable Clear

Figure 8-1095. DIO2 EE_DMA_EGR_A EV1 ENABLE CLEAR

31	13	12	11	10	8
Reserved		SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO	
NA-0		W-0	NA-0	W-0	

7	6	4	3	2	0
Reserved	DMA_EGR_PROG_ERR		Reserved	DMA_EGR_PEND_QUE_OVF_ERR	
NA-0	W-0		NA-0	W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1236. DIO2 EE_DMA_EGR_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.32 DIO2 EE_DMA_EGR_A EV0 ENABLED STATUS [Address = 0x1_8100]

EV0 Enabled Status

Figure 8-1096. DIO2 EE_DMA_EGR_A EV0 ENABLED STATUS

31	13	12	11	10	8
Reserved		SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO	
NA-0		R-0	NA-0	R-0	

7	6	4	3	2	0
Reserved	DMA_EGR_PROG_ERR		Reserved	DMA_EGR_PEND_QUE_OVF_ERR	
NA-0	R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1237. DIO2 EE_DMA_EGR_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.33 DIO2 EE_DMA_EGR_A EV1 ENABLED STATUS [Address = 0x1_8104]

EV1 Enabled Status

Figure 8-1097. DIO2 EE_DMA_EGR_A EV1 ENABLED STATUS

31	13	12	11	10	8
Reserved		SI_ING_IQ_FIFO_FULL_INFO	Reserved	DMA_EGR_XFER_DONE_INFO	
NA-0		R-0	NA-0	R-0	

7	6	4	3	2	0
Reserved	DMA_EGR_PROG_ERR		Reserved	DMA_EGR_PEND_QUE_OVF_ERR	
NA-0	R-0		NA-0	R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1238. DIO2 EE_DMA_EGR_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-13	Reserved	Reserved.
12	SI_ING_IQ_FIFO_FULL_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
11	Reserved	Reserved.
10-8	DMA_EGR_XFER_DONE_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
7	Reserved	Reserved.
6-4	DMA_EGR_PROG_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	Reserved	Reserved.
2-0	DMA_EGR_PEND_QUE_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.34 DIO2 EE_DT_A RAW INTERRUPT STATUS [Address = 0x1_8108]

DIO DataTrace Interrupt Raw Status Register A

Figure 8-1098. DIO2 EE_DT_A RAW INTERRUPT STATUS

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1239. DIO2 EE_DT_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Data Trace one shot capture done info
0	DT_BUFF_OVF_ERR	Data Trace buffer overflow error

8.7.34.35 DIO2 EE_DT_A RAW SET [Address = 0x1_810C]

Raw Set

Figure 8-1099. DIO2 EE_DT_A RAW SET

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1240. DIO2 EE_DT_A RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	DT_BUFF_OVF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.36 DIO2 EE_DT_A RAW CLEAR [Address = 0x1_8110]

Raw Clear

Figure 8-1100. DIO2 EE_DT_A RAW CLEAR

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1241. DIO2 EE_DT_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	DT_BUFF_OVF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.37 DIO2 EE_DT_A EV0 ENABLE STATUS [Address = 0x1_8114]

EV0 Enable Status

Figure 8-1101. DIO2 EE_DT_A EV0 ENABLE STATUS

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1242. DIO2 EE_DT_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	DT_BUFF_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.38 DIO2 EE_DT_A EV0 ENABLE SET [Address = 0x1_8118]

EV0 Enable Set

Figure 8-1102. DIO2 EE_DT_A EV0 ENABLE SET

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1243. DIO2 EE_DT_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	DT_BUFF_OVF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.39 DIO2 EE_DT_A EV0 ENABLE CLEAR [Address = 0x1_811C]

EV0 Enable Clear

Figure 8-1103. DIO2 EE_DT_A EV0 ENABLE CLEAR

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1244. DIO2 EE_DT_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	DT_BUFF_OVF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.40 DIO2 EE_DT_A EV1 ENABLE STATUS [Address = 0x1_8120]

EV1 Enable Status

Figure 8-1104. DIO2 EE_DT_A EV1 ENABLE STATUS

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1245. DIO2 EE_DT_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	DT_BUFF_OVF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.41 DIO2 EE_DT_A EV1 ENABLE SET [Address = 0x1_8124]

EV1 Enable Set

Figure 8-1105. DIO2 EE_DT_A EV1 ENABLE SET

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1246. DIO2 EE_DT_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	DT_BUFF_OVF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.42 DIO2 EE_DT_A EV1 ENABLE CLEAR [Address = 0x1_8128]

EV1 Enable Clear

Figure 8-1106. DIO2 EE_DT_A EV1 ENABLE CLEAR

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1247. DIO2 EE_DT_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	DT_BUFF_OVF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.43 DIO2 EE_DT_A EV0 ENABLED STATUS [Address = 0x1_812C]

EV0 Enabled Status

Figure 8-1107. DIO2 EE_DT_A EV0 ENABLED STATUS

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1248. DIO2 EE_DT_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	DT_BUFF_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.44 DIO2 EE_DT_A EV1 ENABLED STATUS [Address = 0x1_8130]

EV1 Enabled Status

Figure 8-1108. DIO2 EE_DT_A EV1 ENABLED STATUS

31	2	1	0
Reserved		DT_DONE_INFO	DT_BUFF_OVF_ERR
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1249. DIO2 EE_DT_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	DT_DONE_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	DT_BUFF_OVF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.45 DIO2 EE_SII_A RAW INTERRUPT STATUS [Address = 0x1_8134]

SI si_i IQ errors and info.

Figure 8-1109. DIO2 EE_SII_A RAW INTERRUPT STATUS

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1250. DIO2 EE_SII_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	DIO SI Ingress IQ IFE transmitted valid data phase
3	SI_ING_IQ_IFE_EOP_INFO	DIO SI Ingress IQ IFE transmitted EOP
2	SI_ING_IQ_IFE_SOP_INFO	DIO SI Ingress IQ IFE transmitted SOP
1	SI_ING_IQ_ICC_DAT_INFO	DIO SI Ingress IQ ICC data transfer received
0	SI_ING_IQ_ICC_SOF_INFO	DIO SI Ingress IQ ICC Start of Frame received

8.7.34.46 DIO2 EE_SII_A RAW SET [Address = 0x1_8138]

Raw Set

Figure 8-1110. DIO2 EE_SII_A RAW SET

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1251. DIO2 EE_SII_A RAW SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.47 DIO2 EE_SII_A RAW CLEAR [Address = 0x1_813C]

Raw Clear

Figure 8-1111. DIO2 EE_SII_A RAW CLEAR

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1252. DIO2 EE_SII_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.48 DIO2 EE_SII_A EV0 ENABLE STATUS [Address = 0x1_8140]

EV0 Enable Status

Figure 8-1112. DIO2 EE_SII_A EV0 ENABLE STATUS

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1253. DIO2 EE_SII_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.49 DIO2 EE_SII_A EV0 ENABLE SET [Address = 0x1_8144]

EV0 Enable Set

Figure 8-1113. DIO2 EE_SII_A EV0 ENABLE SET

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1254. DIO2 EE_SII_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.50 DIO2 EE_SII_A EV0 ENABLE CLEAR [Address = 0x1_8148]

EV0 Enable Clear

Figure 8-1114. DIO2 EE_SII_A EV0 ENABLE CLEAR

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1255. DIO2 EE_SII_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.51 DIO2 EE_SII_A EV1 ENABLE STATUS [Address = 0x1_814C]

EV1 Enable Status

Figure 8-1115. DIO2 EE_SII_A EV1 ENABLE STATUS

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1256. DIO2 EE_SII_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.52 DIO2 EE_SII_A EV1 ENABLE SET [Address = 0x1_8150]

EV1 Enable Set

Figure 8-1116. DIO2 EE_SII_A EV1 ENABLE SET

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1257. DIO2 EE_SII_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.53 DIO2 EE_SII_A EV1 ENABLE CLEAR [Address = 0x1_8154]

EV1 Enable Clear

Figure 8-1117. DIO2 EE_SII_A EV1 ENABLE CLEAR

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		W-0	W-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1258. DIO2 EE_SII_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_ING_IQ_IFE_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_ING_IQ_IFE_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_ING_IQ_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_ICC_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.54 DIO2 EE_SII_A EV0 ENABLED STATUS [Address = 0x1_8158]

EV0 Enabled Status

Figure 8-1118. DIO2 EE_SII_A EV0 ENABLED STATUS

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1259. DIO2 EE_SII_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.55 DIO2 EE_SII_A EV1 ENABLED STATUS [Address = 0x1_815C]

EV1 Enabled Status

Figure 8-1119. DIO2 EE_SII_A EV1 ENABLED STATUS

31	5	4	3
Reserved		SI_ING_IQ_IFE_DAT_INFO	SI_ING_IQ_IFE_EOP_INFO
NA-0		R-0	R-0

2	1	0
SI_ING_IQ_IFE_SOP_INFO	SI_ING_IQ_ICC_DAT_INFO	SI_ING_IQ_ICC_SOF_INFO
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1260. DIO2 EE_SII_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_ING_IQ_IFE_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	SI_ING_IQ_IFE_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_ING_IQ_IFE_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_ING_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.56 DIO2 EE_SII_C RAW INTERRUPT STATUS [Address = 0x1_8160]

SI si_i IQ per-channel start of frame errors

Figure 8-1120. DIO2 EE_SII_C RAW INTERRUPT STATUS

31 16	15 0
Reserved	SI_ING_IQ_SOF_ERR
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1261. DIO2 EE_SII_C RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	DIO SI Ingress IQ per channel Start of Frame alignment error

8.7.34.57 DIO2 EE_SII_C RAW SET [Address = 0x1_8164]

Raw Set

Figure 8-1121. DIO2 EE_SII_C RAW SET

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1262. DIO2 EE_SII_C RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.58 DIO2 EE_SII_C RAW CLEAR [Address = 0x1_8168]

Raw Clear

Figure 8-1122. DIO2 EE_SII_C RAW CLEAR

31 16	15 0
Reserved	SI_ING_IQ_SOF_ERR
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1263. DIO2 EE_SII_C RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.59 DIO2 EE_SII_C EV0 ENABLE STATUS [Address = 0x1_816C]

EV0 Enable Status

Figure 8-1123. DIO2 EE_SII_C EV0 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1264. DIO2 EE_SII_C EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.60 DIO2 EE_SII_C EV0 ENABLE SET [Address = 0x1_8170]

EV0 Enable Set

Figure 8-1124. DIO2 EE_SII_C EV0 ENABLE SET

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1265. DIO2 EE_SII_C EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.61 DIO2 EE_SII_C EV0 ENABLE CLEAR [Address = 0x1_8174]

EV0 Enable Clear

Figure 8-1125. DIO2 EE_SII_C EV0 ENABLE CLEAR

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1266. DIO2 EE_SII_C EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.62 DIO2 EE_SII_C EV1 ENABLE STATUS [Address = 0x1_8178]

EV1 Enable Status

Figure 8-1126. DIO2 EE_SII_C EV1 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1267. DIO2 EE_SII_C EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.63 DIO2 EE_SII_C EV1 ENABLE SET [Address = 0x1_817C]

EV1 Enable Set

Figure 8-1127. DIO2 EE_SII_C EV1 ENABLE SET

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

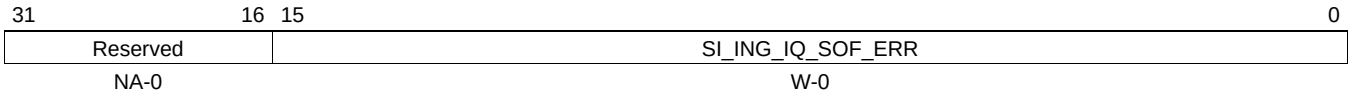
Table 8-1268. DIO2 EE_SII_C EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.64 DIO2 EE_SII_C EV1 ENABLE CLEAR [Address = 0x1_8180]

EV1 Enable Clear

Figure 8-1128. DIO2 EE_SII_C EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1269. DIO2 EE_SII_C EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.65 DIO2 EE_SII_C EV0 ENABLED STATUS [Address = 0x1_8184]

EV0 Enabled Status

Figure 8-1129. DIO2 EE_SII_C EV0 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1270. DIO2 EE_SII_C EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.66 DIO2 EE_SII_C EV1 ENABLED STATUS [Address = 0x1_8188]

EV1 Enabled Status

Figure 8-1130. DIO2 EE_SII_C EV1 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_IQ_SOF_ERR	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1271. DIO2 EE_SII_C EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_SOF_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.67 DIO2 EE_SIE_A RAW INTERRUPT STATUS [Address = 0x1_8210]

SI si_e IQ errors and info.

Figure 8-1131. DIO2 EE_SIE_A RAW INTERRUPT STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1272. DIO2 EE_SIE_A RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	DIO SI Egress IQ transmitted data to ICC
3	SI_EGR_IQ_ICC_SOF_INFO	DIO SI Egress IQ transmitted Start of Frame to ICC
2	SI_EGR_IQ_EFE_SYM_ERR	DIO SI Egress IQ EFE symbol number error. (Packet boundary errors due to a missing, early, or late SOP disable the reporting of any symbol errors since the symbol number is only valid for SOPs)
1	SI_EGR_IQ_EFE_PKT_ERR	DIO SI Egress IQ EFE packet boundary error
0	SI_EGR_IQ_EFE_STARVE_ERR	DIO SI Egress IQ EFE data starvation error

8.7.34.68 DIO2 EE_SIE_A RAW SET [Address = 0x1_8214]

Raw Set

Figure 8-1132. DIO2 EE_SIE_A RAW SET

31 5	4	3
Reserved	SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0	W-0	W-0
2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1273. DIO2 EE_SIE_A RAW SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.69 DIO2 EE_SIE_A RAW CLEAR [Address = 0x1_8218]

Raw Clear

Figure 8-1133. DIO2 EE_SIE_A RAW CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1274. DIO2 EE_SIE_A RAW CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.70 DIO2 EE_SIE_A EV0 ENABLE STATUS [Address = 0x1_821C]

EV0 Enable Status

Figure 8-1134. DIO2 EE_SIE_A EV0 ENABLE STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1275. DIO2 EE_SIE_A EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.71 DIO2 EE_SIE_A EV0 ENABLE SET [Address = 0x1_8220]

EV0 Enable Set

Figure 8-1135. DIO2 EE_SIE_A EV0 ENABLE SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0
2		1	0
SI_EGR_IQ_EFE_SYM_ERR		SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1276. DIO2 EE_SIE_A EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.72 DIO2 EE_SIE_A EV0 ENABLE CLEAR [Address = 0x1_8224]

EV0 Enable Clear

Figure 8-1136. DIO2 EE_SIE_A EV0 ENABLE CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1277. DIO2 EE_SIE_A EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.73 DIO2 EE_SIE_A EV1 ENABLE STATUS [Address = 0x1_8228]

EV1 Enable Status

Figure 8-1137. DIO2 EE_SIE_A EV1 ENABLE STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1278. DIO2 EE_SIE_A EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.74 DIO2 EE_SIE_A EV1 ENABLE SET [Address = 0x1_822C]

EV1 Enable Set

Figure 8-1138. DIO2 EE_SIE_A EV1 ENABLE SET

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1279. DIO2 EE_SIE_A EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.75 DIO2 EE_SIE_A EV1 ENABLE CLEAR [Address = 0x1_8230]

EV1 Enable Clear

Figure 8-1139. DIO2 EE_SIE_A EV1 ENABLE CLEAR

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		W-0	W-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
W-0	W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1280. DIO2 EE_SIE_A EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
3	SI_EGR_IQ_ICC_SOF_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
2	SI_EGR_IQ_EFE_SYM_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_EFE_PKT_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_EFE_STARVE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.76 DIO2 EE_SIE_A EV0 ENABLED STATUS [Address = 0x1_8234]

EV0 Enabled Status

Figure 8-1140. DIO2 EE_SIE_A EV0 ENABLED STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1281. DIO2 EE_SIE_A EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.77 DIO2 EE_SIE_A EV1 ENABLED STATUS [Address = 0x1_8238]

EV1 Enabled Status

Figure 8-1141. DIO2 EE_SIE_A EV1 ENABLED STATUS

31	5	4	3
Reserved		SI_EGR_IQ_ICC_DAT_INFO	SI_EGR_IQ_ICC_SOF_INFO
NA-0		R-0	R-0

2	1	0
SI_EGR_IQ_EFE_SYM_ERR	SI_EGR_IQ_EFE_PKT_ERR	SI_EGR_IQ_EFE_STARVE_ERR
R-0	R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1282. DIO2 EE_SIE_A EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-5	Reserved	Reserved.
4	SI_EGR_IQ_ICC_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
3	SI_EGR_IQ_ICC_SOF_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
2	SI_EGR_IQ_EFE_SYM_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_IQ_EFE_PKT_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_IQ_EFE_STARVE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.78 DIO2 EE_SII_E RAW INTERRUPT STATUS [Address = 0x1_823C]

SI si_i IQ info.

Figure 8-1142. DIO2 EE_SII_E RAW INTERRUPT STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1283. DIO2 EE_SII_E RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	DIO SI Ingress IQ data transmitted to PSI
0	SI_ING_IQ_PSI_EOP_INFO	DIO SI Ingress IQ EOP transmitted to PSI

8.7.34.79 DIO2 EE_SII_E RAW SET [Address = 0x1_8240]

Raw Set

Figure 8-1143. DIO2 EE_SII_E RAW SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1284. DIO2 EE_SII_E RAW SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.80 DIO2 EE_SII_E RAW CLEAR [Address = 0x1_8244]

Raw Clear

Figure 8-1144. DIO2 EE_SII_E RAW CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1285. DIO2 EE_SII_E RAW CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.81 DIO2 EE_SII_E EV0 ENABLE STATUS [Address = 0x1_8248]

EV0 Enable Status

Figure 8-1145. DIO2 EE_SII_E EV0 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1286. DIO2 EE_SII_E EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.82 DIO2 EE_SII_E EV0 ENABLE SET [Address = 0x1_824C]

EV0 Enable Set

Figure 8-1146. DIO2 EE_SII_E EV0 ENABLE SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1287. DIO2 EE_SII_E EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.83 DIO2 EE_SII_E EV0 ENABLE CLEAR [Address = 0x1_8250]

EV0 Enable Clear

Figure 8-1147. DIO2 EE_SII_E EV0 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1288. DIO2 EE_SII_E EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.84 DIO2 EE_SII_E EV1 ENABLE STATUS [Address = 0x1_8254]

EV1 Enable Status

Figure 8-1148. DIO2 EE_SII_E EV1 ENABLE STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1289. DIO2 EE_SII_E EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.85 DIO2 EE_SII_E EV1 ENABLE SET [Address = 0x1_8258]

EV1 Enable Set

Figure 8-1149. DIO2 EE_SII_E EV1 ENABLE SET

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1290. DIO2 EE_SII_E EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.86 DIO2 EE_SII_E EV1 ENABLE CLEAR [Address = 0x1_825C]

EV1 Enable Clear

Figure 8-1150. DIO2 EE_SII_E EV1 ENABLE CLEAR

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1291. DIO2 EE_SII_E EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_ING_IQ_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.87 DIO2 EE_SII_E EV0 ENABLED STATUS [Address = 0x1_8260]

EV0 Enabled Status

Figure 8-1151. DIO2 EE_SII_E EV0 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1292. DIO2 EE_SII_E EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.88 DIO2 EE_SII_E EV1 ENABLED STATUS [Address = 0x1_8264]

EV1 Enabled Status

Figure 8-1152. DIO2 EE_SII_E EV1 ENABLED STATUS

31	2	1	0
Reserved		SI_ING_IQ_PSI_DAT_INFO	SI_ING_IQ_PSI_EOP_INFO
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1293. DIO2 EE_SII_E EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-2	Reserved	Reserved.
1	SI_ING_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_ING_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.89 DIO2 EE_SII_G RAW INTERRUPT STATUS [Address = 0x1_8268]

SI si_i IQ per-channel SOP transmitted to PSI info

Figure 8-1153. DIO2 EE_SII_G RAW INTERRUPT STATUS

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1294. DIO2 EE_SII_G RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	DIO SI Ingress IQ SOP transmitted to PSI

8.7.34.90 DIO2 EE_SII_G RAW SET [Address = 0x1_826C]

Raw Set

Figure 8-1154. DIO2 EE_SII_G RAW SET

31 16	15 0
Reserved	SI_ING_IQ_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1295. DIO2 EE_SII_G RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.91 DIO2 EE_SII_G RAW CLEAR [Address = 0x1_8270]

Raw Clear

Figure 8-1155. DIO2 EE_SII_G RAW CLEAR

31 16	15 0
Reserved	SI_ING_IQ_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1296. DIO2 EE_SII_G RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.92 DIO2 EE_SII_G EV0 ENABLE STATUS [Address = 0x1_8274]

EV0 Enable Status

Figure 8-1156. DIO2 EE_SII_G EV0 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1297. DIO2 EE_SII_G EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.93 DIO2 EE_SII_G EV0 ENABLE SET [Address = 0x1_8278]

EV0 Enable Set

Figure 8-1157. DIO2 EE_SII_G EV0 ENABLE SET

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1298. DIO2 EE_SII_G EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.94 DIO2 EE_SII_G EV0 ENABLE CLEAR [Address = 0x1_827C]

EV0 Enable Clear

Figure 8-1158. DIO2 EE_SII_G EV0 ENABLE CLEAR

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1299. DIO2 EE_SII_G EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.95 DIO2 EE_SII_G EV1 ENABLE STATUS [Address = 0x1_8280]

EV1 Enable Status

Figure 8-1159. DIO2 EE_SII_G EV1 ENABLE STATUS

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1300. DIO2 EE_SII_G EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.96 DIO2 EE_SII_G EV1 ENABLE SET [Address = 0x1_8284]

EV1 Enable Set

Figure 8-1160. DIO2 EE_SII_G EV1 ENABLE SET

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1301. DIO2 EE_SII_G EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.97 DIO2 EE_SII_G EV1 ENABLE CLEAR [Address = 0x1_8288]

EV1 Enable Clear

Figure 8-1161. DIO2 EE_SII_G EV1 ENABLE CLEAR

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1302. DIO2 EE_SII_G EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.98 DIO2 EE_SII_G EV0 ENABLED STATUS [Address = 0x1_828C]

EV0 Enabled Status

Figure 8-1162. DIO2 EE_SII_G EV0 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1303. DIO2 EE_SII_G EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.99 DIO2 EE_SII_G EV1 ENABLED STATUS [Address = 0x1_8290]

EV1 Enabled Status

Figure 8-1163. DIO2 EE_SII_G EV1 ENABLED STATUS

31	16	15	0
Reserved		SI_ING_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1304. DIO2 EE_SII_G EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_ING_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.100 DIO2 EE_SIE_D RAW INTERRUPT STATUS [Address = 0x1_8318]

SI si_e IQ errors and info.

Figure 8-1164. DIO2 EE_SIE_D RAW INTERRUPT STATUS

31	3	2
Reserved		SI_EGR_IQ_PSI_DAT_INFO
NA-0		R-0

1	0
SI_EGR_IQ_PSI_EOP_INFO	SI_EGR_IQ_PSI_DATA_TYPE_ERR
R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1305. DIO2 EE_SIE_D RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	DIO SI Egress IQ valid data received from PSI
1	SI_EGR_IQ_PSI_EOP_INFO	DIO SI Egress IQ EOP received from PSI
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	DIO SI Egress IQ PSI data type error

8.7.34.101 DIO2 EE_SIE_D RAW SET [Address = 0x1_831C]

Raw Set

Figure 8-1165. DIO2 EE_SIE_D RAW SET

31	3	2
Reserved		SI_EGR_IQ_PSI_DAT_INFO
NA-0		W-0

1	0
SI_EGR_IQ_PSI_EOP_INFO	SI_EGR_IQ_PSI_DATA_TYPE_ERR
W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1306. DIO2 EE_SIE_D RAW SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.102 DIO2 EE_SIE_D RAW CLEAR [Address = 0x1_8320]

Raw Clear

Figure 8-1166. DIO2 EE_SIE_D RAW CLEAR

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

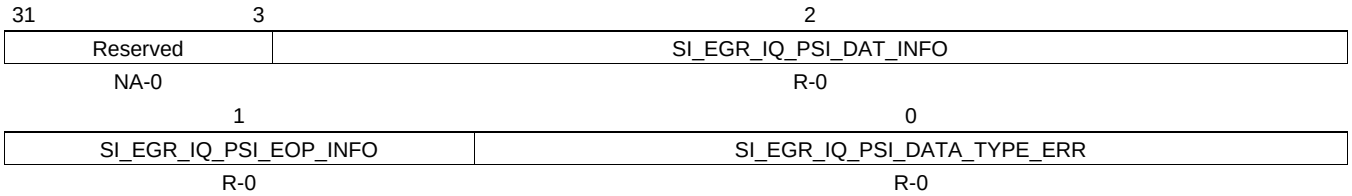
Table 8-1307. DIO2 EE_SIE_D RAW CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.103 DIO2 EE_SIE_D EV0 ENABLE STATUS [Address = 0x1_8324]

EV0 Enable Status

Figure 8-1167. DIO2 EE_SIE_D EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1308. DIO2 EE_SIE_D EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.104 DIO2 EE_SIE_D EV0 ENABLE SET [Address = 0x1_8328]

EV0 Enable Set

Figure 8-1168. DIO2 EE_SIE_D EV0 ENABLE SET

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		W-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
W-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

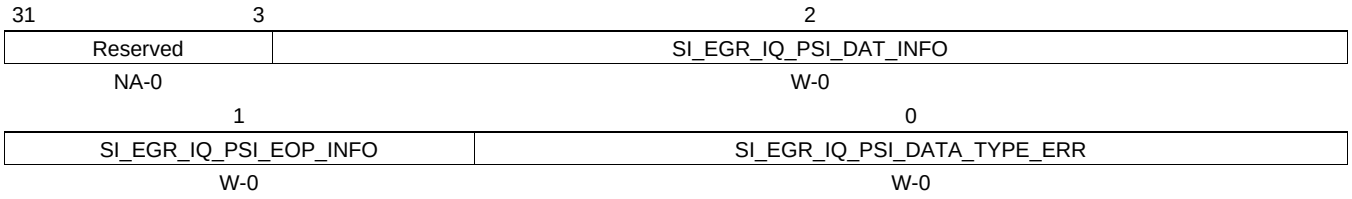
Table 8-1309. DIO2 EE_SIE_D EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.105 DIO2 EE_SIE_D EV0 ENABLE CLEAR [Address = 0x1_832C]

EV0 Enable Clear

Figure 8-1169. DIO2 EE_SIE_D EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1310. DIO2 EE_SIE_D EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.106 DIO2 EE_SIE_D EV1 ENABLE STATUS [Address = 0x1_8330]

EV1 Enable Status

Figure 8-1170. DIO2 EE_SIE_D EV1 ENABLE STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1311. DIO2 EE_SIE_D EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.107 DIO2 EE_SIE_D EV1 ENABLE SET [Address = 0x1_8334]

EV1 Enable Set

Figure 8-1171. DIO2 EE_SIE_D EV1 ENABLE SET

31	3	2
Reserved		SI_EGR_IQ_PSI_DAT_INFO
NA-0		W-0

1	0
SI_EGR_IQ_PSI_EOP_INFO	SI_EGR_IQ_PSI_DATA_TYPE_ERR
W-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

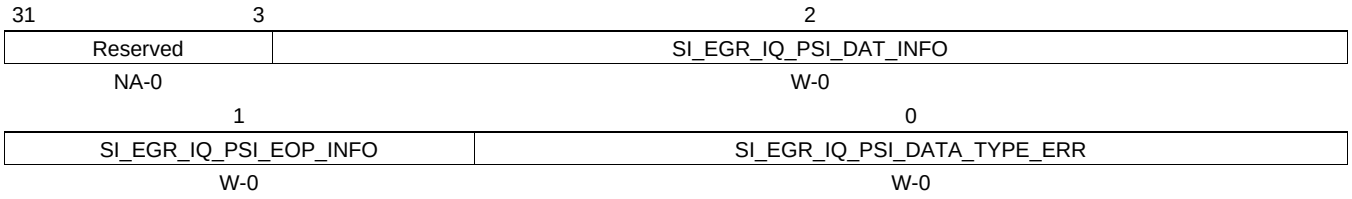
Table 8-1312. DIO2 EE_SIE_D EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.108 DIO2 EE_SIE_D EV1 ENABLE CLEAR [Address = 0x1_8338]

EV1 Enable Clear

Figure 8-1172. DIO2 EE_SIE_D EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1313. DIO2 EE_SIE_D EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
1	SI_EGR_IQ_PSI_EOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.109 DIO2 EE_SIE_D EV0 ENABLED STATUS [Address = 0x1_833C]

EV0 Enabled Status

Figure 8-1173. DIO2 EE_SIE_D EV0 ENABLED STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1314. DIO2 EE_SIE_D EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.110 DIO2 EE_SIE_D EV1 ENABLED STATUS [Address = 0x1_8340]

EV1 Enabled Status

Figure 8-1174. DIO2 EE_SIE_D EV1 ENABLED STATUS

31	3	2	
Reserved		SI_EGR_IQ_PSI_DAT_INFO	
NA-0		R-0	
1		0	
SI_EGR_IQ_PSI_EOP_INFO		SI_EGR_IQ_PSI_DATA_TYPE_ERR	
R-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

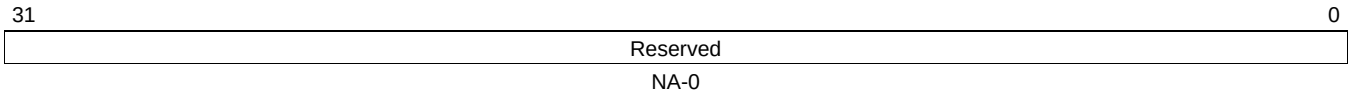
Table 8-1315. DIO2 EE_SIE_D EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-3	Reserved	Reserved.
2	SI_EGR_IQ_PSI_DAT_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
1	SI_EGR_IQ_PSI_EOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.
0	SI_EGR_IQ_PSI_DATA_TYPE_ERR	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.111 DIO2 EE_SIE_E RAW INTERRUPT STATUS [Address = 0x1_8344]

SI si_e IQ errors and info.

Figure 8-1175. DIO2 EE_SIE_E RAW INTERRUPT STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1316. DIO2 EE_SIE_E RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.112 DIO2 EE_SIE_E RAW SET [Address = 0x1_8348]

Raw Set

Figure 8-1176. DIO2 EE_SIE_E RAW SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1317. DIO2 EE_SIE_E RAW SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.113 DIO2 EE_SIE_E RAW CLEAR [Address = 0x1_834C]

Raw Clear

Figure 8-1177. DIO2 EE_SIE_E RAW CLEAR

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

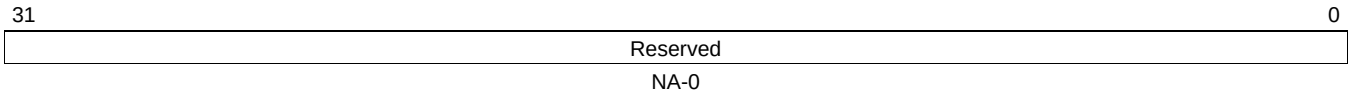
Table 8-1318. DIO2 EE_SIE_E RAW CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.114 DIO2 EE_SIE_E EV0 ENABLE STATUS [Address = 0x1_8350]

EV0 Enable Status

Figure 8-1178. DIO2 EE_SIE_E EV0 ENABLE STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

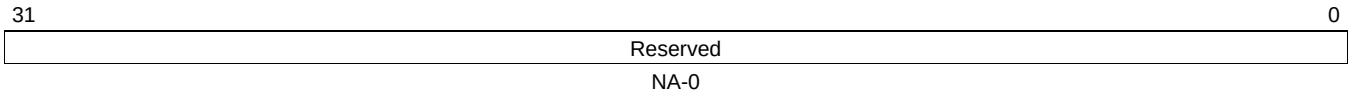
Table 8-1319. DIO2 EE_SIE_E EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.115 DIO2 EE_SIE_E EV0 ENABLE SET [Address = 0x1_8354]

EV0 Enable Set

Figure 8-1179. DIO2 EE_SIE_E EV0 ENABLE SET



Legend: R = Read only; W = Write only; - *n* = value after reset

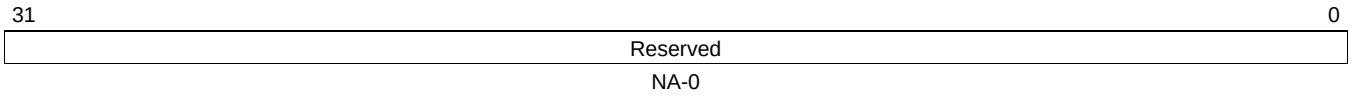
Table 8-1320. DIO2 EE_SIE_E EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.116 DIO2 EE_SIE_E EV0 ENABLE CLEAR [Address = 0x1_8358]

EV0 Enable Clear

Figure 8-1180. DIO2 EE_SIE_E EV0 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1321. DIO2 EE_SIE_E EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.117 DIO2 EE_SIE_E EV1 ENABLE STATUS [Address = 0x1_835C]

EV1 Enable Status

Figure 8-1181. DIO2 EE_SIE_E EV1 ENABLE STATUS

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1322. DIO2 EE_SIE_E EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.118 DIO2 EE_SIE_E EV1 ENABLE SET [Address = 0x1_8360]

EV1 Enable Set

Figure 8-1182. DIO2 EE_SIE_E EV1 ENABLE SET

31	0
Reserved	
NA-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

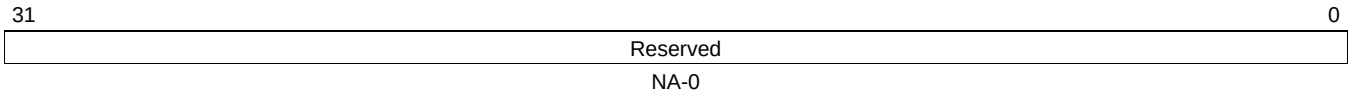
Table 8-1323. DIO2 EE_SIE_E EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.119 DIO2 EE_SIE_E EV1 ENABLE CLEAR [Address = 0x1_8364]

EV1 Enable Clear

Figure 8-1183. DIO2 EE_SIE_E EV1 ENABLE CLEAR



Legend: R = Read only; W = Write only; - *n* = value after reset

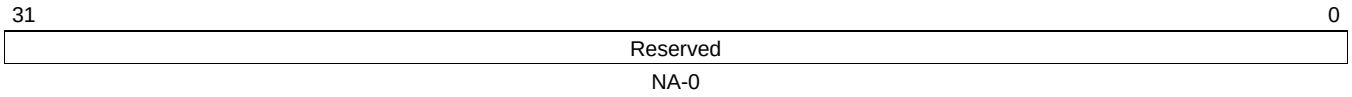
Table 8-1324. DIO2 EE_SIE_E EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.120 DIO2 EE_SIE_E EV0 ENABLED STATUS [Address = 0x1_8368]

EV0 Enabled Status

Figure 8-1184. DIO2 EE_SIE_E EV0 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

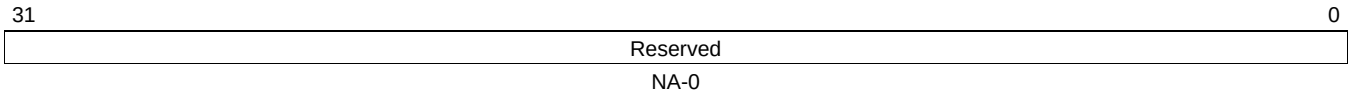
Table 8-1325. DIO2 EE_SIE_E EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.121 DIO2 EE_SIE_E EV1 ENABLED STATUS [Address = 0x1_836C]

EV1 Enabled Status

Figure 8-1185. DIO2 EE_SIE_E EV1 ENABLED STATUS



Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1326. DIO2 EE_SIE_E EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-0	Reserved	Reserved.

8.7.34.122 DIO2 EE_SIE_F RAW INTERRUPT STATUS [Address = 0x1_8370]

SI si_e IQ per-channel SOP received from PSI info

Figure 8-1186. DIO2 EE_SIE_F RAW INTERRUPT STATUS

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1327. DIO2 EE_SIE_F RAW INTERRUPT STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	DIO SI Ingress IQ per channel SOP received from PSI

8.7.34.123 DIO2 EE_SIE_F RAW SET [Address = 0x1_8374]

Raw Set

Figure 8-1187. DIO2 EE_SIE_F RAW SET

31 16	15 0
Reserved	SI_EGR_IQ_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1328. DIO2 EE_SIE_F RAW SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.124 DIO2 EE_SIE_F RAW CLEAR [Address = 0x1_8378]

Raw Clear

Figure 8-1188. DIO2 EE_SIE_F RAW CLEAR

31 16	15 0
Reserved	SI_EGR_IQ_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1329. DIO2 EE_SIE_F RAW CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the raw_status register when set. Write only, self-clears.

8.7.34.125 DIO2 EE_SIE_F EV0 ENABLE STATUS [Address = 0x1_837C]

EV0 Enable Status

Figure 8-1189. DIO2 EE_SIE_F EV0 ENABLE STATUS

31	16	15	0
Reserved		SI_EGR_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1330. DIO2 EE_SIE_F EV0 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr_sts interrupt. Read only.

8.7.34.126 DIO2 EE_SIE_F EV0 ENABLE SET [Address = 0x1_8380]

EV0 Enable Set

Figure 8-1190. DIO2 EE_SIE_F EV0 ENABLE SET

31 16	15 0
Reserved	SI_EGR_IQ_PSI_SOP_INFO
NA-0	W-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1331. DIO2 EE_SIE_F EV0 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.127 DIO2 EE_SIE_F EV0 ENABLE CLEAR [Address = 0x1_8384]

EV0 Enable Clear

Figure 8-1191. DIO2 EE_SIE_F EV0 ENABLE CLEAR

31	16	15	0
Reserved		SI_EGR_IQ_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1332. DIO2 EE_SIE_F EV0 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the enable register when set. Write only, self-clears.

8.7.34.128 DIO2 EE_SIE_F EV1 ENABLE STATUS [Address = 0x1_8388]

EV1 Enable Status

Figure 8-1192. DIO2 EE_SIE_F EV1 ENABLE STATUS

31 16	15 0
Reserved	SI_EGR_IQ_PSI_SOP_INFO
NA-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1333. DIO2 EE_SIE_F EV1 ENABLE STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	When set allows the corresponding bit in the raw_status register to generate the intr1_sts interrupt. Read only.

8.7.34.129 DIO2 EE_SIE_F EV1 ENABLE SET [Address = 0x1_838C]

EV1 Enable Set

Figure 8-1193. DIO2 EE_SIE_F EV1 ENABLE SET

31	16	15	0
Reserved		SI_EGR_IQ_PSI_SOP_INFO	
NA-0		W-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1334. DIO2 EE_SIE_F EV1 ENABLE SET Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	Sets the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.130 DIO2 EE_SIE_F EV1 ENABLE CLEAR [Address = 0x1_8390]

EV1 Enable Clear

Figure 8-1194. DIO2 EE_SIE_F EV1 ENABLE CLEAR

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1335. DIO2 EE_SIE_F EV1 ENABLE CLEAR Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	Clears the corresponding bit in the intr1_status register when set. Write only, self-clears.

8.7.34.131 DIO2 EE_SIE_F EV0 ENABLED STATUS [Address = 0x1_8394]

EV0 Enabled Status

Figure 8-1195. DIO2 EE_SIE_F EV0 ENABLED STATUS

31	16	15	0
Reserved		SI_EGR_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1336. DIO2 EE_SIE_F EV0 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the enable_status register. Read only.

8.7.34.132 DIO2 EE_SIE_F EV1 ENABLED STATUS [Address = 0x1_8398]

EV1 Enabled Status

Figure 8-1196. DIO2 EE_SIE_F EV1 ENABLED STATUS

31	16	15	0
Reserved		SI_EGR_IQ_PSI_SOP_INFO	
NA-0		R-0	

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1337. DIO2 EE_SIE_F EV1 ENABLED STATUS Field Descriptions

Bits	Name	Description
31-16	Reserved	Reserved.
15-0	SI_EGR_IQ_PSI_SOP_INFO	AND-ed raw_status bits with the corresponding bit in the intr1_status register. Read only.

8.7.34.133 DIO2 DIO2_ORIG_REG [Address = 0x1_8420]

This is the DIO2 origination register provided as a shortcut way to determine where an interrupt originated.

Figure 8-1197. DIO2 DIO2_ORIG_REG

31	27	26	24	23	22	20	19
Reserved		Reserved		ORIG_BITFIELD_ING_F	Reserved		ORIG_BITFIELD_ING_E
NA-0		NA-0		R-0	NA-0		R-0

18	17	15	14	13
ORIG_BITFIELD_ING_D	Reserved		ORIG_BITFIELD_EGR_E	ORIG_BITFIELD_EGR_D
R-0	NA-0		R-0	R-0

12	11	9	8
ORIG_BITFIELD_ING_C	Reserved		ORIG_BITFIELD_EGR_C
R-0	NA-0		R-0

7	6	5
ORIG_BITFIELD_EGR_B	ORIG_BITFIELD_DT_A	ORIG_BITFIELD_EGR_A
R-0	R-0	R-0

4	2	1	0
Reserved		ORIG_BITFIELD_ING_B	ORIG_BITFIELD_ING_A
NA-0		R-0	R-0

Legend: R = Read only; W = Write only; - *n* = value after reset

Table 8-1338. DIO2 DIO2_ORIG_REG Field Descriptions

Bits	Name	Description
31-27	Reserved	Reserved
26-24	Reserved	Reserved
23	ORIG_BITFIELD_ING_F	DIO ee_ing_f group of DIO Ingress (SI egress ee_sie_f) registers
22-20	Reserved	Reserved
19	ORIG_BITFIELD_ING_E	DIO ee_ing_e group of DIO Ingress (SI egress ee_sie_e) registers
18	ORIG_BITFIELD_ING_D	DIO ee_ing_d group of DIO Ingress (SI egress ee_sie_d) registers
17-15	Reserved	Reserved
14	ORIG_BITFIELD_EGR_E	DIO ee_egr_e group of DIO Egress (SI ingress ee_sii_g) registers
13	ORIG_BITFIELD_EGR_D	DIO ee_egr_d group of DIO Egress (SI ingress ee_sii_e) registers
12	ORIG_BITFIELD_ING_C	DIO ee_ing_c group of DIO Ingress (SI egress ee_sie_a) registers
11-9	Reserved	Reserved
8	ORIG_BITFIELD_EGR_C	DIO ee_egr_c group of DIO Egress (SI ingress ee_sii_c) registers
7	ORIG_BITFIELD_EGR_B	DIO ee_egr_b group of DIO Egress (SI ingress ee_sii_a) registers
6	ORIG_BITFIELD_DT_A	DIO ee_dt_a group of DIO Data Trace registers
5	ORIG_BITFIELD_EGR_A	DIO ee_dma_egr_a group of DIO Egress core registers
4-2	Reserved	Reserved
1	ORIG_BITFIELD_ING_B	DIO ee_dma_ing_b group of DIO Ingress core registers
0	ORIG_BITFIELD_ING_A	DIO ee_dma_ing_a group of DIO Ingress core registers

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