JAMR3

User's Guide

Literature Number: SPRUI52
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JAMR3

This user's guide only discusses the hardware for the JAMR3 application board. Details for the CPU board are not discussed in this document.

1 Scope

JAMR3 is the third generation of the Jacinto Medio Radio (JAMR) hardware reference design evaluation module (EVM) based on Texas Instruments Jacinto series SoC silicon solutions. It is architected to maximize the scalability and re-use strategy for current and future SoC silicon devices. When assembled to the EVM CPU Board [1], it allows for early software development using the Jacinto 6 SoC and typical peripherals that are commonly found in an automotive infotainment head unit and system.

The JAMR3 application board hardware consists of:

- Four Radio Tuners
- Four Dual Band DAB LNA's
- Three Audio Codecs
- CDM Interface
- USB to I2C Gateway
- Four NTSC/PAL Inputs
- FPD-Link
- Video Mux
- Two Audio Microphone Inputs
- Aux Audio Input
- Three Stereo Audio Outputs
- Audio Amplifier Interface
- Interface to Jacinto 6 Processor Board

In order to emulate an infotainment system, the JAMR3 board must be plugged into a required EVM CPU Board.

Figure 1 is an illustrative top view of the JAMR3 application board.

This document only discusses the hardware for the JAMR3 application board. Details for the CPU board are not discussed in this document.

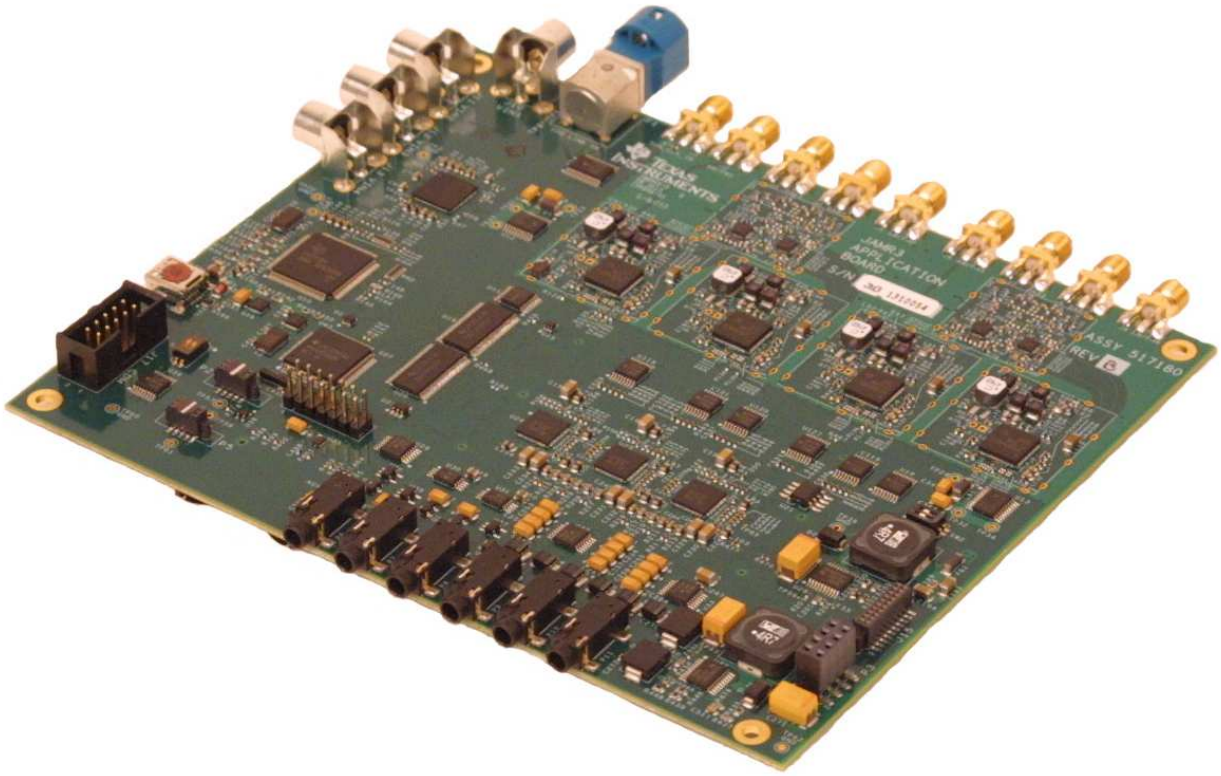


Figure 1. JAMR3 Application Board Top View

2 Overview

JAMR3 application board is the 3rd generation of JAMR reference design based on the Texas Instruments Jacinto series SoC processor for media radio applications in the automotive infotainment market space.

2.1 JAMR3 Application Board

JAMR3 application board has the following key features and hardware functions:

- Power supply: 12V, negative grounding system, the same as a vehicle battery provides
- PCB dimension (W x H x D): 170mm x 35mm x 140mm (without LCD panel)
- PCB design: 6 layer board stack
- Connections
  - Front Connections
    - Standard SD Socket
    - Two – 3.5 mm Microphone Inputs
    - One – 3.5 mm Stereo Aux Audio Input
    - Three – 3.5 mm Stereo Audio Outputs
  - Rear Connections:
    - One Composite Camera Video Input
    - FPD-Link [2]
    - RF antennas

    - Tuner Clock Input
  - Side Connections:
    - Three Composite Camera Video Inputs
    - USB Mini-B (For Conversion to I2C)
  - Other Connections or Connectors on the Top Side of the PCB:
    - Audio Amplifier Interface
    - iPod authentication daughter board
    - HD Radio conditional access daughter board
    - For debug and software development: CDM (Control and Diagnostic Monitor I2C interface to the Aardvark [3] interface pod)
  - Bottom Connections:
    - Signals and Power Rail Supplies to/from Processor Board
- Other Hardware Functions:
  - TVP5158 Video Decoder [4]
  - 3 x AIC3106 Audio CODEC's [5]
  - 4 x AFE8310D RF2bits Tuners
  - 4 x AFE8316 DAB LNA's

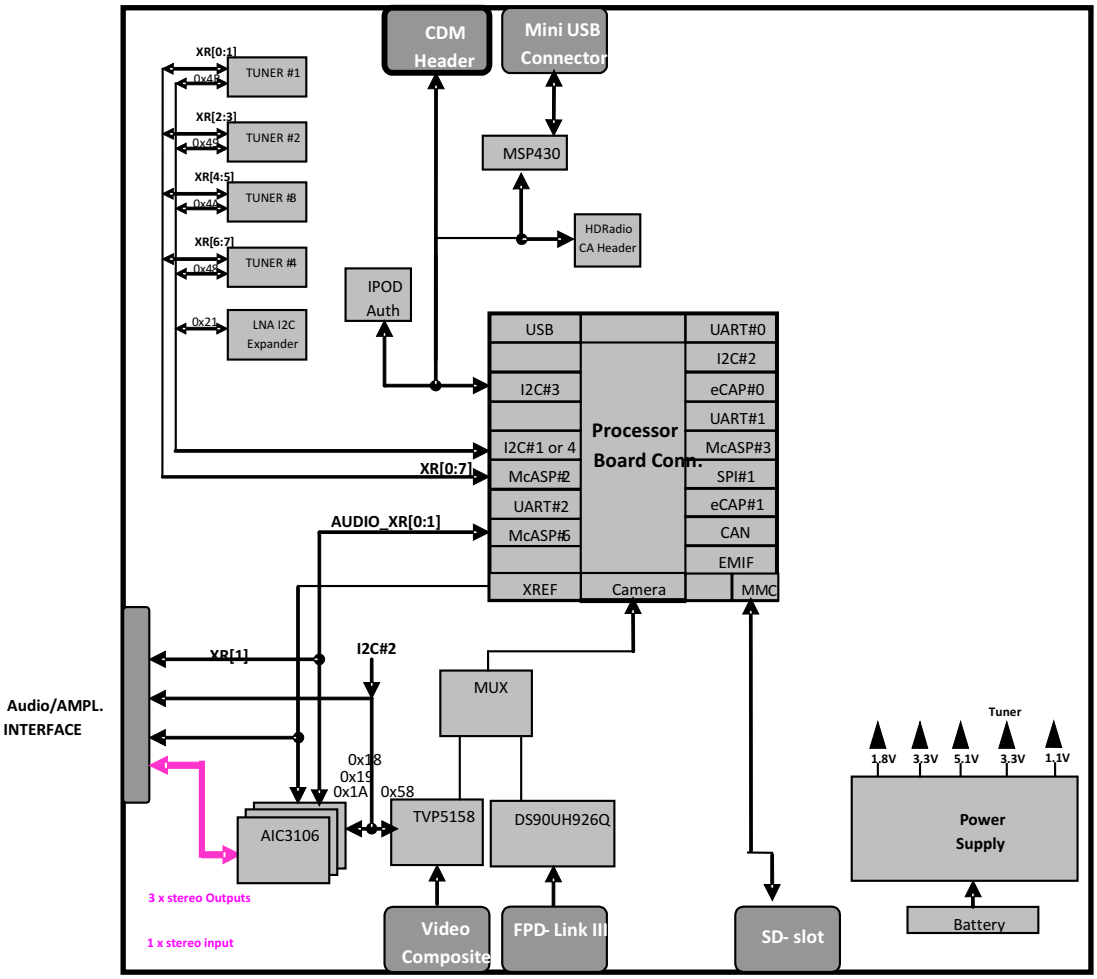
Features and hardware functions not supported in JAMR3 application board are listed below:

- Ethernet RJ45 (On Processor Board)
- JTAG Header (On Processor Board)
- Serial CD Mechanisms (Deleted)
- Socket for iPod Authentication IC (Changed to Header on JAMR3 Application Board)
- Connector for Off – Board Standard Size SD Socket (Replaced with Standard Size SD Socket.)
- NOR Flash Memory (On Processor Board)
- NAND Flash Memory (On Processor Board)
- Bootmode Switch (On Processor Board)
- Header to Support SPI Bootmode (On Processor Board)
- Header for Two Additional RF2bits Tuners (Two Additional Tuners Added to Board)

3 Hardware

3.1 Application Board Hardware Architecture

The JAMR3 application board block diagram is shown in Figure 2.



A Pink lines are analog audio signal connections

B Functions with bold outline are for debug purpose

Figure 2. JAMR3 Hardware Functional Block Diagram

3.1.1 Processor Board Connections

Three Samtec QTE [6] high speed terminal strip connectors with 5mm in height are used for the connections to a processor board.

The signal list for the processor interface connector (EXP_P1 in the schematic) is listed in Table 1.

Table 1. Processor Connector EXP_P1 Pin Assignment

Peripherals	Signals	Pin No	Pin Count	Usage/Comments
I2C	I2C3_SCL	1	1	CDM, iPod, HDRadio
	I2C3_SDA	3	2	CDM, iPod, HDRadio
	I2C4_SCL	11	3	Tuners/LNA's
	I2C4_SDA	12	4	Tuners/LNA's
FPD-Link III	VIN[5]A_D[9]_McASP5_AXR0	6	5	FPD-Link III Audio
	VIN[5]A_D[10]_McASP5_FSX	7	6	FPD-Link III Audio
	VIN[5]A_D[11]_McASP5_ACLKX	8	7	FPD-Link III Audio
	GP6[17]_XREF_CLK0	15	8	FPD-Link III Audio
IRQ	IRQ2DSP_GP5[22]	33	9	HDRadio CA
	IRQ2DSP_GP5[25]	35	10	HDRadio CA
Audio Amplifier Interface	FAULT_GP5[29]	34	11	Audio Amplifier
	CLIP_OTW_GP5[30]	36	12	Audio Amplifier
	MUTE_EN_GP5[31]	38	13	Audio Amplifier
Ground	GND	2	14	Ground
	GND	4	15	Ground
	GND	10	15	Ground
	GND	19	17	Ground
	GND	20	18	Ground
	GND	29	19	Ground
	GND	30	20	Ground
	GND	39	21	Ground
	GND	40	22	Ground
Unused	N/C	5	23	
	N/C	9	24	
	N/C	13	25	
	N/C	14	26	
	N/C	16	27	
	N/C	17	28	
	N/C	18	29	
	N/C	21	30	
	N/C	22	31	
	N/C	23	32	
	N/C	24	33	
	N/C	25	34	
	N/C	26	35	
	N/C	27	36	
	N/C	28	37	
	N/C	31	38	
	N/C	32	39	
	N/C	37	40	

The signal list for the processor interface connector (EXP_P2 in the schematic) is listed in Table 2.

Table 2. Processor Connector EXP_P2 Pin Assignment

Peripherals	Signals	Pin No	Pin Count	Usage/Comments
VDIN	VIN[1]A_HSYNC0	1	1	
	VIN[1]A_VSYNC0	2	2	
	VIN[1]A_DE0	25	3	
	VIN[1]A_CLK	48	4	Video input pixel clock0
	VIN[1]B_CLK1	75	5	Video input pixel clock1
	VIN[1]A_D[0]	40	6	Video input data
	VIN[1]A_D[1]	41	7	Video input data
	VIN[1]A_D[2]	42	8	Video input data
	VIN[1]A_D[3]	43	9	Video input data
	VIN[1]A_D[4]	44	10	Video input data
	VIN[1]A_D[5]	45	11	Video input data
	VIN[1]A_D[6]	46	12	Video input data
	VIN[1]A_D[7]	47	13	Video input data
	VIN[1]A_D[8]	68	14	Video input data
	VIN[1]A_D[9]	67	15	Video input data
	VIN[1]A_D[10]	70	16	Video input data
	VIN[1]A_D[11]	69	17	Video input data
	VIN[1]A_D[12]	72	18	Video input data
	VIN[1]A_D[13]	71	19	Video input data
	VIN[1]A_D[14]	74	20	Video input data
	VIN[1]A_D[15]	73	21	Video input data
	VIN[1]A_D[16]	3	22	Video input data
	VIN[1]A_D[17]	4	23	Video input data
	VIN[1]A_D[18]	5	24	Video input data
	VIN[1]A_D[19]	6	25	Video input data
	VIN[1]A_D[20]	7	26	Video input data
	VIN[1]A_D[21]	8	27	Video input data
	VIN[1]A_D[22]	9	28	Video input data
	VIN[1]A_D[23]	10	29	Video input data
McASP	C_MCASP2_ACLKX	29	30	Tuner Bit Clock
	C_MCASP2_AFSX	31	31	Tuner Frame Sync
	C_MCASP2_AXR[0]	37	32	Tuner serial port
	C_MCASP2_AXR[1]	33	33	Tuner serial port
	C_MCASP2_AXR[2]	39	34	Tuner serial port
	C_MCASP2_AXR[3]	35	35	Tuner serial port
	C_MCASP2_AXR[4]	23	36	Tuner serial port
	C_MCASP2_AXR[5]	24	37	Tuner serial port
	C_MCASP2_AXR[6]	22	38	Tuner serial port
	C_MCASP2_AXR[7]	38	39	Tuner ref clock enable
	C_MCA6_ACLKX	104	40	Serial port CLK audio amp
	C_MCA6_AFSX	102	41	Serial port FSX audio amp
	C_MCA6_AXR0	103	42	Audio serial port
	C_MCA6_AXR1	105	43	Audio serial port
	C_MCA6_AHCLKX	106	44	Audio ref clock
I2C	I2C1_SCL	30	45	Tuners/LNA's
	I2C1_SDA	28	46	Tuners/LNA's

Table 2. Processor Connector EXP_P2 Pin Assignment (continued)

Peripherals	Signals	Pin No	Pin Count	Usage/Comments
GPIO	GP5[17]	32	47	Maybe or Unconnected
	GP5[1]	36	48	Maybe or Unconnected
Power	DC_12V	49	49	12 V DC from processor board
	DC_12V	50	50	12 V DC from processor board
	DC_12V	51	51	12 V DC from processor board
	DC_12V	52	52	12 V DC from processor board
	DC_12V	53	53	12 V DC from processor board
	DC_12V	54	54	12 V DC from processor board
	EXP_DC_1V8	55	55	CPU 1.8V power supply from JAMR3 board
	EXP_DC_1V8	56	56	CPU 1.8V power supply from JAMR3 board
	EXP_DC_3V3	57	57	I/O and board level supply (from processor board)
	EXP_DC_3V3	58	58	I/O and board level supply (from processor board)
	EXP_DC_3V3	59	59	I/O and board level supply (from processor board)
	EXP_DC_3V3	60	60	I/O and board level supply (from processor board)
	DC_5V1	65	61	5.1 V Analog Audio (from processor board)
	DC_5V1	66	62	5.1 V Analog Audio (from processor board)
Reset	RESET_GP5[0]	34	63	HDRadio CA
	APP_BD_PORz	76	64	System reset from processor board
Ground	GND	26	65	Ground
	GND	27	66	Ground
	GND	77	67	Ground
	GND	78	68	Ground
	GND	115	69	Ground
	GND	116	70	Ground

Table 2. Processor Connector EXP_P2 Pin Assignment (continued)

Peripherals	Signals	Pin No	Pin Count	Usage/Comments
Open	N/C	11	71	
	N/C	12	72	
	N/C	13	73	
	N/C	14	74	
	N/C	15	75	
	N/C	16	76	
	N/C	17	77	
	N/C	18	78	
	N/C	19	79	
	N/C	20	80	
	N/C	21	81	
	N/C	61	82	
	N/C	62	83	
	N/C	63	84	
	N/C	64	85	
	N/C	79	86	
	N/C	80	87	
	N/C	81	88	
	N/C	82	89	
	N/C	83	90	

Table 2. Processor Connector EXP_P2 Pin Assignment (continued)

Peripherals	Signals	Pin No	Pin Count	Usage/Comments
Open	N/C	84	91	
	N/C	85	92	
	N/C	86	93	
	N/C	87	94	
	N/C	88	95	
	N/C	89	96	
	N/C	90	97	
	N/C	91	98	
	N/C	92	99	
	N/C	93	100	
	N/C	94	101	
	N/C	95	102	
	N/C	96	103	
	N/C	97	104	
	N/C	98	105	
	N/C	99	106	
	N/C	100	107	
	N/C	101	108	
	N/C	107	109	
	N/C	108	110	
	N/C	109	111	
	N/C	110	112	
	N/C	111	113	
	N/C	112	114	
	N/C	113	115	
	N/C	114	116	
	N/C	117	117	
	N/C	118	118	
	N/C	119	119	
	N/C	120	120	

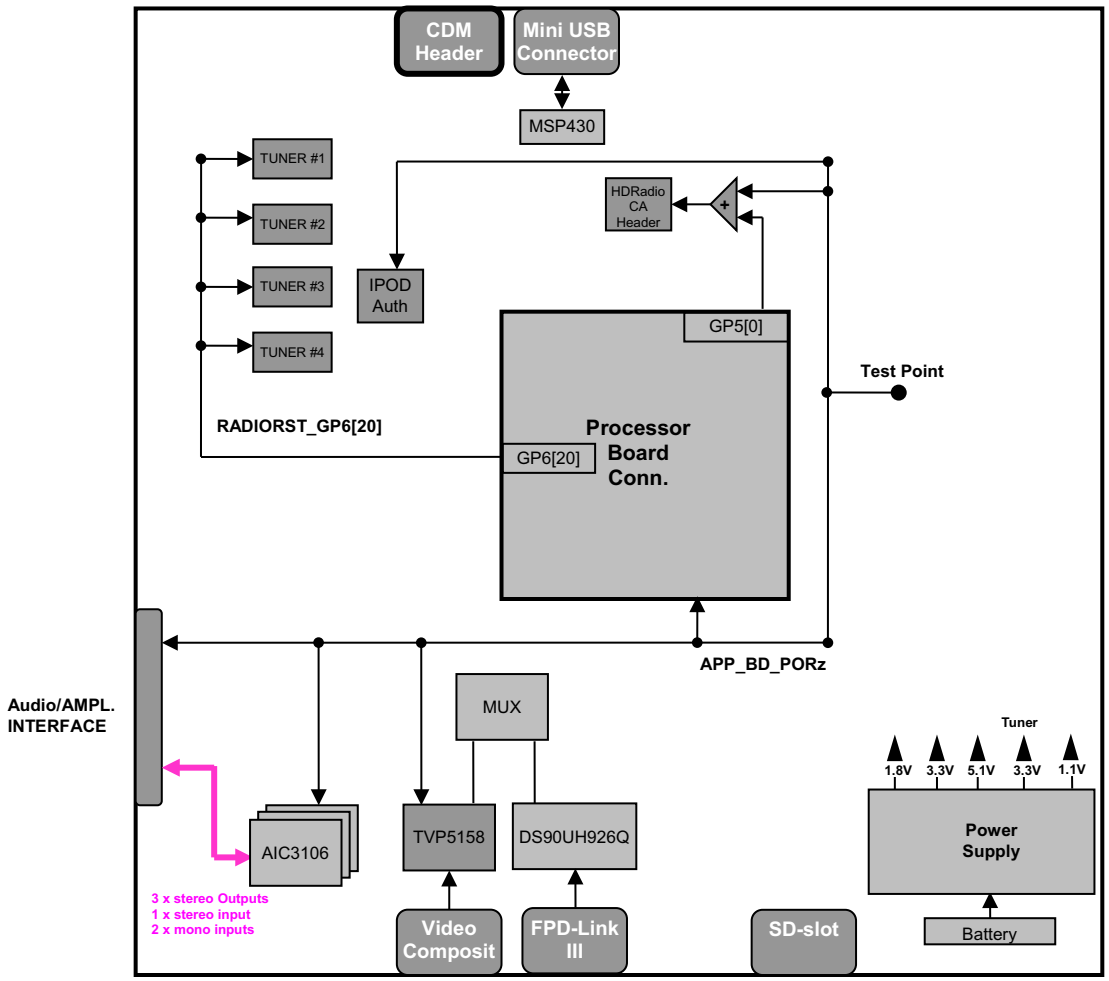
The signal list for the processor interface connector (EXP_P3 in the schematic) is listed in Table 3.

Table 3. Processor Connector EXP_P3 Pin Assignment

Peripherals	Signals	Pin No	Pin Count	Usage/Comments
GOIO	RADIORST_GP6[20]	11	1	Tuner reset
	RADIORST_GP6[20]	13	2	Tuner reset
MMC	MMC3_CLK	25	3	MMC clock
	MMC3_CMD	26	4	MMC command
	MMC3_DAT0	28	5	MMC data
	MMC3_DAT1	30	6	MMC data
	MMC3_DAT2	27	7	MMC data
	MMC3_DAT3	29	8	MMC data
I2C	I2C2_SDA	21	9	AIC3106's, TVP5158, FPD-Link III
	I2C2_SCL	22	10	AIC3106's, TVP5158, FPD-Link III
Ground	GND	19	11	Ground
	GND	20	12	Ground
	Optional GND	40	13	Optional Ground or Pull Down R183
Open	N/C	1	14	
	N/C	2	15	
	N/C	3	16	
	N/C	4	17	
	N/C	5	18	
	N/C	6	19	
	N/C	7	20	
	N/C	8	21	
	N/C	9	22	
	N/C	10	23	
	N/C	12	24	
	N/C	14	25	
	N/C	15	26	
	N/C	16	27	
	N/C	17	28	
	N/C	18	29	
	N/C	23	30	
	N/C	24	31	
	N/C	31	32	
	N/C	32	33	
	N/C	33	34	
	N/C	34	35	
	N/C	35	36	
	N/C	36	37	
	N/C	37	38	
	N/C	38	39	
	N/C	39	40	

3.1.2 Reset Structure

Figure 3 shows the block diagram of the reset structure.



A Functions with bold outline are for debug purpose

Figure 3. Reset Structure Block Diagram

The supervisor chip (TPS3808G09DBVR [7]) is responsible for generating the power-on system reset signal, SYS_RESETn, for the board which is qualified by the core and the I/O supplies during the power ramp cycle. The manual reset push button SW4 also generates the system reset for the JAMR3 system. When an external controller is connected, the system reset can be activated by the external controller.

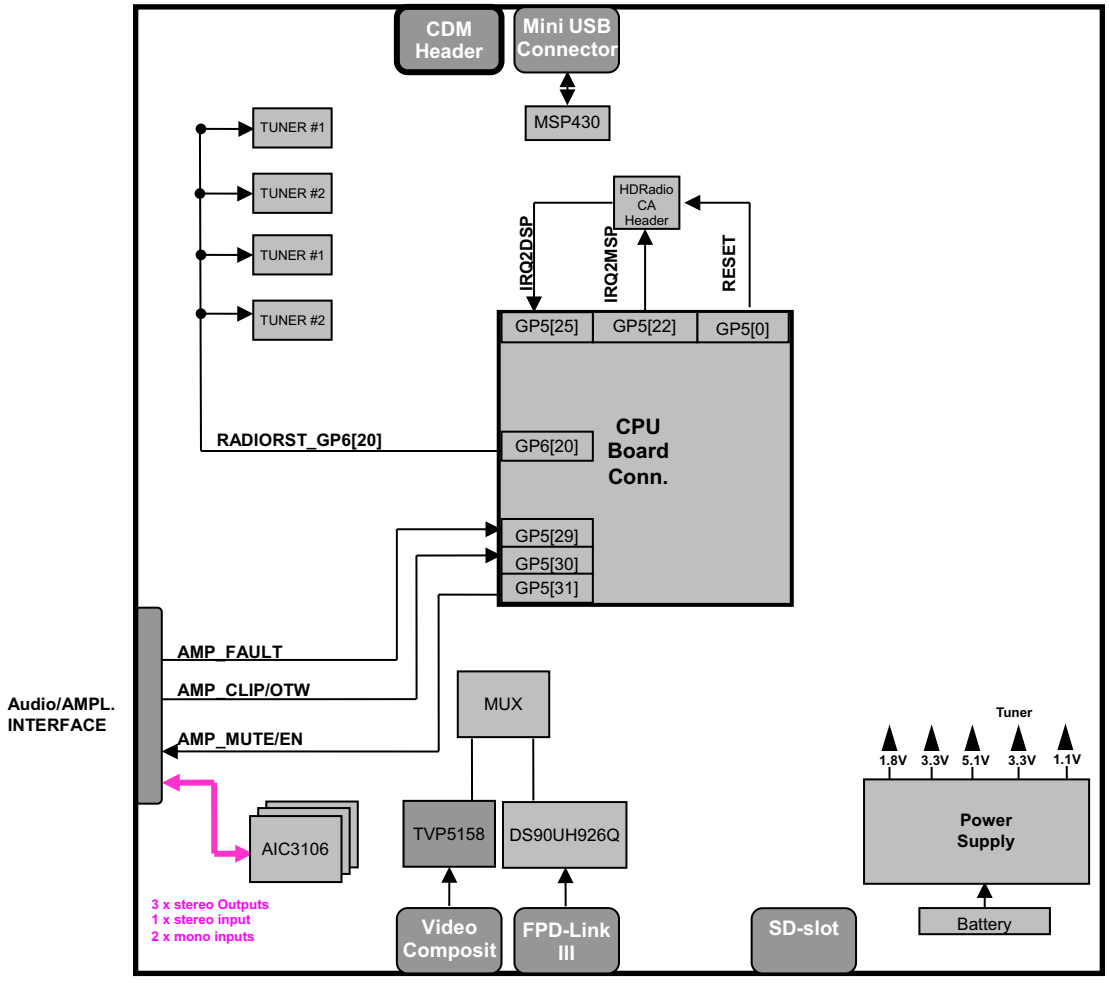
Table 4 summarizes the reset implementation.

Table 4. Reset Types

Reset Type	Initiators	Effects
POR_RESET (active low)	Power-up	JAMR3 whole system reset
	SW4	Hardware reset for the following items: • Processor • Tuner-1, Tuner-2, Tuner-3, Tuner-4 • iPod Auth. module, HD Radio conditional access module • iPod Auth. module, HD Radio conditional access module
	External Controller via HMI connector	
Processor Software controlled Resets	GP5[0], GP6[20]	• Hardware reset for HD Radio conditional access module • Tuner-1, Tuner-2, Tuner-3, Tuner-4

3.1.3 GPIO Usage

The GPIOs are required for control and information feedback purpose in the system, Figure 4 is the block diagram.



A Functions with bold outline are for debug purpose

Figure 4. GPIO Usage Block Diagram

There are seven GPIOs provided by the processor to the JAMR3 board. Table 5 summarizes the usage of the GPIOs.

Table 5. GPIO Usage Summary

JAMR3 Functions	GPIO Ports	I/O Type [1]	GPIO Usage
Tuners	GP6[20]	O	RADIORST, reset radio tuner chips
HD Radio Conditional Access	GP5[25]	IN	HD Radio conditional access control, interrupt to processor.
	GP5[0]	O	DSP reset to HD Radio conditional access control
	GP5[22]	O	HD Radio conditional access control, interrupt from processor
Audio Power Amplifier	GP5[30]	I	CLIP_OTW, the amplifier module clip/over-temperature detection
	GP5[29]	I	FAULT, the amplifier module faulty detection
	GP5[31]	O	MUTE_EN, the amplifier module mute or enable

[1] The I/O type is relevant to the processor.

3.1.4 Power Supply

The power supply circuits require a DC input of 10.5 V to 19.5 V from a processor board. Figure 5 shows the power supply block diagram.

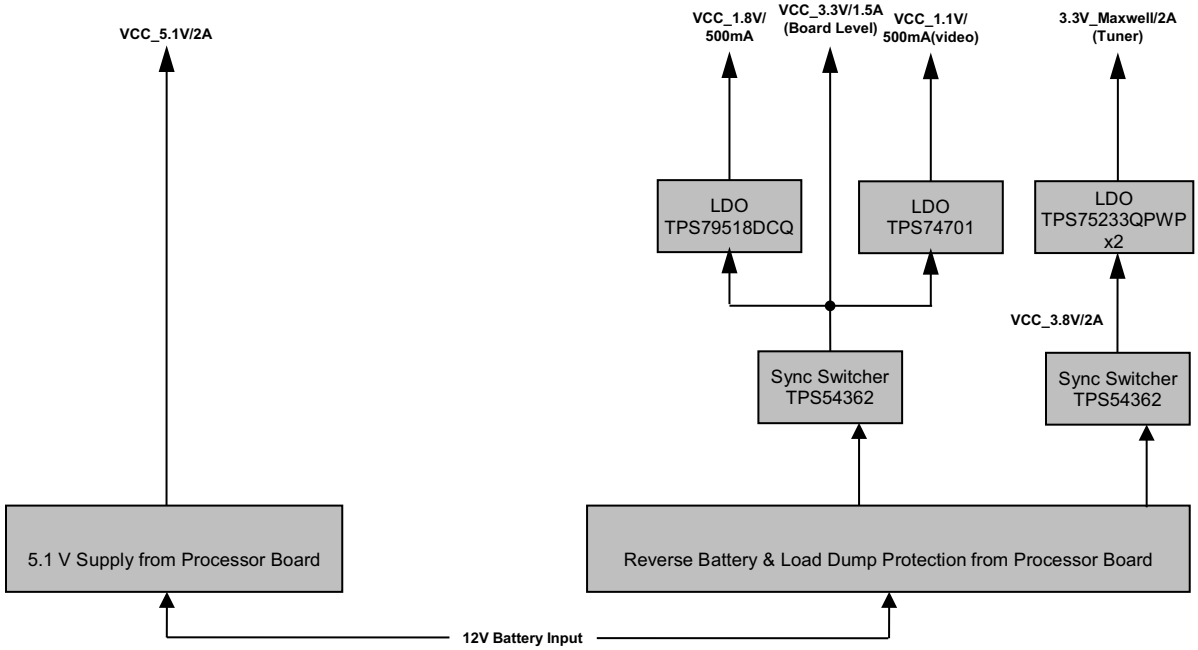


Figure 5. Power Supply Block Diagram

3.1.4.1 Reverse Battery and Load Dump Protection

Battery reversal and load dump over-voltage are common improper operations or occurrences in automotive applications. RBO40_40G is a single chip safeguard solution to protect the internal circuits from damage due to battery reversal and load dump over-voltage. This is implemented on the processor board.

3.1.4.2 Switching and Linear Power Supplies

There are 2 switching power supply regulators and four LDO linear regulators.

Table 6 shows the characteristics of the power supplies.

Table 6. Power Supply Regulator Characteristics

Power Domains	Regulator Chips	Free Running /Sync Switching Frequency	Input Voltage	Output Current (Max)
VCC_3.3V	TPS54362QPWPRQ1 [8]	1910 KHz SYNC	12 V battery	1 A
VCC_3.8V	TPS54362QPWPRQ1	1910 KHz SYNC	12 V battery	2 A
3.3V_Maxwell	TPS75233QPWP x2 [9]	(LDO linear regulator)	VCC_3.8V	2 A
VCC_1.1V	TPS74701 [10]	(LDO linear regulator)	VCC_3.3V	200 mA
VCC_1.8V	TPS74701	(LDO linear regulator)	VCC_3.3V	500 mA
5.1 V	From Processor		From Processor	

12V and 5.1V enter the board through the interface connectors from the processor board. The VCC_3.3V is generated on the JAMR3 board and also exported to the processor board. VCC_1.8V supplies power to the TVP5158 camera encoder, the AIC3106's, and is exported to the processor board through the interface connectors. VCC_1.1V supplies power to the TVP5158. The VCC_3.8V and 3.3V_Maxwell supplies support the tuner (AFE8310D) and LNA (AFE8316) chips.

For more information on the power supply regulator chips, see the relevant documents in Section 7.

3.1.5 Interface for Debug

The CDM header (for interface with Aardvark interface pod) is for debug and software development, it is required for radio application bring-up.

The CDM 10 pin header supports the connection to the Aardvark Embedded System Interface, which allows a PC based GUI to control the audio applications, such as starting radio in one audio zone and playing media audio in a second audio zone. I2C#3 interfaces with the CDM header and acts as an I2C bus slave.

In addition to using an Aardvark interface pod, a Mini USB connector that interfaces to an MSP430 has been added to the board to convert USB input into I2C commands on I2C#3.

3.2 Quad-Tuner Radio

The quad-tuner radio configurations are achieved by leveraging four of TI's single-chip AFE8310 tuner ICs. The AFE8310 is an RF-in digital I/Q-out tuner for low cost automotive-class AM/FM/FMRDS/WB/HD/DAB/SW reception. It includes integrated LNAs, mixer, PLL, VCO, ADC and digital decimation filters to support glue-less connections to the processor. For each AFE8310, there is an SMA connector for AM/FM and another for DAB3/DABL. Each AFE 8310 has associated with it a DAB LNA (AFE8316). The DAB3/DABL SMA connectors route to the AFE8316's prior to the AFE8310's. The inputs can be configured for signals from one or two DAB3/DABL antenna connectors driving 2 AFE8310/AFE8216 combinations. The AM/FM inputs can also be configured for one or two AM/FM antenna signals driving 2 AFE8310's.

For AM/FM, the board is built with one AM/FM RF input driving one AFE5310 Tuner. There are unpopulated pads in each tuner section that can link multiple tuners together for either AM or FM. Examining pages 9 to 12 of the JAMR3 schematic shows what pads are available for this use. Connecting multiple tuners together should be done with caution and by someone that is skilled in RF engineering or the assistance of someone with RF engineering skills.

In its default build state, RF DAB signals entering the DAB3/DABL 1 connector (J3) are routed through a DAB Diplexer/preselector, then onto LNA1 (U3), and subsequently to Tuner 1 (U6). RF DAB signals entering the DAB3/DABL 2 connector (J4) are routed through a DAB Diplexer/preselector, then onto LNA2 (U1) and subsequently to Tuner 2 (U7). RF DAB signals entering the DAB3/DABL 3 connector (J7) are routed through a DAB Diplexer/preselector/power divider (for each band), then onto LNA3 (U4) and LNA4 (U2) and subsequently to Tuner 3 (U8 from LNA3) and Tuner 4 (U9 from LNA4), respectively. RF DAB signals entering the DAB3/DABL 4 connector (J8) do not ultimately connect to any tuners.

Circuitry between the RF DAB input connectors and the LNA's is flexible. It can be configured for each RF DAB input to ultimately feed a single tuner, or signals from any one RF connector can ultimately feed 2 tuners. In the one connector to 2 tuners mode, either the DAB3/DABL 1 connector (J3) or the DAB3/DABL 2 connector (J4) can ultimately, simultaneously feed Tuner 1 and Tuner 2. The opposite connector will be unused in this use case. Tuner 3 and Tuner 4 can be ultimately, simultaneously fed by either the DAB3/DABL 3 connector (J7) or the DAB3/DABL 4 connector (J8). Again the opposite connector will be unused in this use case.

There are zero ohm jumpers and additional component pads available as needed to reconfigure the circuitry that is downstream of the DAB3/DABL 1 connector (J3) and the DAB3/DABL 2 connector (J4) so that either one can be ultimately used as a single source for both Tuner 1 and Tuner 2. The as built circuitry from the DAB3/DABL 3 connector (J7) and the DAB3/DABL 4 connector (J8) side of the board should be used as a guide for hardware component changes to the DAB3/DABL 1 connector (J3) and the DAB3/DABL 2 connector (J4) side of the board when attempting to make such a change.

The corollary is true on the DAB3/DABL 3 connector (J7) and the DAB3/DABL 4 connector (J8) side of the board when attempting to change the signal structure so the DAB3/DABL 3 connector (J7) signals route only to Tuner 3 and the DAB3/DABL 4 connector (J8) signals to route only to Tuner 4.

RF hardware changes to the board should only be performed by those skilled in RF engineering or under the guidance of someone that is skilled in RF engineering. Schematics for the RF DAB Diplexers/preselectors/power dividers are located on pages 7 and 8 of the JAMR3 schematic.

Each DAB LNA has 3 GPIO control lines associated with it. As the board is built, one of the 3 control lines comes from the respective tuner and the state of the others is controlled by the processor. The state of the HG_x lines are controlled by the respective Tuner x. For each LNA there is an LNA_HI_ISOL_x line controlled by the processor. Control of this line can also be managed by the state of the corresponding HG_x line. If it is desired to control the LNA_HI_ISOL_x with the HG_x line there are pad sets CF1, CF2, CF3, and CF4 for this purpose. Disconnecting pads 1 and 2 on CFx and reconnecting pads 1 and 4 achieves this goal. There is also pad 3 on CFx that permanently connects LNA_HI_ISOL_x to 3.3 V.

2 GPIO signals on each DAB LNA are controlled from the processor via an I2C expander (U14, page 6 of the JAMR3 Schematic). Care must be taken when setting up the I2C expander, because MMC_WP, MMC_CD, and the video mux are also connected to this I2C expander. When changing LNA controls, care must be taken not to overwrite the state of the video mux (SEL_TVP_FPD) on the expander when the LNA states are changed.

The I2C#1 or I2C#4 bus configure all of the tuner chips and the I2C expander (U14). The I2C bus is switch selectable. If slider "1-4" of SW2 is in the "4" position, the tuners are connected to the I2C#1 bus; if in the "1" position, they are connected to the I2C#4 bus. Table 7 lists the tuner I2C addresses along with GPIO and McASP#2 connections.

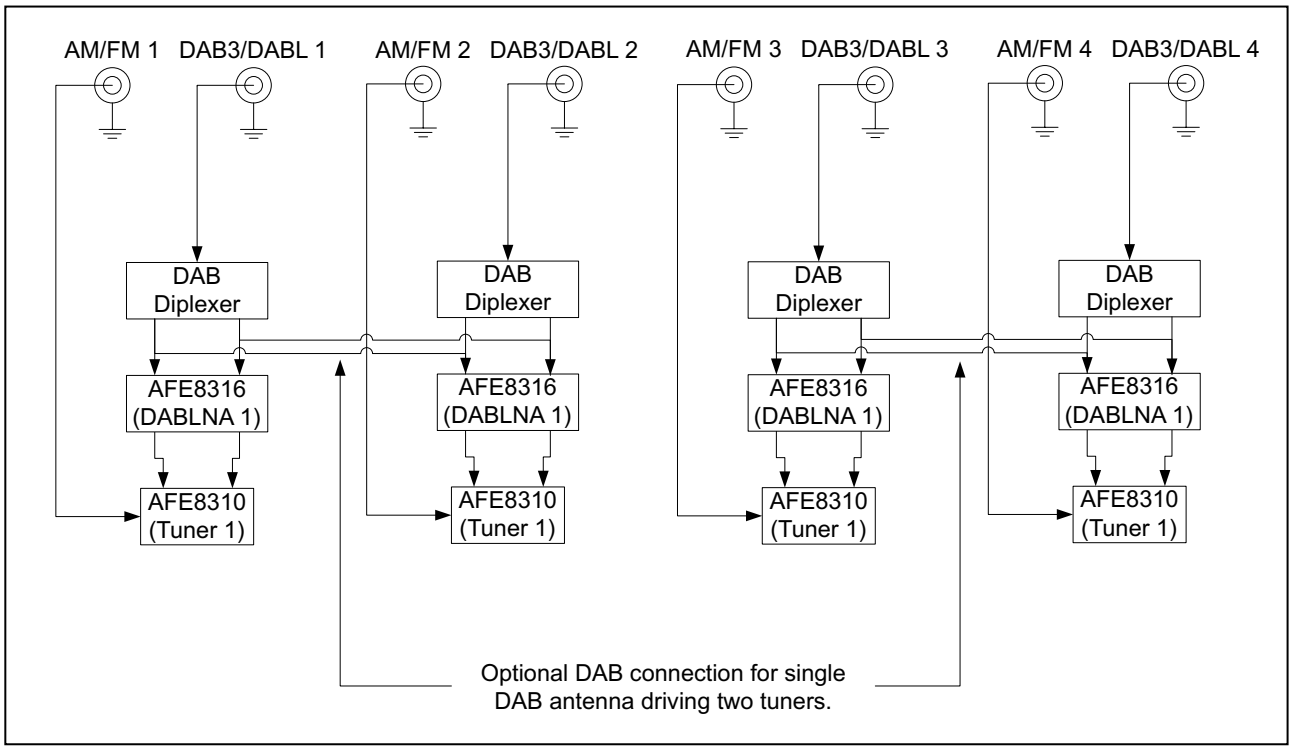


Figure 6. Radio Functional Block Diagram

In addition the RF input connectors, the JAMR3 board has a clock input connector, J1. The board can be modified to drive the tuner subsystem with an external reference clock instead of the crystal (X1 – see p. 9 of the schematic) attached to Tuner 1 from connector J1. To do this, remove C168 and R82, and add a 1000 pF capacitor into C167. Now an external oscillator source is needed to drive the tuner subsystem.

Table 7. AFE8310 I2C, McASP, and GPIO Signals

Tuner Number	I2C Address	Connections to McASP2				Reset GPIO
		d0	d1	Bit Clock	Frame Sync	
1	0x4B11	XR[0]	XR[1]	CLKX	FSX	GP6[20]
2	0x4901	XR[2]	XR[3]			
3	0x4A10	XR[4]	XR[5]			
4	0x4800	XR[6]	XR[7]			

SMA RF connectors are used for antenna connections and the tuner clock input connector. Tuner RF connector numbering is listed in Section 6.

3.3 Audio Functions

3.3.1 Audio Functions on Application Board

Three AIC3106 audio CODECs are utilized to interface from the TDM audio to the analog audio I/O in the system. The low cost audio codec AIC3106 performs the digital-to-analog conversion (DAC) and/or analog-to-digital conversion (ADC).

There is also an Audio/Amplifier Interface for a digital input amplifier. The interface consists of two connectors: one connector provides 12 V power and ground, and the other connector interfaces to the same TDM audio source as the AIC3106's.

Listed below are the audio channels and signals on AUDIO/AMP connectors:

- 3 x stereo outputs
- 1 x stereo input
- 2 x mono inputs
- 3 GPIOs:
  - AMP_FAULT
  - AMP_CLIP/OTW
  - MUTE_EN
- System reset
- Other signals: MICDET
- Power supplies: 12V for power amplifier, 5.1V for filtering circuits

There are two connectors for the audio functions:

- 12 V power connector: 12V supply.
- TDM audio output, GPIO, and 5.1V amplifier interface.

Figure 7 is the audio functional block diagram.

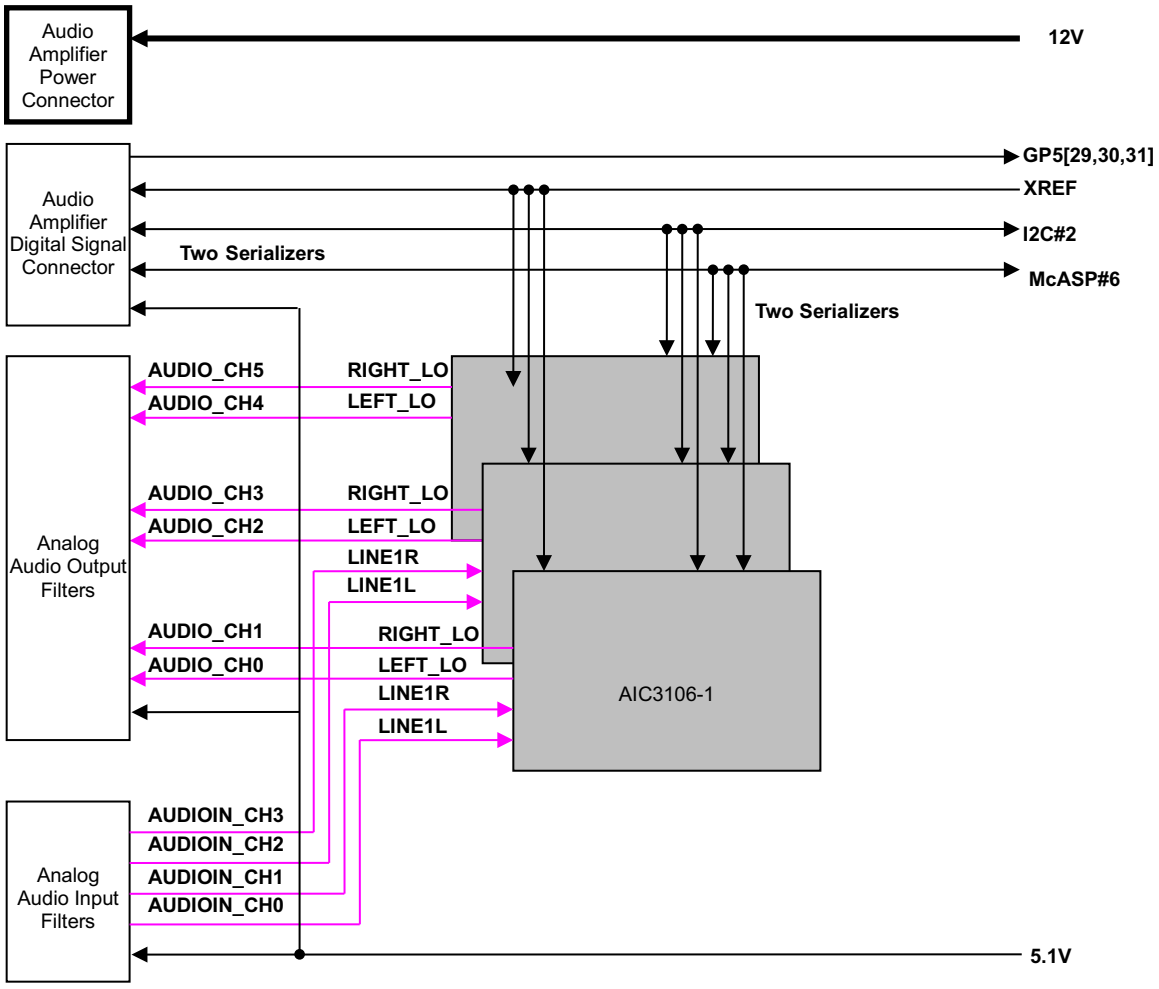


Figure 7. Audio Functional Block Diagram

A SamTec 8 pin SSW type connector (SSW-104-22-F-G-D [11]) is used for the 12 V supply. A 20-pin SFM connector (SFM-110-02-S-D-LC [12]) is utilized for the Audio Amplifier Digital Audio Connector.

Table 8 lists the signals on audio amplifier digital signal connector.

Table 8. Audio/AMP Interface Signals

Connectors	Signals	I/O Type	Pin Number	Descriptions
Audio Amplifier Digital Signal Connector	RMCA6_ACLKX	O	13	Audio serial port bit clock
	RMCA6_AFSX	O	15	Audio serial port frame sync
	RMCA6_AXR0	O	7	Audio serial port data
	RMCA6_AXR1	O	11	Audio serial port data
	I2C#2_SCL	I/O	16	I2C#2 serial clock
	I2C#2_SDA	I/O	14	I2C#2 serial data
	MCA6_AHCLKX (XREF)	O	9	System clock from processor
	GP5[29]	I	10	Used as MICDET or AMP_FAULT, the amplifier module faulty detection,
	GP5[30]	I	8	Used as CLIP/OTW, the amplifier module clip/over-temperature detection
	GP5[31]	O	6	Used as mute or enable control to the amplifier module
	SYS_RESET	O	5	System reset signal from JAMR3 system

The I2C#2 is the control bus that allows the processor to control and configure each codec that is an I2C slave, with the slave addresses being 0x18, 0x19 and 0x1A for AIC3106 unit #1, #2 and #3.

McASP#6 serial port connects the digital audio data output from the processor to the audio codecs and the Audio Amplifier Digital Signal Connector. The analog audio input is converted into digital data format by the ADC of the codec and sent to the processor via McASP#6 serial ports as well.

GP5[29] is used as the interrupt signal to the processor for microphone detection with an audio amplifier attached.

The system clock (22.5792MHz) of the AIC3106 is provided via the processor connector and is also connected to the AUDIO/AMP interface as the system clock for the audio amplifier module.

The ADC common mode voltage is 1.35V while the DAC common mode voltage is programmable and is used as 1.65V. The low noise reference of these common mode voltages is required for the differential circuit operations.

The rest of the audio subsystem includes the following signal routing and features:

- 3.5 mm audio jacks:
  - AUX stereo audio input
  - Two mono MIC inputs
  - Three stereo audio outputs
- Differential-to-single conversion for audio outputs
- Single-to-differential conversion for audio inputs

Figure 8 shows the block diagram of the analog audio circuits.

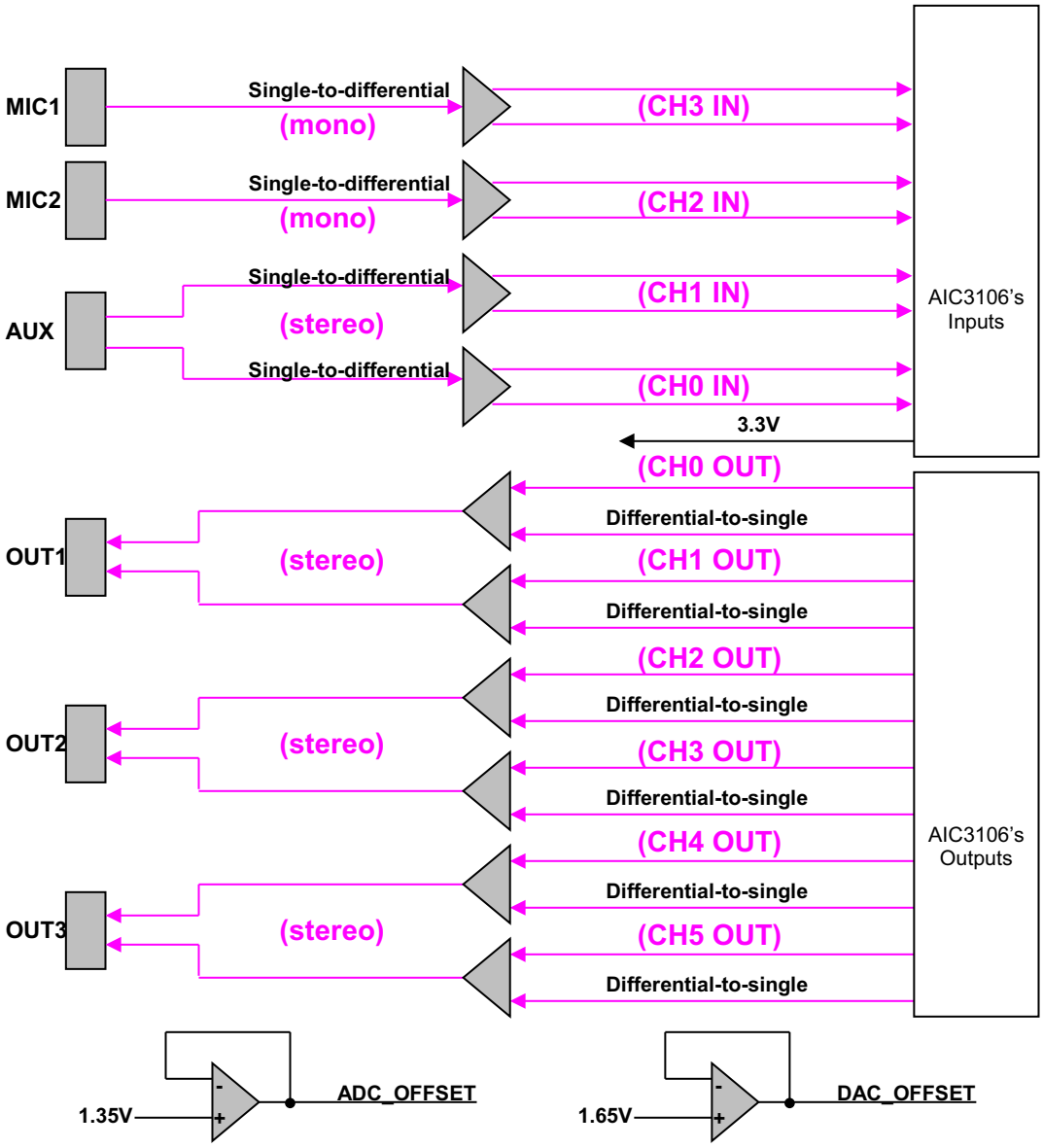


Figure 8. Audio Analog Signal Block Diagram

3.4 Video Processing

The video processing section includes the LCD display panel and backup camera video input. The block diagram is shown in Figure 9.

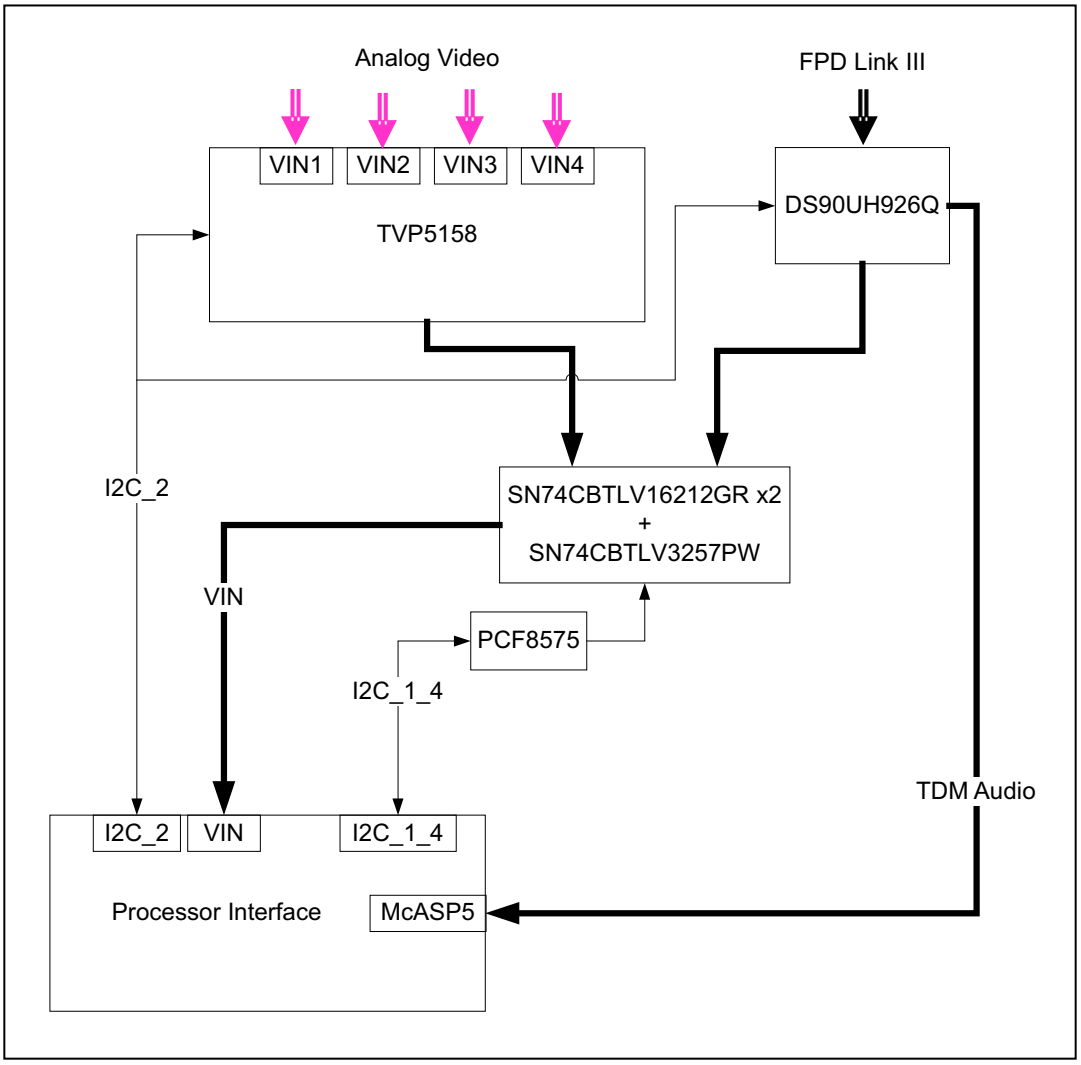


Figure 9. Video Processing Block Diagram

3.4.1 Camera Input

The system consists of four NTSC/PAL video inputs plus an FPD-Link III input. The analog camera input ports accept composite NTSC or PAL video signals through RCA connectors. The TVP5158, 4-channel high quality video decoder, converts the NTSC or PAL video signals to 8-bit ITU-R BT.656 digital format. The FPD-Link III deserializer outputs digital RGB signals. A mux system consisting of 2 – SN74CBTLV16212's [13] and an SN74CBTLV3257 [14] is utilized to route digital video data from either the TVP5158 or FPD-Link III outputs to the processor VDIN module.

The mux is controlled by the SEL_TVP_FPD output of an I2C expander (U14, page 6 of the JAMR3 Schematic). When changing the state of the video mux, care must be taken not to change the states of the LNA controls that also emanate from the same I2C expander.

The I2C#2 bus controls and configures the TVP5158 video decoder with the default I2C slave address 0x58. The DS90UH926Q deserializer is also on the I2C#2 bus with the same slave address. Only one set of inputs can be used at a time, either the TVP5158 or the FPD-Link III. Selection of the device is controlled by an I2C GPIO expander on I2C#1 or #4 bus. The controlling I2C bus is selectable with the same DIP switch that controls the tuner I2C bus, SW2. Whatever I2C bus is selected for the tuners is the same bus that controls the I2C expander that selects the state of the video mux. For SW2 switch details, see Section 3.2. Video characteristics including hue, contrast, brightness, saturation, and sharpness can be programmed via the I2C bus. FPD-Link III audio output is routed into the processor through McASP6.

3.5 Portable Media and iPod

A standard SD card socket is included on the JAMR3 board. SD cards (the socket may need to be placed on the PCB bottom side).

An iPod can be connected to JAMR3 via a daughter card that includes an iPod authentication chip. A header is provided for the daughter card. With iPod authentication, JAMR3 can navigate the iPod file system and control and play back the media files from the iPod player.

3.6 iPod Authentication and HD Radio Conditional Access

iPod authentication is required in order to connect an iPod device. A 10-pin Samtec (SFM-105-02-S-D-LC) connector is populated and routes necessary signals for a prospective authentication daughter card, the signals include the followings:

- I2C#3 bus
- SYS_RESET
- 3.3 V supply

HD radio conditional access allows the system to bring up HD radio function, a 10-pin Samtec (SFM-105-02-S-D-LC) connector routes the following signals for a prospective daughter card:

- I2C#3 bus
- System reset: SYS_RESET ORed with GP5[0]
- GP5[22] and GP5[30]
- 3.3 V supply

4 Debug Capability

The CDM connector is for HD Radio command and control using I2C#3 with an Aardvark; a 3M connector (part #: 30310-6002HB) should be used.

A Mini USB to I2C#3 converter interface utilizing an MSP430 [15] is built onto the board. This eliminates the need to always use an Aardvark. The radio system can be controlled through a USB gateway interface on the MSP430 to I2C#3.

Other debug interfaces will be on the processor board, like JTAG, RS232, Ethernet, and so forth.

5 Major Components and Connectors

- RF Signal Path
  - Dual Band DAB LNA's: U1, U2, U3, U4, Texas Instruments, AFE8316A1RGTR, QFN16
  - RF 2 bits Tuner Processors: U6, U7, U8, and U9, Texas Instruments, AFE8310DRVB, QFN56
- Audio Codec's: U24, U25 and U26, Texas Instruments, TLV320AIC3106-Q1
- Power Supply
  - Supervisor: U23, Texas Instruments, TPS3808
  - 1.1 V Supply: U16, Texas Instruments, TPS74701
  - 1.8 V Supply: U43, Texas Instruments, TPS74701
  - 3.8 V Supply: U28, Texas Instruments, TPS54362-Q1
  - 3.3 V Maxwell Supplies: U12 and U13, Texas Instruments, TPS75233-Q1

  - 3.3 V Supply: U42, Texas Instruments, TPS54362-Q1
- Video: U10, Texas Instruments, TVP5158
- FPD-Link III Deserializer: U5, Texas Instruments, DS90UH926Q
- USB to I2C Converter: U27, Texas Instruments, MSP430F5529IPN
- Connectors
  - Radio – Tuner Antenna Connectors
    - AM/FM J2, J5, J6, J9, Johnson Components, P/N: 142-0711-821
    - DAB3/DABL J3, J4, J7, J8, Johnson Components, P/N: 142-0711-821
    - Optional Tuner Clock Input: J1, Johnson Components, P/N: 142-0711-821
  - SD Card Slot: P4, Morethanall Co P/N: MHC-W21-601
  - Audio Out1, Audio Out2, Audio Out3: P9, P10, P11, Kycon, P/N: STX-3500-4NTR
  - Aux Jack: P6, Kycon, P/N: STX-3500-4NTR
  - Mic Input1 and Mic Input2: P7, P8, Kycon, P/N: STX-3500-3
  - Debug Interfaces
    - CDM, 5 x 2 Header: J17, vertical, Samtec, P/N: TST-105-01-G-D
    - CDM USB “Mini B” receptacle: J14, Samtec, P/N: MUSB-05-S-B-SM-A-K-TR
  - CPU Board Interface: EXP_P1, EXP_P2 and EXP_P3, Samtec QSE/QTE High Speed Socket/Terminal 0.8 mm Pitch

6 Typical Characteristics

Table 9. Typical Characteristics

GENERAL	
Power Supply	10.5V to 19.5V
Grounding System	Negative Type
Typical current without power Amp module	TBD
Board Dimensions (W x H x D)	170mm x 35mm x 140mm
Weight	TBD
AUDIO	
THD+N (DAC)	-94dB
Signal-to-Noise Ratio (DAC)	112dB
Dynamic Range (DAC)	112dB
Sampling Rate (DAC)	44.1 KHz
DAC Converter	24-Bit
Power Amplifier (future version)	TBD
HD RADIO	
HD Radio	TBD
FM TUNER	
Tuning Range	87.5 MHz - 107.9 MHz
Usable Sensitivity	8.5 dBf
Signal-to-Noise Ratio	75dB
Frequency Response	30Hz to 15kHz
Stereo Separation	45dB at 1kHz
AM TUNER	
Tuning Range	530kHz-1710kHz
Usable Sensitvity	20dBuV
Signal-to-Noise Ratio	65 dB
Frequency Response	30Hz to 2.2kHz
DAB	
Tuning Range	TBD
Usable Sensitivity	TBD
Signal-to-Noise Ratio	TBD
Frequency Range	TBD
MEDIA	
USB flash drive	USB 2.0 High-Speed
SD card	SD 2.0, SDHC
Supported Media File Format	
MP3	MPEG-1 and 2 Audio Layer 3
WMA	Ver. 7, 7.1, 8,9,10 (2 channel audio)
AAC	MPEG-4 AAC
WAV	Linear PCM and MS ADPCM
iPod Connection	Via USB Port
BACKUP CAMERA INPUTS	
Camera Input Connection	NTSC or PAL Composite Video

7 Reference Documents

1. *DRA7x EVM CPU Board User's Guide* (SPRUI50)
2. *DS90UH926Q-Q1 720p 24-Bit Color FPD-Link III Deserializer With HDCP Data Sheet* (SNLS337)
3. Total Phase, Inc. Aardvark I2C/SPI Embedded Systems Interface Host Adaptor Data Sheet (http://www.totalphase.com/products/aardvark-i2cspi/)
4. *TVP5158, TVP5157, TVP5156 Four-Channel NTSC/PAL Video Decoders Data Manual* (SLES243)
5. *TLV320AIC3106-Q1 Low-Power Stereo Audio Codec for Portable Audio/Telephony Data Sheet* (SLAS663)
6. Processor Board Connectors Samtec QTE High Speed Socket/Terminal 0.8mm Pitch Specification Revision: F, Rev Date: 6/11/12 https://wwws.samtec.com/technical-specifications/Default.aspx?SeriesMaster=QTE
7. *TPS3808 Low-Quiescent-Current, Programmable-Delay Supervisory Circuit Data Sheet* (SBVS050)
8. *TPS54362-Q1 3-A, 60-V Step-Down DC-DC Converter With Low $I_{(q)}$ Data Sheet* (SLVS845)
9. *TPS752xxQ with $\overline{RESET}$ Output, TPS754xxQ with Power Good Output FAST-TRANSIENT-RESPONSE 2-A LOW-DROPOUT VOLTAGE REGULATORS Data Sheet* (SLVS242)
10. *TPS74701 500-mA Low-Dropout Linear Regulator With Programmable Soft-Start Data Sheet* (SBVS099)
11. Amplifier Power Connector Samtec .100 [2.54] SURFACE MOUNT ASSEMBLY SSW-1XX-22-XXX-X-XX-XX-X-XX, Revision AS http://www.samtec.com/documents/webfiles/cpdf/SSW-1XX-22-XXX-X-XX-XX-X-XX-MKT.pdf
12. Amplifier Signal Connector Samtec .050 x .050 SOCKET STRIP DOUBLE ROW ASSEMBLY SFM-1XX-XX-XXX-D-XXX, Revision CZ http://www.samtec.com/documents/webfiles/cpdf/SFM-1XX-XX-XXX-D-XXX-MKT.pdf
13. *SN74CBTLV16212 Low-Voltage 24-Bit FET Bus-Exchange Switch Data Sheet* (SCDS044)
14. *SN74CBTLV3257 Low-Voltage 4-Bit 1-of-2 FET Multiplexer/Demultiplexer Data Sheet* (SCDS040)
15. *MSP430F552x, MSP430F551x Mixed-Signal Microcontrollers Data Manual* (SLAS590)
16. *JAMR3 Tuner EVM Application Board PCB Rev B* (SPRR214)
17. *JAMR3 Tuner EVM Application Board Schematic Rev B* (SPRR215)
18. *JAMR3 Tuner EVM Application Board BOM Rev B* (SPRR216)
19. *JAMR3 Tuner EVM Application Board CPU Assembly Drawing Rev B* (SPRR217)
20. *JAMR3 Tuner EVM Application Board CPU PCB Drawing Rev B* (SPRR218)

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3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

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