User's Guide

Migration Between TMS320F28003x and TMS320F28P55x

ABSTRACT

This migration guide describes the hardware and software differences to be aware of when moving between F28003x and F28P55x C2000™ real-time MCUs. This document shows the block diagram between the two MCUs as a visual representation on what blocks are similar or different. It also highlights the features that are unique between the two devices for all available packages in a device comparison table. The F28003x and F28P55x devices have three packages in common; 100-pin, 80-pin and 64-pin so a PCB hardware section has been added to aid in migration between the three common packages. The digital general-purpose input/output (GPIO) and analog multiplex comparison tables show pin functionality between the two MCUs. This is a good reference for hardware design and signal routing when considering a move between the two devices. Lastly, like the F28003x device, the F28P55x software support is only in EABI format.

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1 Feature Differences Between F28003x and F28P55x

F28P55x is a superset of F28003x. They have three packages in common, 64-pin, 80-pin and 100-pin. It is possible to migrate between F28003x and F28P55x with the caveats in this document taken into account.

Note

This comparison guide focuses on the super-set devices: F280039C and F28P55xSJ9. Other part numbers in this product family have reduced feature support. For details specific to part numbers, see the device-specific data sheet.

1.1 F28003x and F28P55x Feature Comparison

An overlaid block diagram of F28003x and F28P55x is shown in F28003x and F28P55x Overlaid Functional Block Diagram while feature comparison of the superset part numbers for the F28003x and F28P55x devices is shown in Table 1-1.

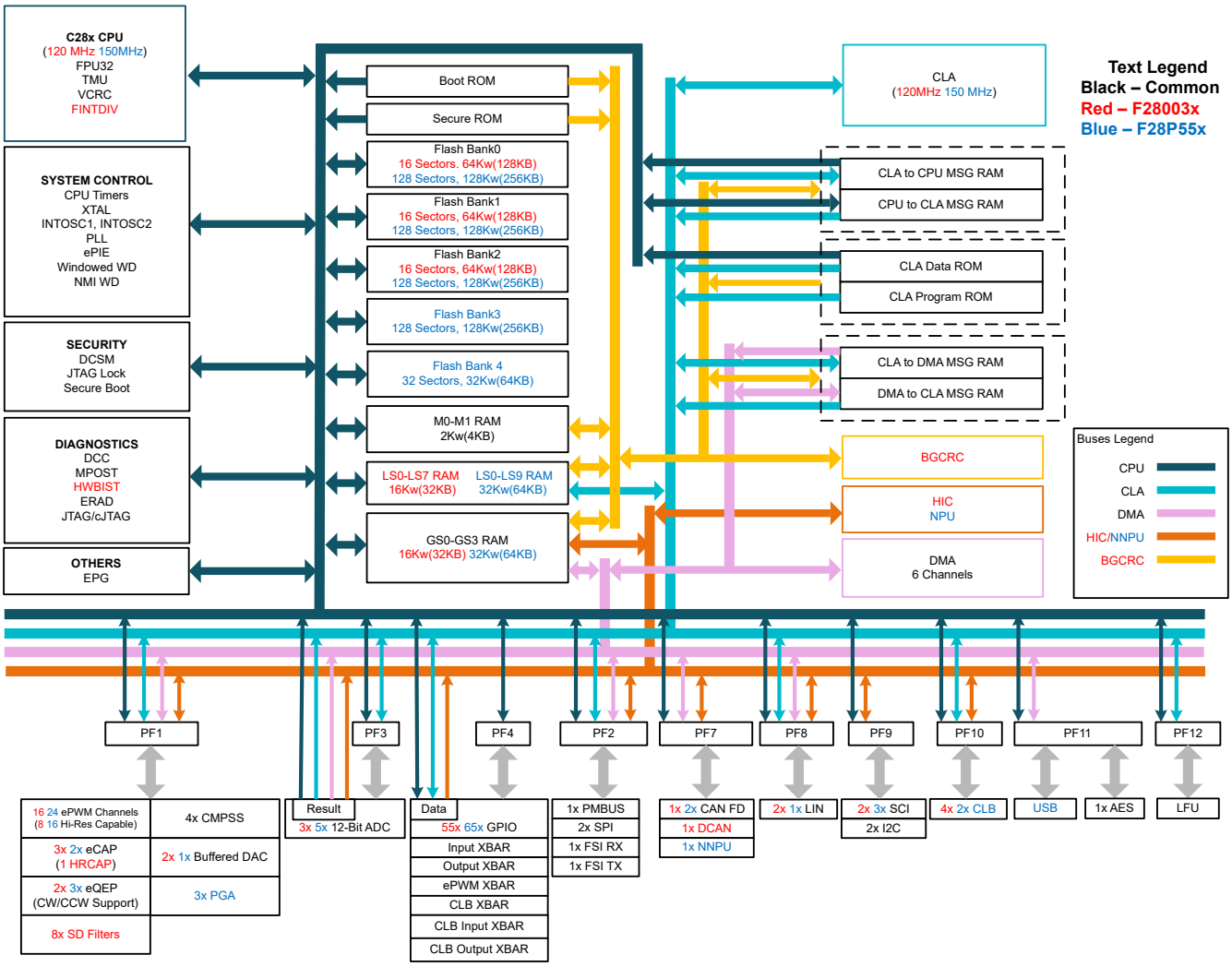

Figure 1-1. F28003x and F28P55x Overlaid Functional Block Diagram

Table 1-1. IP Differences

Feature		F28003x	F28P55x
CPU Frequency (MHz)		120	150
Fast Integer Division (FINTDIV)		Yes	No
Memory			
Flash		384KB	1088KB
RAM	Local Shared	32KB	64KB
	Global Shared	32KB	64KB
System			
Configurable Logic Block(CLB)		4 Tiles	2 Tiles
Motor Control Libraries in ROM		Yes	No
Background CRC(BGCRC)		Yes	No
HWBIST		Yes	No
Neural-Network Processing Unit (NNPU)		No	1 - Type 0
Analog Peripherals			
ADC 12-bit	Number of ADCs	3 - Type 5	5 - Type 6
	MSPS	4	4
	Conversion Time (ns)	250	255
CMPSS		4 - Type 2	4 - Type 6
Buffered DAC - Type 2		2	1
Programmable Gain Amplifier (PGA)		-	3 - Type 2
Output DAC from CMPSS DACL		0	1
Control Peripherals			
eCAP/HRCAP Modules		3(1 with HRCAP capability) - Type 2	2 - Type 2
ePWM/HRPWM channels - Type 4		16 (8 with HRPWM)	24 (16 with HRPWM)
eQEP - Type2		2	3
Communication Periperhals			
SDFM		8 - Type 2	-
CAN (DCAN) - Type 0		1	-
CANFD (MCAN) - Type 1		1	2
I2C		2 - Type 1	2 - Type 2
LIN - Type 1		2	1
HIC		1 - Type 1	-
PMBUS		1 - Type 1	1 - Type 2
SCI - Type 0		2	3
USB		-	1 - Type 0

Table 1-2. 100-pin IO and Analog Channel Counts

IO Type	F28003x	F28P55x
Digital		
AIO (analog with digital inputs)	23	16
AGPIO (analog with digital inputs and outputs)	2	19
Additional GPIO	4 (2 from cJTAG and 2 from X1/X2)	4 (2 from cJTAG and 2 from X1/X2)
Standard GPIO	49	43
Total GPIO	55	66
Total GPIO + AIO	78	82
Analog		
ADC Channels (single-ended)	23	35

Table 1-3. 80-pin IO and Analog Channel Counts

IO Type	F28003x	F28P55x
Digital		
AIO (analog with digital inputs)	16	12
AGPIO (analog with digital inputs and outputs)	2	16
Additional GPIO	4 (2 from cJTAG and 2 from X1/X2)	4 (2 from cJTAG and 2 from X1/X2)
Standard GPIO	37	32
Total GPIO	43	52
Total GPIO + AIO	59	64
Analog		
ADC Channels (single-ended)	18	28

Table 1-4. 64-pin IO and Analog Channel Counts

IO Type	F28003x	F28P55x
Digital		
AIO (analog with digital inputs)	16	12
AGPIO (analog with digital inputs and outputs)	2	13
Additional GPIO	4 (2 from cJTAG and 2 from X1/X2)	4 (2 from cJTAG and 2 from X1/X2)
Standard GPIO	24	17
Total GPIO	30	37
Total GPIO + AIO	46	49
Analog		
ADC Channels (single-ended)	16	28

2 PCB Hardware Changes

The F28003x and F28P55x devices have three packages in common: 100-pin PZ, 80-pin PN/PNA and 64-pin PM. The following sections describe the pin migration in detail.

Note

Overall compatibility depends on more than just the pins. Review all of the changes in this document during the migration process.

2.1 PCB Hardware Changes for the 100-Pin PZ, 80-Pin PNA and 64-Pin PM Packages

This section describes the F28003x and F28P55x differences that exist between the 100-Pin PZ, 80-Pin PNA and 64-Pin PZ packages.

100-Pin PZ: There are increased mux options on many analog pins on the F28P55x vs the F28003x. There is an additional 2 GPIOs on F28P55x that replace 2 power pins on the F28003x. Figure 2-1 outlines the differences.

80-Pin PN/PNA: There are increased mux options on many analog pins on the F28P55x vs the F28003x. There are an additional 2 GPIOs on F28P55x that replace 2 power pins on the F28003x. There is one less GPIO on the F28P55x due to the VREGENZ pin. Please note that the package pitch is changed with the F28003x having a 0.5mm pin pitch and the F28P55x having a 0.4mm pin pitch. Figure 2-2 outline the differences.

64-Pin PM: There are increased mux options on many analog pins on the F28P55x vs the F28003x. There is an additional 2 GPIOs on F28P55x that replace 2 power pins on the F28003x. There is one less GPIO on the F28P55x vs the F28003x Q100 variant due to the VREGENZ pin. Figure 2-3 outlines the differences.

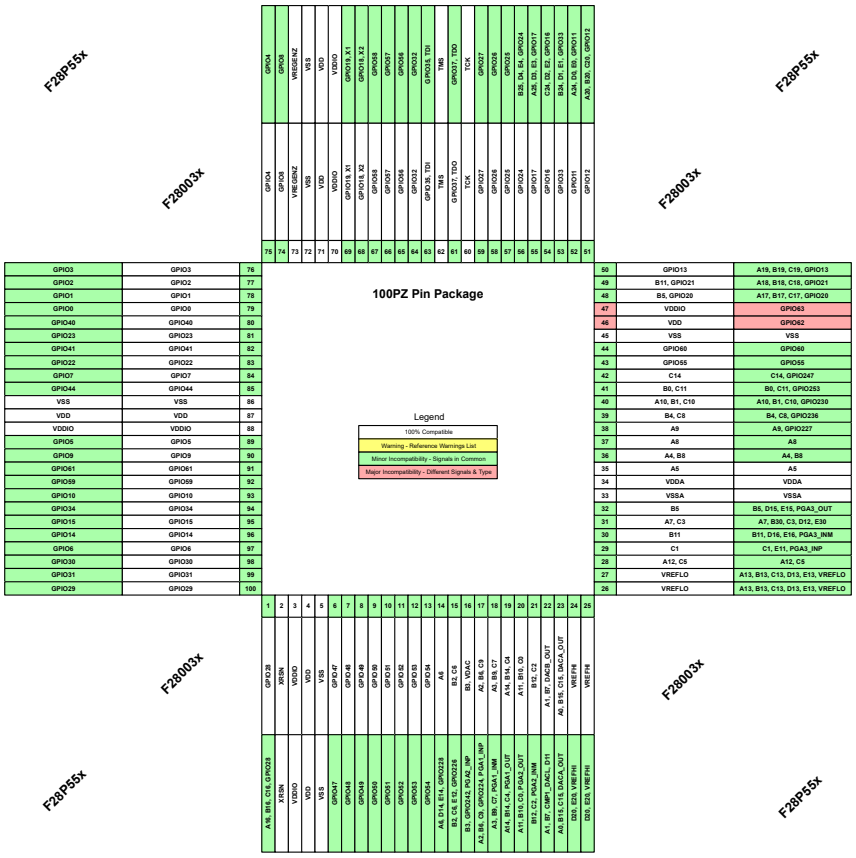

Figure 2-1. 100-Pin PT, F28003x and F28P55x Pin-Overlay

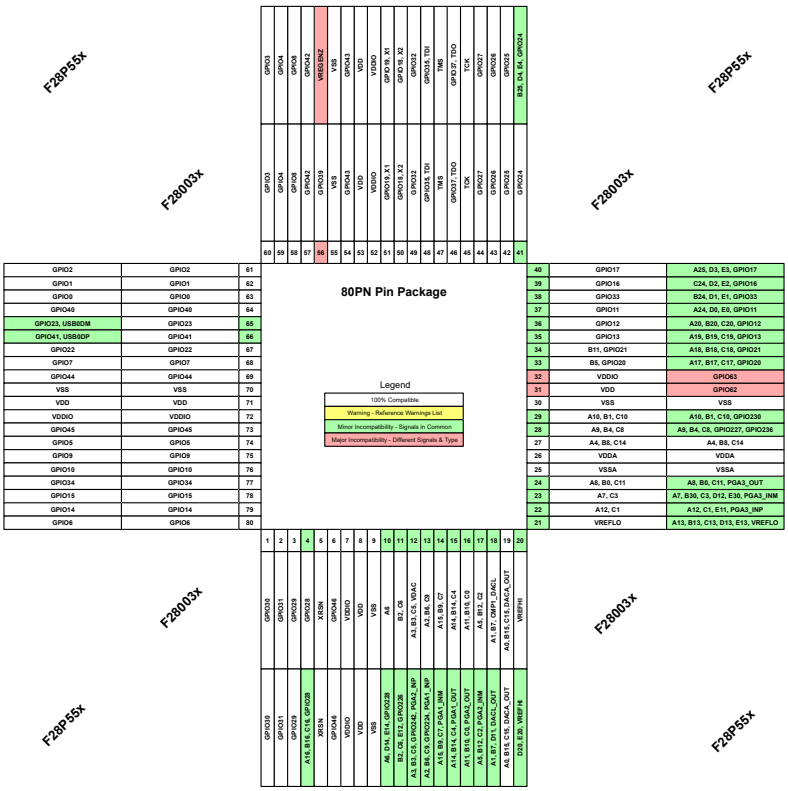

Figure 2-2. 80-Pin PN/PNA, F28003x and F28P55x Pin-Overlay

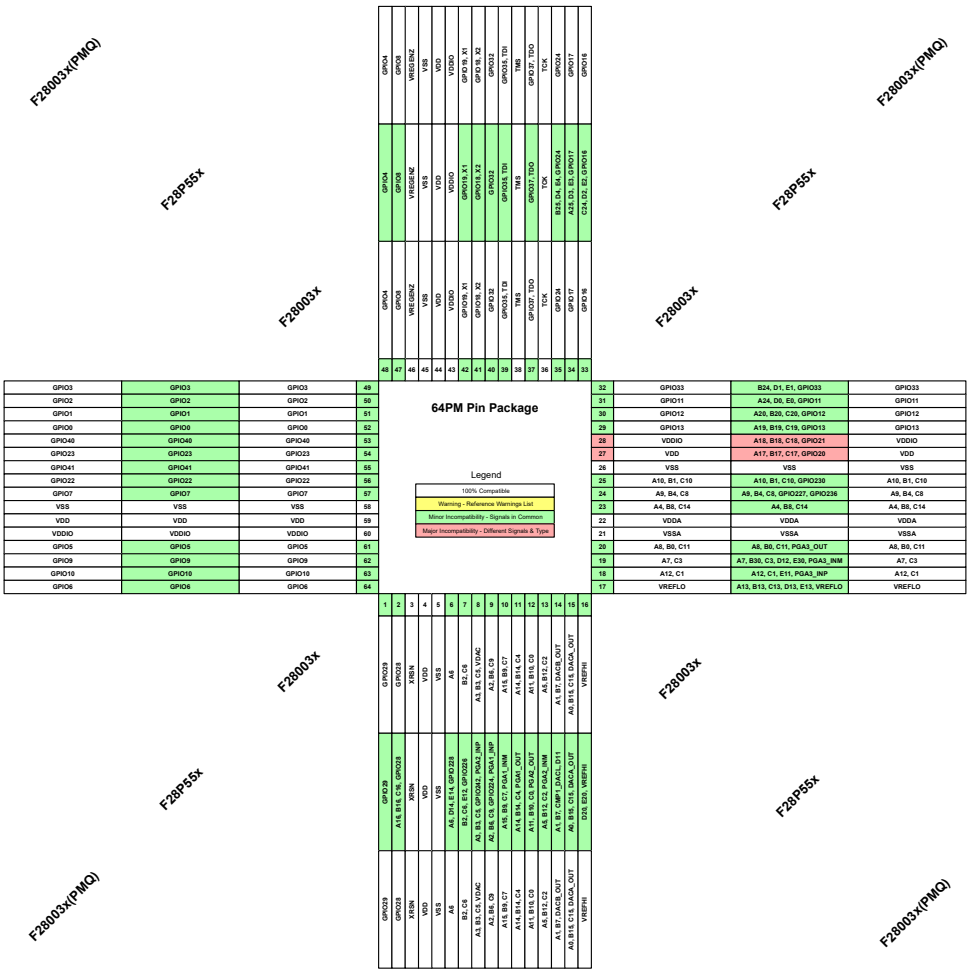

Figure 2-3. 64-Pin PM All Variants, F28003x and F28P55x Pin-Overlay

2.2 100-Pin PZ, 80-Pin PNA and 64-Pin PM Migration Between F28003x and F28P55x For New and Existing PCB

For the color legend, see Figure 2-2 through Figure 2-1.

Table 2-1. 100-Pin PZ, 80-Pin PNA and 64-Pin PM Migration Between F28003x and F28P55x For New and Existing PCB

Pin No			Pin Name			Action
100	80	64	F28003x	F28P55x	Transition Type	F28003x to F28P55x
Minor Incompatibility - Signals in Common (1)						
1	4	2	GPIO28	A16,B16,C16,GPIO28	GPIO to AGPIO	UseGPIO28
14	10	6	A6	A6,D14,E14,GPIO228	Analog Input to Analog Input with AGPIO	Use A6
15	11	7	B2,C6	B2,C6,E12,GPIO226		Use B2 or C6
16	-	-	B3,VDAC	B3,GPIO242,PGA2_INP		Use B3

Table 2-1. 100-Pin PZ, 80-Pin PNA and 64-Pin PM Migration Between F28003x and F28P55x For New and Existing PCB (continued)

Pin No			Pin Name			Action
100	80	64	F28003x	F28P55x	Transition Type	F28003x to F28P55x
-	12	8	A3,B3,C5,VDAC	A3,B3,C5,GPIO242,PGA2_INP	Analog Input to Analog Input with AGPIO	Use A3,B3 or C5
17	13	9	A2,B6,C9	A2,B6,C9,GPIO224,PGA1_INP		Use A2,B6 or C9
18	-	-	A3,B9,C7	A3,B9,C7,PGA1_INM		Use A3,B9 or C7
-	14	10	A15,B9,C7	A15,B9,C7,PGA1_INM		Use A15,B9 or C7
19	15	11	A14,B14,C4	A14,B14,C4,PGA1_OUT		Use A14,B14 or C4
2	13	12	A11,B10,C0	A11,B10,C0,PGA2_OUT		Use A11,B10 or C0
21	-	-	B12,C2	B12,C2,PGA2_INM		Use B12 or C2
-	17	13	A5,B12,C2	A5,B12,C2,PGA2_INM		Use A5,B12 or C2
22	18	14	A1,B7,DACB_OUT	A1,B7,D11,DACB_OUT		Use A1,B7 or DACB_OUT
24	20	16	VREFHIB,VREFHIC	D20,E20,VREFHI		Use VREFHI
25	-	-	VREFHIA	D20,E20,VREFHI		Use VREFHI
26	21	17	VREFLOB,VREFLOC	A13, B13, C13, D13, E13, VREFLO		Use VREFLO
27	-	-	VREFLOA	A13, B13, C13, D13, E13, VREFLO		Use VREFLO
29	-	-	C1	C1,E11,PGA3_INP		Use C1
-	22	18	A12,C1	A12,C1,E11,PGA3_INP		Use A12,C1
30	-	-	B11	B11,D16,E16,PGA3_INM		Use B11
-	23	19	A7,C3	A7,B30,C3,D12,E30,PGA3_INM		Use A7 or C3
31	-	-	A7,C3	A7,B30,C3,D12,E30		Use A7 or C3
-	24	20	A8,B0,C11	A8,B0,C11,PGA3_OUT		Use A8,B0 or C11
32	-	-	B5	B5,D15,E15,PGA3_OUT		Use B5
39		-	B4,C8	B4,C8,GPIO227,GPIO236		Use B4 or C8
38	-	-	A9	A9, GPIO227		Use A9
-	28	24	A9,B4,C8	A9,B3,C8,GPIO227,GPIO236		Use A9,B4 or C8
40	29	25	A10,B1,C10	A10,B1,C10,GPIO230		Use A10,B1 or C10
41	-	-	B0,C11	B0,C11,GPIO253		Use B0 or C11
42	-	-	C14	C14,GPIO247		Use C14
48		-	B5,GPIO20	A17,B17,C17,GPIO20		Use GPIO20
49	34	-	B11,GPIO21	A18,B18,C18,GPIO21		Use GPIO21

Table 2-1. 100-Pin PZ, 80-Pin PNA and 64-Pin PM Migration Between F28003x and F28P55x For New and Existing PCB (continued)

Pin No			Pin Name			Action
100	80	64	F28003x	F28P55x	Transition Type	F28003x to F28P55x
50	35	29	GPIO13	A19,B19,C19,GPIO13	GPIO to Analog with GPIO	Use GPIO13
51	36	30	GPIO12	A20,B20,C20,GPIO12		Use GPIO12
52	37	31	GPIO11	A24,D0,E0,GPIO11		Use GPIO11
53	38	32	GPIO33	B24,D1,E1,GPIO33		Use GPIO33
54	39	33	GPIO16	C24,D2,E2,GPIO16		Use GPIO16
55	40	34	GPIO17	A25,D3,E3,GPIO17		Use GPIO17
56	41	35	GPIO24	B25,D4,E4,GPIO24		Use GPIO24
81	65	54	GPIO23	GPIO23,USB0DM		Use GPIO23
82	66	55	GPIO41	GPIO41,USB0DP		Use GPIO41
Major Incompatibility - Different Signals and Types						
46	31	-	VDD	GPIO63	Power to GPIO	Tie to VDD, disable the digital input for the GPIO on the F28P55x by setting the appropriate bit in the GPIOINENACTRL register
47	32	-	VDDIO	GPIO62		Tie to VDDIO
-	-	27	VDD	A17,B17,C17,GPIO20		Tie to VDD, disale the digital input for the GPIO on the F28P55x by setting the appropriate bit in the GPIOINENACTRL register
-	-	28	VDDIO	A18,B18,C18,GPIO21		Tie to VDDIO
-	56	-	GPIO39	VREGENZ	GPIO to VREG Enable	External VREG not supported on F28003x. Tie to VSS through 0-Ohm resistor. Depopulate resistor when using F28003x and enable internal pull-up for the GPIO
(Q Variant) Major Incompatibility - Different Signals and Types						
-	-	46	GPIO39	VREGENZ	GPIO to VREG Enable	External VREG not supported on F28003xQ100. Tie to VSS through 0-Ohm resistor. Depopulate resistor when using F28003x and enable internal pull-up for the GPIO

(1) Channel to use selected in software.

2.3 GPIO Input Buffer Control Register

The F28P55x replaces a pair of VDDIO/VDD pins with GPIOs. When migrating from the F28003x it is necessary to disable the input buffer on the what was the VDD pin, so that the GPIO is not improperly driven(assuming the connection to VDD persists). The GPIOINENACTRL register disables the input buffer when cleared to 0. The default state at reset of this register is a 1, which enables the input buffer of the corresponding GPIO. The other GPIO can be safely connected to VDDIO, but if desired the input buffer can also be disabled on the corresponding GPIO if there are noise concerns in the system.

This address exists within the analog subsystem registers, which has a base address of 0x0005 D700. The GPIO input buffer control register (GPIOINENACTRL) has an offset of 0x132, within the analog subsystem base address.

Table 2-2. GPIOINENACTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
31-4	RESERVED	R	0h	Reserved
3	GPIO63	R/W	1h	One time configuration for GPIO63 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
2	GPIO62	R/W	1h	One time configuration for GPIO62 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
1	GPIO21	R/W	1h	One time configuration for GPIO21 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn
0	GPIO20	R/W	1h	One time configuration for GPIO20 to decide whether Input buffer (INENA control) is enabled or disabled 0 - Input buffer is disabled 1 - Input buffer is enabled Reset type: XRSn

3 Feature Differences for System Consideration

The differences and similarities that exist when moving between the F28003x and F28P55x devices is explored in this section.

3.1 New Features in F28P55x

This section outlines features that only exist in the F28P55x device. For details on each of these new features, see the *TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual* (SPRUJ53).

3.1.1 Programmable Gain Amplifier(PGA)

The F28P55x adds 3 Programmable Gain Amplifiers(PGA) inline with the ADC. Supporting unity gain and gains by a factor of 2 from 2 to 64, the PGA can be used to amplify small signal sources to take advantage of the full dynamic range of the on-chip ADC. Post gain filtering is also supported. While the PGA was also on the TMS320F28004x device, this is a new type, please consult the F28P55x documentation for the full feature set supported.

3.1.2 Universal Serial Bus (USB)

The USB controller operates as a full-speed function controller during point-to-point communications with the USB host. The controller complies with the USB 2.0 standard, which includes SUSPEND and RESUME signaling. The USB controller has thirty-two endpoints, one-half of them being for IN transactions and one-half of them being for OUT transactions. One IN and one OUT endpoint are fixed-function endpoints used for control transfers; the others are defined by firmware. A dynamically sizeable FIFO supports queuing multiple packets. Software-controlled connect and disconnect allow flexibility during USB device startup.

3.1.3 5V Failsafe IOs

The F28P55x device has four GPIOs: GPIO2, GPIO3, GPIO9, and GPIO32 that support 5V inputs. These pins also support applied voltage prior to power applied to the device.

3.1.4 Flash Write Protection

The F28P55x device has capability to permanently block the erase or program of 32 flash sectors in both flash banks 0 and 2. After writing specific values to the OTP memory, the corresponding sectors can no longer be erased or programmed. This capability allows the user to create immutable flash regions and along with the DCSM security module can be used to realize new secure code functions, including authentication algorithms. For more information, see the *Boot ROM* chapter of the TRM.

3.1.5 Neural-Network Processing Unit (NPU)

The Neural-network Processing Unit (NPU) supports intelligent inferencing running pre-trained models. Capable of 600–1200MOPS (Mega Operations Per Second), the NPU provides up to 10x Neural Network (NN) inferencing cycle improvement versus a software only based implementation. Using TI supplied tools, users can train and evaluate models as well as acquire and visualize the data stream from the MCU. The model is then compiled to a standalone library that is added to the main project to utilize the NPU in a system.

3.2 Communication Module Changes

Communication module changes between the F28003x and F28P55x devices affect the number of modules, removal of the DCAN and HIC modules. Details are available in Table 3-1.

Table 3-1. Communication Module Instances

Module	Category	F28003x	F28P55x	Notes
LIN	Number	2 - LINA, LINB	1- LINA	Type 1 LIN on both devices
CAN	Number	1- CANA	-	
MCAN	Number	1 - MCANA(CAN-FD)	2 - MCANA, MCANB(CAN-FD)	F28003x has 8KB Message RAM F28P55x has 4KB Message RAM
SCI	Number	2 - SCIA, SCIB	3 - SCIA, SCIB, SCIC	Type 0 SCI on both devices
SPI	Number	2 - SPIA, SPIB	2 - SPIA, SPIB	Type 2 SPI on both devices
	HW		High Speed Mode Support	GPIO2, 3, 9, 21, 32, and 41 do not support High Speed SPI mode.
I2C	Number	2 -I2CA, I2CB	2 - I2CA, I2CB	F28003x has Type 1 I2C F28P55x has Type 2 I2C
	Register			
PMBUS	Number	1 - PMBUSA	1 - PMBUSA	F28003x has Type 0 PMBUS F28P55x has Type 1 PMBUS
	HW Change		Supports Fast+ mode - 1MHz clock	
	Register	-	PMBUS_IO_DRVSEL	Configure increased drive strength to support Fast+ mode(1MHz)
		-	PMBUS_IO_MODESEL	Configure pin level, either 3.3V or 1.35V support
FSI	Number	1 - FSIA	1 - FSIA	Type 2 FSI on both devices
	Register	RX_MASTER_CTRL	RX_MAIN_CTRL	Register name change
		TX_MASTER_CTRL	TX_MAIN_CTRL	Register name change
HIC	Number	1 - HICA	-	

3.3 Control Module Changes

There are minimal changes in the control modules between the F28003x and F28P55x devices. There are significantly more ePWM modules on the F28P55x. The SDFM module and the HRCAP module are removed from the F28P55x device. Table 3-2 shows the module instances differences which should be considered when migrating applications between F28003x and F28P55x.

Table 3-2. Control Module Differences

Module	Category	F28003x	F28P55x	Notes
SDFM	Number	8 - SD1_D1C1..D4C4, SD2_D1C1..D4C4	-	
eQEP	Number	2 - EQEP1, EQEP2	3 - EQEP1, EQEP2, EQEP3	Type 2 eQEP on both devices
eCAP	Number	3 - ECAP1..3	2 - ECAP1, ECAP2	Type 2 eCAP on both devices
HRCAP	Number	1 - HRCAP3	-	
ePWM	Number	8 - EPWM1..8	12 - EPWM1..12	Type 4 PWM on both devices
HRPWM	Number	4 - HRPWM1..4	8 - HRPWM1..8	Type 4 HRPWM on both devices

3.4 Analog Module Differences

This section outlines the analog differences between F28003x and F28P55x. Three Programmable Gain Amplifiers(PGA) are a new addition to the F28P55x and there are now five ADCs vs the 3 ADCs on the F28003x device. There are several enhancements inside the CMPSS and ADC modules. There is only one GPDAC on the F28P55x devices vs two on the F28003x devices. There is capability to use the low side DAC from CMPSS1 module to act as the second DAC on the F28P55x, but there are electrical differences with the GPDAC. Please the device DS for more information.

Table 3-3. Analog Module Differences

Module	Category	F28003x	F28P55x	Notes
Analog Sysctrl	HW Changes	-	Global Sychronous SW Trigger for ADC	Allows for SW Trigger to ADC sent to selected ADCs simultaneously
		-	New register for VREFHI selection	Support for per ADC VREFHI selection reference voltage: 1. Internal VREFHI 2. External VREFHI 3. VDDA
		-	New register for VREFHI selection	Support for per ADC VREFLO selection reference voltage: 1. VREFLO pin 2. VSSA
		-	Support for full 3.3V FSR with External VREFHI	Can supply 1.65V on VREFHI in external mode to have FSR = 3.3V
		-	12mA Drive on Select GPIOs	For compatiblity with I2C and PMBUS High Speed + mode, GPIO 2/3/9/32 have option for 12mA drive strength
		-	1.35V VIH compatibility on select GPIOs	Changes VIH for GPIO 2/3/9/32 to 1.35V
	Register	ANAREFCTL.ANAREFSEL	ANAREFPCTRL.REFPMUXSELx	x = ADC A/B/C/D/E Each ADC is now configured independently for VREFHI source
		-	ANAREFNCTL.REFNMUXSELx	x = ADC A/B/C/D/E Each ADC has VREFLO selection capability
		ANAREFCTL.ANAREF2P5SEL	ANAREFPCTL.ANAREFx1P65SEL	x = ADC A/B/C/D/E Each ADC has independent 1.65V(3.3V FSR) or 2.5V FSR selection. Also effects external reference mode.
		-	IO_DRVSEL	Configure selected GPIO (IOL) drive strength for either 4mA(default) or 12mA (IOL)
		-	IO_MODESEL	Configure selected GPIO VIH to either 3.3V(default) or 1.35V

Table 3-3. Analog Module Differences (continued)

Module	Category	F28003x	F28P55x	Notes
ADC [1]	Number	3 - ADCA, ADCB, ADCC	5 - ADCA, ADCB, ADCC, ADCD, ADCE	F28003x has Type 5 ADC F28P55x has Type 6 ADC
	Max Speed	60 MHz	75MHz	Max throughput is 3.9MSPS on the F28P55x vs 4MSPS on the F28003x device
	HW Changes	-	New PPB features 1. Summing/Max/Min/Abs value 2. Oversampling Support w repeat block 3. Previous Conversion Delta 4. Output Filtering	1. Ability for PPB to Sum/Max/Min/Abs value of concurrent results 2. Automatically aggregates and averages user defined number of samples, returns only the average to a result register. Used with ADC Repeater Block 3. Compares last conversion to current conversion and generates corresponding action 4. Returns values that are in range of filter window only, discarding others.
		-	ADC Repeater Logic	Ability to initiate subsequent triggers automatically, with option to add phase delay. Can use with PPB to realize oversampling without CPU overhead
		-	Global SW Force SOC Trigger	Ability to initiate a SW SOC trigger to all ADCs simultaneously
		-	ADC S/H Cap Reset	Ability to reset the S/H Cap to VSSA between samples
	Register	ADCTL1	ADCTL1	Addition of External Mux Control and DMA Trigger Timings
		ADCSOCxCTL.TRIGSEL	ADCSOCxCTL.TRIGSEL	Increased Trigger Options for ePWM and repeat block support
		INTFLGCLR	ADCINTFLGCLR	
		ADCINTSOCSEL2	ADCINTSOCSEL1	All SOC interrupt triggers moved to INTSOCSEL1
GPDAC	Number	2 - GPDACA, GPDACB	1- GPDACA	Type 1 GPDAC on both devices

Table 3-3. Analog Module Differences (continued)

Module	Category	F28003x	F28P55x	Notes
CMPSS [1]	Number	4 - CMPSS1 to CMPSS4	4 - CMPSS1 to CMPSS4	F28003x has Type 2 CMPSS F28P55x has Type 6 CMPSS
	HW changes		1. Added DAC Ramp Generator to Low Side Comparator 2. Ramp Generator includes up ramp support 3. CMPSS1 can bring out its low side DAC to pin as CMP1_DACL [2]	
	Registers	RAMPMAXREFA	RAMPHREFA	Register Name Change
		RAMMAXREFS	RAMPHREFS	Register Name Change
		RAMPDECVALA	RAMPHSTEPVALA	Register Name Change
		RAMPDECVALS	RAMPHSTEPVALS	Register Name Change
		RAMPSTS	RAMPHSTS	Register Name Change
		RAMPDLYA	RAMPHDLYA	Register Name Change
		RAMPDLYS	RAMPHDLYS	Register Name Change
		CTRIPLFILCTL	CTRIPLFILCTL - Field Changes	Additions and changes to fields within this register. For more details, see the device-specific TRMs.
		CTRIPLFILCLKCTL	CTRIPLFILCLKCTL - Field Changes	Increased prescalar range
		CTRIPHFILCTL	CTRIPHFILCTL - Field Changes	Additions and changes to fields within this register. For more details, see the device-specific TRMs.
		CTRIPHFILCLKCTL	CTRIPHFILCLKCTL - Field Changes	Increased prescalar range
		-	COMPDACLCTL	Register and functionality added to support dual ramp generators
		-	RAMPLREFA	Register and functionality added to support dual ramp generators
		-	RAMPLREFS	Register and functionality added to support dual ramp generators
		-	RAMPLSTEPVALA	Register and functionality added to support dual ramp generators
		-	RAMPLSTEPVALS	Register and functionality added to support dual ramp generators
		-	RAMPLSTS	Register and functionality added to support dual ramp generators
		-	RAMPLDLYA	Register and functionality added to support dual ramp generators
		-	RAMPLDLYS	Register and functionality added to support dual ramp generators
		-	CTRIPLFILCLKCTL2	Register and functionality added to support dual ramp generators
		-	CTRIPHFILCLKCTL2	Register and functionality added to support dual ramp generators
Temp Sensor	Number	1 - (in ADCC ch 12)	1 - (in ADCC ch12)	

1. In porting software from F28003x to F28P55x (or the other way around), care must be taken to ensure that the correct ADC channels are used because of a difference in channel assignment, see Analog Multiplexing Changes.

2. Use of DACL from CMPSS1 and normal CMPSS1 fucntion are mutually exclusive.

3.5 Other Device Changes

This section describes feature differences between F28003x and F28P55x that were not covered in the previous sections, as such the changes identified below must be considered when migrating applications between devices.

3.5.1 PLL

The PLL blocks of F28003x and F28P55x devices are the same, however the maximum PLL Raw Clock for F28P55x is higher to accommodate the SYSCLK frequency requirement of F28P55x. Table 3-4 lists the PLL features for both devices for comparison. for more information, consult the TMS320F28P55x microcontrollers technical reference manual.

Table 3-4. PLL Features

Feature	F28003x	F28P55x
Max CPU Clock	120 MHz	150 MHz
VCO Range	220 - 600 MHz	220 - 600 MHz
PLL Raw Clock Range	6 - 240 MHz	6- 300 MHz
X1 Input Range (PLL enable)	2 - 25 MHz	2 - 25 MHz
REFCLK Divider	Yes [1..32]	Yes [1..32]
PLL Slip Detect	No (use DCC)	No (use DCC)
Fractional PLLMULT	No	No

3.5.2 PIE Channel Mapping

Pie channel mapping between F28003x and F28P55x is different due to peripheral module changes between these devices. Table 3-6 summarizes the common and unique pie channel assignments on these two devices.

Table 3-5. Pie Channel Legend

Color	Description
	Pie channel common for both devices
	Pie channel applicable only for F28003x
	Pie channel applicable only for F28P55x

Table 3-6. Pie Table Comparison

	INTx.1	INTx.2	INTx.3	INTx.4	INTx.5	INTx.6	INTx.7	INTx.8	INTx.9	INTx.10	INTx.11	INTx.12	INTx.13	INTx.14	INTx.15	INTx.16
INT1.y	INT_ADCA1	INT_ADCB1	INT_ADCC1	INT_XINT1	INT_XINT2	INT_SYS_ERR	INT_TIMER0	INT_WAKE	INT_ADCD1	INT_ADCE1 INT_SYS_ERR						
INT2.y	INT_EPWM1_TZ	INT_EPWM2_TZ	INT_EPWM3_TZ	INT_EPWM4_TZ	INT_EPWM5_TZ	INT_EPWM6_TZ	INT_EPWM7_TZ	INT_EPWM8_TZ	INT_EPWM9_TZ	INT_EPWM10_TZ	INT_EPWM11_TZ	INT_EPWM12_TZ				
INT3.y	INT_EPWM1	INT_EPWM2	INT_EPWM3	INT_EPWM4	INT_EPWM5	INT_EPWM6	INT_EPWM7	INT_EPWM8	INT_EPWM9	INT_EPWM10	INT_EPWM11	INT_EPWM12				
INT4.y	INT_ECAP1	INT_ECAP2	INT_ECAP3								INT_ECAP3_2					
INT5.y	INT_EQEP1	INT_EQEP2	INT_EQEP3		INT_CLB1	INT_CLB2	INT_CLB3	INT_CLB4	INT_SDFM1	INT_SDFM2			INT_SDFM1DR1	INT_SDFM1DR2	INT_SDFM1DR3	INT_SDFM1DR4
INT6.y	INT_SPIA_RX	INT_SPIA_TX	INT_SPIB_RX	INT_SPIB_TX			INT_DCC0	INT_DCC1					INT_SDFM2DR1	INT_SDFM2DR2	INT_SDFM2DR3	INT_SDFM2DR4
INT7.y	INT_DMA_CH1	INT_DMA_CH2	INT_DMA_CH3	INT_DMA_CH4	INT_DMA_CH5	INT_DMA_CH6	INT_PMBUSA				INT_FSITXA1	INT_FSITXA2	INT_FSIRXA1	INT_FSIRXA2		INT_DCC0
INT8.y	INT_I2CA	INT_I2CA_FIFO	INT_I2CB	INT_I2CB_FIFO	INT_SCIC_RX	INT_SCIC_TX			INT_LINA_0	INT_LINA_1	INT_LINB_0	INT_LINB_1	INT_PMBUSA			INT_DCC1
INT9.y	INT_SCIA_RX	INT_SCIA_TX	INT_SCIB_RX	INT_SCIB_TX	INT_CANA0	INT_CANA1	INT_MCANA_0	INT_MCANA_1	INT_MCANB_0 INT_MCANA_0	INT_MCANB_1 INT_MCANA_1	INT_MCANB_ECC INT_MCANA_ECC	INT_MCANB_WAKE INT_MCANA_WAKE	INT_BGCRC		INT_USB	INT_HICA
INT10.y	INT_ADCA_EVT	INT_ADCA2	INT_ADCA3	INT_ADCA4	INT_ADCB_EVT	INT_ADCB2	INT_ADCB3	INT_ADCB4	INT_ADCC_EVT	INT_ADCC2	INT_ADCC3	INT_ADCC4	INT_ADCD_EVT	INT_ADCD2	INT_ADCD3	INT_ADCD4
INT11.y	INT_CLA1_1	INT_CLA1_2	INT_CLA1_3	INT_CLA1_4	INT_CLA1_5	INT_CLA1_6	INT_CLA1_7	INT_CLA1_8	INT_ADCE_EVT	INT_ADCE2	INT_ADCE3	INT_ADCE4				
INT12.y	INT_XINT3	INT_XINT4	INT_XINT5	INT_MPOST	INT_FLSS INT_FMC	INT_VCU	INT_MCANA_ECC INT_FPU_OVERFLOW	INT_MCANA_WAKE INT_FPU_UNDERFLOW		INT_RAM_CORR_ERR	INT_FLASH_CORR_ERR	INT_RAM_ACC_VIOL	INT_AES INT_AES_SINTREQUEST	INT_BGCRC_CLA1	INT_CLA_OVERFLOW	INT_CLA_UNDERFLOW

3.5.3 Bootrom

For bootrom similarities and differences between F28003x and F28P55x see Table 3-8 and Table 3-9.

Table 3-7. Boot options Legend

Color	Description
	Options common for both devices but BOOTDEFx values may differ
	Options applicable only for F28003x
	Options applicable only for F28P55x

Table 3-8. Bootloaders and GPIO Assignment Comparison

Bootloader	Option	BOOTDEFx	F28003x	F28P55x
Parallel	0	0x00	D0-D7=GPIO0 to 7; DSP=16; Host=29	D0-D7=GPIO0 to 7; DSP=16; Host=29
	1	0x20	D0-D7=GPIO0 to 7; DSP=16; Host=11	D0-D7=GPIO0,1,2,3,5,6,7,24; DSP=12; Host=13
SCIA	0	0x01	TX=29; RX=28	TX=29; RX=28
	1	0x21	TX=16; RX=17	TX=1; RX=0
	2	0x41	TX=8; RX=9	TX=8; RX=9
	3	0x61	TX=2; RX=3	TX=7; RX=3
	4	0x81	TX=16; RX=3	TX=16; RX=3
CAN [1]	0	0x02	TX=4; RX=5	TX=4; RX=5
	1	0x22	TX=32; RX=33	TX=1; RX=0
	2	0x42	TX=2; RX=3	TX=13; RX=12
	3	0x62	TX=13; RX=12	-
MCAN(CAN-FD)	0	0x08	TX=4; RX=5	TX=4; RX=5
	1	0x28	TX=1; RX=0	TX=1; RX=0
	2	0x48	TX=13; RX=12	TX=13; RX=12
	3 (DEBUG - Send Test)	0x68	-	TX=4; RX=5
	4 (DEBUG - Send Test)	0x88	-	TX=1; RX=0
	5 (DEBUG - Send Test)	0xA8	-	TX=13; RX=12

Table 3-8. Bootloaders and GPIO Assignment Comparison (continued)

Bootloader	Option	BOOTDEFx	F28003x	F28P55x
SPI	0	0x06	SIMO=2 SOMI=1; CLK=3; STE=5	PICO=2 POCI=1; CLK=3; PTE=5
	1	0x26	SIMO=16 SOMI=1; CLK=3; STE=0	PICO=16 POCI=1; CLK=3; PTE=0
	2	0x46	SIMO=8 SOMI=10; CLK=9; STE=11	PICO=8 POCI=10; CLK=9; PTE=11
	3	0x66	SIMO=8 SOMI=17; CLK=9; STE=11	PICO=16 POCI=12; CLK=9; PTE=24
I2C	0	0x07	SDA=32; SCL=33	SDA=0; SCL=1
	1	0x27	SDA=0; SCL=1	SDA=32; SCL=33
	2	0x47	SDA=10; SCL=8	SDA=5; SCL=4
USB	0	0x09	-	DM=23; DP=41

1. For the F28P55x device "CAN" boot mode is supported by the MCAN module with FD mode set to "off"

Table 3-9. Boot Modes Comparison

Boot Mode	Option	BOOTDEFx	F28003x	F28P55x
Flash/Secure Flash	0	0x03	Entry=0x00080000' Bank/Sector=0/0	Entry=0x00080000; Bank/Sector=0/0
	1	0x23	Entry=0x00088000; Bank/Sector=0/8	Entry=0x00088000; Bank/Sector=0/32
	2	0x43	Entry=0x0008FFF0; Bank/Sector=0/15	Entry=0x000C0000; Bank/Sector=0/64
	3	0x63	Entry=0x00090000; Bank/Sector=1/0	Entry=0x000C8000; Bank/Sector=1/64
	4	0x83	Entry=0x00097FF0; Bank/Sector=1/7	Entry=0x00100000; Bank/Sector=2/16
	5	0xA3	Entry=0x0009FFF0; Bank/Sector=1/15	-
	6	0xC3	Entry=0x000A0000; Bank/Sector=2/0	-
	7	0xE3	Entry=0x000AFFF0; Bank/Sector=2/15	-

Table 3-9. Boot Modes Comparison (continued)

Boot Mode	Option	BOOTDEFx	F28003x	F28P55x
LFU Flash	0	0x0B	Entry=0x00080000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2	Entry=0x00080000; Bank=0 Entry=0x000C0000; Bank=2
	1	0x2B	Entry=0x00088000; Bank=0 Entry=0x00098000; Bank=1 Entry=0x000A8000 Bank=2	Entry=0x00088000; Bank=0 Entry=0x000C8000; Bank=2
	2	0x4B	Entry=0x0008FFF0; Bank=0 Entry=0x0009FFF0; Bank=1 Entry=0x000AFFF0 Bank=2	-
	3	0x6B	Entry=0x00088000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2	-
Secure LFU Flash	0	0x0C	Entry=0x00080000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2	-
	1	0x2C	Entry=0x00088000; Bank=0 Entry=0x00098000; Bank=1 Entry=0x000A8000 Bank=2	-
	2	0x4C	Entry=0x0008FFF0; Bank=0 Entry=0x0009FFF0; Bank=1 Entry=0x000AFFF0 Bank=2	-
	3	0x6C	Entry=0x00088000; Bank=0 Entry=0x00090000; Bank=1 Entry=0x000A0000 Bank=2	-
	4	0x8C	Entry=0x0008EFF0; Bank=0 Entry=0x00097FF0; Bank=1 Entry=0x000A7FF0 Bank=2	-
Wait	0	0x04	Watchdog enabled	Watchdog enabled
	1	0x24	Watchdog disabled	Watchdog disabled
RAM	0	0x05	Entry=0x00000000	Entry=0x00000000

3.5.4 SW Libraries Included in the ROM

F28P55x has the C2000 STL library embedded in the on chip ROM. F28003x does not include the STL library in its on chip ROM.

3.5.5 AGPIO

F28P55x has many more(up to 22)AGPIO channels that support both normal GPIO and AGPIO (analog) pin functionality vs the F28003x(2 total). See the F28P55x data manual for configuration details.

3.6 Power Management

The F28003x and F28P55x devices both support dual-rail (3.3 V and 1.2 V) or single-rail (3.3 V) with the internal LDO VREG providing the 1.2 V rail. This section describes the power management differences and similarities between the two devices.

3.6.1 LDO/VREG

Both F28003x and F28P55x supports internal and external VREG for the 1.2V supply selectable using the VREGENZ pin. However, not all packages of F28003x support the external VREG option. For F28P55x all packages have a VREGENZ pin.

3.6.2 POR/BOR

There are no functional changes for the POR and BOR.

3.6.3 Power Consumption

If similar IP sets and target frequency is identical between the F28003x and F28P55x then the power consumption should be approximately the same. See the datasheet for per peripheral and max currents for either device.

3.7 Memory Module Changes

RAM and FLASH memories in F28003x and F28P55x devices have some similarities and differences. Table 3-10 summarizes the memory features including error-checking and security assignment.

Table 3-10. RAM and FLASH memory changes

Memory		F28003x			F28P55x		
		Size	**Parity/ ECC**	**Secured**	**Size**	**Parity/ ECC**	**Secured**
RAM	Dedicated(M0, M1)	4KB	ECC	No	4KB	ECC	No
	Local Shared(LS0-LS7)	32KB	ECC	DCSM-controlled	32KB	Parity	DCSM-controlled
	Local Shared(LS8-LS9)	-	-	-	32KB	Parity	DCSM-controlled
	Global Shared(GS0-GS3)	32KB	ECC	No	64KB	Parity	No
	Message	512B(CPU-CLA) 512B(CLA-DMA)	ECC	No	512B(CPU-CLA) 512B(CLA-DMA)	Parity	No
	Total RAM	**69KB**			**133KB**		
FLASH	Per Sector	8KB	-	-	2KB	-	-
	Per Bank	128KB(3 banks)	ECC	DCSM-controlled	256KB(4 banks) 64KB(1 bank)	ECC	DCSM-controlled
	Total FLASH	**384KB(3 banks)**			**1088KB(5 banks)**		

3.8 GPIO Multiplexing Changes

Table 3-11 outlines the differences and similarities that exist in the GPIO mux between F28003x and F28P55x.

Table 3-11. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F28003x
	mux function applicable only for F28P55x

Table 3-12. GPIO Muxed Pins

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO0	EPWM1_A		OUTPUTXBAR7	SCIA_RX	I2CA_SDA	SPIA_PTE SPIA_STE	FSIRXA_CLK	MCANA_RX MCAN_RX	CLB_OUTPUTXBAR8	EQEP1_INDEX	HIC_D7	EPWM3_A HIC_BASESEL1
GPIO1	EPWM1_B	EMU0		SCIA_TX	I2CA_SCL	SPIA_POCI SPIA_SOMI	EQEP1_STROBE	MCANA_TX MCAN_TX	CLB_OUTPUTXBAR7	EPWM10_B HIC_A2	FSITXA_TDM_D1	EPWM3_B HIC_D10
GPIO2	EPWM2_A	EMU1		OUTPUTXBAR1	PMBUSA_SDA	SPIA_PICO SPIA_SIMO	SCIA_TX	FSIRXA_D1	I2CB_SDA	EPWM10_A HIC_A1	MCANB_TX CANA_TX	EPWM4_A HIC_D9
GPIO3	EPWM2_B	OUTPUTXBAR2		OUTPUTXBAR2	PMBUSA_SCL	SPIA_CLK	SCIA_RX	FSIRXA_D0	I2CB_SCL	HIC_NOE	MCANB_RX CANA_RX	EPWM4_B HIC_D4
GPIO4	EPWM3_A	I2CA_SCL	MCANA_TX MCAN_TX	OUTPUTXBAR3	CANA_TX	SPIB_CLK	EQEP2_STROBE	FSIRXA_CLK	CLB_OUTPUTXBAR6	EPWM11_B HIC_BASESEL2	SPIA_POCI	EPWM1_A HIC_NWE
GPIO5	EPWM3_B	I2CA_SDA	OUTPUTXBAR3	MCANA_RX MCAN_RX	CANA_RX	SPIA_PTE SPIA_STE	FSITXA_D1	CLB_OUTPUTXBAR5	SCIA_RX	HIC_A7	HIC_D4	EPWM1_B HIC_D15
GPIO6	EPWM4_A	OUTPUTXBAR4	SYNCOUT	EQEP1_A		SPIB_POCI SPIB_SOMI	FSITXA_D0		FSITXA_D1	USB0_IVBUSVALID HIC_NBE1	CLB_OUTPUTXBAR8	EPWM2_A HIC_D14
GPIO7	EPWM4_B	EPWM2_A	OUTPUTXBAR5	EQEP1_B		SPIB_PICO SPIB_SIMO	FSITXA_CLK	CLB_OUTPUTXBAR2	SCIA_TX	HIC_A6	MCANA_TX	EPWM2_B HIC_D14
GPIO8	EPWM5_A		ADCSOCAO	EQEP1_STROBE	SCIA_TX	SPIA_PICO SPIA_SIMO	I2CA_SCL	FSITXA_D1	CLB_OUTPUTXBAR5	EPWM11_A HIC_A0	FSITXA_TDM_CLK	HIC_D8

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO9	EPWM5_B	SCIB_TX	OUTPUTXBAR6	EQEP1_INDEX	SCIA_RX	SPIA_CLK	I2CA_SCL	FSITXA_D0	LINA_RX LINB_RX	PMBUSA_SCL HIC_BASESEL0	I2CB_SCL	EQEP3_B HIC_NRDY
GPIO10	EPWM6_A		ADCSOCBO	EQEP1_A	SCIB_TX	SPIA_POCI SPIA_SOMI	I2CA_SDA	FSITXA_CLK	LINA_TX LINB_TX	EQEP3_STROBE HIC_NWE	FSITXA_TDM_D0	CLB_OUTPUTXBAR4
GPIO11	EPWM6_B	MCANA_RX	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_PTE SPIA_STE	FSIRXA_D1	LINA_RX LINB_RX	EQEP2_A	SPIA_PICO SPIA_SIMO	HIC_D6	EQEP3_INDEX HIC_NBE0
GPIO12	EPWM7_A		MCANA_RX MCAN_RX	EQEP1_STROBE	SCIB_TX	PMBUSA_CTL	FSIRXA_D0	LINA_TX LINB_TX	SPIA_CLK	CANA_RX	HIC_D13	HIC_INT
GPIO13	EPWM7_B		MCANA_TX MCAN_TX	EQEP1_INDEX	SCIB_RX	PMBUSA_ALERT	FSIRXA_CLK	LINA_RX LINB_RX	SPIA_POCI SPIA_SOMI	CANA_TX	HIC_D11	HIC_D5
GPIO14	EPWM8_A	SCIB_TX		I2CB_SDA	OUTPUTXBAR3	PMBUSA_SDA	SPIB_CLK	EQEP2_A	LINA_TX LINB_TX	EPWM3_A	CLB_OUTPUTXBAR7	USB0_ODPDAT HIC_D15
GPIO15	EPWM8_B	SCIB_RX		I2CB_SCL	OUTPUTXBAR4	PMBUSA_SCL	SPIB_PTE SPIB_STE	EQEP2_B	LINA_RX LINB_RX	EPWM3_B	CLB_OUTPUTXBAR6	USB0_ODMSE0 HIC_D12
GPIO16	SPIA_PICO SPIA_SIMO		OUTPUTXBAR7	EPWM9_A EPWM5_A	SCIA_TX	SD1_D1	EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_B	SPIB_POCI SPIB_SOMI	EQEP3_STROBE HIC_D1
GPIO17	SPIA_POCI SPIA_SOMI		OUTPUTXBAR8	EPWM9_B EPWM5_B	SCIA_RX	SD1_C1	EQEP1_INDEX	PMBUSA_SDA	MCANA_TX CANA_TX		EPWM6_A	HIC_D2
GPIO18	SPIA_CLK	SCIB_TX	MCANB_RX CANA_RX	EPWM6_A	I2CA_SCL	SD1_D2	EQEP2_A	PMBUSA_CTL	XCLKOUT	LINA_TX LINB_TX	FSITXA_TDM_CLK	EQEP3_INDEX HIC_INT
GPIO19	SPIA_PTE SPIA_STE	SCIB_RX	MCANB_TX CANA_TX	EPWM6_B	I2CA_SDA	SD1_C2	EQEP2_B	PMBUSA_ALERT	CLB_OUTPUTXBAR1	LINA_RX LINB_RX	FSITXA_TDM_D0	HIC_NBE0
GPIO20	EQEP1_A			EPWM12_A	SPIB_PICO SPIB_SIMO	SD1_D3	MCANA_TX MCAN_TX	ADCE_EXTMUXSEL0	I2CA_SCL			SCIC_TX
GPIO21	EQEP1_B			EPWM12_B	SPIB_POCI SPIB_SOMI	SD1_C3	MCANA_RX MCAN_RX	ADCE_EXTMUXSEL1	I2CA_SDA			SCIC_RX
GPIO22	EQEP1_STROBE		SCIB_TX		SPIB_CLK	SD1_D4	LINA_TX	CLB_OUTPUTXBAR1	LINA_TX LINB_TX	HIC_A5	EPWM4_A	EQEP3_A HIC_D13

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO23	EQEP1_INDEX		SCIB_RX		SPIB_PTE SPIB_STE	SD1_C4	LINA_RX	CLB_OUTPUTXBAR3	LINA_RX LINB_RX	EPWM12_A HIC_A3	EPWM4_B	HIC_D11
GPIO24	OUTPUTXBAR1	EQEP2_A	SPIA_PTE	EPWM8_A	SPIB_PICO SPIB_SIMO	SD2_D1	LINA_TX LINB_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS	EPWM9_A	HIC_D3
GPIO25	OUTPUTXBAR2	EQEP2_B		EQEP1_A	SPIB_POCI SPIB_SOMI	SD2_C1	FSITXA_D1	PMBUSA_SDA	SCIA_RX	EQEP3_A	HIC_BASESEL0	
GPIO26	OUTPUTXBAR3	EQEP2_INDEX		OUTPUTXBAR3	SPIB_CLK	SD2_D2	FSITXA_D0	PMBUSA_CTL	I2CA_SDA	EQEP3_B	HIC_D0	HIC_A1
GPIO27	OUTPUTXBAR4	EQEP2_STROBE		OUTPUTXBAR4	SPIB_PTE SPIB_STE	SD2_C2	FSITXA_CLK	PMBUSA_ALERT	I2CA_SCL	EQEP3_STROBE	HIC_D1	HIC_A4
GPIO28	SCIA_RX		EPWM7_A	OUTPUTXBAR5	EQEP1_A	SD2_D3	EQEP2_STROBE	LINA_TX	SPIB_CLK	ERRORSTS	I2CB_SDA	HIC_NOE
GPIO29	SCIA_TX		EPWM7_B	OUTPUTXBAR6	EQEP1_B	SD2_C3	EQEP2_INDEX	LINA_RX	SPIB_PTE SPIB_STE	ERRORSTS	I2CB_SCL	HIC_NCS
GPIO30	CANA_RX		SPIB_PICO SPIB_SIMO	OUTPUTXBAR7	EQEP1_STROBE	SD2_D4	FSIRXA_CLK	MCANA_RX MCAN_RX	EPWM1_A	EQEP3_INDEX	HIC_D8	
GPIO31	CANA_TX		SPIB_POCI SPIB_SOMI	OUTPUTXBAR8	EQEP1_INDEX	SD2_C4	FSIRXA_D1	MCANA_TX MCAN_TX	EPWM1_B		HIC_D10	
GPIO32	I2CA_SDA	EQEP1_INDEX	SPIB_CLK	EPWM8_B	LINA_TX	SD1_D2	FSIRXA_D0	MCANB_TX CANA_TX	PMBUSA_SDA	ADCSOCBO		HIC_INT
GPIO33	I2CA_SCL		SPIB_PTE SPIB_STE	OUTPUTXBAR4	LINA_RX	SD1_C2	FSIRXA_CLK	MCANB_RX CANA_RX	EQEP2_B	ADCSOCAO	SD1_C1	SCIC_RX HIC_D0
GPIO34	OUTPUTXBAR1				PMBUSA_SDA					HIC_NBE1	I2CB_SDA	HIC_D9
GPIO35	SCIA_RX	SPIA_POCI	I2CA_SDA	MCANB_RX CANA_RX	PMBUSA_SCL	LINA_RX	EQEP1_A	PMBUSA_CTL	EPWM5_B	SD2_C1	HIC_NWE	TDI
GPIO37	OUTPUTXBAR2	SPIA_PTE	I2CA_SCL	SCIA_TX	MCANB_TX CANA_TX	LINA_TX	EQEP1_B	PMBUSA_ALERT	EPWM5_A		HIC_NRDY	TDO
GPIO39					MCAN_RX	FSIRXA_CLK	EQEP2_INDEX		CLB_OUTPUTXBAR2	SYNCOUT	EQEP1_INDEX	HIC_D7
GPIO40	SPIB_PICO SPIB_SIMO		EMU0	EPWM2_B	PMBUSA_SDA	FSIRXA_D0	SCIB_TX	EQEP1_A	LINA_TX LINB_TX		CLB_OUTPUTXBAR4 HIC_NBE1	EQEP3_STROBE HIC_D5
GPIO41	EPWM7_A		EMU1	EPWM2_A	PMBUSA_SCL	FSIRXA_D1	SCIB_RX	EQEP1_B	LINA_RX LINB_RX	EPWM12_B HIC_A4	SPIB_POCI SPIB_SOMI	HIC_D12

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO42		LINA_RX	OUTPUTXBAR5	PMBUSA_CTL	I2CA_SDA	SCIC_RX		EQEP1_STROBE	CLB_OUTPUTXBAR3		HIC_D2	HIC_A6
GPIO43			OUTPUTXBAR6	PMBUSA_ALERT	I2CA_SCL	SCIC_TX	PMBUSA_ALERT	EQEP1_INDEX	CLB_OUTPUTXBAR4	SD2_D3	HIC_D3	HIC_A7
GPIO44			OUTPUTXBAR7	EQEP1_A	PMBUSA_SDA	FSITXA_CLK	PMBUSA_CTL	CLB_OUTPUTXBAR3	FSIRXA_D0	HIC_D7	LINA_TX LINB_TX	HIC_D5
GPIO45			OUTPUTXBAR8			FSITXA_D0	PMBUSA_ALERT	CLB_OUTPUTXBAR4		SD2_C3		HIC_D6
GPIO46			LINA_TX	MCANA_TX MCAN_TX		FSITXA_D1	PMBUSA_SDA			SD2_C4		HIC_NWE
GPIO47			LINA_RX	MCANA_RX MCAN_RX		CLB_OUTPUTXBAR2	PMBUSA_SCL			SD2_D4	FSITXA_TDM_CLK	HIC_A6
GPIO48	OUTPUTXBAR3		CANA_TX	MCANA_TX	SCIA_TX	SD1_D1	PMBUSA_SDA					HIC_A7
GPIO49	OUTPUTXBAR4		CANA_RX	MCANA_RX	SCIA_RX	SD1_C1	LINA_RX			SD2_D1	FSITXA_D0	HIC_D2
GPIO50	EQEP1_A			MCANA_TX MCAN_TX	SPIB_PICO SPIB_SIMO	SD1_D2	I2CB_SDA			SD2_D2	FSITXA_D1	HIC_D3
GPIO51	EQEP1_B			MCANA_RX MCAN_RX	SPIB_POCI SPIB_SOMI	SD1_C2	I2CB_SCL			SD2_D3	FSITXA_CLK	HIC_D6
GPIO52	EQEP1_STROBE			CLB_OUTPUTXBAR5	SPIB_CLK	SD1_D3	SYNCOUT			SD2_D4	FSIRXA_D0	HIC_NWE
GPIO53	EQEP1_INDEX			CLB_OUTPUTXBAR6	SPIB_PTE SPIB_STE	SD1_C3	ADCSOCAO	MCANB_RX CANA_RX		SD1_C1	FSIRXA_D1	
GPIO54	SPIA_PICO SPIA_SIMO			EQEP2_A	OUTPUTXBAR2	SD1_D4	ADCSOCBO	LINA_TX LINB_TX		SD1_C2	FSIRXA_CLK	FSITXA_TDM_D1
GPIO55	SPIA_POCI SPIA_SOMI			EQEP2_B	OUTPUTXBAR3	SD1_C4	ERRORSTS	LINA_RX LINB_RX		SD1_C3		HIC_A0
GPIO56	SPIA_CLK	CLB_OUTPUTXBAR7	MCANA_TX MCAN_TX	EQEP2_STROBE	SCIB_TX	SD2_D1	SPIB_PICO SPIB_SIMO	I2CA_SDA	EQEP1_A	SD1_C4	FSIRXA_D1	HIC_D6
GPIO57	SPIA_PTE SPIA_STE	CLB_OUTPUTXBAR8	MCANA_RX MCAN_RX	EQEP2_INDEX	SCIB_RX	SD2_C1	SPIB_POCI SPIB_SOMI	I2CA_SCL	EQEP1_B		FSIRXA_CLK	HIC_D4
GPIO58				OUTPUTXBAR1	SPIB_CLK	SD2_D2	LINA_TX	MCANB_TX CANA_TX	EQEP1_STROBE	SD2_C2	FSIRXA_D0	HIC_NRDY
GPIO59				OUTPUTXBAR2	SPIB_PTE SPIB_STE	SD2_C2	LINA_RX	MCANB_RX CANA_RX	EQEP1_INDEX	SD2_C3	FSITXA_TDM_D1	

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO60	EPWM12_B		MCANA_TX MCAN_TX	OUTPUTXBAR3	SPIB_PICO SPIB_SIMO	SD2_D3				SD2_C4		HIC_A0
GPIO61			MCANA_RX MCAN_RX	OUTPUTXBAR4	SPIB_POCI SPIB_SOMI	SD2_C3					MCANB_RX CANA_RX	
GPIO62	EPWM10_A	OUTPUTXBAR3		MCANA_TX	SCIA_TX		PMBUSA_SDA					USB0_OIDPULLUP
GPIO63	EPWM10_B	OUTPUTXBAR4		MCANA_RX	SCIA_RX		LINA_RX					USB0_OSPEED
GPIO64	SCIA_RX	EPWM11_A	EPWM7_A	OUTPUTXBAR5	EQEP1_A		EQEP2_STROBE	LINA_TX	SPIB_CLK	ERRORSTS	I2CB_SDA	USB0_OSUSPEND
GPIO65	EQEP1_A	EPWM11_B			SPIB_PICO		MCANA_TX		I2CA_SCL		USB0_OFSD_1_N	
GPIO66	EQEP1_B	EPWM12_A			SPIB_POCI		MCANA_RX		I2CA_SDA		USB0_ODISCHRGVBUS	
GPIO67	EPWM7_B	EPWM12_B	MCANA_TX	EQEP1_INDEX	SCIB_RX	PMBUSA_ALERT	FSIRXA_CLK	LINA_RX	SPIA_POCI		USB0_OCHRGVBUS	SCIC_RX
GPIO68	EPWM7_A	EPWM3_A	MCANA_RX	EQEP1_STROBE	SCIB_TX	PMBUSA_CTL	FSIRXA_D0	LINA_TX	SPIA_CLK		USB0_ODMPULLDN	SCIC_TX
GPIO69	EPWM6_B	EPWM3_B	OUTPUTXBAR7	EQEP1_B	SCIB_RX	SPIA_PTE	FSIRXA_D1	LINA_RX	EQEP2_A	SPIA_PICO	USB0_ODPPULLDN	EQEP3_INDEX
GPIO70	I2CA_SCL		SPIB_PTE	OUTPUTXBAR4	LINA_RX		FSIRXA_CLK	MCANA_RX	EQEP2_B	ADCSOCAO	USB0_OLSD_2_N	EQEP3_A
GPIO71	SPIA_PICO	EPWM4_B	OUTPUTXBAR7	EPWM9_A	SCIA_TX		EQEP1_STROBE	PMBUSA_SCL	XCLKOUT	EQEP2_INDEX	SPIB_POCI	EQEP3_STROBE
GPIO72	SPIA_POCI	EPWM5_A	OUTPUTXBAR8	EPWM9_B	SCIA_RX		EQEP1_INDEX	PMBUSA_SDA	MCANA_TX	USB0_OLSD_1_N	EPWM6_A	EQEP3_B
GPIO73	OUTPUTXBAR1	EPWM5_B	SPIA_PTE	EPWM8_A	SPIB_PICO		LINA_TX	PMBUSA_SCL	SCIA_TX	ERRORSTS	EPWM9_A	USB0_OOE
GPIO74	EPWM2_B		ADCSOCAO	MCANA_TX	SPIA_POCI				EQEP1_B	USB0_IID		
GPIO75	EPWM1_B		LINA_RX	EPWM6_A	SPIA_CLK				EQEP1_STROBE	USB0_ISESSEND	SCIC_RX	
GPIO76	EPWM4_A			OUTPUTXBAR2	SPIA_PTE			MCANA_RX	EQEP1_INDEX	USB0_IAVALID		
GPIO77	EPWM1_A			OUTPUTXBAR3	SPIA_PICO			MCANA_TX	EQEP1_A	USB0_IXRCV	SCIC_TX	
GPIO78		EPWM8_A	EPWM3_A	OUTPUTXBAR1	EPWM2_B		FSITXA_CLK			USB0_IDM		
GPIO79		EPWM8_B	EPWM3_B	MCANA_RX	EPWM2_A	I2CA_SDA	PMBUSA_SCL			USB0_IDP		

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
GPIO80	EPWM1_A		OUTPUTXBAR7	SCIA_RX	I2CB_SDA	SPIA_PTE	FSITXA_D0	MCANA_RX	CLB_OUTPUTXBAR8	EQEP1_INDEX	USB0_OFSD_2_N	EPWM3_A
GPIO81	EPWM1_B	OUTPUTXBAR6	SCIC_RX	SPIB_CLK	I2CB_SCL		FSITXA_D1	MCANA_TX	EQEP3_INDEX			
GPIO211	EPWM10_A			EQEP3_A								
GPIO212	EPWM10_B			EQEP3_B								
GPIO213	EPWM11_A			EQEP3_STROBE								
GPIO214	EPWM11_B			EQEP3_INDEX								
GPIO215	EPWM7_B			EQEP2_A								
GPIO224	EPWM11_B			OUTPUTXBAR3	SPIA_PICO		EPWM1_A	MCANA_TX	EQEP1_A	ADCE_EXTMUXSEL3	SCIC_TX	
GPIO226	EPWM10_B		LINA_RX	EPWM6_A	SPIA_CLK		EPWM1_B		EQEP1_STROBE	ADCE_EXTMUXSEL1	SCIC_RX	
GPIO227	I2CB_SCL		EPWM3_A	OUTPUTXBAR1	EPWM2_B							
GPIO228	EPWM10_A	EMU1	ADCSOCAO	MCANA_TX	SPIA_POCI		EPWM2_B		EQEP1_B	ADCE_EXTMUXSEL0		
GPIO230	I2CB_SDA		EPWM3_B	MCANA_RX	EPWM2_A	I2CA_SDA	PMBUSA_SCL					
GPIO236												
GPIO242	EPWM11_A			OUTPUTXBAR2	SPIA_PTE		EPWM4_A	MCANA_RX	EQEP1_INDEX	ADCE_EXTMUXSEL2		
GPIO247	EPWM12_B											
GPIO253	EPWM12_A											
AIO208												
AIO209												
AIO210												
AIO224		SD2_D3										HIC_A3
AIO225		SD2_C2										HIC_NWE
AIO226		SD2_D4										HIC_A1
AIO227		SD1_C3										HIC_NBE0
AIO228		SD2_C1										HIC_A0
AIO229												
AIO230		SD1_C4										HIC_BASESEL2

Table 3-12. GPIO Muxed Pins (continued)

0	1	2	3	5	6	7	9	10	11	13	14	15
AIO231		SD1_C1										HIC_BASESEL1
AIO232		SD1_D4										HIC_BASESEL0
AIO233		SD2_D1										HIC_A4
AIO234												
AIO235												
AIO236												
AIO237		SD1_D2										HIC_A6
AIO238		SD2_C3										HIC_NCS
AIO239		SD1_D1										HIC_A5
AIO240		SD2_C1										HIC_NBE1
AIO241		SD2_C1										HIC_NBE1
AIO242		SD2_D2										HIC_A2
AIO244		SD1_D3										HIC_A7
AIO245		SD1_C2										HIC_NOE
AIO247												
AIO248												
AIO249												
AIO251												
AIO252		SD2_C4										
AIO253												

3.9 Analog Multiplexing Changes

Table 3-14 outlines the differences and similarities that exist in the analog mux between F28003x and F28P55x for the 80-Pin PNA and 64-Pin PM packages. Table 3-15 outlines the differences and similarities that exist in the analog mux between F28003x and F28P55x for the 100 PZ package. The legend for the table is Table 3-13. The main change is the addition of ADCD, ADCE and the PGA. There are also many more AGPIOs on the F28P55x

Table 3-13. Mux Legend

Color	Description
	mux function common for both devices
	mux function applicable only for F28003x
	mux function applicable only for F28P55x

Table 3-14. F28003x and F28P55x 80-Pin PNA and 64-Pin PM Analog Mux Table Differences

(F28003x Pin Name)	Package Pin		ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	80 PNA	64 PM	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
VREFHI	20	16										
VREFLO	21	17	-	-	C13	-	-					
			A13	B13		D13	E13					
Analog Group 1								**CMP1**				
(A6)	10	6	A6	-	-	-	-	CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		AIO228
A6/D14/E14						D14	E14					AGPIO228
(A2/B6/C9)	13	9	A2	B6	C9	-	-	CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		AIO224
A2/B6/C9/ PGA1_INP												AGPIO224
(A15/B9/C7)	14	10	A15	B9	C7	-	-	CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
A15/B9/C7/ PGA1_INM												AGPIO223
(A11/B10/C0)	16	12	A11	B10	C0	-	-	CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
A11/B10/C0/ PGA2_OUT												
(A1/B7/ DACB_OUT)	18	14	A1	B7	-	-	-	CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
A1/B7/D11/ DACB_OUT						D11						
Analog Group 2								**CMP2**				
(A10/B1/C10)	29	25	A10	B1	C10	-	-	CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	AIO230
A10/B1/C10												GPIO230
Analog Group 3								**CMP3**				
(B2/C6)	11	7	-	B2	C6	-	-	CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		AIO226
B2/C6/E12							E12					GPIO226
(A3/B3/C5/VDAC)	12	8	A3	B3	C5	-	-	CMP3 (HPMXSEL=3) CMP3 (HPMXSEL=5)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3)CMP 3 (LPMXSEL=5)	CMP3 (LNMXSEL=0)	AIO242
A3/B3/C5/ PGA2_INP												GPIO242
(A14/B14/C4)	15	11	A14	B14	C4	-	-	CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
A14/B14/C4/ PGA1_OUT												
(A0/B15/C15/ DACA_OUT)	15	11	A0	B15	C15	-	-	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
Analog Group 4								**CMP4**				
(A7/C3)	23	19	A7	-	C3	-	-	CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	AIO245
A7/B30/C3/D12/E30				B30		D12	E30					
-	-	-	-	-	-	-	-	-		-		
A8/B0/C11/ PGA3_OUT	24	20	A8	B0	C11	-	-	CMP4(HPMXSEL=4)		CMP4(LPMXSEL=4)		AIO241
Analog Group 2/3								**CMP2/3**				

Table 3-14. F28003x and F28P55x 80-Pin PNA and 64-Pin PM Analog Mux Table Differences (continued)

(F28003x Pin Name)	Package Pin		ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	80 PNA	64 PM	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
(A5/B12/C2)	17	13	A5	B12	C2	-	-	CMP3 (HPMXSEL=1)CMP 2 (HPMXSEL=5)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1)CMP 2 (LPMXSEL=5)	CMP3 (LNMXSEL=1)	AIO244/ AIO249
A5/B12/C2/ PGA2_INM												
Combined Analog Group 2/4								CMP2/4				
(A12/C1)	22	18	A12	-	C1	-	-	CMP2 (HPMXSEL=1) CMP4 (HPMXSEL=2)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1) CMP4 (LPMXSEL=2)	CMP2 (LNMXSEL=1)	AIO238/ AIO248
A12/C1/E11/ PGA3_INP							E11					
(A8/B0/C11)	24	20	A8	B0	C11	-	-	CMP2 (HPMXSEL=4) CMP4 (HPMXSEL=4)		CMP2 (LPMXSEL=4) CMP4 (LPMXSEL=4)		AIO241
-	-	-	-	-	-			-		-		-
A4/B8/C14	27	23	A4	B8	C14	-	-	CMP2 (HPMXSEL=0) CMP4 (HPMXSEL=3)	CMP4 (HNMXSEL=0)	CMP2 (LPMXSEL=0) CMP4 (LPMXSEL=3)	CMP4 (LNMXSEL=0)	AIO225
(A9/B4/C8)	28	24	A9	B4	C8	-	-	CMP2 (HPMXSEL=2) CMP4 (HPMXSEL=0)		CMP2 (LPMXSEL=2) CMP4 (LPMXSEL=0)		AIO236/ AIO227
A9/B4/C8												AIO236/ AGPIO227
Other Analog												
B5	33	-	-	B5	-	-	-	CMP1 (HPMXSEL=5)		CMP1 (LPMXSEL=5)		AGPIO20
A17/B17/C17		27	A17	B17	C17	-	-	-		-		
B11	34	-	-	B11	-	-	-	CMP4 (HPMXSEL=5)		CMP4 (LPMXSEL=5)		AGPIO21
A18/B18/C18		28	A18	B18	C18	-	-	-		-		
-	35	29	-	-	-	-	-					GPIO13
A19/B19/C19			A19	B19	C19	-	-					AGPIO13
-	36	30	-	-	-	-	-					GPIO12
A20/B20/C20			A20	B20	C20	-	-					AGPIO12
-	37	31	-	-	-	-	-					GPIO11
A24/D0/E0			A24	-	-	D0	E0					AGPIO11
-	38	32	-	-	-	-	-					GPIO33
B24/D1/E1			-	B24	-	D1	E1					AGPIO33
-	39	33	-	-	-	-	-					GPIO16
C24/D2/E2			-	-	C24	D2	E2					AGPIO16
-	40	34	-	-	-	-	-					GPIO17
A25/D3/E3			A25	-	-	D3	E3					AGPIO17
-	41	35	-	-	-	-	-					GPIO24
B25/D4/E4			-	B25	-	D4	E4					AGPIO24
PGA1_OUT_INT(internal)								CMP1 (HPMXSEL=6)		CMP1 (LPMXSEL=6)		
PGA2_OUT_INT(internal)								CMP2 (HPMXSEL=6)		CMP2 (LPMXSEL=6)		
PGA3_OUT_INT(internal)								CMP3 (HPMXSEL=6)		CMP=3 (LPMXSEL=6)		
TempSensor(internal)	-	-	-	-	C12	-	-	CMP2 (HPMXSEL=7)				

Table 3-15. F28003x and F28P55x 100-Pin PZ Analog Mux Table Differences

(F28003x Pin Name)	Package Pin	ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	100 PZ	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
VREFHI	24/25										
VREFLO	26/27	-	-	C13	-	-					
		A13	B13		D13	E13					
Analog Group 1							**CMP1**				
(A6)	14	A6	-	-	-	-	CMP1 (HPMXSEL=2)		CMP1 (LPMXSEL=2)		AIO228
A6/D14/E14					D14	E14					AGPIO228
(A2/B6/C9)	17	A2	B6	C9	-	-	CMP1 (HPMXSEL=0)		CMP1 (LPMXSEL=0)		AIO224
A2/B6/C9/ PGA1_INP											AGPIO224
(B9/C7)	18	-	B9	C7	-	-	CMP1 (HPMXSEL=3)	CMP1 (HNMXSEL=0)	CMP1 (LPMXSEL=3)	CMP1 (LNMXSEL=0)	AIO233
A3/B9/C7/ PGA1_INM		A3									AGPIO223
(A11/B10/C0)	20	A11	B10	C0	-	-	CMP1 (HPMXSEL=1)	CMP1 (HNMXSEL=1)	CMP1 (LPMXSEL=1)	CMP1 (LNMXSEL=1)	AIO237
A11/B10/C0/ PGA2_OUT											
(A1/B7/ DACB_OUT)	22	A1	B7	-	-	-	CMP1 (HPMXSEL=4)		CMP1 (LPMXSEL=4)		AIO232
A1/B7/D11/ DACB_OUT					D11						
B5	32	-	B5	-	-	-	CMP1 (HPMXSEL=5)		CMP1 (LPMXSEL=5)		AIO252
B5/D15/E15/ PGA3_OUT	32				D15	E15					
Analog Group 2							**CMP2**				
A10/B1/C10	40	A10	B1	C10	-	-	CMP2 (HPMXSEL=3)	CMP2 (HNMXSEL=0)	CMP2 (LPMXSEL=3)	CMP2 (LNMXSEL=0)	AIO230
											GPIO230
(A12)	28	A12	-	-	-	-	CMP2 (HPMXSEL=1)	CMP2 (HNMXSEL=1)	CMP2 (LPMXSEL=1)	CMP2 (LNMXSEL=1)	AIO238
A12/C5				C5							
A4/B8	36	A4	B8	-	-	-	CMP2 (HPMXSEL=0)		CMP2 (LPMXSEL=0)		AIO225
A9	38	A9	-	-	-	-	CMP2 (HPMXSEL=2)		CMP2 (LPMXSEL=2)		AIO227
											AGPIO227
A5	35	A5	-	-	-	-	CMP2(HPMXSEL=5)		CMP2(LPMXSEL=5)		AIO249
Analog Group 3							**CMP3**				
(B2/C6)	15	-	B2	C6	-	-	CMP3 (HPMXSEL=0)		CMP3 (LPMXSEL=0)		AIO226
B2/C6/E12						E12					GPIO226
(B3/VDAC)	16	-	B3	-	-	-	CMP3 (HPMXSEL=3)	CMP3 (HNMXSEL=0)	CMP3 (LPMXSEL=3)	CMP3 (LNMXSEL=0)	AIO242
B3/PGA2_INP											GPIO242
(A14/B14/C4)	19	A14	B14	C4	-	-	CMP3 (HPMXSEL=4)		CMP3 (LPMXSEL=4)		AIO239
A14/B14/C4/ PGA1_OUT											

Table 3-15. F28003x and F28P55x 100-Pin PZ Analog Mux Table Differences (continued)

(F28003x Pin Name)	Package Pin	ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	100 PZ	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
(B12/C2) B12/C2/ PGA2_INM	21	-	B12	C2	-	-	CMP3 (HPMXSEL=1)	CMP3 (HNMXSEL=1)	CMP3 (LPMXSEL=1)	CMP3 (LNMXSEL=1)	AIO244
(A0/C15/ DACA_OUT) A0/B15/C15/ DACA_OUT	23	A0	- B15	C15	-	-	CMP3 (HPMXSEL=2)		CMP3 (LPMXSEL=2)		AIO231
(B9/C7) A3/B9/C7/ PGA1_INM	18	- A3	B9	C7	-	-	- CMP3 (HPMXSEL=5)		- CMP3 (LPMXSEL=5)		AIO233 AGPIO223
Analog Group 4							**CMP4**				
(A7/C3) A7/B30/C3/D12/E30	31	A7	- B30	C3	- D12	- E30	CMP4 (HPMXSEL=1)	CMP4 (HNMXSEL=1)	CMP4 (LPMXSEL=1)	CMP4 (LNMXSEL=1)	AIO245
(C1) C1/E11/ PGA3_INP	29	-	-	C1	-	E11	CMP4 (HPMXSEL=2)		CMP4 (LPMXSEL=2)		AIO241
B4/C8	39	- -	B4	C8	- -	- -	CMP4 (HPMXSEL=0)		CMP4 (LPMXSEL=0)		AIO236
B11 B11/D16/E16/ PGA3_INM	30	- -	B11	- -	- D16	- E16	CMP4 (HPMXSEL=5)		CMP4 (LPMXSEL=5)		AIO251
Other Analog											
B5 A17/B17/C17	48	- A17	B5 B17	- C17	- -	- -					AGPIO220
B11 A18/B18/C18	49	- A18	B11 B18	- C18	- -	- -					AGPIO221
- A19/B19/C19	50	- A19	- B19	- C19	- -	- -					GPIO13 AGPIO213
- A20/B20/C20	51	- A20	- B20	- C20	- -	- -					GPIO12 AGPIO212
- A24/D0/E0	52	- A24	- -	- -	- D0	- E0					GPIO11 AGPIO211
- B24/D1/E1	53	- -	- B24	- -	- D1	- E1					GPIO33 AGPIO233
- C24/D2/E2	54	- -	- -	- C24	- D2	- E2					GPIO16 AGPIO216
- A25/D3/E3	55	- A25	- -	- -	- D3	- E3					GPIO17 AGPIO217
- B25/D4/E4	56	- -	- B25	- -	- D4	- E4					GPIO24 AGPIO224

Table 3-15. F28003x and F28P55x 100-Pin PZ Analog Mux Table Differences (continued)

(F28003x Pin Name)	Package Pin	ADC					Comparator Subsystem (MUX)				AIO/ AGPIO Input
F28P55x Pin Name	100 PZ	A	B	C	D	E	High Positive	High Negative	Low Positive	Low Negative	
PGA1_OUT_INT(internal)							CMP1 (HPMXSEL=6)		CMP1 (LPMXSEL=6)		
PGA2_OUT_INT(internal)							CMP2 (HPMXSEL=6)		CMP2 (LPMXSEL=6)		
PGA3_OUT_INT(internal)							CMP3 (HPMXSEL=6)		CMP3 (LPMXSEL=6)		
TempSensor(internal)	-	-	-	C12	-	-	CMP2 (HPMXSEL=7)				

4 Application Code Migration From F28003x to F28P55x

The following section describes code changes when migrating from F28003x to F28P55x. Software examples for the new features in F28P55x are also discussed in this section.

4.1 C2000Ware Header Files

Header files for both F28003x and F28P55x devices are available in C2000Ware under the device_support sub directory.

4.2 Linker Command Files

Linker command files for both F28003x and F28P55x devices are available in C2000Ware under the device_support sub directory. Both F28003x and F28P55x, have to be compiled to the Embedded Application Binary Interface (EABI) format, section names would also need to conform to the EABI standard.

4.3 C2000Ware Examples

C2000Ware has examples specific for both F28003x and F28P55x devices.

5 Specific Use Cases Related to F28P55x New Features

This section outlines the new examples in C2000Ware for the F28P55x device to support new features.

5.1 PGA

C2000Ware has examples that demonstrate the capability of the new PGA on the F28P55x device.

5.2 USB

C2000Ware has examples that support the USB module that is on the F28P55x

6 EABI Support

Both F28003x and F28P55x devices use the Embedded Application Binary Interface (EABI) format for the binary executable output. All F28003x and F28P55x libraries supplied by TI will be released as EABI.

6.1 Flash API

F28003x has three Flash banks. F28P55x has up to five Flash banks. Both F28003x and F28P55x Flash API library is compiled for EABI format. Note that F28003x and F28P55x have different sector sizes. Also, the Flash wait-state configuration requirement is different between the two devices. These features are summarized in Table 6-1.

Table 6-1. Flash API Differences

Feature	F28003x	F28P55x
Library Name	FlashAPI_F28003x_FPU32.lib	FlashAPI_F28P55x_FPU32.lib
Library Executable Output	EABI	EABI
Erase, Blank-check, Program and Verify	Operation on three banks	Operation on five banks
Sector Size	4K x 16-bit word	1K x 16-bit word
Flash Wait States	5 (120MHz)	3 (150MHz)
Flash API Major Version	1	4
FlashAPI Minor Version	58	0

7 References

- Texas Instruments: *TMS320F28P55x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28003x Microcontrollers Technical Reference Manual*
- Texas Instruments: *TMS320F28P55x Microcontrollers Data Sheet*
- Texas Instruments: *TMS320F28003x Microcontrollers Data Sheet*

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (April 2024) to Revision A (September 2024) **Page**

- Updated Section 1.1 3
- Updated Section 2.1 6
- Added Section 3.1.4 11
- Added Section 3.1.5 12
- Updated Section 3.4 13

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