EVM User's Guide: SK-AM62-SIP

AM62x-SIP SK Evaluation Module

Description

The SK-AM62-SIP starter kit (SK) evaluation module (EVM) is a stand-alone test and development platform built around the AM6254 system-on-a-chip (SoC) with integrated 512MB LPDDR4 SDRAM in a single package. AM625SIP processors are comprised of a quad-core 64-bit Arm®-Cortex®-A53 microprocessor and single-core Arm Cortex-M4F MCU.

SK-AM62-SIP allows the user to experience a dual-display feature with 3D GPU through high-definition multimedia interface (HDMI™) over dots per inch (DPI) and low-voltage differential signaling (LVDS), as well as industrial communication applications using serial, Ethernet, USB and other interfaces.

Get Started

1. Order the EVM at SK-AM62-SIP.
2. Download the EVM design files.
3. Download the reference software for many applications from AM62x Development Portal.
4. Read this EVM user's guide thoroughly before operation.

Features

- USB-C powered standalone mode of operation
- Power optimized discrete DC-DC power management
- Onboard XDS110 JTAG interface with USB connectivity for code development and debugging
- Onboard 32 GB eMMC memory and 512 Mb OSPI NOR Flash
- 2x RGMII RJ45 connectors
- 2x USB 2.0 on type A and type C connectors
- Test automation interface through XDS110
- Expansion econnectors to access the interfaces
- M.2 connector for Wi-Fi/BT module

This design incorporates HDMI® technology.

Table of Contents

1 Evaluation Module Overview

1.1 Introduction

This technical User's Guide describes the hardware architecture of the SK-AM62-SIP EVM, a low cost Starter Kit built around the AM62x SIP SoC. The AM62x SIP processor comprises of a Quad-Core 64-bit Arm®-Cortex® A53 microprocessor, Single-core Arm Cortex-R5F MCU and an Arm Cortex-M4F MCU.

SK-AM62-SIP includes high-security field-securable (HS-FS) silicon to optionally customize keys and encryption for security applications.

SK-AM62-SIP can be used for display applications (for example, human machine interface (HMI) and control panel) with either an HDMI display and an external LVDS panel, up to 2K 60fps resolution. The powerful Arm performance of quad-A53 at 1.4GHz with rich industrial interfaces, offers good control and communication capabilities for a wide range of applications, such as programmable logic controllers (PLC), automation control, gateway, EV charging, medical, or building automation systems.

1.2 Kit Contents

- SK-AM62-SIP EVM
- EVM user guide pamphlet
- EVM disclaimer and standard terms

1.3 Device Information

In addition, SK-AM62-SIP can communicate with other processors or systems and act as a communication gateway. SK-AM62-SIP can directly operate as a standard remote I/O system or simple sensor connected to an industrial communication network.

The embedded emulation logic allows for emulation and debugging using standard development tools such as the Code Composer Studio™ integrated development environment (IDE) (CCSTUDIO). Reference software for many applications can be downloaded from AM62x Development Portal.

1.4 EVM Revisions and Assembly Variants

The various SK-AM62-SIP EVM PCB design revisions, and assembly variants are listed in Table 1-1. The specific PCB revision is indicated in silkscreen on the PCB and the specific assembly variant is indicated with an additional sticker label

Table 1-1. EVM PCB design revisions and assembly variants

OPN	PCB Revision	Assembly Variant	Revision and Assembly Variant Description
SK-AM62-SIP	PROC162E1	N/A	First prototype, early release revision of the AM62X SIP EVM. Implements the Sitara AM62X SIP MPU with a PMIC power solution.

1.5 Specification

The figure below shows the functional block diagram of the AM62x SIP SK EVM.

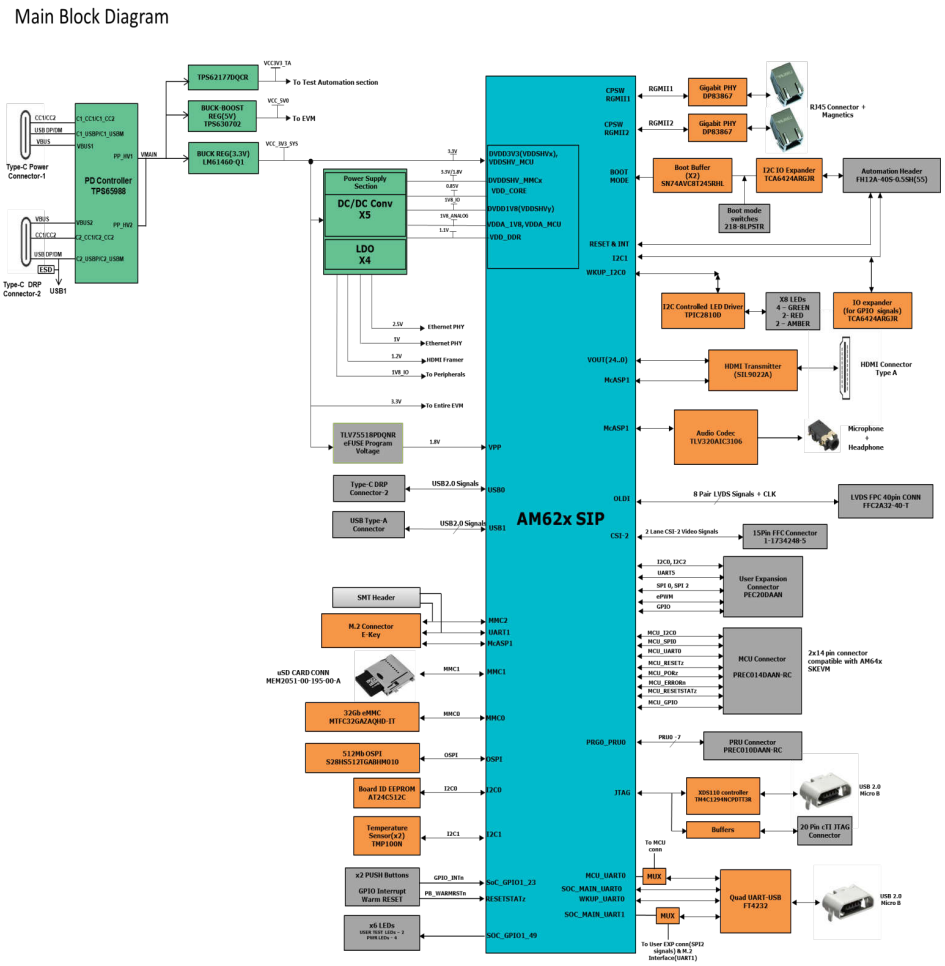

Figure 1-1. Functional Block Diagram of AM62x SIP SK EVM

2 Hardware

2.1 Additional Images

This section shows the EVM pictures and the location of various blocks on the board.

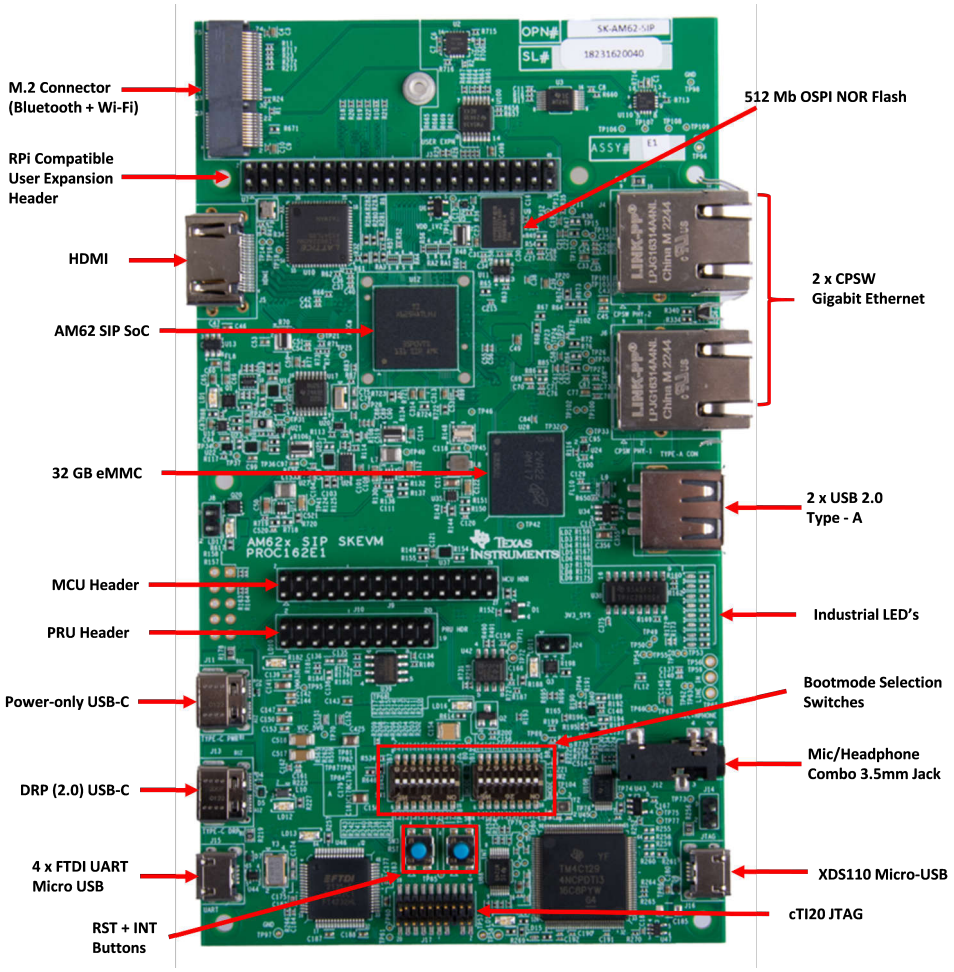

Figure 2-1. EVM Top Side

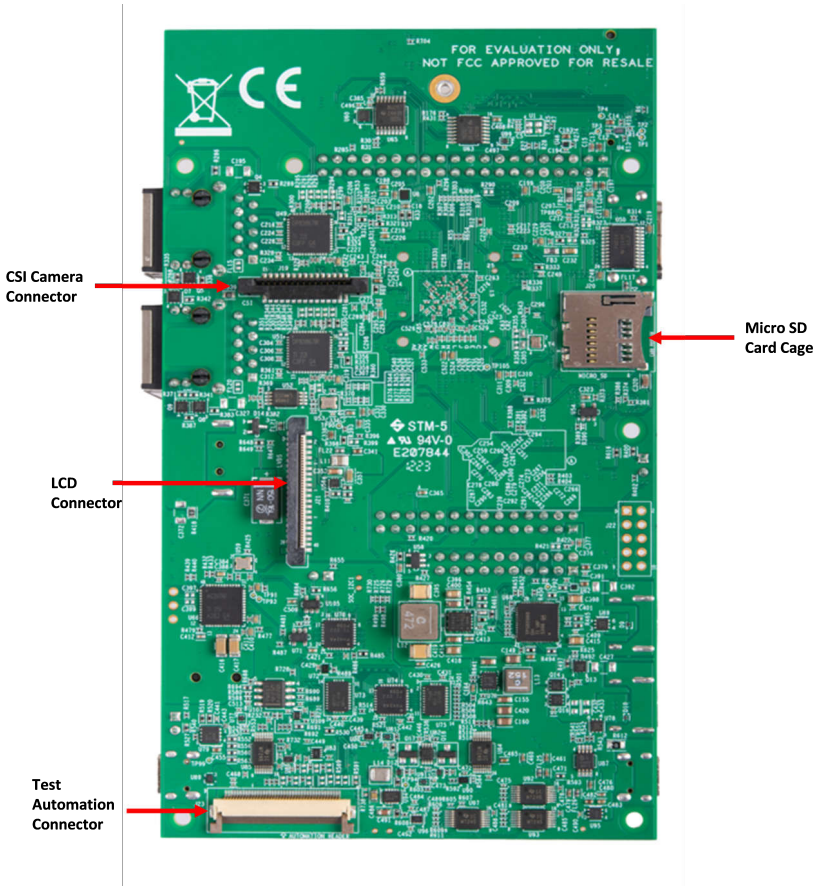

Figure 2-2. EVM Bottom Side

2.2 Key Features

The AM62x SIP SK EVM is a high performance, standalone development platform that enable users to evaluate and develop industrial applications for the Texas Instrument's AM62x SIP System-on-Chip (SoC).

The following sections discuss the key features of the SK EVM.

2.2.1 Processor

- AM62x SIPSoC, 13mm x 13mm, 0.5mm pitch, 425-pin VCA FBGA

2.2.2 Power Supply

- Two USB Type-C® ports (5V-15V input range)
- Optimized power design with discrete regulators and LDOs for the processor and peripherals

2.2.3 Memory

- MicroSD Card slot with UHS-1 support
- 512MbitOctal SPI Flash memory
- 512Kbit Inter-Integrated Circuit (I2C) board ID EEPROM
- 32GBeMMC Flash with HS-400 support

2.2.4 JTAG/Emulator

- XDS110 On-Board Emulator
- Supports20-pin JTAG connection from external emulator

2.2.5 Support Interfaces and Peripherals

- 1xUSB2.0 Type C interface, support DFP and UFP roles
- 1xUSB2.0 Host interface, Type A
- 1xHDMI interface
- Audio line in and mic + headphone out
- M.2 Key E interface support for both Wi-Fi and Bluetooth modules
- 2x Gigabit Ethernet ports supporting 10/100/1000Mbps data rate on two RJ45 connectors
- Quadport UART to USB circuit over microB USB connector
- Industrial Ethernet LEDs
- INA devices for current monitoring
- 1x Temperature sensor near SoC for thermal monitoring

2.2.6 Expansion Connectors/Headers

- CSI Camera Header
- LVDS Display connector
- User Expansion connector
- PRU Header
- MCU Header

2.3 Power

2.3.1 Power Requirements

AM62x SIP SKEVM can be powered through either of the two USB Type C Connectors:

- Connector 1 (J11) - Power role – SINK, No Data role
- Connector 2 (J13) - Power role – DRP, Data role – USB2.0 DFP or UFP

The AM62x SIP SK EVM supports voltage input ranges of 5V - 15V and 3A of current. A USB PD controller Mfr.Part# TPS65988DHRSHR is used for PD negotiation upon cable detection to get necessary power required for the board. Connector 1 is configured to be an UFP Port and has no Data role. Connector 2 is configured as a DRP port and can act as DFP only when the board is being powered by Connector 1. When both the connectors are connected to external power supply, the port with highest PD power contract is selected to power the board.

Table 2-1. Type-C Port Power Roles

J11(UFP)	J13(DRP)	Board Power	Remarks
Plugged in	NC	ON- J11	J11is UFP and only sinks power and J13 can act as DFP if a peripheral is connected.
NC	Plugged in	ON - J13	J13 is UFP and can only sink power.
Plugged in	Plugged in	ON- J11 or J13	Board is powered by the port with highest PD power contract.

The PD IC uses a SPI EEPROM to load the necessary configuration on power up so the PD IC can negotiate a power contract with a compatible power source.

The configuration file is loaded to the EEPROM using header J22. Once the EEPROM is programmed the PD obtains the configuration files via SPI communication. Upon loading the configuration files the PD negotiates with the source to obtain the necessary power requirement.

Note

The EEPROM is pre-programmed with the configuration file for the operation of the PD controller.

Power indication LEDs are provided for both the Type-C connectors for the user to identify which connector is powering the SK EVM Board.

An external power supply (Type-C output) can be used to power the EVM but is not included as part of the SK EVM kit.

The external power supply requirements (Type-C) are:

Minimum voltage: 5 VDC, recommended minimum current: 3000mA

Maximum voltage: 15VDC, maximum current: 5000mA

Table 2-2. Recommended External Power Supply

DigiKeyPart No.	Manufacturer	Manufacturer Part No.
1939-1794-ND	GlobTek,Inc.	TR9CZ3000USBCG2R6BF2
Q1251-ND	Qualtek	QADC-65-20-08CB

Note

Because SK-AM62 SIP implements USB PD for power, the device is able to negotiate to the highest Voltage/Current combination supported by both the Device and Power Adapter. If the power supply exceeds the maximum voltage and the current requirements listed above are acceptable, then the power adapter is compliant with the USB-C PD specification.

2.3.2 Power Input

Both USB Type-C Connectors (VBUS and CC lines) are connected to a dual PD controller (Mfr Part# TPS65988). The TPS65988 is a stand-alone USB Type-C and Power Delivery (PD) controller providing cable plug and orientation detection for two USB Type-C Connectors. Upon cable detection, the TPS65988 communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65988 enables the appropriate power path. The two internal power paths of TPS65988 are configured as sink paths for the two Type-C ports and an external FET path is provided for Type-C CONN 2 to source 5V when acting as DFP. The external FET path is controlled by GPIO17/PP_EXT2 of the PD controller.

TPS65988 PD controller can provide an output of 3A (15V max) through CC negotiation. The VBUS pins from both the Type C connectors are connected to the VBUS pins of the PD controller. The output of the PD is VMAIN, which is given to on board buck-boost and buck regulators to generate fixed 5V and 3.3V supply for the SK EVM board.

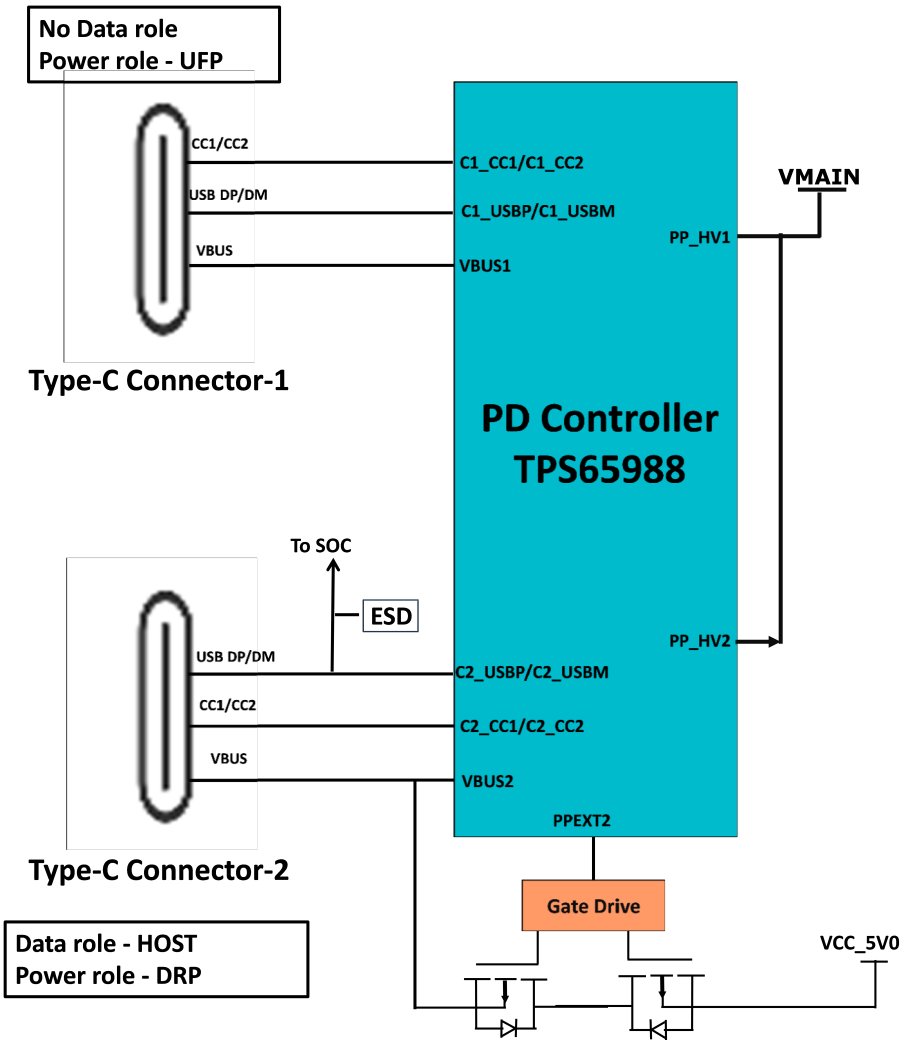

Figure 2-3. PD Controller

The following sections describe the power distribution network topology that supplies the SKEVM board, supporting components and reference voltages.

The AM62x SIP SK EVM board includes a power design based on discrete power supply components. The initial stage of the power supply are VBUS voltage from either of the two USB Type-C connectors J11 and J13. USB Type-C dual PD controller (Mfr. Part# TPS65988DHRSHR) is used for negotiation of the required power to the system.

Buck-Boost controller TPS630702RNMR and buck converter LM61460-Q1 are used for the generation of 5V and 3.3V, respectively, and the input to the regulators is the PD output. These 3.3V and 5V voltages are the primary voltages for the AM62x SIP SK EVM board power resources.

The 3.3V supply generated from the buck regulator LM61460-Q1 is the input supply to the various SoC regulators and LDOs. The 5V supply generated from the Buck-Boost regulator TPS630702RNMR is used for powering the on board peripherals.

Discrete regulators and LDOs used on board are:

- TPS62824DMQR – To generate VDD_2V5 rail for Ethernet PHYs
- TLV75510PDQNR – To generate VDD_1V0 for Ethernet PHYs
- TLV75512PDQNR – To generate VDD_1V2 for HDMI Transmitter
- TLV74018PDQNR – To generate 1.8V Analog supply for SoC

- TPS62A01DRLR – To generate 1.8V IO supply for SoC and for Peripherals namely OSPI, eMMC, Audio codec, M.2 Connector and Clock Buffer
- TLV7103318QDSERQ1 – To generate VDDSHV5_MMC1(SD interface) supply for SoC
- TPS62A01DRLR – To generate DDR Power for SoC
- TPS62826DMQR – To generate Core supply for SoC

Dedicated regulators are also provided on the board for:

- TPS62177 Regulator – Powering the always on circuits of Test Automation Section
- TLV75518LDO – e-Fuse programming of SoC
- TPS79601LDO – XDS110 On board emulator
- TPS73533LDO – FT4232 UART to USB Bridge

Additionally, GPIO from the test automation header is also connected to the TPS630702RNMR Enable to control ON/OFF of the SK EVM via the test automation board. The test automation board only disables the VCC_5V0 output of TPS630702RNMR from which all other power supplies are derived. SoC has different IO groups. Each IO group is powered by specific power supplies as given in the next section.

2.3.3 Power Supply

AM62x SIP SK EVM utilizes an array of DC-DC converters to supply the various memories, clocks, SoC and other components on the board with the necessary voltage and the power required.

The figure below shows the various discrete regulators and LDOs used to generate power rails and the current consumption of each peripheral on AM62x SIP SK EVM board.

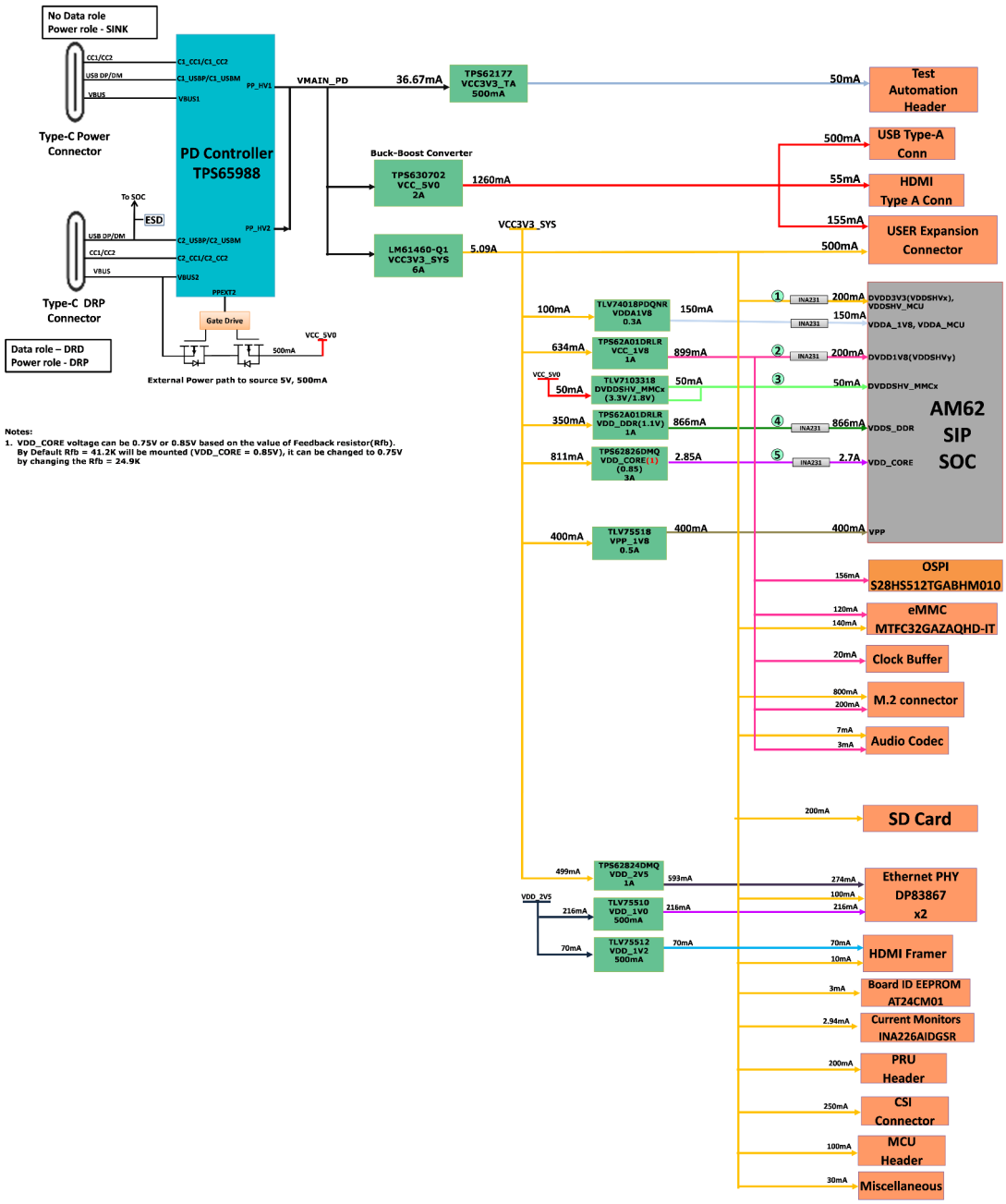

Figure 2-4. Power Architecture

2.3.4 Power Sequencing

The figure below shows the Power Up and Power Down sequence of all the AM62x SIP SK EVM Power supplies. AM62x SIP SoC Power rails are named in red.

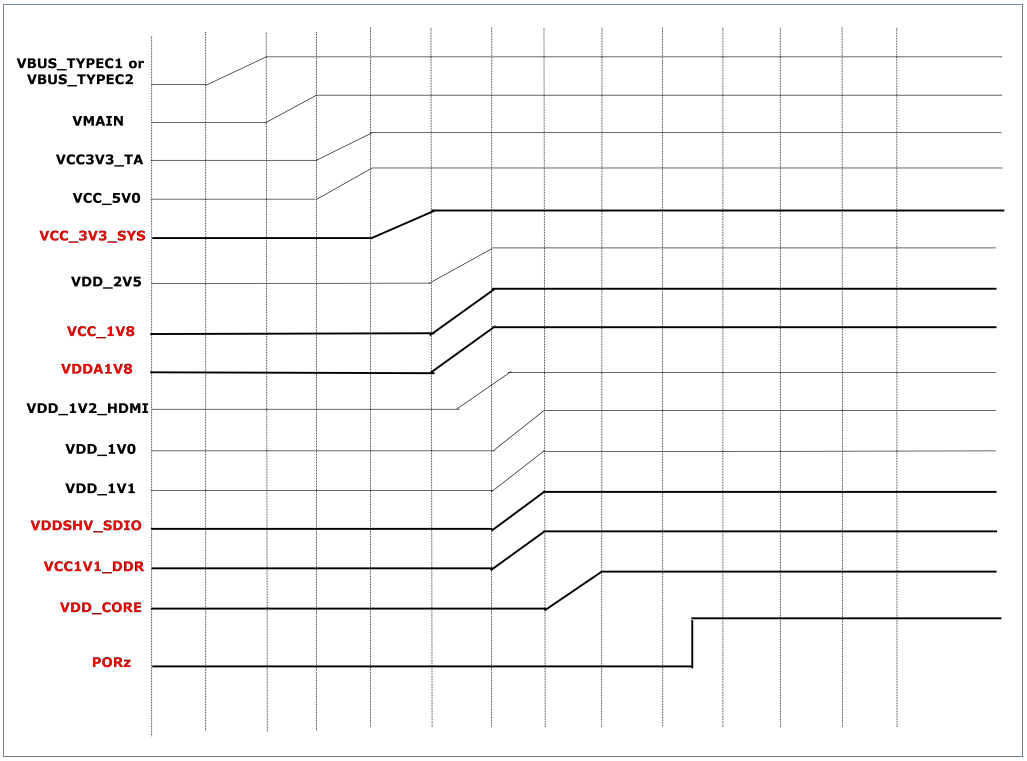

Figure 2-5. Power Up Sequence

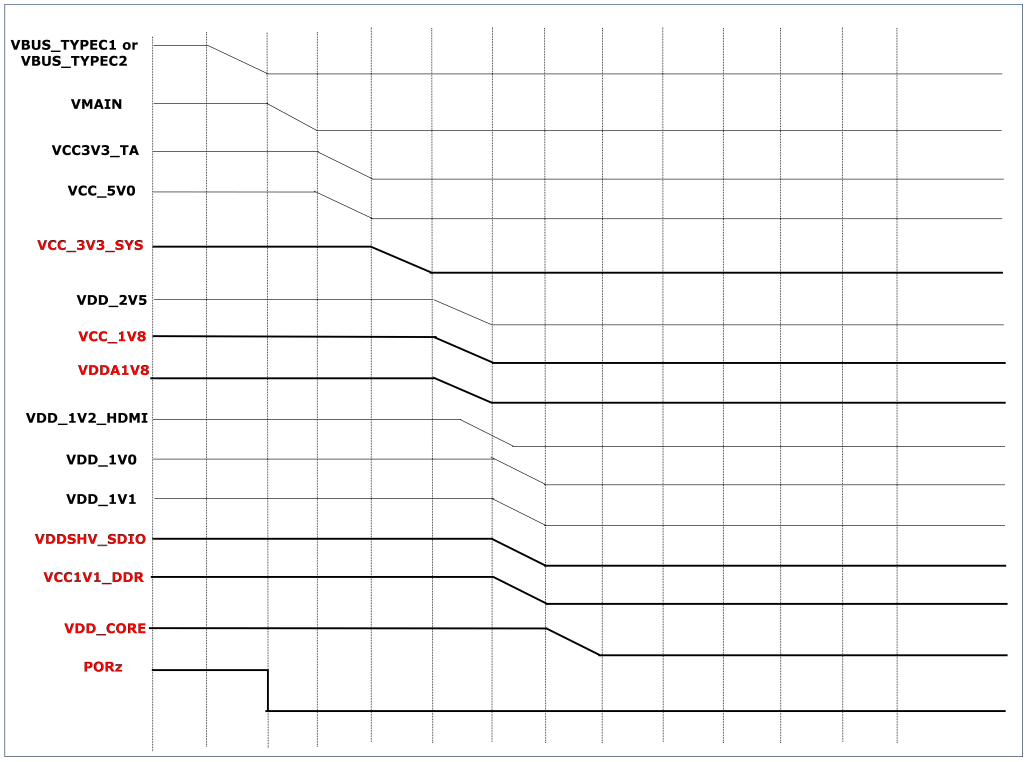

Figure 2-6. Power Down Sequence

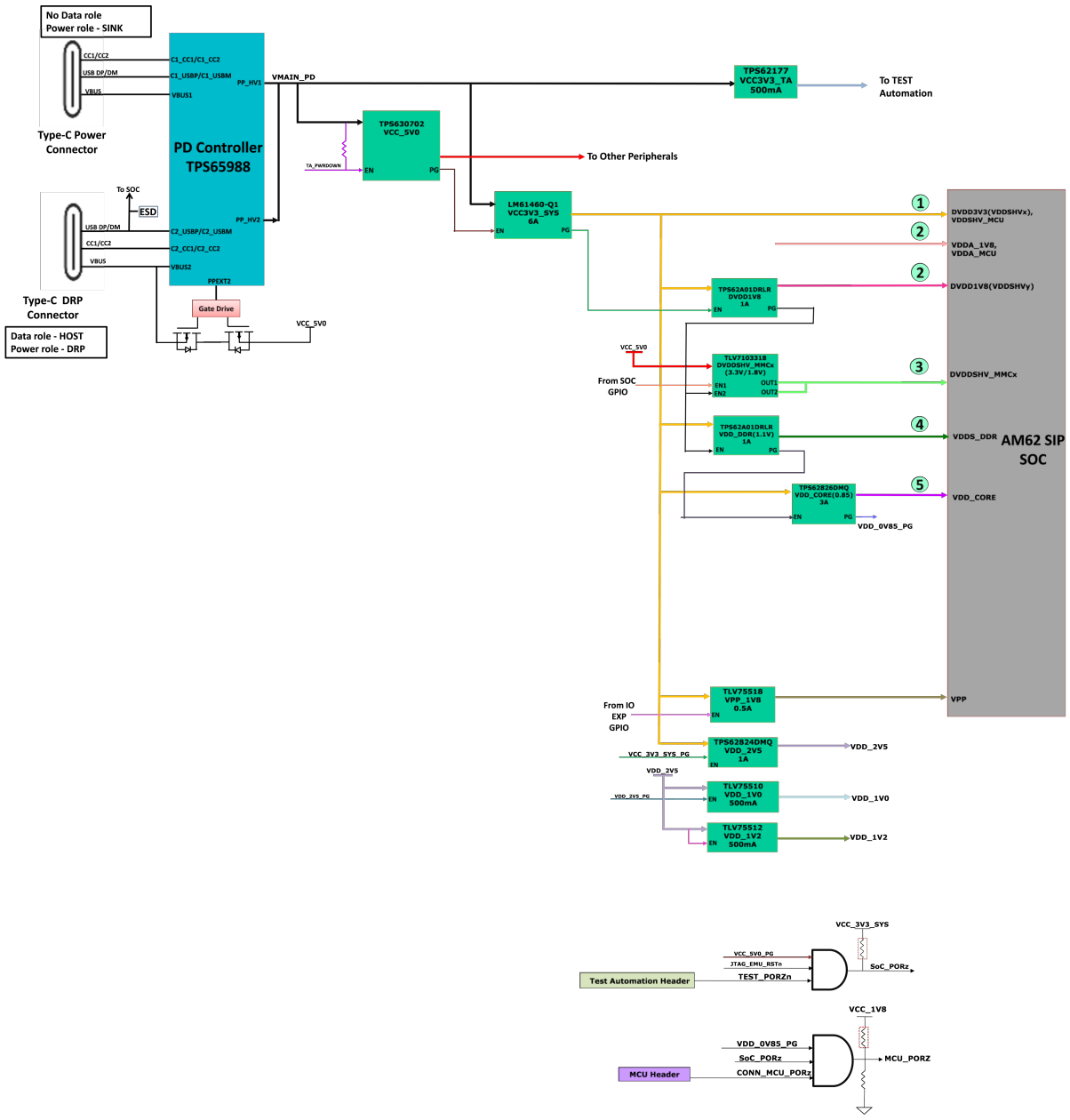

Figure 2-7. Power Supply Sequencing

2.3.5 AM62x SIP SoC Power

The core voltage of the AM62x SIP can be 0.75V or 0.85V based on the Rfb (R150) resistor value and the power optimization requirement. By default, Rfb = 41.2K is mounted (VDD_CORE = 0.85V), and can be changed to 0.75V by changing the Rfb to 24.9K. Current monitors are provided on all the SoC power rails.

The SoC has different IO groups. Each IO group is powered by specific power supplies as shown in the table below.

Table 2-3. SoC Power Supply

Sl.No	Power Supply	SoCSupply Rails	IO Power Group	Voltage
1	VDD_CORE	VDDA_CORE_USB		0.85
		VDDA_CORE_CSI		
		VDD_CANUART	CANUART	
		VDD_CORE	CORE	
		VDDR_CORE	CORE	
2	VDDA_1V8	VDDA_1V8_CSIRX.	CSI	1.8
		VDDA_1V8_USB	USB	
		VDDA_1V8_MCU		
		VDDA_1V8_OLDI	OLDI	
		VDDA_1V8_OSCO	OSCO	
		VDDS_MEM_1P8	DDR	
		VDDA_PLL0, VDDA_PLL1 &VDDA_PLL2		
3	VDD_DDR	VDDS_DDR	DDR0	1.1
		VDDS_DDR_MEM		
5	VPP_1V8	VPP_1V8		1.8
6	SoC_VDDSHV5_SDIO	VDDSHV5	MMC1	
7	SoC_DVDD1V8	VDDSHV0	General	1.8
		VDDSHV1	OSPI	
		VDDSHV4	MMC0	
		VDDSHV6	MMC2	
		VMON_1P8_SOC		
8	SoC_DVDD3V3	VDDSHV0	General	3.3
		VDDSHV2	RGMII	
		VDDSHV3	GPMC	
		VDDSHV_MCU	MCU General	
		VMON_3P3_SOC		
		VDDA_3P3_USB	USB	

2.3.6 Current Monitoring

INA231 power monitor devices are used to monitor current and voltage of various power rails of AM62x SIP processor. The INA231 interfaces to the AM62x SIP through I2C interface (SoC_I2C1). Four terminal, high precision shunt resistors are provided to measure load current.

Table 2-4. INA I2C Device Address

Source	Supply Net	Device Address	Value of the Shunt Connected to the Supply Rail
VCC_CORE	VDD_CORE	0x40	1mΩ± 1%
VCC_3V3_SYS	SoC_DVDD3V3	0x4C	10mΩ± 1%
VCC_1V8	SoC_DVDD1V8	0x45	10mΩ± 1%
VDDA1V8	VDDA_1V8	0x4D	10mΩ± 1%
VCC1V1_DDR	VDD_DDR	0x47	10mΩ± 1%

2.4 Power ON/OFF Procedure

Power to the EVM is provided through an external power supply providing PD voltage and current to the either of the two USB Type-C Ports.

Note

The maximum length of the IO cables shall not exceed 3 meters.

2.4.1 Power ON Procedure

1. Place the SK EVM boot switch selectors (SW1, SW2) into selected boot mode. Example boot-modes for SD card and no-boot are shown below.
2. Connect the boot media (if applicable).
3. Attach the PD capable USB Type-C cable to the SKEVM Type-C (J11 or J13) connector.
4. Connect the other end of the Type-C cable to the source, either AC Power Adapter, or Type C source device (such as a Laptop computer).
5. Visually inspect that either LD10 or LD12 LED are illuminated.
6. XDS110JTAG and UART debug console output are routed to micro-USB ports J16 and J15, respectively.

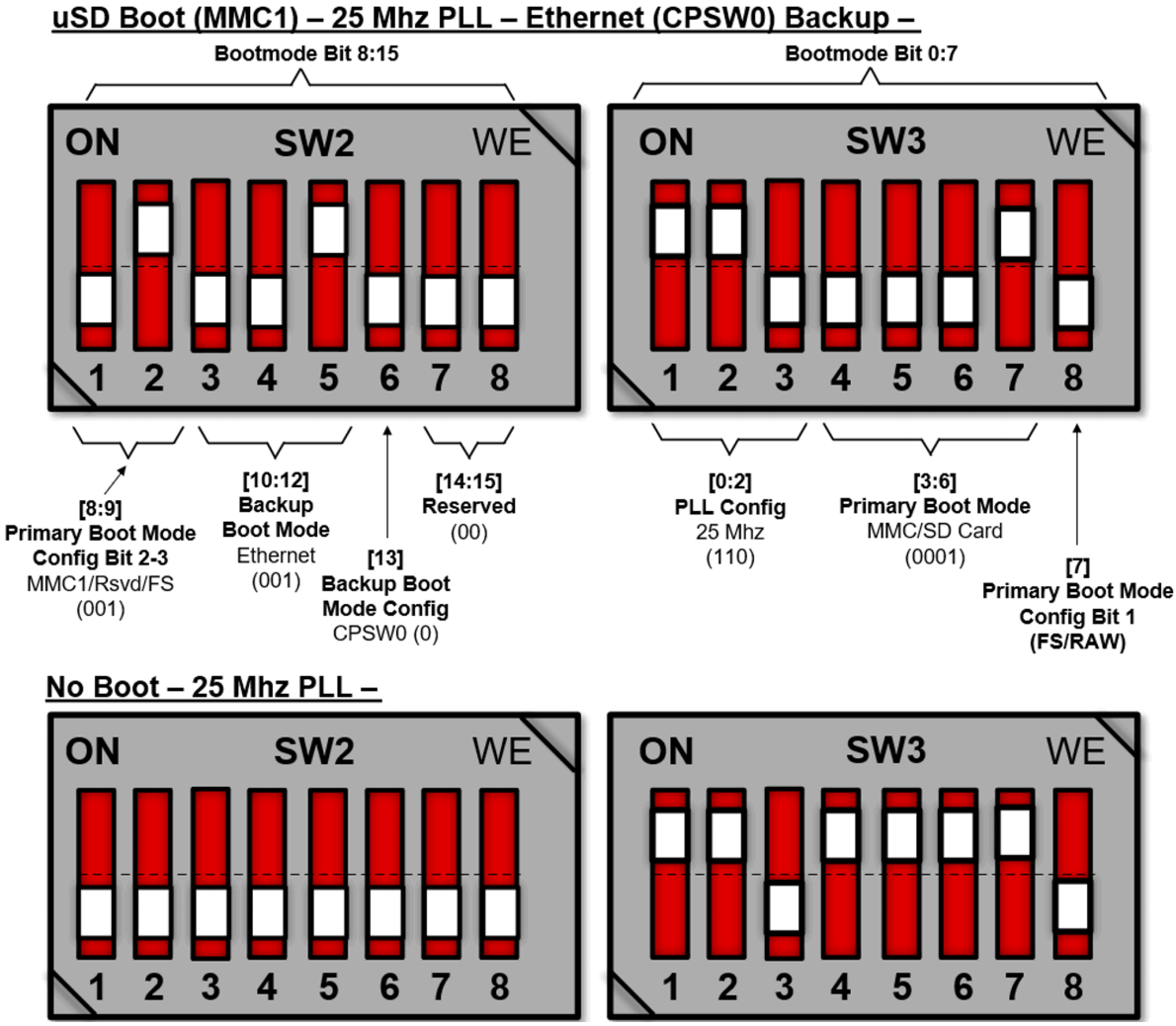

Figure 2-8. SD Boot Mode and No Boot Switch Setting Examples

2.4.2 Power OFF Procedure

1. Disconnect AC power from AC/DC converter.
2. Remove the USB Type-C cable from the SK EVM.

2.4.3 Power Test Points

Test points for each power output on the board is mentioned in the table below.

Table 2-5. Power Test Points

S.No	Power Supply	Test Point	Voltage
1	VBUS_TYPEC1	C398.1	5V-15V
2	VBUS_TYPEC2	C415.1	5V-15V
3	VMAIN	TP95	5V-15V
4	VCC_5V0	TP70	5V
5	VCC_3V3_SYS	TP51	3.3V
6	VDD_2V5	TP42	2.5V
7	VPP_1V8	TP31	1.8V
8	VDD_1V0	TP33	1.0V
9	VDD_1V2	TP10	1.2V
10	VDDA1V8	TP36	1.8V

Table 2-5. Power Test Points (continued)

S.No	Power Supply	Test Point	Voltage
11	VCC_1V8	TP41	1.8V
12	VDDSHV_SDIO	TP29	1.8V/3.3V
13	VCC1V1_DDR	TP40	1.1V
14	VCC_CORE	TP45	0.85V
15	VDD_CORE	TP46	0.85V
16	VCC3V3_TA	TP87	3.3V
17	VCC3V3_XDS	TP77	3.3V
18	VCC_3V3_FT4232	C482.1	3.3V

2.5 Interface Mapping

Table 2-6. Interface Mapping

Interface Name	Port on SoC	Device Part Number
Memory – OSPI	OSPI0	S28HS512TGABHM010
Memory – Micro SD Socket	MMC1	MEM2051-00-195-00-A
Memory – eMMC	MMC0	MTFC32GAZAQHD-IT
Memory – Board ID EEPROM	SoC_I2C0	AT24C512C-MAHM-T
Ethernet 1 – RGMII	SoC_RGMII1	DP83867IRRGZ
Ethernet 2 – RGMII	SoC_RGMII2	DP83867IRRGZ
LED Driver – 8 Communication LEDs	WKUP_I2C0	TPIC2810D
PRU Header – 2x10 HDR	PR0_PRU0_GPO and SoC_I2C0	PREC010DAAN-RC
User Expansion Connector – 2x20 HDR	SPI0, SPI2, UART5, SoC_I2C0, SoC_I2C2 and GPIOs	PEC20DAAN
MCU Header – 2x14 HDR	MCU_UART0,MCU_MCAN0, MCU_SPI0, MCU_I2C0 and MCU GPIOs	PREC014DAAN-RC
USB– 2.0 Type C	USB0	2012670005
USB– 2.0 Type A	USB1	629104151021
LVDS Display Connector	OLDI0	FFC2A32-40-T
CSI Interface	CSI0	1-1734248-5
HDMI	VOUT0	SiI9022ACNU + TPD12S016PWR +10029449-001RLF
AudioCodec	McASP2and SoC_I2C1	TLV320AIC3106IRGZT+ SJ-43514-SMT
GPIO Port Expander	SoC_I2C1	TCA6424ARGJR
UART Terminal (UART-to-USB)	SoC_UART[1:0], WKUP_UART0 and MCU_UART0	FT4232HL+ 629105150521
Test Automation Header	SoC_I2C1	FH12A-40S-0.5SH
Temperature Sensor	SoC_I2C1	TMP100NA/3K
Current Monitors	SoC_I2C1	INA231AIYFDR
Connectivity– M.2 Key E	MMC2, McASP1 and SoC_UART1	2199119-4

2.6 Clocking

The figure below shows the clocking architecture of the AM62x SIP SK EVM.

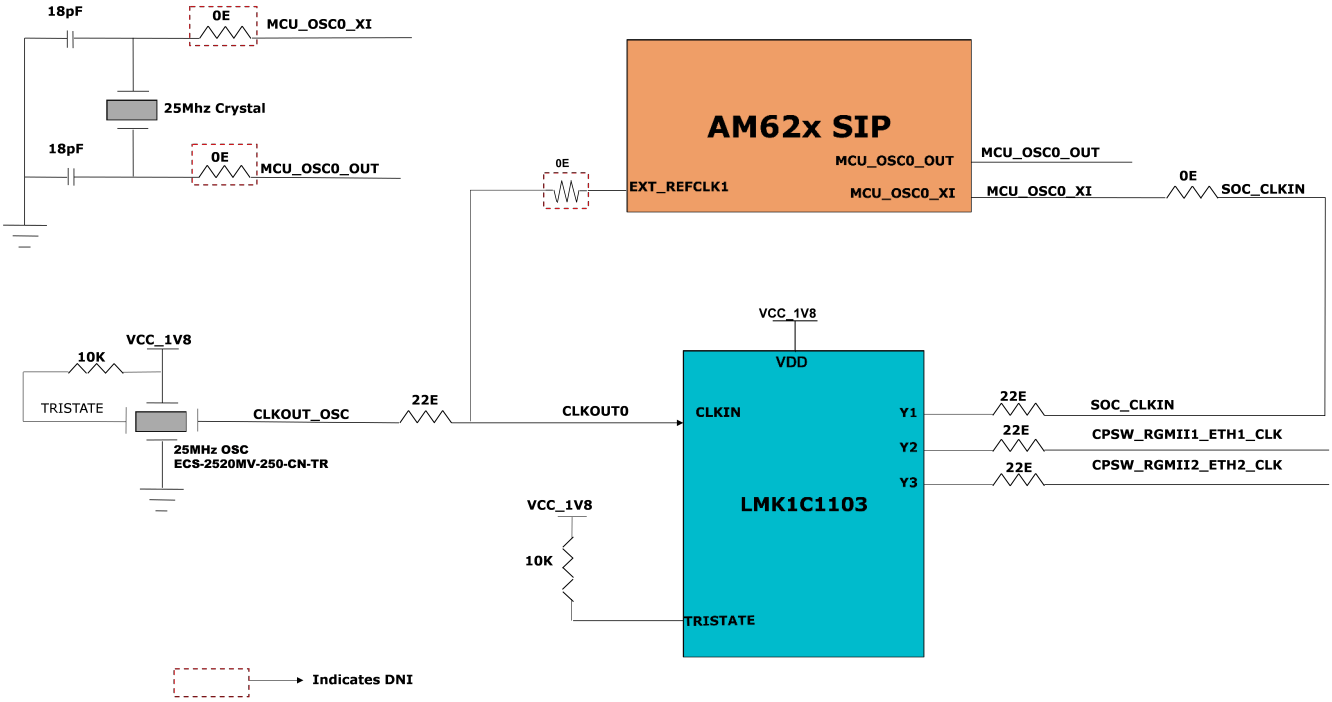

Figure 2-9. Clock Architecture

A clock generator of part number LMK1C1103PWR is used to drive the 25MHz clock to the SoC and two Ethernet PHYs. LMK1C1103PWR is a 1:3 LVCMOS clock buffer, which takes the 25MHz crystal/LVCMOS reference input and provides three 25MHz LVCMOS clock outputs. The source for the clock buffer shall be either the CLKOUT0 pin from the SoC or a 25MHz oscillator; the selection is made using a set of resistors. By default, an oscillator is used as input to the clock buffer on the AM62x SIP SKEVM. Output Y2 and Y3 of the clock buffer are used as reference clock inputs for two Gigabit Ethernet PHYs.

There is one external crystal attached to the AM62x SIP SoC to provide clock to the WKUP domain of the SoC (32.768KHz).

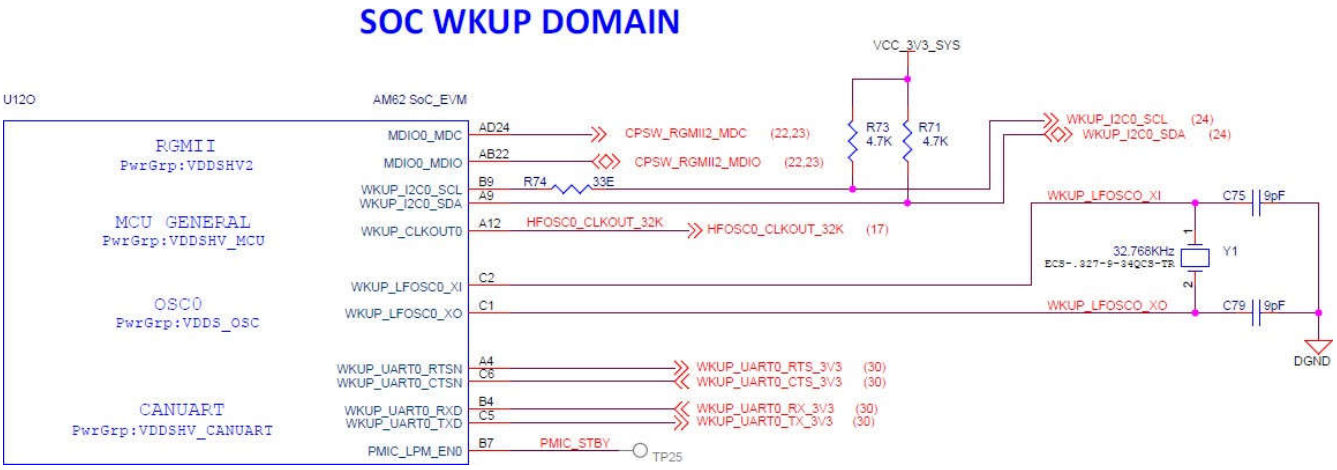

Figure 2-10. SoC WKUP Domain

2.6.1 Peripheral Ref Clock

Clock inputs required for peripherals such as XDS110, FT4232, HDMI Transmitter and Audio Codecare generated locally using separate crystals or oscillators. Crystals or Oscillators used to provide the reference clocks to the EVM peripherals are shown in the table below.

Table 2-7. Clock Table

Peripheral	Mfr. Part Number	Description	Frequency
XDS110 Emulator	XRCGB16M000FXN01R0	CRY 16.000MHz 8pF SMD	16.000MHz
FT4232 Bridge	ECS-120-18-30B-AGN-TR	CRY 12.000MHz 18pF SMD	12.000MHz
Audio Codec	KC2520Z12.2880C1KX00	OSC 12.288MHz CMOS SMD	12.288MHz
HDMI Transmitter	KC2520Z12.2880C1KX00	OSC 12.288MHz CMOS SMD	12.288MHz

The clock required by the HDMI Transmitter can be provided by either the on board oscillator or the SoC's AUDIO_EXT_REFCLK1, which can be selected through a resistor mux. The EXT_REFCLK1 of the SoC is used to provide clock to the User Expansion Connector on the SKEVM. The 32.768KHz clock to the M.2 module is provided by WKUP_CLKOUT0 of AM62x SIP SoC through a voltage translational buffer.

2.7 Reset

The Reset Architecture of AM62x SIP SK EVM is shown below.

The SoC has following resets:

- RESETSTATz is the Main domain warm reset status output
- PORz_OUT is the Main domain power ON reset status output
- RESET_REQz is the Main domain warm reset input
- MCU_PORz is the MCU domain power ON/ Cold Reset input
- MCU_RESETz is the MCU domain warm reset input
- MCU_RESETSTATz is the MCU domain warm reset status output

Upon power on reset, all peripheral devices connected to the main domain get reset by RESETSTATz.

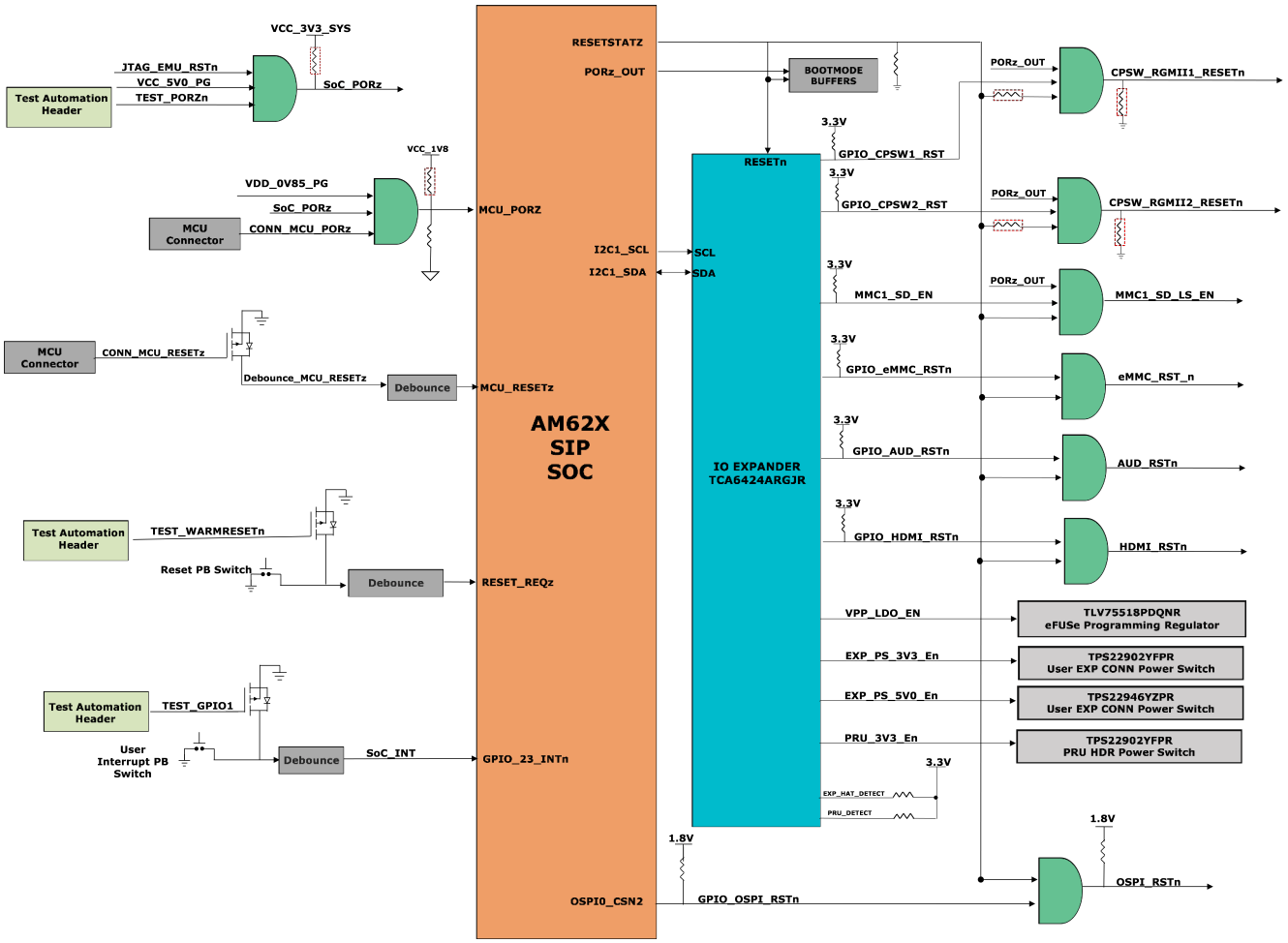

Figure 2-11. Reset Architecture

2.8 CSI Interface

The CSI-2 interface from the AM62x SIP SoC is terminated to a 15 pin Camera FPC connector 1-1734248-5 compatible with the RPi Camera Modules. These modules support 2 Lane CSI RX signals. While the SoC supports 4 CSI RX Lanes, only two are pinned out on the SK EVM.

The CSI connector pin-out is compatible with the RPi camera connector. The below table shows 15 pin CSI Connector pin-out. SoC I2C2 signals are also connected to the CSI Header. IO Expander GPIO signals are connected to the camera GPIO's.

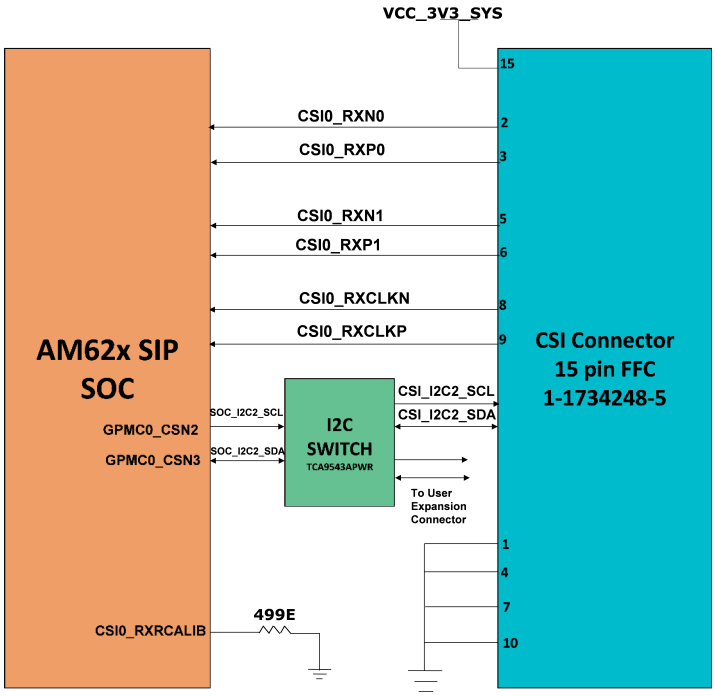

Figure 2-12. CSI Interface

Table 2-8. CSI Camera Connector J19 Pinout

Pin No.	Pin Description
1	GND
2	CSI0_RXN0
3	CSI0_RXP0
4	GND
5	CSI0_RXN1
6	CSI0_RXP1
7	GND
8	CSI0_RXCLKN
9	CSI0_RXCLKP
10	GND
11	CSI_GPIO1
12	CSI_GPIO2
13	CSI_I2C2_SCL
14	CSI_I2C2_SDA
15	VCC_3V3_SYS

2.9 Audio Codec Interface

AM62x SIP SK EVM has TI‘s Low-Power TLV320AIC3106 Stereo Audio Codec to interface with AM62x SIP via McASP.

TLV320AIC3106 is a low-power stereo audio codec with stereo headphone amplifier, as well as multiple inputs and outputs programmable in single ended or fully differential configurations. The record path of the TLV320AIC3106 contains integrated microphone bias, digitally controlled stereo microphone preamplifier and automatic gain control (AGC) with mix/Mux capability among the multiple analog inputs. The stereo audio DAC supports sampling rates from 8kHz to 96kHz.

1xStandard 3.5mm TRRS Audio Jack connector Mfr. Part# SJ-43514 shall be provided for MIC and Headphone output. The line inputs of the Audio Codec are terminated to test points.

SELECT pin shall be held LOW to select I2C as control interface. Codec can be configured over I2C interface, where I2C address can be set by driving pins MFP0 and MFP1 pin either high or low. Both these pins are set to high, so the Device address is set to 0x1B. Unused inputs and outputs of the Audio Codec are connected to ground.

The Controller Clock input, MCLK to the Audio Codec is provided through a 12.288MHz Oscillator. Audio serial data bus bit clock BCLK of the codec is driven by the AM62x SIP SoC through a buffer. Audio serial data bus input and output DIN, DOUT are connected to SoC’s MCASP1_AXR0 and MCASP1_AXR2 through buffers. An AND output of RESETSTATz and a GPIO sourced via IO expander are used to reset the Audio codec.

The TLV320AIC3106 is powered by an analog supply of 3.3V, a digital core supply of 1.8V, and a digital I/O supply 3.3V.

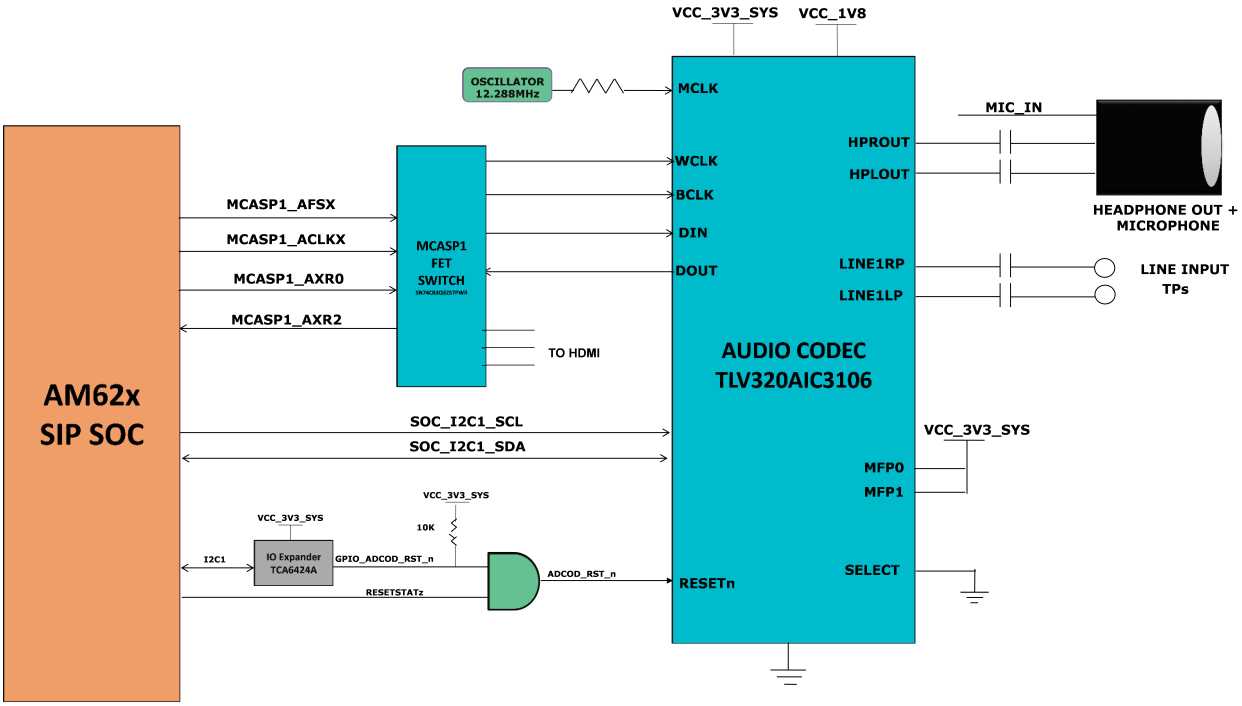

Figure 2-13. Audio Codec Interface

2.10 HDMI Display Interface

The DSS (Display Sub system) interface from AM62x SIP SoC is used on the SKEVM to provide a HDMI Interface through a standard Type-A Connector. The SKEVM features a Sil9022A HDMI Transmitter from Lattice semiconductors to convert the 24-bit Parallel RGB DSS output stream as well as a McASP to a HDMI-compliant digital audio and video signal.

The Data mapping format used is RGB888. The data bus width is 24-bits.

SoC_I2C1 is connected to the HDMI Transmitter to access the compatible mode registers, the TPI registers,and the CPI registers. To use the Sil9022A, the SoC needs to set up the device by the I2C interface between the SoC and the Sil9022A. Audio Data is sent from SoC to HDMI transmitter through the McASP1 instance. HDMI_I2C Bus accesses the EDID and HDCP data on an attached sink device.

TMDS Differential data pairs along with the differential clock signals from the transmitter are connected to the HDMI connector through HDMI ESD device Mfr Part# TPD12S016PWR which also acts as a load switch to limit current supplied to the HDMI connector from board 5V supply.

The HDMI Framer is powered using 3.3V Board IO Supply and 1.2V by a dedicated LDO Mfr Part#-TLV75512PDQNR.

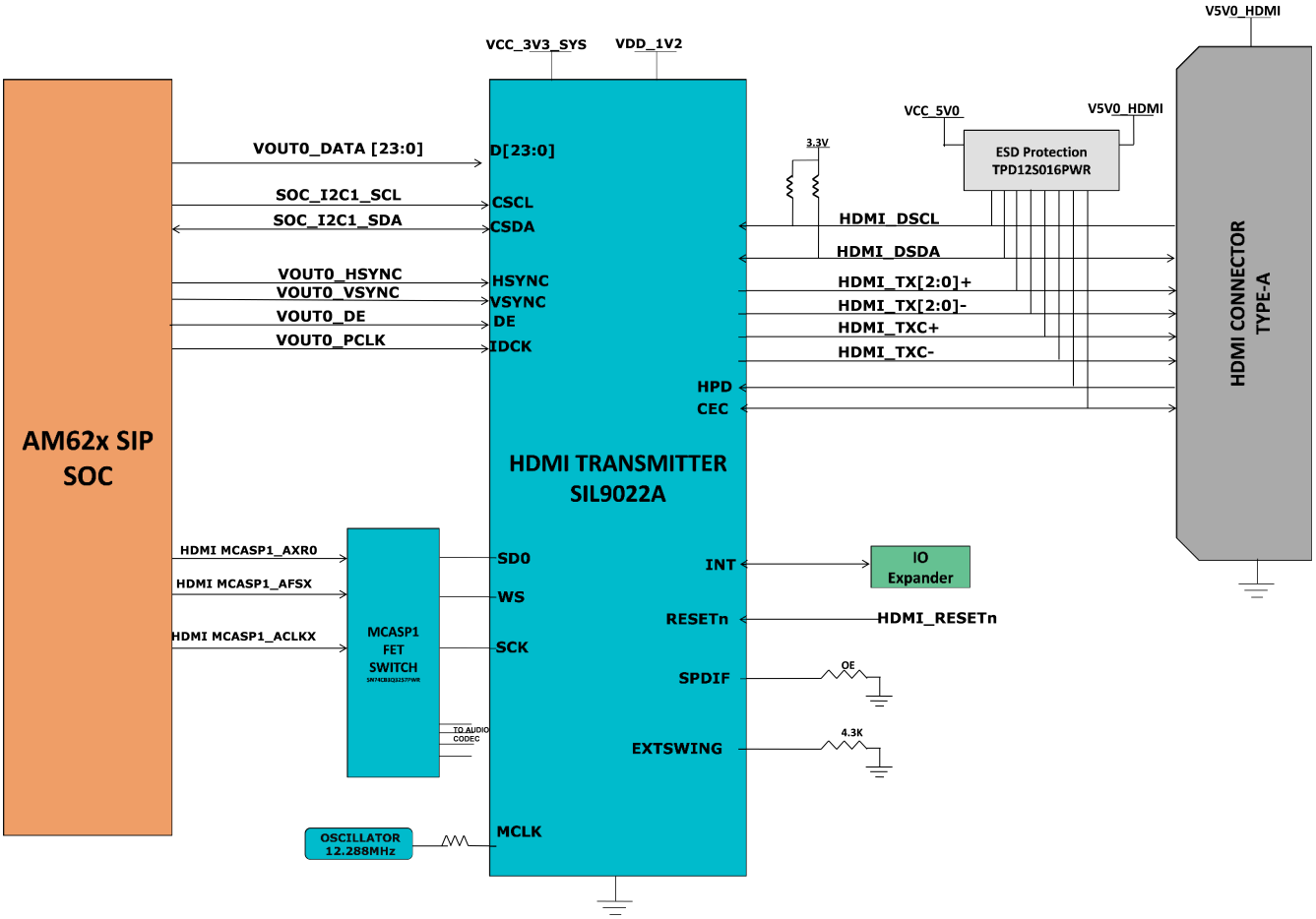

Figure 2-14. HDMI Interface

2.11 JTAG Interface

AM62x SIP SK EVM board include XDS110 class on board emulation. The connection for the emulator uses an USB 2.0 micro-B connector and the circuit act as a bus-powered USB device. The VBUS power from the connector is used to power the emulation circuit so that connection to the emulator is not lost when the power to the SK EVM is removed. Voltage translation buffers are used to isolate the XDS110 circuit from the rest of the SK EVM.

Optionally, JTAG Interface on SK EVM is also provided through 20 Pin Standard JTAG cTI Header J17. This allows the user to connect an external JTAG Emulator Cable. Voltage translation buffers are used to isolate the JTAG signals from cTI header from the rest of the SK EVM. The output from the voltage translators from XDS110 Section and cTI Header Section are muxed and connected to AM62x SIP JTAG Interface. If a connection to the cTI 20 Pin JTAG connector is sensed using a presence detect circuit, then the mux is set to route the 20 pin signals from the cTI connector to the AM62x SIP SoC in place of the on-board emulation circuit.

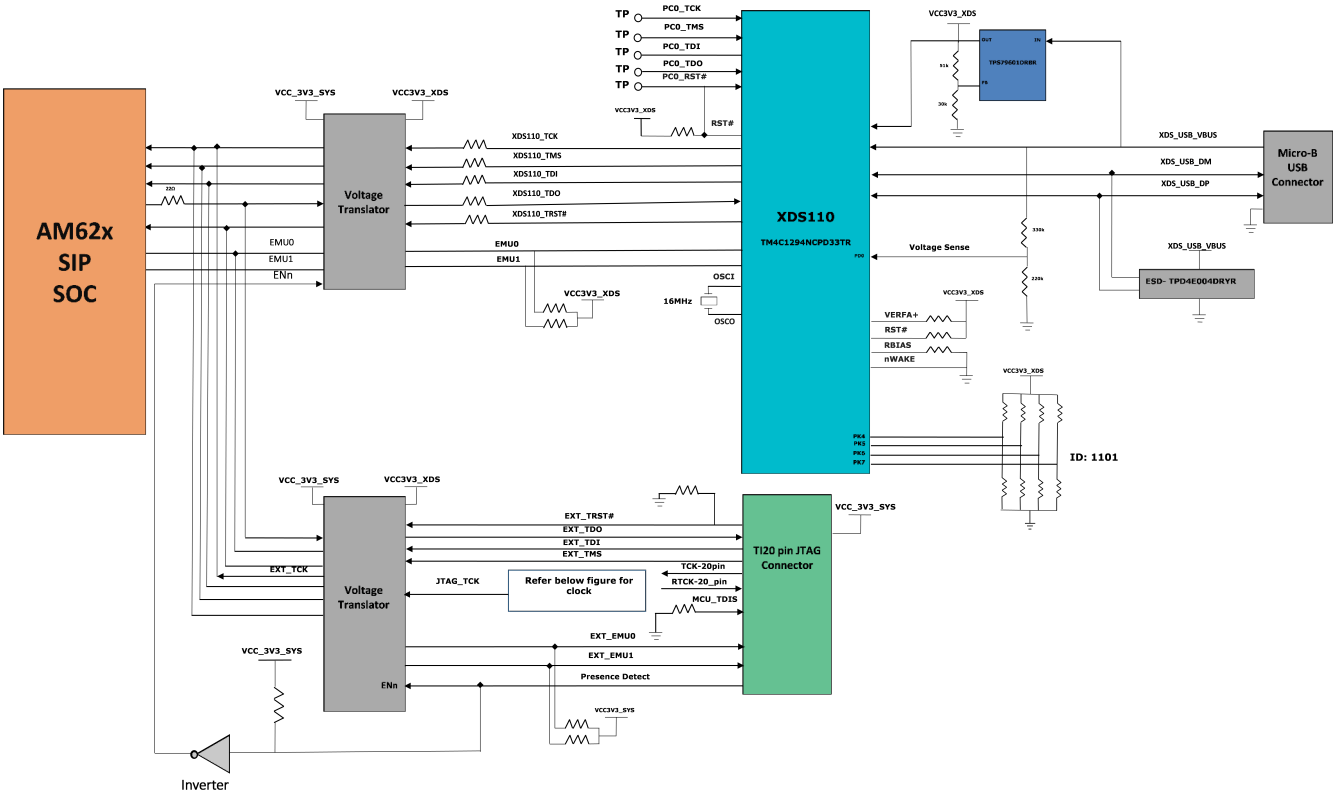

Figure 2-15. JTAG Interface

The pin-outs of the cTI 20 pin JTAG connector are given in the table below. An ESD-protection part number TPD4E004 is provided on USB signals to steer ESD current pulses to VCC or GND. TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) as specified in IEC 61000-4-2 and provides ±8-kV contact discharge and ±12- kV air-gap discharge.

Table 2-9. JTAG Connector (J17) Pin-Out

Pin No.	Signal
1	JTAG_TMS
2	JTAG_TRST#
3	JTAG_TDI
4	JTAG_TDIS
5	VCC3V3_SYS
6	NC
7	JTAG_TDO
8	SEL_XDS110_INV
9	JTAG_cTI_RTCK
10	DGND
11	JTAG_cTI_TCK
12	DGND
13	JTAG_EMU0
14	JTAG_EMU1
15	JTAG_EMU_RSTn
16	DGND
17	NC
18	NC
19	NC
20	DGND

2.12 Test Automation Header

AM62x SIP SK EVM has a 40-pin test automation header (FH12A-40S-0.5SH) to allow an external controller to manipulate some basic operations like Power Down, POR, Warm Reset, Boot Mode control, and so forth.

The Test Automation Circuit is powered by the 3.3V supply generated by a dedicated regulator Mfr. Part# TPS62177DQCR. The SoC's I2C1 is connected to the test automation header. Another I2C instance (BOOTMODE_I2C) from the Test Automation Header is connected to the 24-bit I2C boot mode IO Expander of Mfr. Part# TCA6424ARGJR to allow control of the boot modes for the AM62x SIP SoC.

The test automation circuit has voltage translation circuits so that the controller is isolated from the IO voltages used by the AM62x SIP. Boot mode for the AM62x SIP must be controlled by either the user using DIP Switches or the test automation header through the I2C IO Expander. Boot Mode Buffers are used to isolate the Boot Mode controls driven through DIP Switches or I2C IO Expander. The boot mode is controlled by the user using two 8-bit DIP switches on the board, which connects a pull-up resistor to the output of a buffer when the switch is set to the ON position and to weaker pull-down resistor when set to the OFF position. The output of the buffer is connected to the boot mode pins on the AM62x SIP SoC and the output is enabled when the boot mode is needed during a reset cycle.

When boot mode is to be set through Test Automation header, the required switch values are set at the I2C IO expander output, which overwrites the DIP switch values to give the desired boot values to the SoC. The pins used for boot mode also have other functions which is isolated by disabling the boot mode buffer during normal operation.

The power down signal from the Test automation header instructs the SK EVM to power down all the rails except for dedicated power supplies on the board. Similarly PORZn signal is also provided to give a hard reset to the SoC and WARM_RESETn for warm reset of the SoC. One Interrupt signal from the Test Automation header is routed to the SoC GPIO (GPIO1_23) to provide an external Interrupt.

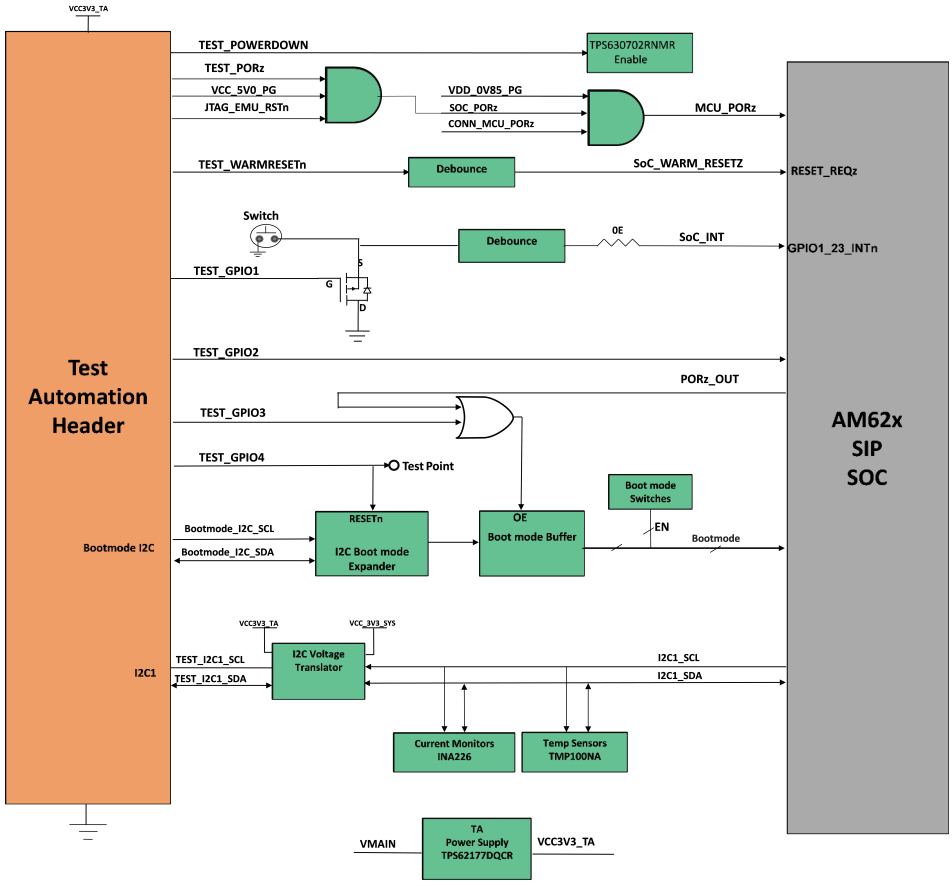

Figure 2-16. Test Automation

Table 2-10. Test Automation Connector (J23) Pin-Out

Pin No.	Signal	IO Direction	Pin No.	Signal	IO Direction
1	VCC3V3_TA	Power	21	NC	NA
2	VCC3V3_TA	Power	22	NC	NA
3	VCC3V3_TA	Power	23	NC	NA
4	NC	NA	24	NC	NA
5	NC	NA	25	DGND	Power
6	NC	NA	26	TEST_POWERDOWN	Input
7	DGND	Power	27	TEST_PORz	Input
8	NC	NA	28	TEST_WARMRESETn	Input
9	NC	NA	29	NC	NA
10	NC	NA	30	TEST_GPIO1	Bidirectional
11	NC	NA	31	TEST_GPIO2	Bidirectional
12	NC	NA	32	TEST_GPIO3	Input
13	NC	NA	33	TEST_GPIO4	Input
14	NC	NA	34	DGND	Power
15	NC	NA	35	NC	NA
16	DGND	Power	36	SoC_I2C1_TA_SCL	Bidirectional
17	NC	NA	37	BOOTMODE_I2C_SCL	Bidirectional
18	NC	NA	38	SoC_I2C1_TA_SDA	Bidirectional
19	NC	NA	39	BOOTMODE_I2C_SDA	Bidirectional
20	NC	NA	40	DGND	Power

2.13 UART Interface

The four UART ports of the SoC (MCU UART0, WKUP UART0, SoC UART0 and SoC UART1) provided by the AM62x SIP are interfaced with an FTDI FT4232HL for UART-to-USB functionality and terminated on a USB micro-B connector (J15) on board. When the AM62x SIP SKEVM is connected to a Host using USB cable, the computer can establish a Virtual COM Port which can be used with any terminal emulation application. The FT4232HL is bus powered.

Since the circuit is powered through BUS power, the connection to the COM port is not lost when the SKEVM power is removed.

Table 2-11. UART Port Interface

UART Port	USB to UART Bridge	USB Connector	COM Port
SoC_UART0	FT4232HL	J15	COM1
SoC_UART1			COM2
WKUP_UART0			COM3
MCU_UART0			COM4

The FT4232 chip is configured to operate in *Single chip USB to four channel UART* mode and takes the configuration file from the external SPI EEPROM connected to the FT4232 chip. The EEPROM (93LC46B) supports 1Mbit/s clock rate. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from the FTDI web site. The FT_PROG is also used for programming the board serial number for users to identify the connected COM port with board serial number when one or more boards are connected to the computer.

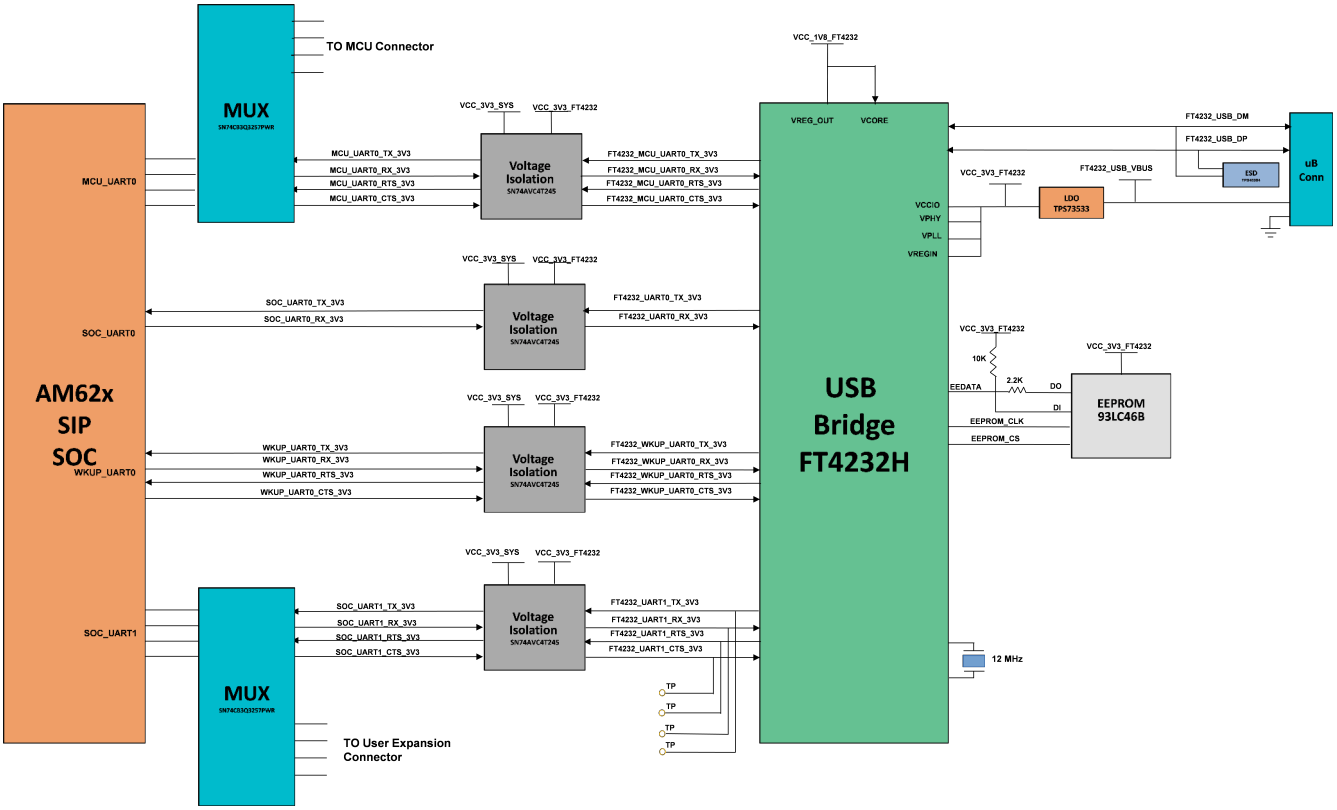

Figure 2-17. UART Interface

2.14 USB Interface

2.14.1 USB 2.0 Type A Interface

On SK EVM, USB 2.0 HOST Interface is offered through a Type-A Ports using Type-A Connector Mfr Part# 629104151021. USB1 Port of AM62x SIP SoC is used for USB 2.0 Type-A Host Interface.

USB Data lines from Type-A connectors are connected to the Current Limit Load Switch and ESD Protection IC Mfr Part# TPD3S014DBVR. This switch limits the current to 500mA and dissipates the ESD strikes above the maximum level specified in the IEC 61000-4-2.

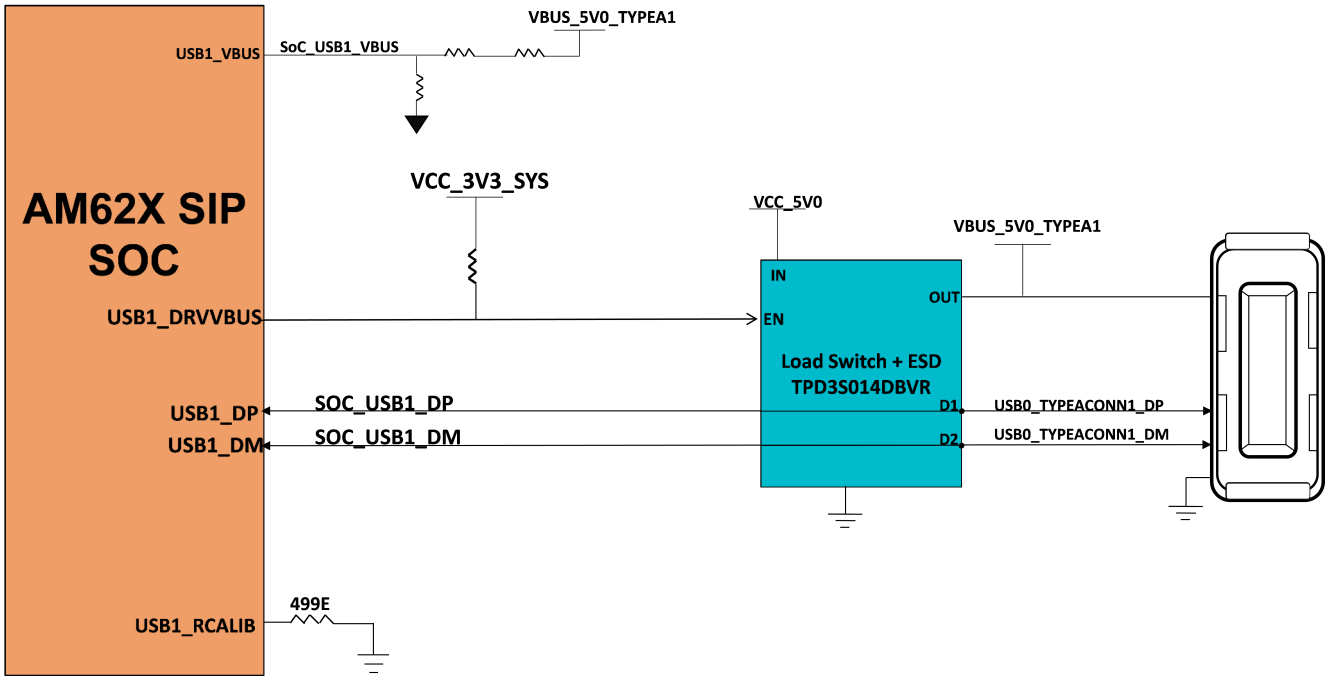

Figure 2-18. USB 2.0 Type A Interface

2.14.2 USB 2.0 Type C Interface

On SK EVM, USB 2.0 Interface is offered through USB Type-C Connector J13 Mfr part# 2012670005, which supports data rate up to 480Mbps. J13 is used for Data communication and also as power connector. J13 is configured as DRP port using PD controller TPS65988DHRSHR IC, so J13 can act as either host or device. The power role of the port depends on the type of the device getting connected on the connector and the ability to either sink or source. When the port is acting as DFP, the port can source up to 5V@500mA.

A GPIO from the PD controller is connected to USB0_DRVVBUS pin of the SoC to indicate the data role of the device connected to J13 Type-C connector. The GPIO is configured to output HIGH/LOW depending on the HOST/ DEVICE behavior of the J13 connector.

USB2.0 Data lines DP and DM from J13 are connected to the USB0 interface of AM62x SIP SoC via choke and ESD protection device. USB0_VBUS to the SoC is provided through a resistor divider network.

A common mode choke of Mfr Part# DLW21SZ900HQ2B is provided on USB Data lines to take care of EMI/ EMC. An ESD protection device of part number ESD122DMXR is included to dissipate ESD strikes on USB2.0 DP/DM Signals. An ESD protection device of part number TPD1E01B04DPLT is included on CC signals and TVS2200DRVR IC is included on VBUS rail of Type-C Connector J13 to dissipate ESD strikes.

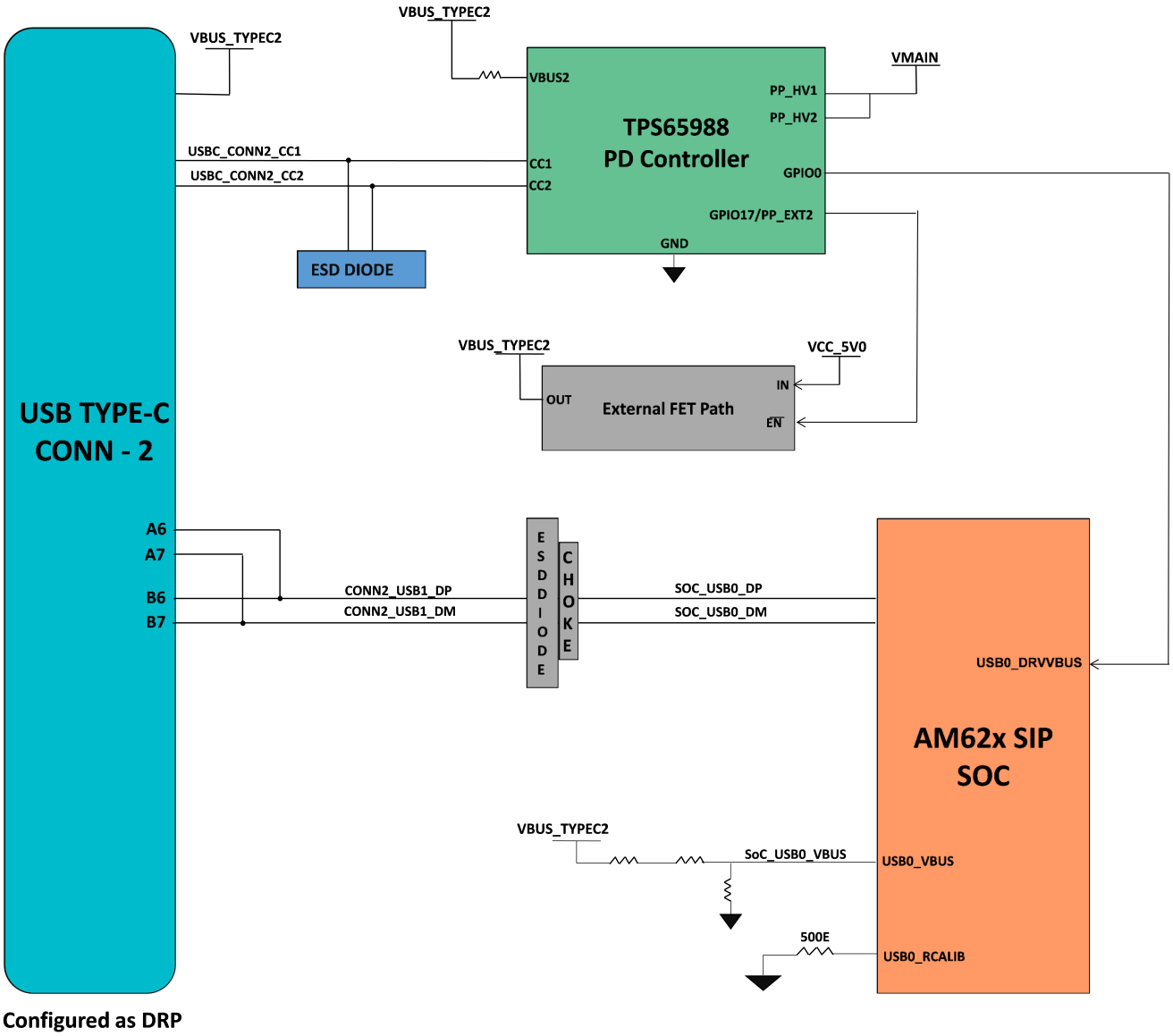

Figure 2-19. USB 2.0 Type C Interface

2.15 Memory Interfaces

2.15.1 OSPI Interface

AM62x SIP SK EVM board has a 512-Mbit OSPI memory device from Cypress Part# S28HS512TGABHM010, which is connected to the OSPI0 interface of the AM62x SIP SoC. The OSPI interface supports single and double data rates with memory speeds up to 200MBps SDR and 400MBps DDR (200MHz clock speed).

OSPI & QSPI implementation: 0 ohm resistors are provided for DATA[7:0], DQS, INT# and CLK signals. Footprints to mount external pull up resistors are provided on DATA[7:0] to prevent bus floating. The footprint for the OSPI memory also allows the installation of either a QSPI memory or an OSPI memory. The 0 ohm series resistors provided for pins OSPI_DATA[4:7] are removed if QSPI flash is to be mounted.

Reset: The reset for the OSPI flash is connected to a circuit that ANDs the RESETSTATz from the AM62x with the signal GPIO_OSPI_RSTn from the SoC GPIO. This applies to reset for warm and cold reset. A pull-up is provided on GPIO_OSPI_RSTn coming from SoC pin to set the default active state.

Power: The OSPI flash is powered by 1.8V IO supply. The 1.8V supply is provided to both VCC and VCCQ pins of the OSPI flash memory.

The OSPI of the SoC is powered by VDDSHV1 Power group of SoC and is connected to 1.8V IO supply.

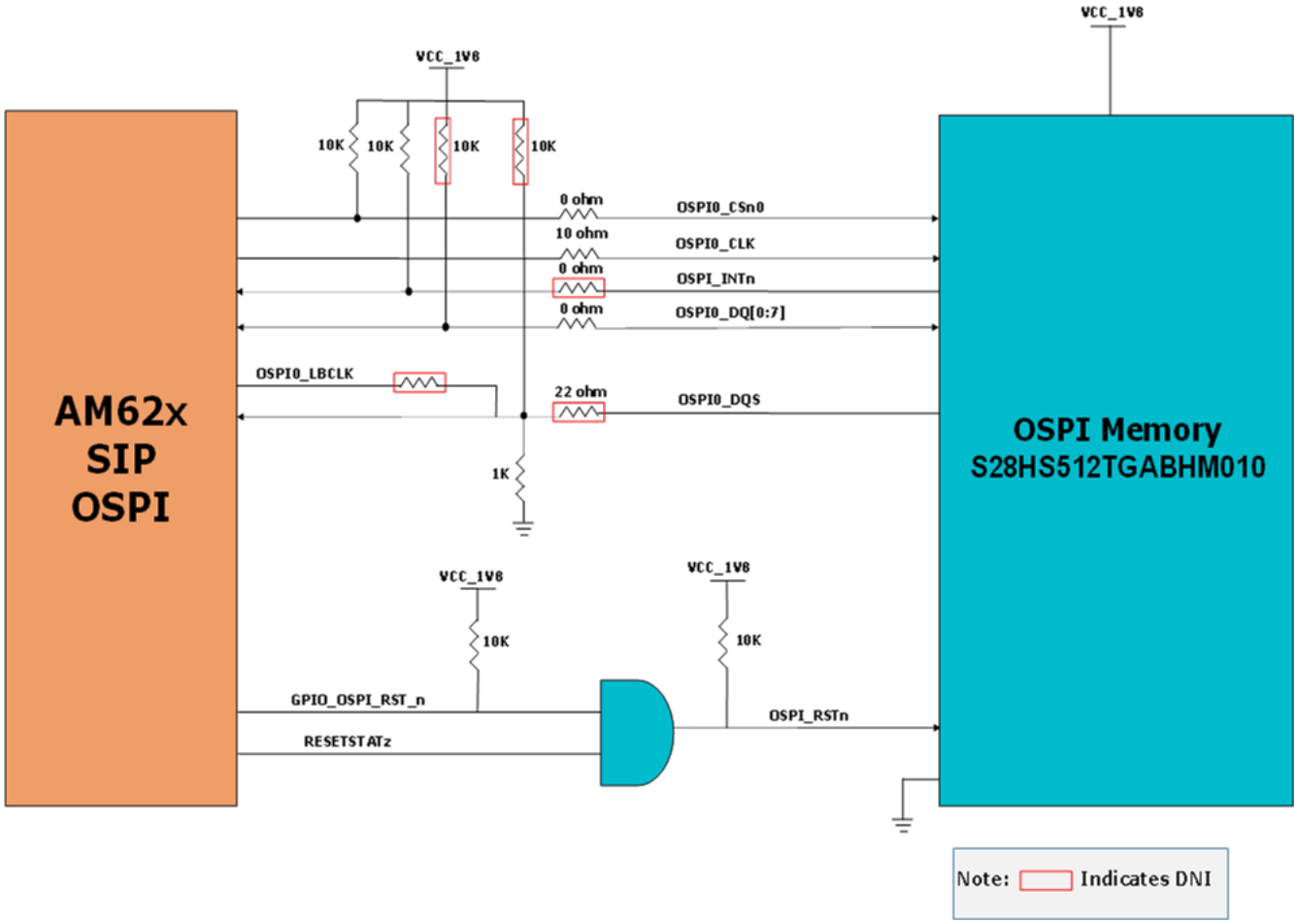

Figure 2-20. OSPI

2.15.2 MMC Interfaces

AM62x SIP SoC has three MMC (MMC0, MMC1 and MMC2) ports. MMC0 is connected to eMMC flash, MMC1 is interfaced with Micro SD Socket on the board and MMC2 is connected to M.2 module for Wi-Fi and BT Interface.

2.15.2.1 MMC0 - eMMC Interface

The SK EVM board contains 32GB of eMMC flash memory from Micron Part# MTFC32GAZAQHD-IT connected to MMC0 port of the AM62x SIP SoC. The flash is connected to 8 bits of the MMC0 interface supporting HS400 double data rates up to 200MHz.

The eMMC device requires two power supplies, 3.3V for NAND memory and 1.8V for the eMMC interface. The MMC0 interface of the SoC is powered by the VDDSHV4 power domain, which is connected to 1.8V IO supply.

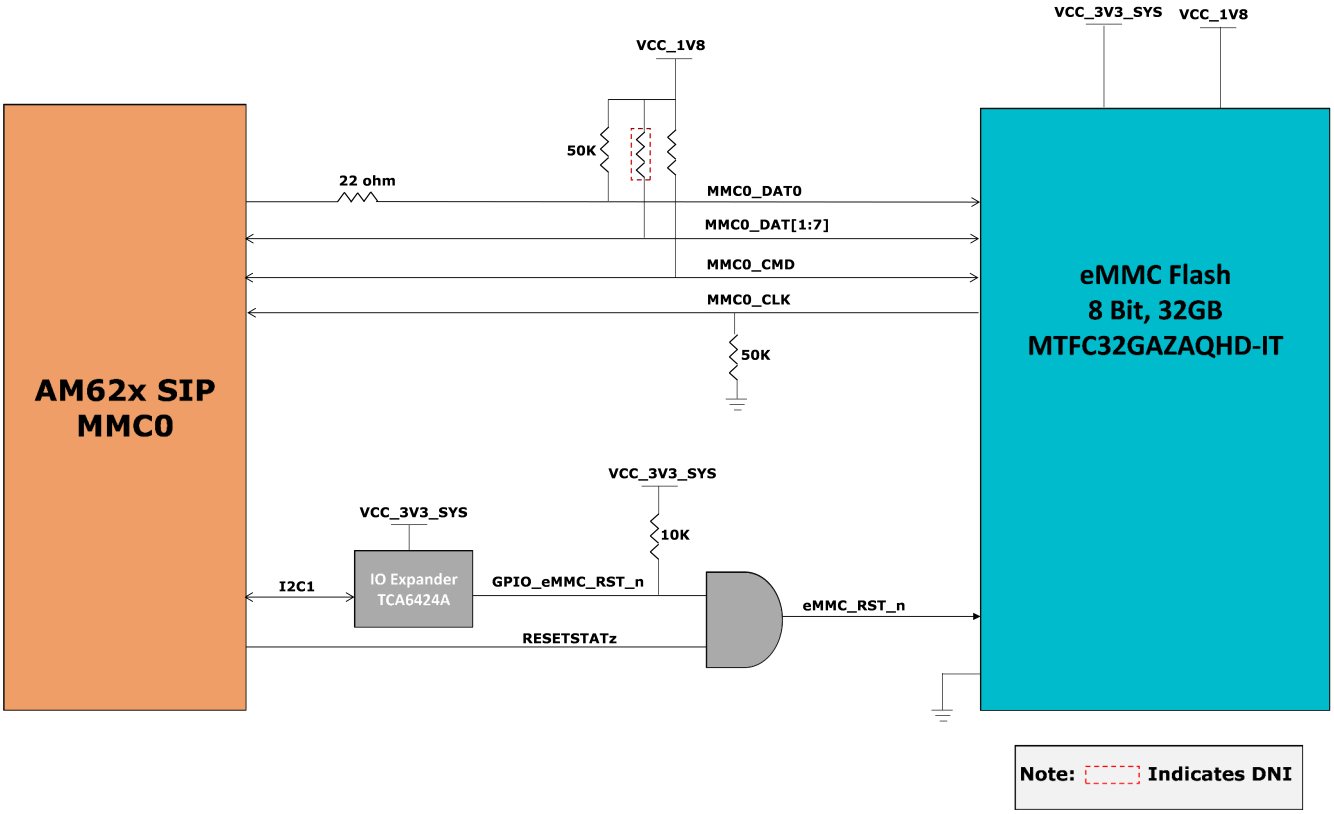

Figure 2-21. eMMC Interface

2.15.2.2 MMC1 - Micro SD Interface

The SK EVM board provides a micro SD card interface connected to the MMC1 port of the AM62x SIP SoC. The Micro SD card socket of Mfr. Part# MEM2051-00-195-00-A is used to interface with the MMC1 port of the SoC. UHS1 operation is supported, including IO operations at both 1.8V and 3.3V. The Micro SD card interface is set to operate in SD mode by default. For high-speed cards, the ROM Code of the SoC attempts to find the fastest speed that the card and controller can support and can have a transition to 1.8V.

The SD Card connector power is provided using a load switch of Mfr. Part # TPS22918DBVR, which is controlled by ANDing the output of RESETSTATz, PORz_OUT and a GPIO from an IO Expander. An ESD protection device of part number TPD6E001RSE is provided for data, clock, and command signals. TPD6E001RSE is a line termination device with integrated TVS diodes providing system-level IEC 61000-4-2 ESD protection, ± 8-kV contact discharge and ± 15kV air-gap discharge.

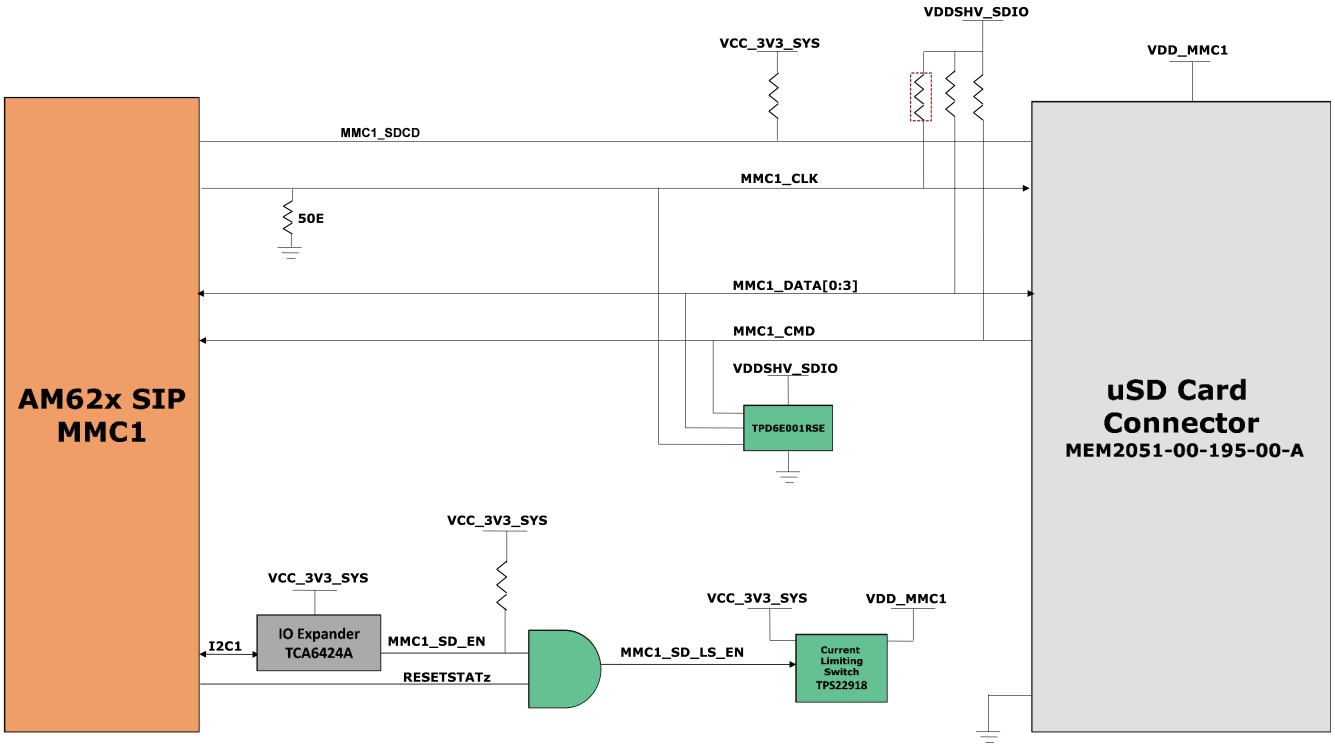

Figure 2-22. Micro SD Interface

2.15.2.3 MMC2 - M.2 Key E Interface

AM62x SIP SK EVM has a M.2 Key E interface for connecting Wi-Fi® BT modules connected to MMC2, UART1 instances and McASP1 interface through buffers. The M.2 Module is connected to 4-bit IO of the MMC2 interface.

The Module requires one power supply, 3.3V. Power to M.2 module is supplied from on board Power supply rails.

The MMC2 interface of the SoC is powered by the VDDSHV6 power domain, which is connected to 1.8V IO supply.

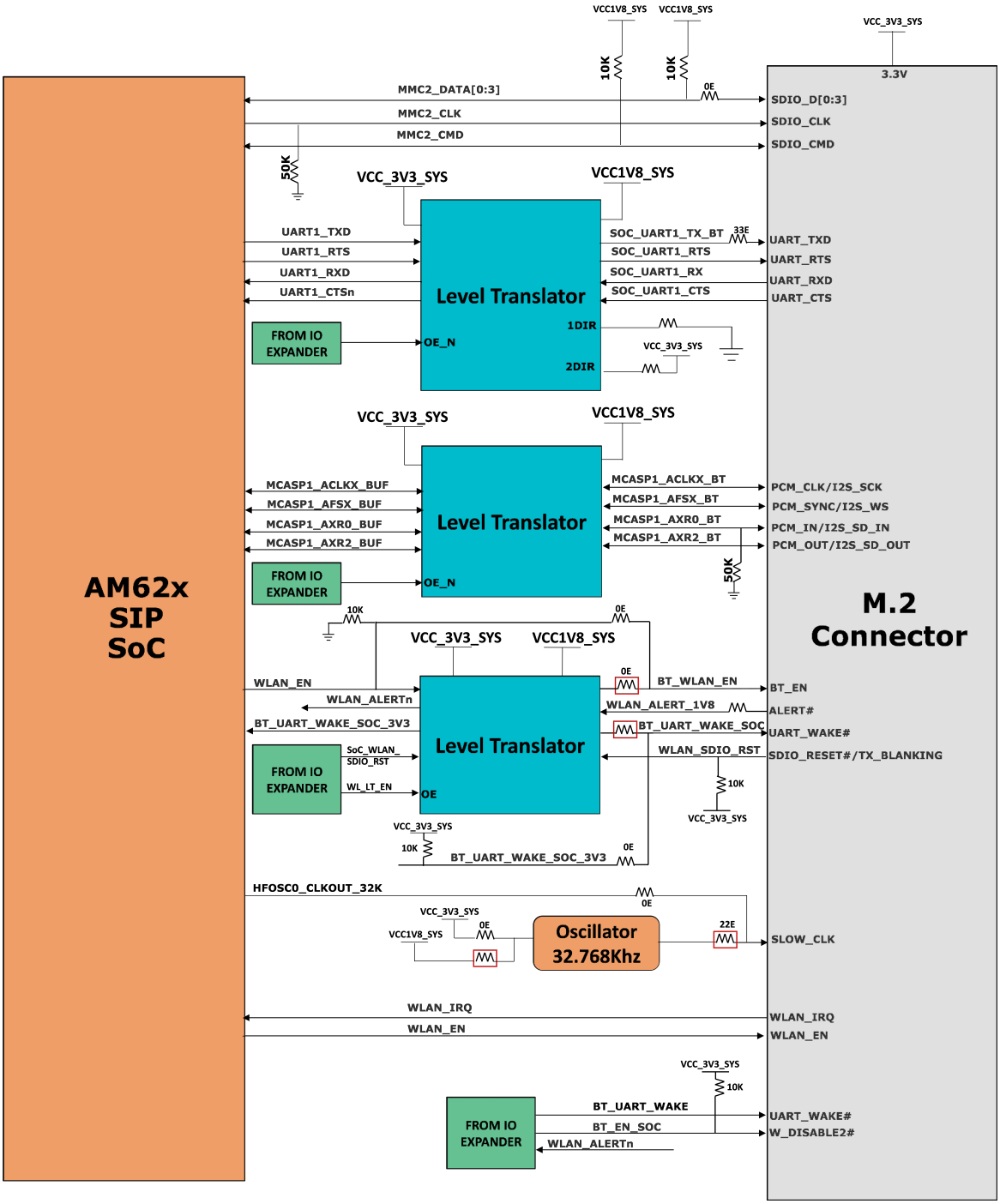

Figure 2-23. Wi-Fi Interface

2.15.3 Board ID EEPROM

AM62x SIP SK EVM boards can be identified remotely from the version and serial number, which are stored on the onboard EEPROM. The EEPROM is accessible from SoC I2C0 port of AM62x SIP SoC.

The Board ID EEPROM I2C address is set to 0x51.

AM62x SIP SK EVM includes an AT24C512C-MAHM-T 512kb EEPROM. The first 259 bytes of memory are preprogrammed with identification information for each board. The remaining 65277 bytes are available to the user for data or code storage.

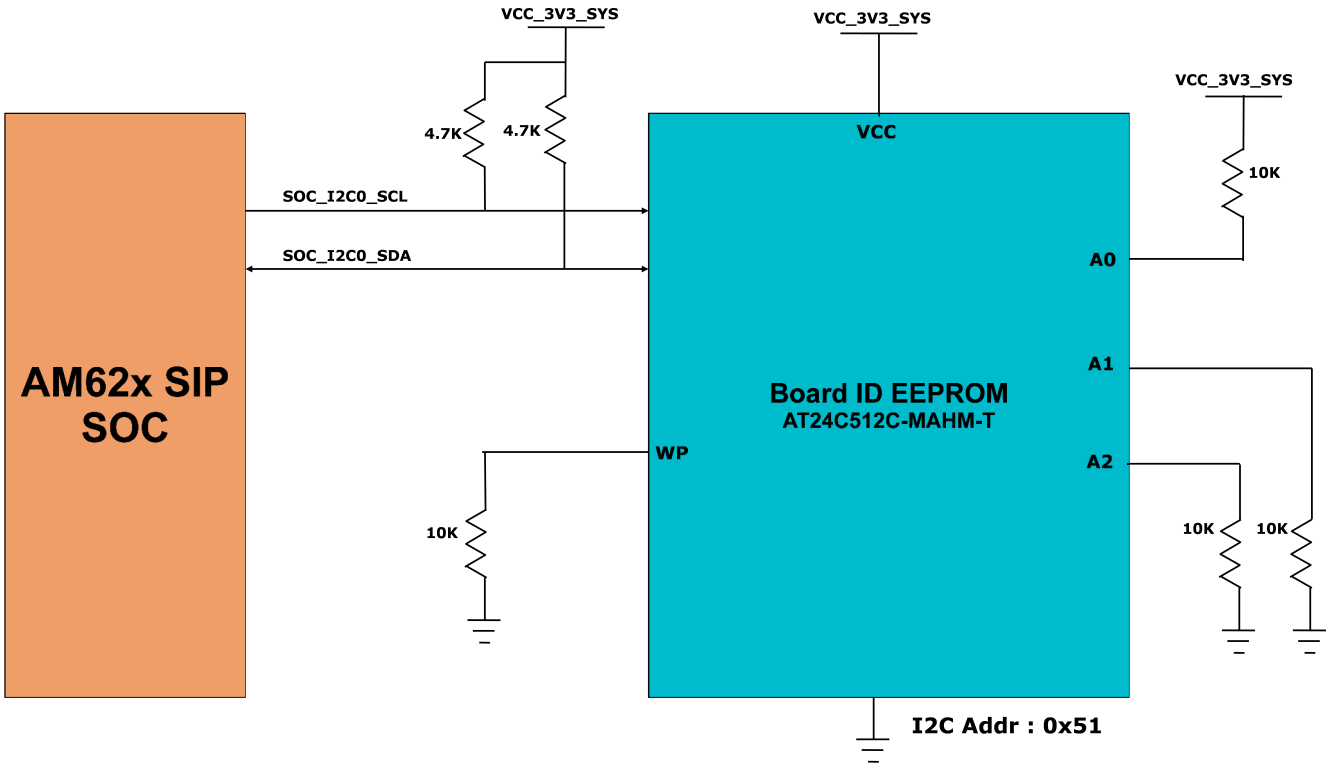

Figure 2-24. Board ID EEPROM

2.16 Ethernet Interface

The AM62x SIP SK EVM offers two Ethernet ports of 1 gigabit speed for external communication. Two channels of RGMII gigabit Ethernet CPSW Ports from AM62x SIP SoC are connected to separate gigabit Ethernet PHY transceivers DP83867, which are finally terminated on two RJ45 connectors with integrated magnetics.

The 48pin version of the PHY DP83867 is configured to advertise 1-Gb operation with the internal delay set to accommodate the internal delay inside the AM62x. CPSW_RGMII1 and CPSW_RGMII2 Ports share a common MDIO Bus to communicate with the external PHY Transceiver.

Two single port RJ45 Connectors Mfr Part# LPJG16314A4NL from Link-PP are used on the board for Ethernet 10/100/1G connectivity. RJ45 Connectors have integrated magnetics and LEDs for indicating 1000BASE-T link as well as receive or transmit activity.

I/O supply to the Ethernet PHY is set 3.3V level.

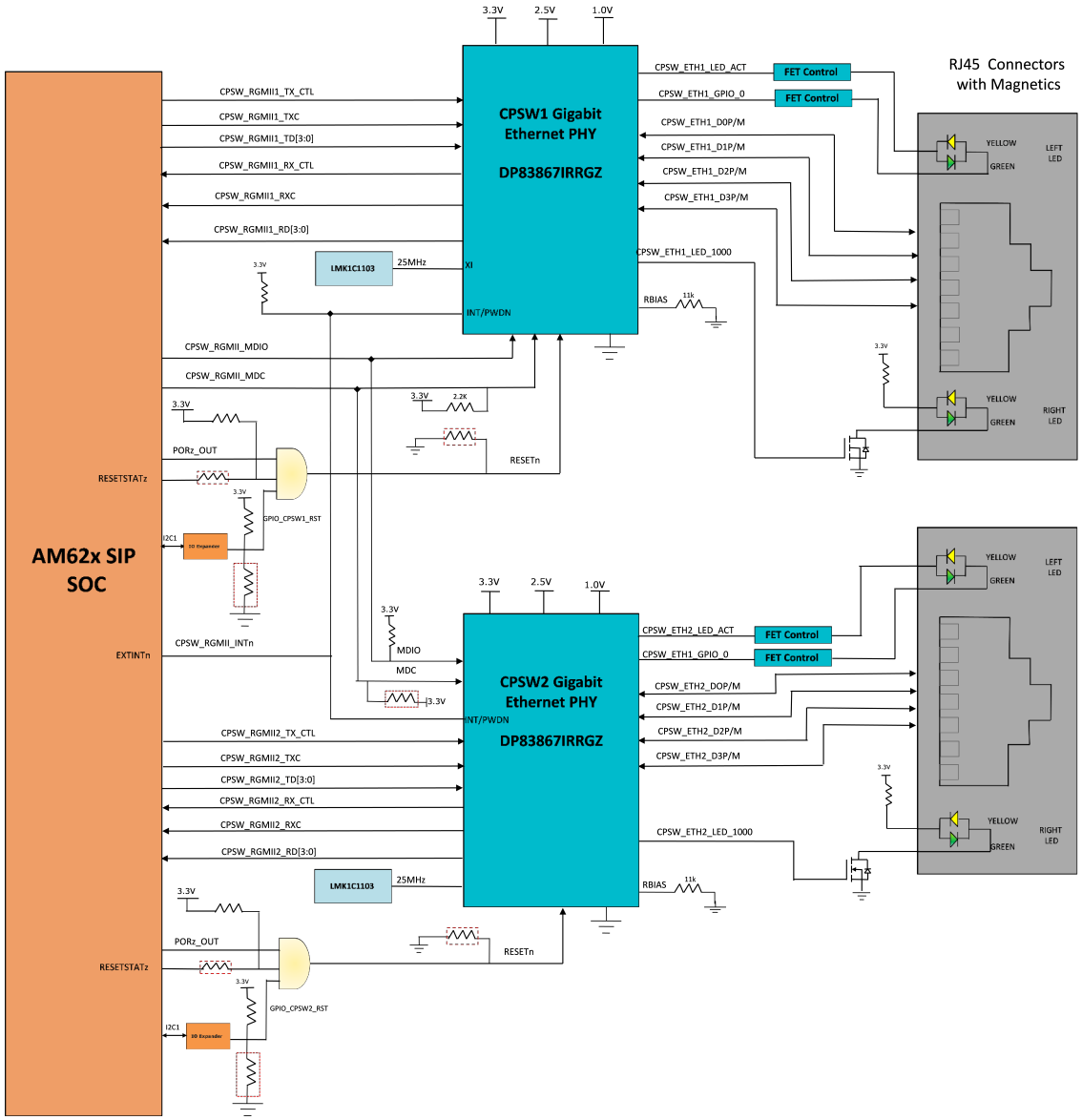

Figure 2-25. Ethernet Interface

2.16.1 CPSW Ethernet PHY 1 Default Configuration

The default configuration of the DP83867 is determined using a number of resistor pull-up and pull-down values on specific pins of the PHY. Depending on the values installed, each of the configuration pins can be set to one of four modes by using the pull up and pull down options provided. The AM62x SIP SK EVM uses the 48-pin QFN package which supports the RGMII interface.

The DP83867 PHY uses four level configurations based on resistor strapping which generate four distinct voltages ranges. The resistors are connected to the RX data and control pins which are normally driven by the PHY and are inputs to the processor. The voltage range for each mode is shown below:

Mode1 - 0V to 0.3V

Mode2 – 0.462V to 0.6303V

Mode3 – 0.7425V to 0.9372V

Mode4 – 2.2902V to 2.9304V

Footprint for both pull-up and pull-down is provided on all the strapping pins except LED_0. LED_0 is for Mirror Enable, which is set to mode 1 by default, Mode 4 is not applicable and Mode2, Mode3 option is not desired.

CPSW_RGMII1 port of the AM62x SIP SoC is connected to DP83867 whose configuration is as given below:

PHYADDR: 00000

Auto_neg: Enabled

ANGsel 10/100/1000

RGMII Clk skew Tx: 2ns

RGMII Clk skew Rx: 2ns

2.16.2 CPSW Ethernet PHY 2 Default Configuration

CPSW_RGMII2 port of the AM62x SIP SoC is connected to DP83867 whose configuration is as given below:

PHYADDR: 00001

Auto_neg: Enabled

ANGsel 10/100/1000

RGMIIClk skew Tx: 2ns

RGMII Clk skew Rx: 2ns

The interrupts generated from two CPSW RGMII PHYs are tied together and is connected to EXTINTn pin of AM62x SIP SoC.

LED1 is connected to RJ45 Right LED (Green) to indicate 1000MHz link.

LED2 is connected to RJ45 Left LED (Yellow) to indicate transmit/receive activity. GPIO_0 is connected to RJ45 Left LED (Green) to indicate 10/100MHz link.

LED Control is achieved through an external MOSFET.

2.17 GPIO Port Expander

The I/O expander used in the AM62x SIP SK EVM is a 24-Bit I2C based I/O expander, which is used for daughtercard plug-in detection and for generating resets and enabling signals to various peripheral devices connected to the I/O expander. The SoC_I2C1 bus of the AM62x SIP SoC is used to interface with the I/O expander. The I2C device address of the I/O expander is 0x21. See the tables below for the list of signals being controlled by the expander.

Table 2-12. IO Expander 1 Signal Details

Pin Number	SIGNAL	DIRECTION	DEVICE
P00	GPIO_CPSW2_RST	OUTPUT	CPSW Ethernet PHY-2 Reset Control GPIO
P01	GPIO_CPSW1_RST	OUTPUT	CPSW Ethernet PHY-1 Reset Control GPIO
P02	PRU_DETECT	INPUT	PRU Board Detection
P03	MMC1_SD_EN	OUTPUT	SD Card Load Switch Enable
P04	VPP_LDO_EN	OUTPUT	SOC eFuse Voltage (VPP=1.8V) Regulator Enable
P05	EXP_PS_3V3_EN	OUTPUT	EXP CONN 3.3V Power Switch Enable
P06	EXP_PS_5V0_EN	OUTPUT	EXP CONN 5V Power Switch Enable
P07	EXP_HAT_DETECT	INPUT	EXP CONN HAT Board Detection
P10	WLAN_ALERT_3V3	OUTPUT	Wi-Fi card alert - M.2 module
P11	BT_UART_WAKE_SOC_3V3	INPUT	BT UART WKUP Signal
P12	UART1_FET_BUF_EN	OUTPUT	SOC UART1 buffer enable
P13	WL_LT_EN	OUTPUT	Enable for Wilink Level Translators
P14	GPIO_HDMI_RSTn	OUTPUT	HDMI Transmitter Reset Control GPIO
P15	CSI_GPIO1	NA	Raspberry Pi Camera CSI0 GPIO1
P16	CSI_GPIO2	NA	Raspberry Pi Camera CSI0 GPIO2
P17	PRU_3V3_EN	OUTPUT	PRU Power Switch Enable
P20	HDMI_INTn	INPUT	HDMI Interrupt
P21	PD_I2C_IRQ	INPUT	Interrupt from PD controller
P22	MCASP1_FET_EN	OUTPUT	MCASP1 Enable and Direction Control
P23	MCASP1_BUF_BT_EN	OUTPUT	
P24	MCASP1_FET_SEL	OUTPUT	
P25	UART1_FET_SEL	OUTPUT	SOC UART1 FET selection
P26	TS_INT#	INPUT	OLDI Display Touch Interrupt
P27	IO_EXP_TEST_LED	OUTPUT	User Test LED 2

Table 2-13. IO Expander 2 Signal Details

Pin Number	SIGNAL	DIRECTION	DEVICE
P0	WLAN_SDIO_RST_3V3	OUTPUT	M.2 Connector SDIO Reset Control GPIO
P1	GPIO_TS_RSTn	OUTPUT	OLDI Display Reset control
P2	GPIO_AUD_RSTn	OUTPUT	Audio Codec Reset Control GPIO
P3	GPIO_eMMC_RSTn	OUTPUT	eMMC Reset control GPIO

2.18 GPIO Mapping

The table below describes the detailed GPIO mapping of AM62x SIP SoC with AM62x SIP SK EVM peripherals.

SL NO.	GPIO DESCRIPTION	GPIO NETNAME	Functionality	GPIO USED	SOC MUXED SIGNAL NAME	DIRECTION WITH RESPECT TO CONTROL	DEFAULT STATE	ACTIVE STATE	VOLTAGE DOMAIN ON SOC SIDE	VOLTAGE CONNECTED ON SKEVM
1	Enable for WLAN Interface	SoC_WLAN_EN_1V8	ENABLE	GPIO0_71	MMC2_SDCD	OUTPUT	LOW	HIGH	VDDSHV6	SoC_DVDD1V8
2	WLAN Interrupt	SoC_WLAN_IRQ_1V8	INTERRUPT	GPIO0_72	MMC2_SDWP	INPUT	HIGH	LOW	VDDSHV6	SoC_DVDD1V8
3	Enable for BT Interface	BT_EN_SOC_3V3	ENABLE	MCU_GPIO0_1	MCU_SPI0_CS0	OUTPUT	HIGH	LOW	VDDSHV_MCU	SoC_DVDD3V3
4	CPSW Ethernet PHY Interrupt PRU Connector Interrupt PMIC_INTn	CPSW_RGMII_INTn/PRU_INTn	INTERRUPT	GPIO1_31	EXTINTn	INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	OSPI Reset Control GPIO	GPIO_OSPI_RSTn	RESET	GPIO0_12	OSPI0_CSn1	OUTPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
6	OSPI Interrupt	OSPI_INTn	INTERRUPT	GPIO0_13	OSPI0_CSn2	INPUT	HIGH	LOW	VDDSHV1	SoC_DVDD1V8
7	SD Card IO Voltage Select	VSEL_SD	ENABLE	GPIO0_31	GPMC0_CLK	OUTPUT	LOW	HIGH	VDDSHV3	SoC_DVDD3V3
8	IO Expander Interrupt	MCU_GPIO0_15	INTERRUPT	MCU_GPIO0_15	MCU_MCAN1_TX	INPUT	HIGH	LOW	VDDSHV_CANUART	SoC_DVDD3V3
9	TEST GPIO1 from Test Automation Connector/ User Interrupt Push Button									
10	User Test LED 1	SOC_GPIO1_49	GPIO	GPIO1_49	MMC1_SDWP	OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 01									
1	CPSW Ethernet PHY-2 Reset Control GPIO	GPIO_CPSW2_RST	RESET	IO EXPANDER - P00		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	CPSW Ethernet PHY-1 Reset Control GPIO	GPIO_CPSW1_RST	RESET	IO EXPANDER - P01		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	PRU Board Detection	PRU_DETECT	DETECTION	IO EXPANDER - P02		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	SD Card Load Switch Enable	MMC1_SD_EN	ENABLE	IO EXPANDER -P03		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
5	SOC eFuse Voltage(VPP=1.8V) Regulator Enable	VPP_LDO_EN	ENABLE	IO EXPANDER - P04		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
6	EXP CONN 3.3V Power Switch Enable	EXP_P5_3V3_EN	ENABLE	IO EXPANDER - P05		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
7	EXP CONN 5V Power Switch Enable	EXP_P5_5V0_EN	ENABLE	IO EXPANDER - P06		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
8	EXP CONN HAT Board Detection	RPI_HAT_DETECT	DETECTION	IO EXPANDER - P07		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
9	M.2 Connector Alert	WLAN_ALERT_3V3	ALERT	IO EXPANDER – P10		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
10	M.2 Connector WAKEUP	BT_UART_WAKE_SOC_3V3	WAKEUP	IO EXPANDER – P11		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
11	SOC UART1 Mux Select	UART1_MUX_SEL	SELECT	IO EXPANDER - P12		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
12	Enable for Wilink Level Translators	WL_LT_EN	ENABLE	IO EXPANDER - P13		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
13	HDMI Transmitter Reset Control GPIO	GPIO_HDMI_RSTn	RESET	IO EXPANDER - P14		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
14	Raspberry Pi Camera CSI0 GPIO1	CSI_GPIO1	INPUT/OUTPUT	IO EXPANDER - P15		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
15	Raspberry Pi Camera CSI0 GPIO2	CSI_GPIO2	INPUT/OUTPUT	IO EXPANDER - P16		NA	NA	NA	VDDSHV0	SoC_DVDD3V3
16	PRU Power Switch Enable	PRU_3V3_EN	ENABLE	IO EXPANDER - P17		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
17	HDMI Interrupt	HDMI_INTn	INTERRUPT	IO EXPANDER - P20		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
18	TEST GPIO2 from Test Automation Connector	TEST_GPIO2	GPIO for communications with AM62x	IO EXPANDER - P21		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
19	MCASP2 Enable and Direction Control	AUD_BUF_EN	ENABLE	IO EXPANDER - P22		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
20		WL_BUF_EN	ENABLE	IO EXPANDER - P23		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
21		AUD_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P24		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
22		WL_BUF_CLK_DIR	DIRECTION CONTROL	IO EXPANDER - P25		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
23	OLDI Display Touch Interrupt	TS_INT#	INTERRUPT	IO EXPANDER - P26		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
24	User Test LED 2	IO_EXP_TEST_LED	GPIO	IO EXPANDER - P27		OUTPUT	LOW	HIGH	VDDSHV0	SoC_DVDD3V3
	IO EXPANDER - 02									
1	M.2 Connector SDIO Reset Control GPIO	WLAN_SDIO_RST_3V3	RESET	IO EXPANDER – P0		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
2	OLDI Display Reset control	GPIO_TS_RSTn	RESET	IO EXPANDER – P1		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
3	Audio Codec Reset Control GPIO	GPIO_AUD_RSTn	DETECTION	IO EXPANDER – P2		INPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3
4	eMMC Reset control GPIO	GPIO_eMMC_RSTn	RESET	IO EXPANDER – P3		OUTPUT	HIGH	LOW	VDDSHV0	SoC_DVDD3V3

Figure 2-26. GPIO Mapping

2.19 OLDI Display Interface

The OLDI0 Display interface of the AM62x SIP SoC is connected to a 40 pin LVDS display connector (J21) Mfr. Part# FFC2A32-40-T from GCT. The OLDI Interface supports dual channel 8-bit LVDS output.

The Pin-out details of the Display connector are given in below table.

Table 2-14. OLDI Display Connector Pinout

Pin No.	Signal	Pin No.	Signal
1	VCC_3V3_SYS (EEPROM_VDD)	21	CH1_LVDS_A2P
2	SoC_I2C0_SCL	22	GND
3	SoC_I2C0_SDA	23	CH1_LVDS_A3N
4	NC	24	CH1_LVDS_A3P
5	NC	25	GND
6	GND	26	CH1_LVDS_A0N
7	GND	27	CH1_LVDS_A0P
8	OLDI_RESETn	28	GND
9	TS_INT#	29	CH2_LVDS_A1N
10	GND	30	CH2_LVDS_A1P
11	CH1_LVDS_A0N	31	GND
12	CH1_LVDS_A0P	32	CH2_LVDS_CLKN
13	GND	33	CH2_LVDS_CLKP
14	CH1_LVDS_A1N	34	GND
15	CH1_LVDS_A1P	35	CH2_LVDS_A2N
16	GND	36	CH2_LVDS_A2P
17	CH1_LVDS_CLKN	37	GND
18	CH1_LVDS_CLKP	38	CH2_LVDS_A3N
19	GND	39	CH2_LVDS_A3P
20	CH1_LVDS_A2N	40	GND

2.20 EVM User Setup/Configuration

2.20.1 EVM DIP Switches

AM62x SIP SK EVM has two 8 - position DIP Switch to set the SoC Boot mode and related parameters.

2.20.2 Boot Modes

The boot mode for the AM62x SIP SK EVM board is defined by two banks of switches SW1 and SW2 or by the I2C buffer connected to the Test automation connector. This allows for AM62x SIP SoC Boot mode control by either the user (DIP Switch Control) or by the Test Automation connector.

All the bits of switch (SW1 and SW2) have weak pull-down resistor and a strong pull up resistor as shown in below picture. Note that OFF setting provides a low logic level (‘0’) and an ON setting provides a high logic level (‘1’).

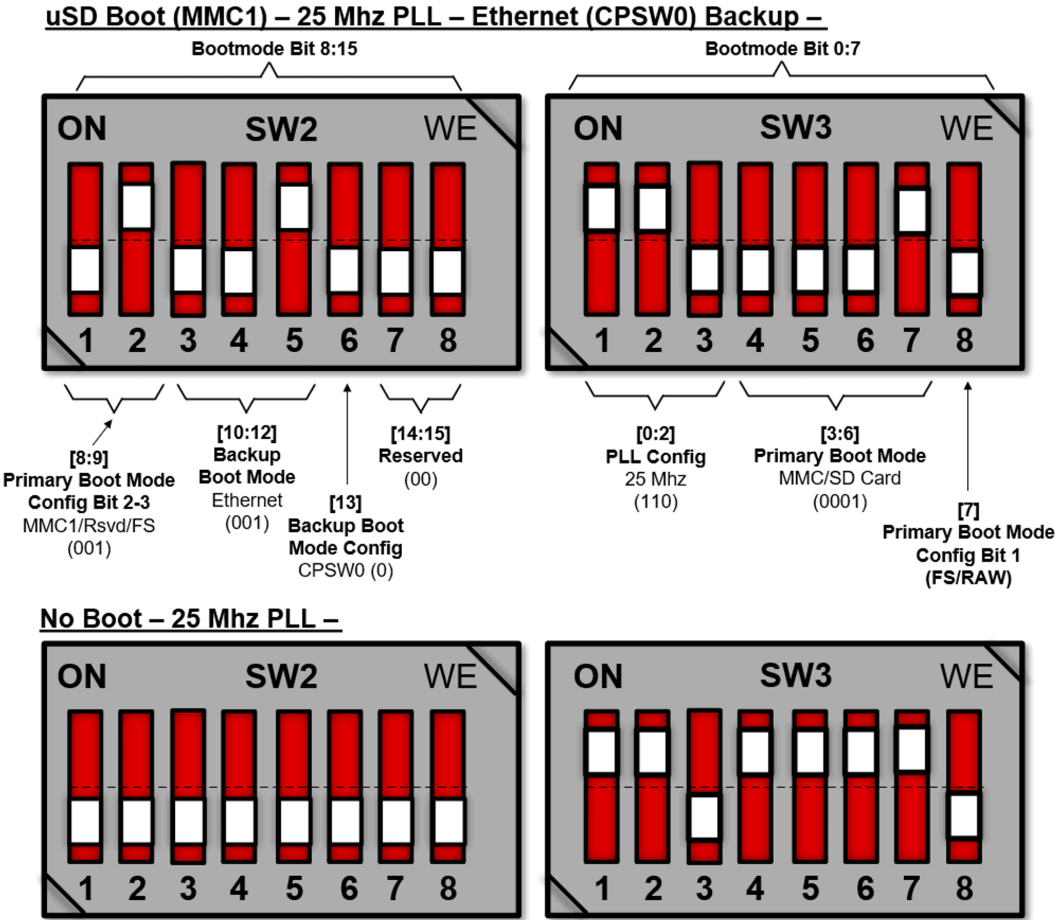

Figure 2-27. Boot Mode Switch Configuration for SD Boot

The boot mode pins of the SoC have associated alternate functions during normal operation. Hence isolation is provided using Buffer IC's to cater for alternate pin functionality. The output of the buffer is connected to the boot mode pins on the AM62x SIP and the output is enabled when the boot mode is needed during a reset cycle.

The input to the buffer is connected to the DIP switch circuit and to the output of an I2C buffer set by the test automation circuit. If the test automation circuit is going to control the bootmode, then all the switches are manually set to the OFF position. The boot mode buffer is powered by an always ON power supply to make sure that the boot mode remains present even if the SoC power is cycled.

Switch SW1 and SW2 bits [15:0] are used to set the SoC Boot mode.

The switch map to the boot mode functions is provided in the tables below.

Table 2-15. Boot Mode Pin Mapping

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Reserved	Reserved	Backup boot mode configuration	Backup boot mode			Primary boot mode configuration			Primary boot mode				PLLConfiguration		

The table below gives details of PLL reference clock selection.

Note

BOOT-MODE[0:2] – Denote system clock frequency for PLL configuration. By default, this bits are set for 25MHz.

Table 2-16. PLL Reference Clock Selection BOOTMODE[2:0]

Bit 2	Bit 1	Bit 0	PLL REF CLK (MHz)
OFF	OFF	OFF	RSVD
OFF	OFF	ON	RSVD
OFF	ON	OFF	24
OFF	ON	ON	25
ON	OFF	OFF	26
ON	OFF	ON	RSVD
ON	ON	OFF	RSVD
ON	ON	ON	RSVD

The table below provides primary boot device selection details.

Note

BOOT-MODE[3:6] – This provides primary boot mode configuration to select the requested boot mode after POR, that is, the peripheral/memory to boot from.

Table 2-17. Boot Device Selection BOOTMODE[6:3]

Bit 6	Bit 5	Bit 4	Bit 3	Primary Boot Device Selected
OFF	OFF	OFF	OFF	Serial NAND
OFF	OFF	OFF	ON	OSPI
OFF	OFF	ON	OFF	QSPI
OFF	OFF	ON	ON	SPI
OFF	ON	OFF	OFF	Ethernet RGMII1
OFF	ON	OFF	ON	Ethernet RMII1
OFF	ON	ON	OFF	I2C
OFF	ON	ON	ON	UART
ON	OFF	OFF	OFF	MMC/SD card
ON	OFF	OFF	ON	eMMC
ON	OFF	ON	OFF	USB0
ON	OFF	ON	ON	GPMC NAND
ON	ON	OFF	OFF	GPMC NOR
ON	ON	OFF	ON	Rsvd
ON	ON	ON	OFF	xSPI
ON	ON	ON	ON	Noboot/Dev Boot

The table below provides backup boot mode selection details.

Note

BOOT-MODE[10:12] – Select the backup boot mode, that is, the peripheral/memory to boot from, if primary boot device failed.

Table 2-18. Backup Boot Mode Selection BOOTMODE[12:10]

Bit 12	Bit 11	Bit 10	Backup Boot Device Selected
OFF	OFF	OFF	None (no backup mode)
OFF	OFF	ON	USB
OFF	ON	OFF	Reserved
OFF	ON	ON	UART
ON	OFF	OFF	Ethernet
ON	OFF	ON	MMC/SD

Table 2-18. Backup Boot Mode Selection BOOTMODE[12:10] (continued)

Bit 12	Bit 11	Bit 10	Backup Boot Device Selected
ON	ON	OFF	SPI
ON	ON	ON	I2C

The table below gives primary boot media configuration details.

Note

BOOT-MODE[9:7] – These pins provide optional settings and are used in conjunction with the primary boot device selected.

Table 2-19. Primary Boot Media Configuration BOOTMODE[9:7]

Bit 9	Bit 8	Bit 7	Boot Device
Reserved	Read Mode 2	Read Mode 1	Serial NAND
Speed	Iclk	Csel	OSPI
Reserved	Iclk	Csel	QSPI
Reserved	Mode	Csel	SPI
Clkout	Delay	Link Stat	Ethernet RGMII
Clkout	Clksrc	Reserved	Ethernet RMII
BusReset	Reserved	Addr	I2C
Reserved		Reserved	UART
Port	Reserved	Fs/raw	MMC/ SD card
Reserved		Voltage	eMMC
Reserved	Mode	Lane Swap	USB0
Reserved			GPMC NAND
Reserved			GPMC NOR
Reserved			Reserved
SFDP	Read Cmd	Mode	xSPI
Reserved		No/Dev	Noboot/Dev Boot

Table 2-20. Serial NAND Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW2.1]	Read Mode 2	0	Reserved (Read mode is taken from Read Mode 1
		1	SPI/ 1-1-1 mode (Read mode is taken from Read Mode 2 and Read Mode 1 is ignored)
7 [SW1.8]	Read Mode 1	0	OSPI/ 1-1-8 Mode (valid only when Read Mode 2 is 0)
		1	OSPI/ 1-1-4 Mode (valid only when Read Mode 2 is 0)

Table 2-21. OSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW2.1]	Iclk	0	Iclock source external
		1	Iclock source internal (pad loopback)
7 [SW1.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-22. QSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW2.1]	Iclk	0	Iclock source external
		1	Iclock source internal (pad loopback)
7 [SW1.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-23. SPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
8 [SW2.1]	Mode	0	SPI Mode 0
		1	SPI Mode 3
7 [SW1.8]	Csel	0	Boot Flash is on CS 0
		1	Boot Flash is on CS 1

Table 2-24. Ethernet RGMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	Clkout	0	25MHz clock not generated on CLKOUT0
		1	25MHz clock generated on CLKOUT0
8 [SW2.1]	Delay	0	Must be set to 0 for RGMII with internal Tx delay
		1	Reserved
7 [SW1.8]	Link info	0	MDIO PHY scan used for link parameters
		1	Link parameters programmed by the ROM

Table 2-25. Ethernet RMII Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	Clkout	0	50MHz clock not generated on CLKOUT0
		1	50MHz clock generated on CLKOUT0
8 [SW2.1]	Clk src	0	External clock source for RMII1_REF_CLK
		1	Internal clock source for RMII1_REF_CLK
7 [SW1.8]	RMII	0	This bit must be set to 0
		1	Reserved

Table 2-26. Ethernet RMII Clocking

BOOTMODE Pin 9 (Clk out)	BOOTMODE Pin 8 (Clk src)	Description
0	0	50MHz external source to RMII_REF_CLK and to external Ethernet PHY input clock (CLKOUT0 is unused) These are the recommended settings
0	1	Not a valid configuration
1	0	CLKOUT0 is configured to 50MHz and connect to both RMII1_REF_CLK and to external Ethernet PHY input clock
1	1	Not a valid configuration

Table 2-27. Ethernet Backup Boot Configuration Field

BOOTMODE Pins	Field	Value	Description
13 [SW2.2]	Interface	0	RGMII with internal TX delay
		1	RMII with external clock source

Table 2-28. I2C Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	Bus reset	0	Hung bus reset attempt after 1ms
		1	No hung bus reset attempted
7 [SW1.8]	Address	0	EEPROM's address is 0x50
		1	EEPROM's address is 0x51

Table 2-29. SD Card Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2] 13[(1)] [SW2.2]	Port	0	Reserved
		1	MMC Port 1 (4 bit width). This bit must be set to 1

Table 2-29. SD Card Boot Configuration Fields (continued)

BOOTMODE Pins	Field	Value	Description
7 [SW1.8]	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode

Table 2-30. eMMC Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2] 13(1) [SW2.2]	Port	0	MMCSD Port 0 (8 bit width). This bit must be set to 0
		1	Reserved
7 [SW1.8]	FS/Raw	0	Filesystem mode
		1	Raw Mode

(1) When MMCSD is the backup mode

Table 2-31. USB Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	Core Voltage	0	0.85V core voltage
		1	0.75V core voltage
8 [SW2.1] 13(1) [SW2.2]	Mode	0	DFU (USB device firmware upgrade)
		1	Host (MSC boot)
7 [SW1.8]	Lane Swap	0	D+/D- lines are not swapped
		1	D+/D- lines are swapped

(1) When USB is the backup mode.

Table 2-32. xSPI Boot Configuration Fields

BOOTMODE Pins	Field	Value	Description
9 [SW2.2]	SFDP	0	SFDP disabled
		1	SFDP enabled
8 [SW2.1]	Read cmd	0	0x0B Read Command
		1	0xEE Read Command
7 [SW1.8]	Mode	0	1S-1S-1S mode @ 50MHz
		1	8D-8D-8D mode @ 25MHz

The table below provides backup boot media configuration options.

Note

- BOOT-MODE[13] – These pins provide optional settings and are used in conjunction with the backup boot device devices. Switch SW2.6 when ON sets 1 and sets 0 if OFF, see the device-specific TRM.
- BOOT-MODE[14:15] – Reserved.

Table 2-33. Backup Boot Media Configuration BOOTMODE[13]

Bit 13	Boot Device
Reserved	None
Mode	USB
Reserved	Reserved
Reserved	UART
IF	Ethernet
Port	MMC/SD
Reserved	SPI
Reserved	I2C

2.20.3 User Test LEDs

The AM62x SIP SK EVM board contains two LEDs for user defined function.

The table below indicates the user test LEDs and the associated GPIOs used to control the user test LEDs.

Table 2-34. User Test LEDs

Sl.No.	LED	GPIO Used	SCH Net Names
1	LD1	GPIO1_49	SOC_GPIO1_49
2	LD11	U70.24(P27)	IO_EXP_TEST_LED

2.21 Expansion Headers

AM62x SIP SK EVM features three expansion Headers, a 40 pin User expansion connector, 20 pin PRU Header and a 28 pin MCU Header.

2.21.1 PRU Connector

AM62x SIP SK EVM has a 20 pin PRU Header which offers Low speed connection to the PRG0 Interface.

PRU_ICSSG signals from PRG0 Port (PRG0_PRU0) are connected to a 10x2 standard 0.1” spaced Receptacle connector Mfr Part # PREC010DAAN-RC. The connector features PR0_PRU0_GPO [0: 7], SoC_I2C0, +3.3V PWR and Ground reference. INTn signal from PRU Header is wired along with the CPSW PHY interrupts and connected to the EXTINTn pin of the SoC.

The 3.3V supply is current limited to 500mA. This is achieved by using load switch TPS22902YFPR. Enable for the load switch is controlled by IO expander. Signals routed from the PRU Connector are listed in the table below.

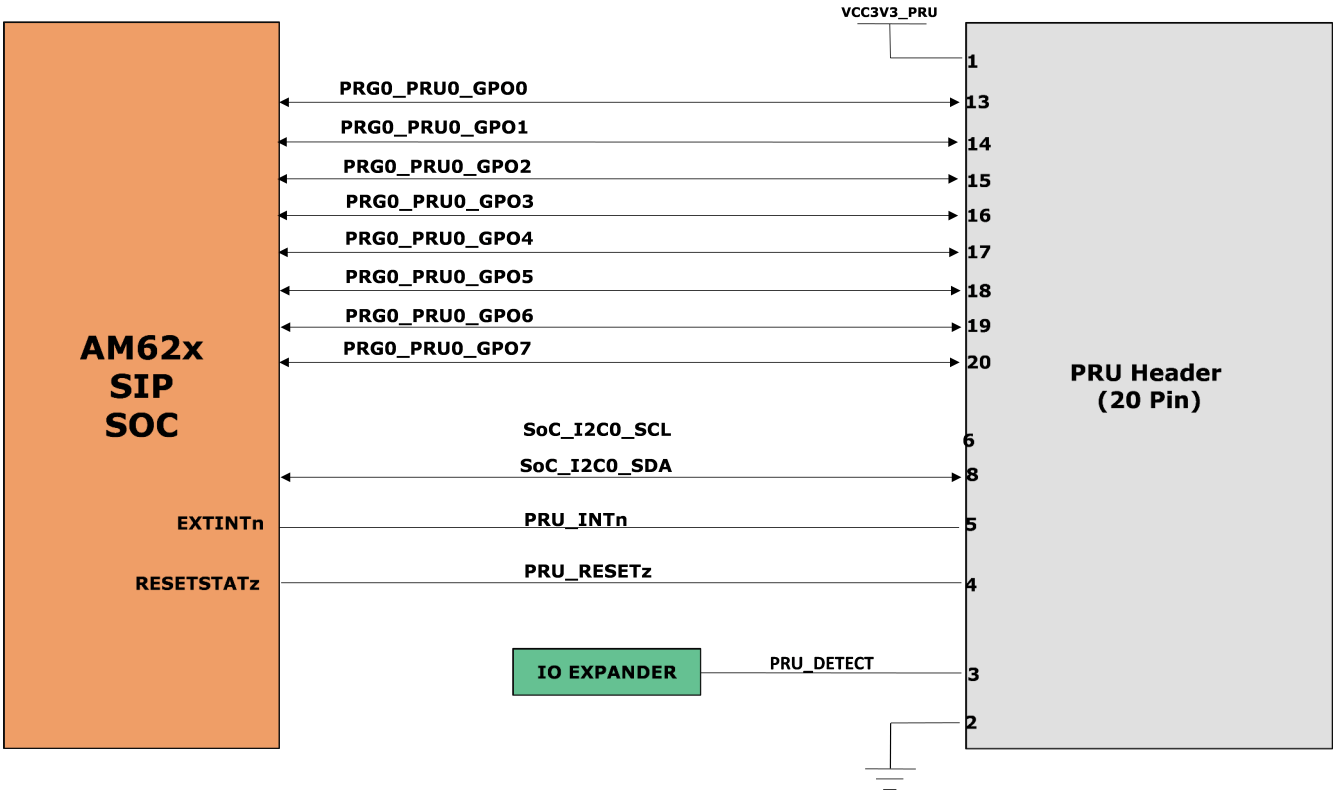

Figure 2-28. PRU Header (J10) Pin-Out

Pin Number	SoC Ball No.	Netname	Pin Multiplexed Signal
1	-	VCC3V3_PRU	
2	-	DGND	
3	-	PRU_DETECT	
4	F22	PRU_RESETz	RESETSTATz
5	D16	PRU_INTn	EXTINTn/ GPIO1_31
6	B16	SoC_I2C0_SCL	I2C0_SCL/ PR0_IEP0_EDIO_DATA_IN_OUT30/ SYNC0_OUT/ OBSCLK0/ UART1_DCDn/ EQEP2_A EHRPWM_SOCA/ GPIO1_26/ ECAP1_IN_APWM_OUT / SPI2_CS0
7	-	NC	
8	A16	SoC_I2C0_SDA	I2C0_SDA/ PR0_IEP0_EDIO_DATA_IN_OUT31/ SPI2_CS2/ TIMER_IO5/ UART1_DSRn/ EQEP2_B/ EHRPWM_SOCB/ GPIO1_27/ ECAP2_IN_APWM_OUT
9		NC	
10	-	NC	
11	-	NC	
12	-	NC	
13	M25	PR0_PRU0_GPO0	GPMC0_AD0/ PR0_PRU1_GPO8/ PR0_PRU1_GPI8/ MCASP2_AXR4/ PR0_PRU0_GPO0/PR0_PRU0_GPI0/ TRC_CLK/ GPIO0_15/ DDR0_IO_PLL_TESTOUT0P/ DDR0_IO_PLL_TESTOUT1P/ GPIO1_112/ LED_DIO0
14	N23	PR0_PRU0_GPO1	GPMC0_AD1/ PR0_PRU1_GPO9/ PR0_PRU1_GPI9/ MCASP2_AXR5/ PR0_PRU0_GPO1/PR0_PRU0_GPI1/ TRC_CTL/ GPIO0_16/ DDR0_IO_PLL_REFCLK_TEST0P/ DDR0_IO_PLL_REFCLK_TEST1P/ GPIO1_113/ LED_DIO1
15	N24	PR0_PRU0_GPO2	GPMC0_AD2/ PR0_PRU1_GPO10/ PR0_PRU1_GPI10/ MCASP2_AXR6/ PR0_PRU0_GPO2/ PR0_PRU0_GPI2/ TRC_DATA0/ GPIO0_17
16	N25	PR0_PRU0_GPO3	GPMC0_AD3/PR0_PRU1_GPO11/ PR0_PRU1_GPI11/MCASP2_AXR7/ PR0_PRU0_GPO3/ PR0_PRU0_GPI3/ TRC_DATA1/GPIO0_18
17	P24	PR0_PRU0_GPO4	GPMC0_AD4/PR0_PRU1_GPO12/ PR0_PRU1_GPI12/MCASP2_AXR8/ PR0_PRU0_GPO4/PR0_PRU0_GPI4/ TRC_DATA2/GPIO0_19
18	P22	PR0_PRU0_GPO5	GPMC0_AD5/PR0_PRU1_GPO13/ PR0_PRU1_GPI13/MCASP2_AXR9/ PR0_PRU0_GPO5/PR0_PRU0_GPI5/ TRC_DATA3/GPIO0_20
19	P21	PR0_PRU0_GPO6	GPMC0_AD6/PR0_PRU1_GPO14/ PR0_PRU1_GPI14/MCASP2_AXR10/ PR0_PRU0_GPO6/PR0_PRU0_GPI6/ TRC_DATA4/GPIO0_21
20	R23	PR0_PRU0_GPO7	GPMC0_AD7/PR0_PRU1_GPO15/ PR0_PRU1_GPI15/MCASP2_AXR11/ PR0_PRU0_GPO7/ PR0_PRU0_GPI7/ TRC_DATA5/GPIO0_22

2.21.2 User Expansion Connector

The AM62x SIP SK EVM supports RPi expansion interface using a 40-pin User expansion connector Mfr. Part# PEC20DAAN. Four mounting holes must be oriented with the connector to allow for connection of these boards.

Following interfaces and IOs shall be included on to the 40 pin User Expansion connector.

- 2x SPI: SPI0 with 2 CS and SPI2 with 3 CS
- 2x I2C: SoC_I2C0 and SoC_I2C2
- 1x UART: UART5
- 2x PWM: EHRPWM0_A, EHRPWM1_B
- 1x CLK: CLKOUT0
- 9x GPI0: GPIOs from main domain
- 5V and 3.3V supply (current limited to 155mA and 500mA)

Each of the power supplies, 5V and 3.3V, are limited to 155mA and 500mA, respectively. This is achieved by using two individual load switch TPS22902YFPR and TPS22946YZPR. Enable for the load switches is driven by I2C based GPIO Port expander.

Signals routed from user expansion connector are listed in the table below.

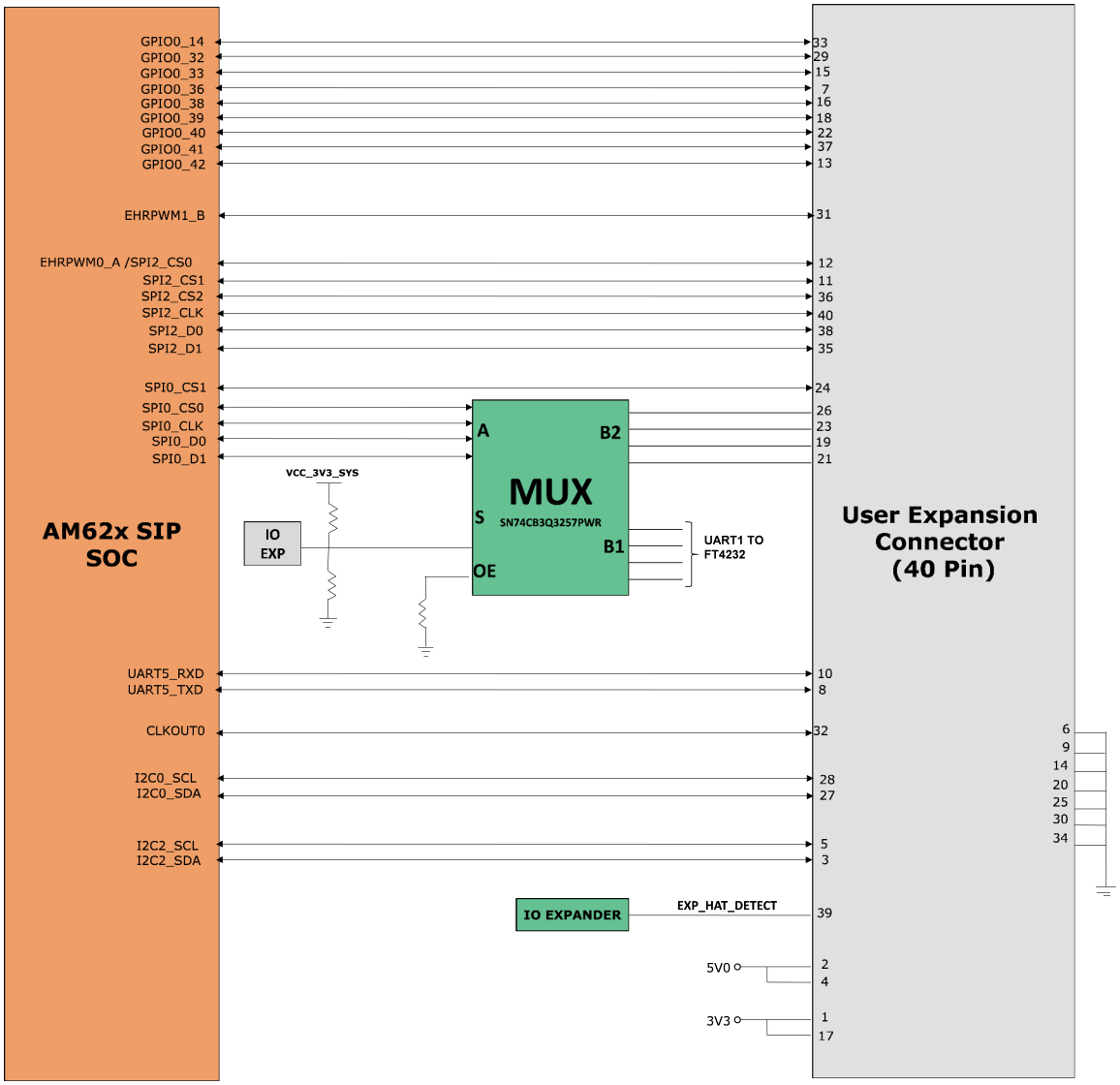

Figure 2-29. Expansion Connector

Pin Number	SoCBall	Net Name	Pin Multiplexed Signals
1	-	VCC3V3_EXP	
2	-	VCC5V0_EXP	
3	K24	SoC_I2C2_SDA	GPMC0_CSN3/ GPMC0_A20/ UART4_TXD/MCASP1_AXR5/ TRC_DATA18/ GPIO0_44/ MCASP1_ACLKR
4	-	VCC5V0_EXP	
5	K22	SoC_I2C2_SCL	GPMC0_CSN2/MCASP1_AXR4/ UART4_RXD/ PR0_PRU0_GPO19/ PR0_PRU0_GPI19/ TRC_DATA17/ GPIO0_43/ MCASP1_AFSR
6	-	DGND	
7	A18	EXP_CLKOUT0	EXT_REFCLK1/ SYNC1_OUT/ SPI2_CS3/SYSCLKOUT0/ TIMER_IO4/ CLKOUT0/ CP_GEMAC_CPTS0_RFT_CLK/ GPIO1_30/ ECAP0_IN_APWM_OUT
8	E15	EXP_UART5_TXD	UART5_TXD/ TIMER_IO3/ SYNC3_OUT/UART1_RIn/ EQEP2_S/ PR0_UART0_TXD/ GPIO1_25/ MCASP2_AXR1/ EHRPWM_TZn_IN4
9	-	DGND	
10	C15	EXP_UART5_RXD	UART5_RXD/ TIMER_IO2/ SYNC2_OUT/UART1_DTRn/ EQEP2_I/ PR0_UART0_RXD/ GPIO1_24/ MCASP2_AXR0/ EHRPWM_TZn_IN3
11	B20	EXP_SPI2_CS1	MCASP0_ACLKX/ SPI2_CS1/ ECAP2_IN_APWM_OUT/ GPIO1_11/ EQEP1_A
12	E19	EXP_SPI2_CS0/EHRPWM0_A	MCASP0_AFSR/SPI2_CS0/ UART1_RXD/ EHRPWM0_A/ GPIO1_13/ EQEP1_S
13	L21	EXP_GPIO0_42	GPMC0_CSn1/ PR0_PRU1_GPO16/ PR0_PRU1_GPI16/ MCASP2_AXR15/ PR0_PRU0_GPO18/ PR0_PRU0_GPI18/ TRC_DATA16/ GPIO0_42
14	-	DGND	
15	L23	EXP_GPIO0_32	GPMC0_ADVn_ALE/ MCASP1_AXR2/ PR0_PRU0_GPO9/ PR0_PRU0_GPI9/ TRC_DATA7/ GPIO0_32
16	V25	EXP_GPIO0_38	GPMC0_WAIT1/ VOUT0_EXTPCLKIN/ GPMC0_A21/ UART6_RXD/ GPIO0_38/ EQEP2_I
17	-	VCC3V3_EXP	
18	K25	EXP_GPIO0_39	GPMC0_WPn/ AUDIO_EXT_REFCLK1/ GPMC0_A22/ UART6_TXD/ PR0_PRU0_GPO15/ PR0_PRU0_GPI15/ TRC_DATA13/ GPIO0_39

Pin Number	SoCBall	Net Name	Pin Multiplexed Signals
19	B13	EXP_SPI0_D0	SPI0_D0/ CP_GEMAC_CPTS0_HW1TSPUSH/ EHRPWM1_B/ GPIO1_18
20	-	DGND	
21	B14	EXP_SPI0_D1	SPI0_D1/ CP_GEMAC_CPTS0_HW2TSPUSH/ HRPWM_TZn_IN0/ GPIO1_19
22	E24	EXP_GPIO0_14	OSPI0_CSn3/ OSPI0_RESET_OUT0/ OSPI0_ECC_FAIL/ MCASP1_ACLKR/ MCASP1_AXR3/ UART5_TXD/ GPIO0_14
23	A14	EXP_SPI0_CLK	SPI0_CLK/ CP_GEMAC_CPTS0_TS_SYNC/ EHRPWM1_A/ GPIO1_17
24	A13	EXP_SPI0_CS0	SPI0_CS0/ EHRPWM0_A/ PR0_ECAP0_SYNC_IN/ GPIO1_15
25	-	DGND	
26	C13	EXP_SPI0_CS1	SPI0_CS1/ CP_GEMAC_CPTS0_TS_COMP/EHRPWM0_B/ ECAP0_IN_APWM_OUT/ GPIO1_16/ EHRPWM_TZn_IN5
27	A16	SoC_I2C0_SDA	I2C0_SDA/ PR0_IEP0_EDIO_DATA_IN_OUT31/ SPI2_CS2/ TIMER_IO5/ UART1_DSRn/EQEP2_B/ EHRPWM_SOCB/ GPIO1_27/ ECAP2_IN_APWM_OUT
28	B16	SoC_I2C0_SCL	I2C0_SCL/ PR0_IEP0_EDIO_DATA_IN_OUT30/ SYNC0_OUT/ OBSCLK0/ UART1_DCDn/EQEP2_A EHRPWM_SOCA/ GPIO1_26/ ECAP1_IN_APWM_OUT / SPI2_CS0
29	N20	EXP_GPIO0_36	GPMC0_BE1n/ MCASP2_AXR12/ PR0_PRU0_GPO13/ PR0_PRU0_GPI13/ TRC_DATA11/ GPIO0_36
30	-	DGND	
31	L24	EXP_GPIO0_33	GPMC0_OEn_REn/ MCASP1_AXR1/ PR0_PRU0_GPO10/ PR0_PRU0_GPI10/ TRC_DATA8/ GPIO0_33
32	M22	EXP_GPIO0_40/ PR0_ECAP0_IN_APWM_OUT	GPMC0_DIR/ PR0_ECAP0_IN_APWM_OUT/ MCASP2_AXR13/ PR0_PRU0_GPO16/ PR0_PRU0_GPI16/ TRC_DATA14/ GPIO0_40/ EQEP2_S

Pin Number	SoCBall	Net Name	Pin Multiplexed Signals
33	E18	EXP_EHRPWM1_B	MCASP0_AXR0/ PR0_ECAP0_IN_APWM_OUT/ AUDIO_EXT_REFCLK0/ PR0_UART0_TXD/ EHRPWM1_B/ GPIO1_10/ EQEP0_I
34	-	DGND	
35	A19	EXP_SPI2_D1/ ECAP2_IN_APWM_OUT	MCASP0_AXR2/ SPI2_D1/ UART1_RTSn/UART6_TXD/ PR0_IEP0_EDIO_DATA_IN_OUT 29/ ECAP2_IN_APWM_OUT/ PR0_UART0_TXD/ GPIO1_8/ EQEP0_B
36	B18	EXP_SPI2_CS2	MCASP0_AXR1/ SPI2_CS2/ ECAP1_IN_APWM_OUT/ PR0_UART0_RXD/ EHRPWM1_A/ GPIO1_9/ EQEP0_S
37	M21	EXP_GPIO0_41	GPMC0_CSn0/ MCASP2_AXR14/ PR0_PRU0_GPO17/ PR0_PRU0_GPI17/ TRC_DATA15/ GPIO0_41
38	B19	EXP_SPI2_D0	MCASP0_AXR3/ SPI2_D0/ UART1_CTSn/UART6_RXD/ PR0_IEP0_EDIO_DATA_IN_OUT 28/ ECAP1_IN_APWM_OUT/ PR0_UART0_RXDGPIO1_7 EQEP0_A
39	-	EXP_HAT_DETECT	
40	A20	EXP_SPI2_CLK	MCASP0_ACLKR/SPI2_CLK/ UART1_TXD/ EHRPWM0_B/ GPIO1_14/ EQEP1_I

2.21.3 MCU Connector

AM62x SIP SK EVM has a 14x2 standard 0.1 inch spaced MCU connector which includes signals connected to the MCU Domain of SoC. 13 Signals include MCU_I2C0, MCU_UART0 (with flow control), MCU_SPI0 and MCU_MCAN0 signals are connected to the MCU Header. Additional control signals provided on the Header include CONN_MCU_RESETz, CONN_MCU_PORz, MCU_RESETSTATz, MCU_SAFETY_ERRORn, 3.3V IO and GND. MCU_UART0 signals from AM62x SoC are connected to both MCU Header and FT4232 Bridge through MUX Mfr Part # SN74CB3Q3257PWR. The MCU header does not include the board ID memory interface. The allowed current limit is 100mA on 3.3V rail.

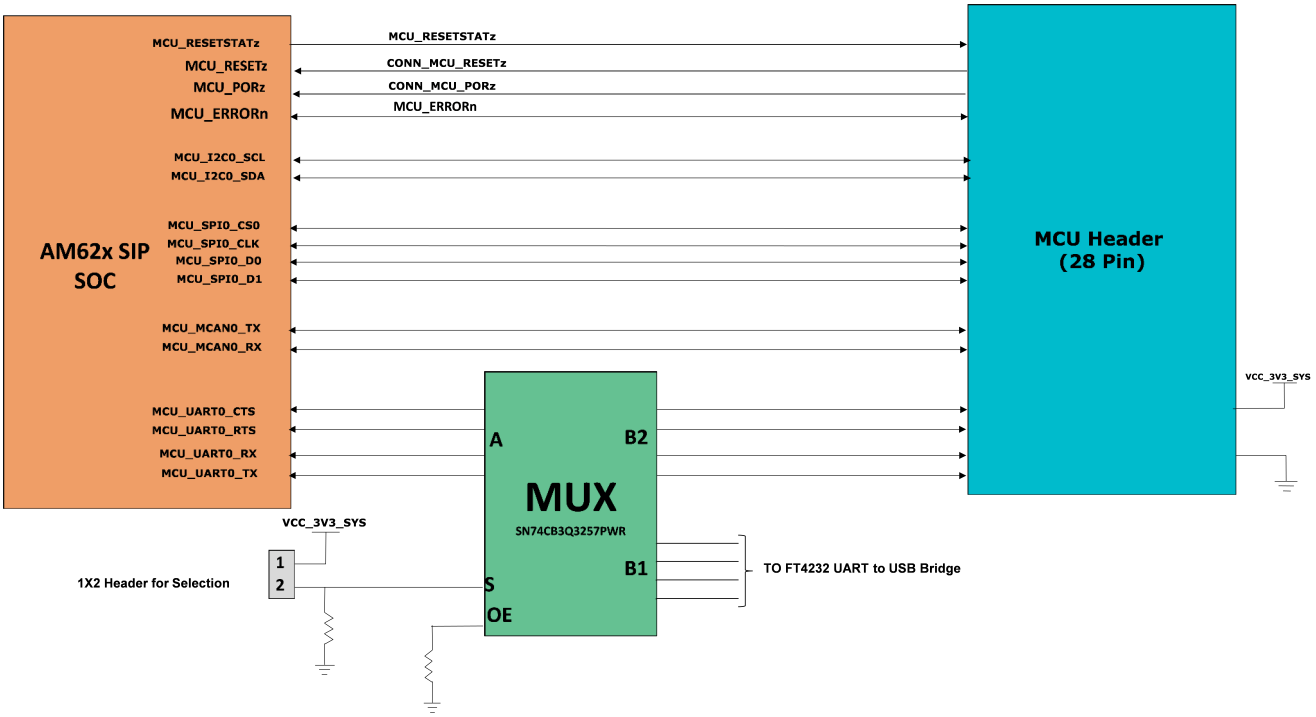

Figure 2-30. MCU Interface

Table 2-35. MCU Connector (J9) Pinout

Pin Number	SoCBall No	Net Name	Pin Multiplexed Signal
1	-	VCC_3V3_SYS	
2	-	DGND	
3	-	NC	
4	C9	MCU_SPI0_D1	MCU_SPI0_D1/MCU_GPIO0_4
5	-	NC	
6	D9	MCU_SPI0_D0	MCU_SPI0_D0/MCU_GPIO0_3
7	-	DGND	
8	B8	MCU_SPI0_CS1	MCU_SPI0_CS1/ MCU_OBSCLK0/ MCU_SYSCLKOUT0/ MCU_EXT_REFCLK0/ MCU_TIMER_IO1/ MCU_GPIO0_1
9	-	NC	
10	E5	MCU_GPIO0_15	MCU_MCAN1_TX/ MCU_TIMER_IO2/ MCU_SPI1_CS1/ MCU_EXT_REFCLK0/ MCU_GPIO0_15

Table 2-35. MCU Connector (J9) Pinout (continued)

Pin Number	SoCBall No	Net Name	Pin Multiplexed Signal
11	D4	MCU_GPIO0_16	MCU_MCAN1_RX/ MCU_TIMER_IO3/ MCU_SPI0_CS2/ MCU_SPI1_CS2/ MCU_SPI1_CLK/ MCU_GPIO0_16
12	A6	MCU_UART0_CTS_CONN	MCU_UART0_CTSn/ MCU_TIMER_IO0/ MCU_SPI1_D0/MCU_GPIO0_7
13	B5	MCU_UART0_RXD_CONN	MCU_UART0_RXD/ MCU_GPIO0_5
14	-	NC	
15	-	DGND	
16	D6	MCU_MCAN0_TX	MCU_MCAN0_TX/ WKUP_TIMER_IO0/ MCU_SPI0_CS3/ MCU_GPIO0_13
17	B6	MCU_UART0_RTS_CONN	MCU_UART0_RTSn/ MCU_TIMER_IO1/ MCU_SPI1_D1/MCU_GPIO0_8
18	A7	MCU_SPI0_CLK	MCU_SPI0_CLK/MCU_GPIO0_2
19	A5	MCU_UART0_TXD_CONN	MCU_UART0_TXD/ MCU_GPIO0_6
20	-	DGND	
21	D10	MCU_I2C0_SDA	MCU_I2C0_SDA/ MCU_GPIO0_18
22	B3	MCU_MCAN0_RX	MCU_MCAN0_RX/ MCU_TIMER_IO0/ MCU_SPI1_CS3/ MCU_GPIO0_14
23	B12	MCU_RESETSTATz	MCU_RESETSTATz/ MCU_GPIO0_21
24	A8	MCU_I2C0_SCL	MCU_I2C0_SCL/ MCU_GPIO0_17
25	E11	CONN_MCU_RESETz	MCU_RESETz
26	D1	MCU_SAFETY_ERRORz_3V3	MCU_ERRORN
27	-	DGND	
28	D2	CONN_MCU_PORz	MCU_PORz

2.22 Interrupt

AM62x SIP SK EVM supports two interrupts for providing Reset input and User Interrupt to the processor. The interrupt are push buttons placed on the Top side of the Board and are listed in below table.

Table 2-36. EVM Push Buttons

SL. Number	Push Buttons	Signal	Function
1	SW3	SoC_WARM_RESETZ	Main domain Warm Reset input
2	SW4	GPIO_INT_SoC	Generates interrupt on GPIO1_23

2.23 I2C Address Mapping

There are three I2C interfaces used in AM62x SIP SK EVM board:

- SoC I2C 0 Interface: SoC I2C [0] is connected to Board ID EEPROM, User Expansion Connector Header, USB PD controller, PRU header, and OLDI Display Touch interface.
- SoC I2C 1 Interface: SoC I2C [1] is connected to Test Automation Header, Current Monitors, Temperature Sensors, Audio Codec, HDMI Transmitter, CSI Camera Connector, GPIO Port Expander.
- SoC I2C 2 Interface: Connected I2C [2] from SoC to the User Expansion Connector Header.
- MCU I2C 0 Interface: Connected MCU I2C [0] to MCU Header.
- WKUP I2C 0 Interface: Connected I2C [0] from SoC to LED Drive.

Table 2-37. I2C Mapping Table

I2C Port	Device/Function	Part Number	I2CAddress
SoC_I2C0	Board ID EEPROM	AT24C512C-MAHM-T	0x51
SoC_I2C0	User Expansion Connector	<connector interface>	
SoC_I2C0	USB PD Controller	TPS65988DHRSHR	0x38, 0x3F
SoC_I2C0	PRU Header	<connector interface>	
SoC_I2C0	OLDI Display Touch Interface		
SoC_I2C1	Test Automation Header	<connector interface>	
SoC_I2C1	Current Monitors	INA231AIYFDR	0x40, 0x47, 0x45, 0x4D& 0x4C
SoC_I2C1	Temperature Sensors	TMP100NA/3K	0x48
SoC_I2C1	Audio Codec	TLV320AIC3106IRGZT	0x1B
SoC_I2C1	HDMI Transmitter	SiI9022ACNU	0x3B, 0x3F, 0x62
SoC_I2C1	GPIO Port Expander	TCA6424ARGJR, TCA6408ARGTR	0x22, 0x20
SoC_I2C2	CSI Camera Connector		
SoC_I2C2	User Expansion Connector	<connector interface>	
MCU_I2C0	MCU Header	<connector interface>	
WKUP_I2C0	LED Driver	TPIC2810D	0x60
Others			
BOOTMODE_I2C	I2CBootmode Buffer	TCA6424ARGJR	0x22
BOOTMODE_I2C	Test Automation Header	<connector interface>	

The image below depicts the I2C tree, and above table provides the complete I2C address mapping details on AM62x SIP SK EVM.

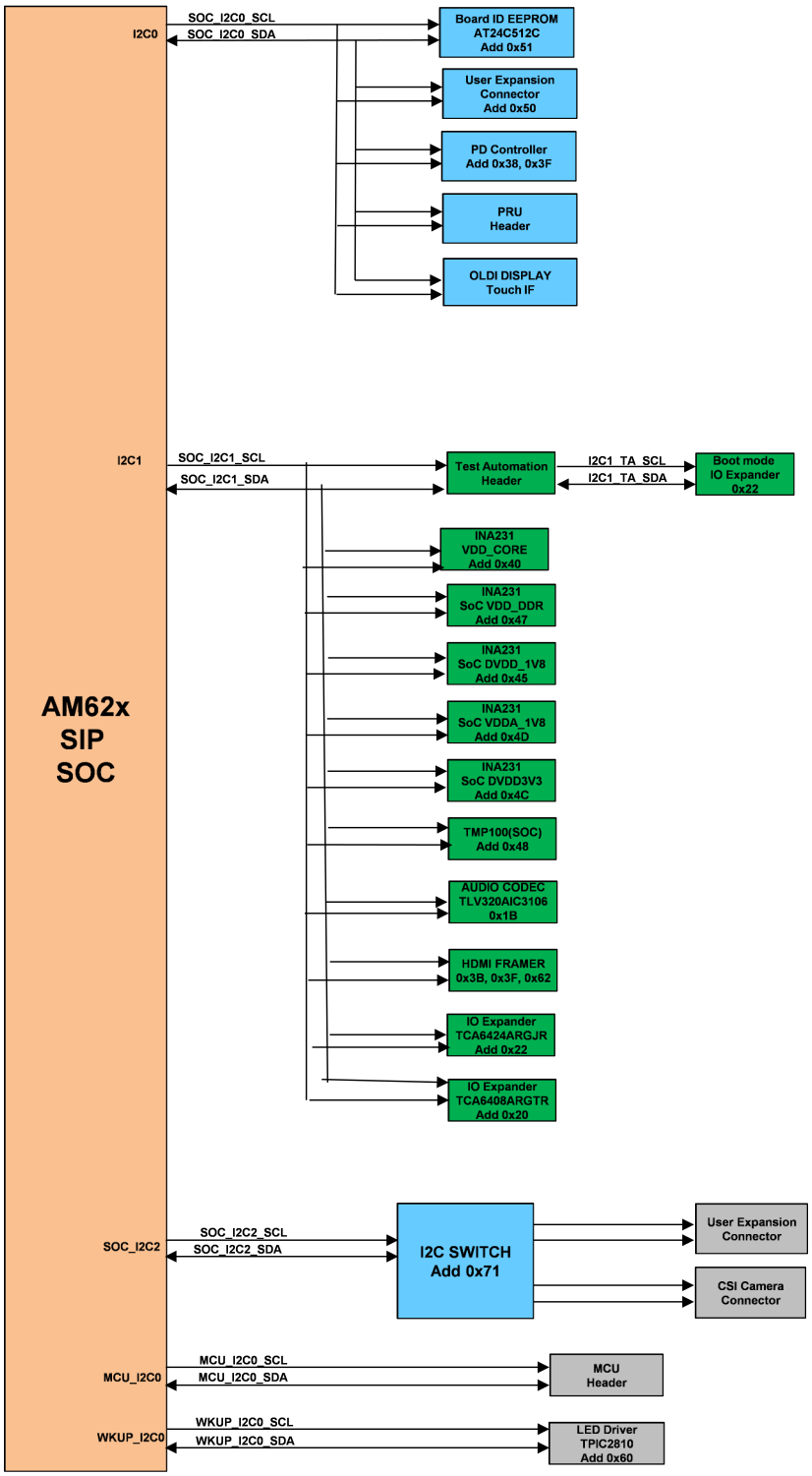

Figure 2-31. I2C Interface

3 Hardware Design Files

The hardware design files such as schematics, BOM, PCB Layout, Assembly Files and Gerber files are available in the link below.

https://www.ti.com/tool/download/SPRR482

4 Compliance Information

4.1 Compliance and Certifications

EMC, EMI & ESD Compliance

Components installed on the product are sensitive to Electric Static Discharge (ESD). TI recommends this product be used in an ESD controlled environment. This can include a temperature or a humidity controlled environment to limit the buildup of ESD. TI also recommends to use ESD protection such as wrist straps and ESD mats when interfacing with the product.

The product is used in the basic electromagnetic environment as in laboratory conditions, and the applied standard is as per EN IEC 61326-1:2021.

5 Additional Information

5.1 Known Hardware or Software Issues

This section describes the currently known issues on each EVM revision and applicable workarounds. Issues that have been patched have modification labels attached to the EVM assembly.

Table 5-1. SK-AM62-SIP EVM Known Issues and Modifications

Issue Number	Issue Title	Issue Description	Variants Affected
1	OLDI Display Touch Broken	OLDI Display touch function not working after power on	E1

5.1.1 Issue 1 - OLDI Display Touch Broken

Applicable EVM Revisions: E1

Issue Description: When power on the EVM, the OLDI Display Touch function is not working.

Fix: To mitigate the issue, the resistor R684, Cap C509 and U105 power supply need to be changed to VCC_3V3_SYS, see below image (OLDI Display RESET Logic for more information. Please follow the Image (PCBA Bottom Image) for the rework information.

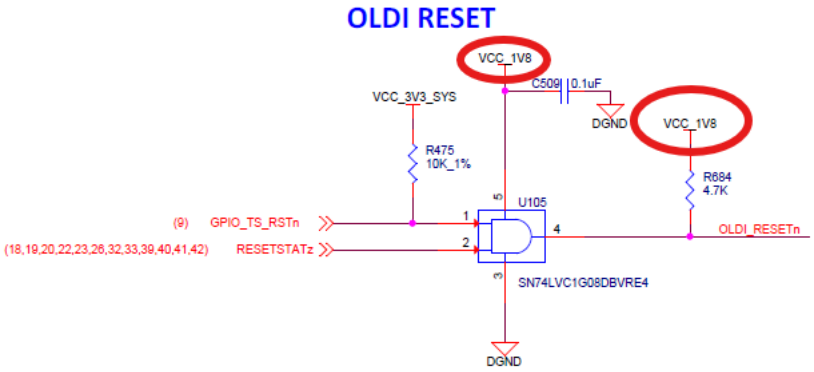

Figure 5-1. OLDI Display RESET Logic

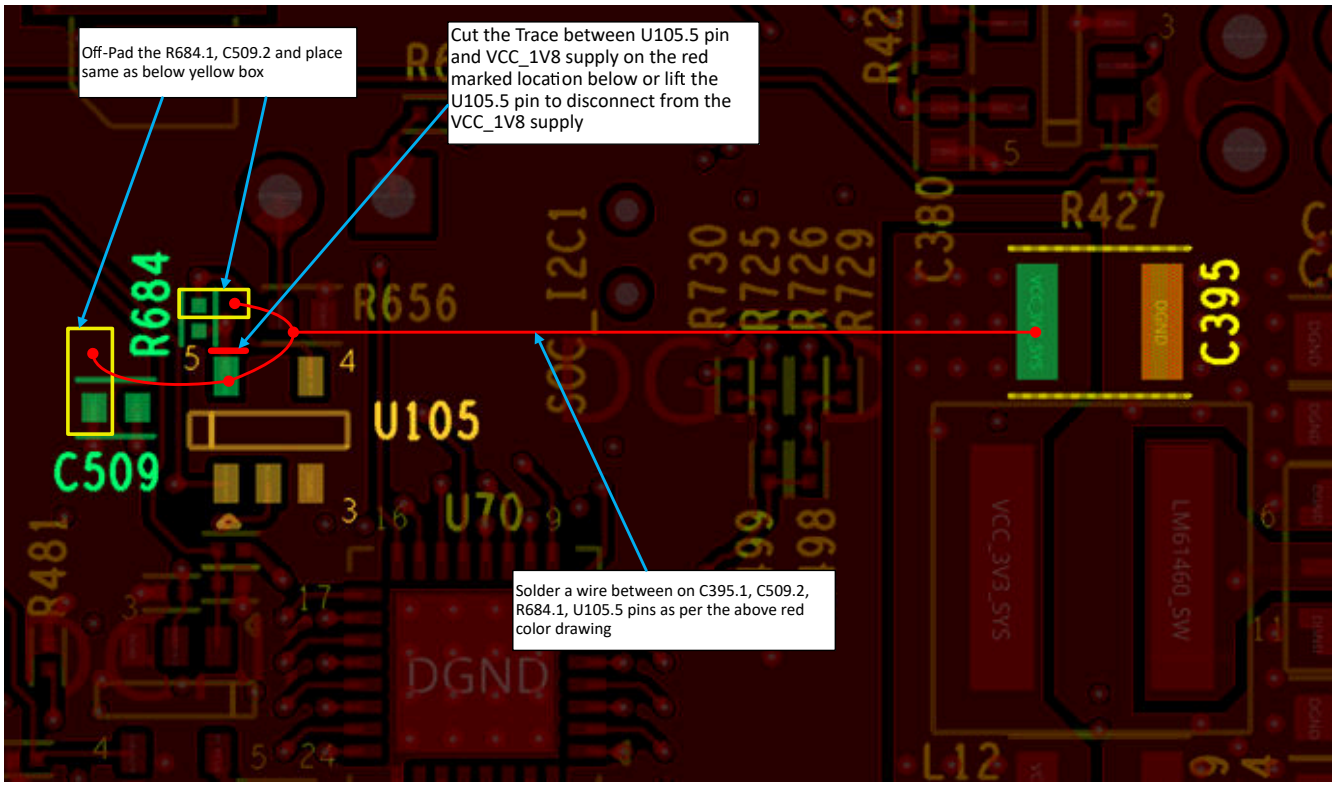

Figure 5-2. PCBA Bottom Image

5.2 Trademarks

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6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2023) to Revision A (December 2025)	Page
• Added HDMI Disclaimer information	1
• Changed *SD Boot Mode and No Boot Switch Setting Examples* figure	15
• Changed *Backup Boot Mode Selection BOOTMODE[12:10]* table	40
• Changed *Boot Mode Switch Configuration for SD Boot* figure	40
• Added Table 2-20 through Table 2-32	40
• Add Issue 1 to Table 5-1	57

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3 *Regulatory Notices:*

3.1 *United States*

3.1.1 *Notice applicable to EVMs not FCC-Approved:*

FCC NOTICE: This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

CAUTION

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。

https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-delivered-in-japan.html

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If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3. 技術基準適合証明を取得後ご使用いただく。

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上記を遵守頂けない場合は、電波法の罰則が適用される可能性があることをご留意ください。 日本テキサス・インスツルメンツ株式会社

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

電力線搬送波通信についての開発キットをお使いになる際の注意事項については、次のところをご覧ください。https://www.ti.com/ja-jp/legal/notice-for-evaluation-kits-for-power-line-communication.html

3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

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