User's Guide

Hardware Design Considerations for Custom Board Design Using AM62L (AM62L32, AM62L31) Family of Processors

ABSTRACT

The *Hardware Design Considerations for Custom Board Design* document gives an overview of the design considerations to be followed by the board designers while designing custom boards using AM62L32, AM62L31 processors. The document is intended to be used as a guideline at different stages of custom board design by board designers.

Additionally, links are provided for specific processor product page, related collaterals, E2E FAQs and other commonly referenced documents that help the board designers optimize the design efforts and schedule during custom board design.

Table of Contents

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1 Introduction

The Hardware Design Considerations user's guide for Custom Board Design Using AM62L (AM62L32, AM62L31) Family of Processors provides a starting point for the board designers designing with any of these processors. The document provides an overview of the recommended design flow at different board design stages and highlights important design requirements that are required to be addressed. Note that the document does not include all of the information required to complete the custom board design. In many cases, the document refers to the device-specific collaterals and various other documents as sources for specific information.

The document is organized in a sequential manner. It starts from decisions that are required to be made during the initial planning stages of the custom board design, through the selection of processor and key attached devices, electrical and thermal requirements. For designing a successful board design, recommendations discussed in each of the section are required to be addressed before moving to the next section.

Note

The document does not cover every aspect of the custom board design.

Note

The processor family has capabilities to address safety requirements.

The focus of the document is non-safety applications.

1.1 Before Getting Started With the Custom Board Design

The processor family includes wide variety of peripherals and processing capabilities, not all of which are used in every design. Consequently, the requirements for different designs using the same processor can vary widely depending on the target application. Board designers are required to understand the requirements before selecting the processor and determining the board level implementation details. In addition, the custom board design can require additional circuitry to operate correctly in the target environment. For selecting the processor and to determine the following, see the latest collaterals on TI.com including the device-specific data sheet, silicon errata, TRM and EVM user's guide :

- Expected environmental conditions for the processor operation, target boot mode, storage type and interfaces
- Processing (Performance) requirements for each of the cores in the selected processor
- External DDR memory type, speed, size that is used
- Processor peripherals used for the attached devices

As a starting point for information on key components used on the EVMs and SKs, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design - Starter kit / EVM variants (versions) and Key components list

1.1.1 AM62Lx Processor Family Change Summary (With Respect to AM62x Processor Family)

Below are some of the processor implementations to note during the AM62Lx-based custom board designs or changes to note when migrating from the AM62x design to the AM62Lx design:

1. The core supply voltage is fixed to 0.75V
2. Reset inputs and reset status outputs have been optimized
3. Implementation of 1.8V only IOs in addition to dual-voltage 1.8V/3.3V IOs. The IO supply for IO groups rails have been named accordingly.
4. Buffer Type 1P8-LVCMOS and RTC-LVCMOS have been implemented and Electrical Characteristics is added
5. Some of the processor peripherals including CPSW3G0 and OSPI0 support only 1.8V IO levels
6. DDR4 and LPDDR4 supported memory range is reduced (supports single rank)
7. OSPI0 interface support x2 interfaces (can be interface to 2 attached devices)
8. Non Muxed interface (connection of address bus and data bus separately) using GPMC0 not supported
9. Integrated LDO for generating 1.8V/3.3V SD interface IO supply to support UHS-I SD card

10. Integrated 1x 10-bit Analog-to-Digital Converter (ADC), Up to 1MSPS, 4x analog inputs (time-multiplexed)
11. Reduced pin count - Using only four of the bootstrap pins BOOTMODE[15:12], Boot from eFuse configured with the reduced pin count configuration and Full pin count - Using all 16 of the bootstrap pins BOOTMODE[15:0]
12. Ethernet boot is not supported
13. Display interface supported includes MIPI DSI (4 lanes DPHY) or DPI (24-bit RGB LVCMOS) (Any one of the display interface is actively supported and supported display is required to be selected during boot)
14. Camera Serial Interface (CSI-2) is not supported
15. RTC only and RTC + IO + DDR Self-refresh low-power modes are supported (Partial IO for CAN/GPIO/UART wakeup not supported)
16. EXT_WAKEUP0 and EXT_WAKEUP1 pins for External Wakeup Inputs
17. I2C interfaces including open-drain output type I2C interface have been optimized
18. IOSETs added for multiple peripherals (see the device-specific data sheet)
19. One VTM temp sensor provided, Temp Sensor 0: DDR/A53
20. VMON_VSYS Voltage monitor pin is not supported
21. VMON_3P3_SOC Voltage monitor for 3.3V processor power supply and VMON_1P8_SOC Voltage monitor for 1.8V processor power supply are not supported
22. PMIC_LPM_EN0 has a special output cell that turns on a weak pullup as soon as power is applied. The weak internal pullup turns off at the same time the output is driven high on the rising edge of RTC_PORz. (An external pull was required on AM62Lx processors because the PMIC_LPM_EN0 IO was turned off while reset was asserted. In this case, the PMIC can never turn on without the external pullup resistor.)
23. Pin connectivity requirements for I2C interface with open-drain output type I2C buffers has been updated. A pullup is required only when the IO is used

1.2 Processor Selection

Selection of processor is the most important stage of custom board design. To get an overview of the processor architecture and for selecting the processor variant, features, package (ANB) and speed grade, see the *Functional Block Diagram* and *Device Comparison* sections of the device-specific data sheet.

1.3 Technical Documentation

A number of documents relevant to the selected processor are available on the processor product page on TI.com. Before starting the custom board design, reading all the documents is strongly recommended.

The below FAQ summarizes the collaterals that can be referred to when starting the custom board design.

[FAQ] AM62L: Custom board hardware design – Collaterals to Get started

1.3.1 Updated EVM Schematic With Design, Review and Cad Notes Added

During custom board design, designers frequently reuse and edit the EVM design files. Alternatively, designers reuse common implementations, including processor, memory and communication interfaces. Because the EVM is expected to have additional functions, designers optimize the EVM implementation to suit board design requirements. While optimizing the EVM schematics, errors are introduced into the custom design that cause functional, performance or reliability problems. When optimizing, designers have queries regarding the EVM implementation, resulting in design errors. Many of the optimization and design errors are common across designs. Based on the user inputs and data sheet pin connectivity recommendations, comprehensive Design Notes (D-Note), Review Notes (R-Note) and CAD Notes (CAD-Note) are added near each section of the EVM schematic for designers to review and follow to minimize errors.

1.3.1.1 AM62Lx

Additional files as part of the design downloads have been included to support evaluation.

TMDS62LEVM: https://www.ti.com/lit/zip/sprcal6

The downloadable documents are listed in the product overview document added to the above zip file.

The following FAQ includes the PDF schematics and additional information related to EVM TMDS62LEVM:

[FAQ] AM62L: Custom board hardware design - Design and Review notes for Reuse of EVM TMDS62LEVM Schematics

1.3.2 FAQs to Support Custom Board Design

Based on interactions with board designers, queries from multiple board designers and learning from board designer queries, FAQs have been created to answer some of the commonly asked design question or provide design guidelines to support board designers during custom board design.

There is a primary list of FAQs available that includes all the Sitara™ processor families including AM62Lx:

[FAQ] Custom board hardware design - Master (Complete) list of FAQs for all Sitara processor (AM62x, AM64x, AM243x, AM335x) families

The FAQs processor family wise has also been listed:

[FAQ] AM62L: Custom board hardware design - FAQs related to Processor collaterals, functioning, peripherals, interface and EVM

Note

The FAQs are being updated frequently. Recommendation is to review the FAQs of interest on a regular basis for updated information.

1.4 Custom Board Design Documentation

Updating the design documents periodically to capture all the requirements and design updates, observations during different stages of the custom board design is recommended. The updated information provides the basis for the documentation package and the design document is required when requesting external review support.

1.5 Queries During Custom Board Design

For any queries related to custom board design start a new thread on E2E for experts to support. Recommendation is to include queries related to a specific section or peripheral or topic in a E2E query to reduce delay in assignment and answering.

2 Block Diagram

A detailed block diagram, covering all the required functional blocks and interfaces is key to a successful custom board design.

2.1 Constructing the Block Diagram

Preparing a detailed block diagram is an important stage during the custom board design. The block diagram is expected to include all major functional blocks, associated devices for processor functioning (PMIC) and attached devices. The block diagram is required to illustrate the interfaces and IOs used for interconnecting the processor and attached devices.

The below resources can be used as supporting documents when preparing the detailed block diagram:

- *TMDS62LEVM* (AM62L evaluation module) can be used as a reference or reuse the design, when starting a custom board design.
- The link referenced below for processor product folder on TI.com provides device-specific Functional Block Diagrams, Data Sheet, TRM, User Guides, Silicon Errata, Application Notes, design considerations, and other related information for different applications. The design and development section include EVM information, design tools, simulation models and software information. As part of information related to support and training, links to commonly applicable E2E threads and FAQs are available.

The processor product folder link on TI.com is referenced below:

- AM62L Product Folder

2.2 Configuring the Boot Mode

The processor family supports reduced pin count (x4 pins) or full pin count (x16 pins) boot modes. The processor family additionally supports eFuse BOOTMODE1 and eFuse BOOTMODE2. Board designers have the flexibility to choose the required boot mode to optimize use of external components.

Recommendation is to indicate the configured boot mode in the block diagram. Includes the boot configuration (reduced pin count or full pin count or eFuse), primary boot and the backup boot.

The processor family includes multiple peripheral interfaces that support boot. For the available boot mode configurations and supported peripherals, see the device-specific TRM. The processor family supports a primary boot mode option and an optional backup boot mode option. If the primary boot source fails to boot, then the ROM moves on to the backup boot mode.

The boot mode resistors connected to the processor boot mode input pins provide information on the boot mode to be used by the ROM code during boot. The boot mode inputs are sampled at reset status output (RESETSTATz). The boot mode configuration inputs are required to be stable before releasing (deassertion) the cold reset (PORz).

The reduced pin count boot mode mapping offers the advantage of requiring less bootstrap pins, which can translate to fewer pullup or pulldown components required. The reduced pin count boot mode comes at the cost of making fewer boot mode options pin selectable.

However, two (eFuse BOOTMODE1, eFuse BOOTMODE2) of the boot mode configuration options selectable from the *Reduced BOOTMODE Pin Mapping* table can be customized to any of the full 16-bit options by programming a new value to the eFuse. To program the eFuse, supply is required to be connected to the VPP pin.

Note

The recommendation is to provide provision to connect the VPP supply (On-board LDO or connect external supply for production programming through a test point with on-board capacitors added and a processor IO used to control the VPP supply timing) to the processor VPP pin used for eFuse programming. For more information, see the Section 3.2.7.

To determine the desired reduction in pullup/pulldown components required, the input buffers for pins BOOTMODE[11:0] are disabled during POR unless BOOTMODE[15:14] are '00'. Disabling the buffers avoids power consumption due to floating inputs on these pins when the reduced pin count option is used. For more information, see the device-specific TRM.

Reduced Pin Count Boot Mode:

Reduced pin count boot mode uses BOOTMODE [15:12] (x4 pins) and the configuration is summarized below:

BOOTMODE [13:12] – Configures the required primary and secondary boot mode

BOOTMODE [15:14] – Selects boot mode configuration (reduced or full pin count). For more information, see the device-specific TRM.

Note

BOOTMODE [11:00] – IO buffers are off during reset and after reset. These pins can be left unconnected when the IOs are not configured for alternate functions or can be configured for available alternate functions. Recommendation is to connect the boot mode IOs to the alternate functions through a 0Ω series resistor. Series resistor can be used to isolate the alternate function during testing.

Note

Leaving BOOTMODE [15:12] pins unconnected is not an allowed or recommended option.

Full Pin Count Boot Mode:

Full pin count boot mode uses BOOTMODE [15:00] (x16 pins) and the configuration is summarized below:

PLL Config: BOOTMODE [02:00] – Indicates the system clock (PLL reference clock selection) frequency (WKUP_OSC0_XI/XO) to ROM code for PLL configuration

Primary Boot Mode: BOOTMODE [06:03] – Configures the required primary boot mode, the peripheral/memory to boot from

Primary Boot Mode Config: BOOTMODE [09:07] – Provides optional configurations for primary boot and are used in conjunction with the boot mode selected

Backup Boot Mode: BOOTMODE [12:10] – Configures the required backup boot mode. the peripheral/memory to boot from, in case primary boot fails

Backup Boot Mode Config: BOOTMODE [13] – Provides additional configuration options (optional - depends on the selected backup boot mode) for the backup boot devices

BOOTMODE [15:14] – Selects boot mode configuration (reduced or full pin count). For configuration, see the device-specific TRM.

For more information on full and reduced pin count boot mode mappings, see the *Boot Mode Pin Mapping Options* section of device-specific TRM.

Key considerations for boot mode configuration:

- Recommendation is to always include provision to configure boot modes used during development, such as USB boot, UART boot or No-boot/Dev boot mode for JTAG debug
- Boot mode pins have alternate functions after latching of boot mode configuration. The board design is required to take the alternate function implemented into account when choosing pullup or pulldown resistors. If these pins are driven by another device, they are required to return to the proper boot configuration levels whenever the processor is reset (indicated by the RESETSTATz pin) to enable the processor to boot properly

For details regarding supported boot modes, see the *Initialization* chapter of the device-specific TRM.

For implementing the required boot mode (reduced pin count or full pin count), see the EVM *TMDS62LEVM* schematic.

Note

Board designer is responsible for providing provision to set the required boot mode configuration (using pullups or pulldowns, or optionally using jumpers/switches (with external ESD when set in uncontrolled environment)) depending on the required boot configuration. Recommendation is to provide provision for pullup and pulldown for the boot mode pins that have configuration capability for design flexibility.

Shorting the boot mode pins together, leaving any of the boot mode pins unconnected or shorting of the boot mode inputs directly to supply or ground in not recommended or allowed.

Note

When the full pin count boot mode option is configured, each of these balls (BOOTMODE[15:0]) are required to be connected to the corresponding power supply or VSS through separate external pull resistors to make sure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.

When the reduced pin count boot mode option is configured, each of these balls (BOOTMODE[15:12]) are required to be connected to the corresponding power supply or VSS through separate external pull resistors to make sure the inputs associated with these balls are held to a valid logic high or low level as appropriate to select the desired device boot mode.

Note

Recommendation is to connect the boot mode IOs to the alternate functions through a 0Ω series resistor. Series resistor is used to isolate the alternate function during testing.

Note

For information related to supported boot modes and available boot mode functionality, see the device specific silicon errata.

Note

Boot mode configuration resistors are recommended to be pulled to VDDSHV0.

Note

For reduced pin count boot mode configuration, 25MHz (Crystal or LVCMOS clock) is the only supported clock frequency.

For full pin count boot mode, see the device-specific data sheet for the supported clock frequencies and the device-specific TRM to configure the supported clock frequency.

The following FAQs captures the boot mode implementation approach when boot mode buffers are used and not used.

[FAQ] AM625 / AM623 / AM644x / AM243x / AM62A / AM62P - Bootmode implementation with buffers

[FAQ] AM625 / AM623 / AM644x / AM243x / AM62A / AM62P - Bootmode implementation without buffers

The FAQs are generic and can also be used for AM62Lx processor family.

2.3 Confirming PinMux (PinMux Configuration)

The processor family supports number of peripheral interfaces. To optimize size, pin count and package while maximizing functionality, many of the processor pads (pins) provide provision to multiplex up to eight signal functions. Thus, not all peripheral interface instances are available or can be used simultaneously.

TI provides the SysConfig-PinMux Tool that supports board designer to configure the required function using PinMux tool for AM62Lx family of processors.

Note

Recommendation is to save the PinMux configuration generated using SysConfig-PinMux Tool along with other design documentation.

3 Power Supply

After completion of the processor selection and block diagram updates, the next stage of the custom board design is to determine the power supply architecture for the selected processor.

3.1 Power Supply Architecture

The power supply architectures that can be considered are listed below:

3.1.1 Integrated Power

The architecture can be based on Multi-channel ICs (PMIC) such as TSP65214x or similar.

For more information on the AM62L power architecture using PMIC, see the EVM *TMDS62LEVM* schematic.

For more information, see the *AM62L Power Supply Implementation* application note.

Note

PMIC MODE/RESET pin was configured as cold reset and connecting RESETSTATz to the pin is not an option. For applications using the “RTC only” low-power mode, customers can drive the pin with the “power-good” signal of the external DC/DC or LDO generating the RTC supply rails. The connection triggers a cold reset on the PMIC if there is a fault on VDD_RTC or VDDS_RTC.

It is allowed or acceptable (safe) to leave the pin floating since an internal (approximately 25nA) pulldown is available and enabled.

3.1.2 Discrete Power

The architecture is based on discrete DC-DC converters and LDOs.

For information related to available or recommended discrete power architecture, see the device-specific (AM62L) product page on TI.com.

AM62L product page provides the updated information on the available power architecture.

PORz is required to be held low (active) during power-up until all the processor supplies are valid (using external crystal circuit) plus minimum delay of 9.5ms or PORz held low (active) until all the processor supplies are valid and external clock is stable (when using external LVCMOS clock source) plus minimum delay of 1.2µs.

3.2 Power (Supply) Rails

For the complete list of processor power supply rails and allowed supply range, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet. The following sections provide additional details for some select power rails.

For more information about design recommendations of processor ROC, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – SOC ROC Recommended Operating Condition

The FAQ is generic and can also be used for AM62Lx processor family.

For more information about dynamic voltage scaling (DVS) and dynamic frequency scaling (DFS), see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – Dynamic Voltage Scaling

The FAQ is generic and can also be used for AM62Lx processor family.

Note

Verify that the power supplies connected to the processor supply rails are within the *Recommended Operating Conditions* of the device-specific data sheet.

3.2.1 Supported Low-Power Modes

For the supported low-power modes, see the device-specific data sheet.

For implementation of RTC only or RTC + IO + DDR Self-refresh low-power mode, see the EVM *TMDS62LEVM* schematic.

For additional information, see the device-specific TRM.

PMIC_LPM_EN0 has a special output cell that turns on a weak pullup as soon as power is applied. The weak internal pullup turns off at the same time the output is driven high on the rising edge of RTC_PORz (an external pull was required on AM62Lx processors because the PMIC_LPM_EN0 IO was turned off while reset was asserted. In the case, the PMIC can never turn on without the external pullup resistor).

3.2.2 Core Supply

The processor is specified to operate at a fixed core voltage of 0.75V.

Core supplies VDD_CORE, VDDA_CORE_DSI, VDDA_CORE_DSI_CLK, VDDA_CORE_USB and VDDA_DDR_PLL0 are recommended to be powered from the same power source (specified operating range as per the *Recommended Operating Conditions* (ROC) table).

A 0.75V Fixed-voltage always on supply is recommended to be connected to VDD_RTC RTC Core Supply voltage when low-power modes (including RTC only mode) are used.

Recommendation is to connect VDD_CORE and VDD_RTC to the same power source when low-power mode (RTC only mode) is not used.

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.3 Peripheral Power Supply

The processor family supports dedicated peripheral supplies for PLL, USB (common for USB0 and USB1), DSITX0 and ADC0. The operating voltage ROC is 1.8V. An additional 3.3V analog supply is required for USB.

Depending on the memory selected DDR PHY IO (VDDS_DDR) supply rail is specified to be 1.1V (LPDDR4) or 1.2V (DDR4).

For more information, see the *Recommended Operating Conditions* section in the *Specifications* chapter of the device-specific data sheet.

3.2.4 Integrated LDO for SD Card Interface (Supply for Dynamic Switching Dual-voltage IOs)

The processor family supports an integrated LDO (SDIO_LDO) to power the SDIO interface IO supply for IO group and SD interface pullups, capable of dynamically switching between 1.8V and 3.3V voltage. Recommended output capacitor are recommended to be connected close to the LDO output pin (CAP_VDDSHV_MMC). For guidance on recommended capacitance and connection, see the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet.

V1P8_SIGNAL_ENA bit is used to control the LDO output level used for controlling the SD card interface IO (signaling). The output of the LDO can be connected to one of the processor IO supply for IO group used for SD card interface (VDDSHV3 or VDDSHV4 for UHS-I support).

For connecting the LDO (SDIO_LDO and CAP_VDDSHV_MMC) when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

3.2.5 Internal LDOs for IO Supply for IO groups (Processor)

The processor family supports internal LDOs (CAP_VDDS_GENERAL1, CAP_VDDS_GPMC and CAP_VDDS_MMCx [x = 0-2]) and each of the LDO output connects to a separate ball (pin) for connecting an external capacitor. For guidance on recommended capacitance and connections, see the *Power Supply* sub-section in the *Signal Descriptions* section of the device-specific data sheet. Follow the EVM *TMDS62LEVM* schematic for selection of the capacitor package. Not following the CAP_VDDSxxx recommended guidelines can affect the processor performance.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Custom board hardware design – CAP_VDDSx CAP_VDDS

3.2.6 Processor IO Supply for IO Group

The processor family supports the following:

- Dual-voltage IO supply for IO group (3.3V or 1.8V)
- Fixed IO supply for IO group (1.8V)

3.2.6.1 1.8V or 3.3V Dual-voltage IO Supply for IO Group

The processor family provides VDDSHV0, VDDSHV1 - dual-voltage fixed 1.8V or 3.3V IO supply and VDDSHV2, VDDSHV3, VDDSHV4 dual-voltage dynamically switched 1.8V or 3.3V IO supply, where each IO supply for IO group powers a predefined set of IOs. Each IO supply for IO group can be individually configured for 3.3V or 1.8V. Recommendation is to source the processor IO supply for IO group supply and the IO supply for the attached devices from the same power source.

VDDSHV2, VDDSHV3 and VDDSHV4 IO supply for IO groups for MMC0-2 have been designed to support power-up, power-down, or dynamic supply voltage change without any dependency on other supplies. The capability is required to support UHS-I SD card.

3.2.6.1.1 Additional Information

Most of the processor IOs are not fail-safe. For information on available fail-safe IOs, see the device-specific data sheet. Recommendation is to power IO supply of attached devices from the same power source as the respective processor dual-voltage IO groups (VDDSHVx supply rail) to make sure that the system/board never applies potential to an IO that is not powered. Taking care of fail-safe operation is recommended to protect the IOs of processor and attached devices.

For more information, see the following FAQ:

[FAQ] AM625/AM623 Custom board hardware design – Power sequencing between SOC (Processor) and the Attached devices (Fail-safe)

The FAQ is generic and can also be used for AM62Lx processor family.

Available IO supply for IO groups information is summarized below:

- VDDSHV0 – Dual-voltage IO supply for GPMC0 IO group (Fixed supply)
- VDDSHV1 – Dual-voltage IO supply for General interface IO group (Fixed supply)
- VDDSHV2 – Dual-voltage IO supply for MMC0 IO group (Dynamically switched)
- VDDSHV3 – Dual-voltage IO supply for MMC1 IO group (Dynamically switched)
- VDDSHV4 – Dual-voltage IO supply for MMC2 IO group (Dynamically switched)

3.2.6.2 1.8V Fixed IO Supply for IO Group

The processor family supports Fixed-voltage 1.8V IO supply rails (VDDS0, VDDS1, VDDS_RTC and VDDS_WKUP). All attached devices (IOs) connected to these IOs are required to be powered from the same power source that is being used to power the respective processor supply rails.

A 1.8V Fixed-voltage always on supply is recommended to be connected to VDDS_RTC IO supply for LFOSC0 and RTC IO group when low-power modes (including RTC only mode) are used.

Recommendation is to connect IO supply for LFOSC0 and RTC IO group VDDS_RTC to a valid 1.8V IO power source when low-power modes (including RTC only mode) are not used.

Available IO supply for IO groups information is summarized below:

- VDDS0 – IO supply for GENERAL0 IO group (RGMII1, RGMII2 IO groups)
- VDDS1 – IO supply for OSPI0 IO group
- VDDS_RTC – IO supply for LFOSC0 and RTC IO group
- VDDS_WKUP – IO supply for WKUP IO group

3.2.7 VPP (eFuse ROM Programming) Supply

VPP supply can be sourced on-board or externally.

VPP pin can be left floating (HiZ) or pulled down to ground through a resistor during processor power-up, power-down and during normal processor operation.

The following hardware requirements are required to be met when programming keys in the OTP eFuses:

- The VPP power supply must applied only after completion of processor power-up sequence.
- Recommendation is to use a fixed LDO with higher input supply (2.5V or 3.3V) and enable input. The enable input is required to be controlled by the processor GPIO for timing.
- The VPP power supply is expected to see high load current transients and local bulk capacitors are likely required near the VPP pin to support the LDO transient response.
- Select the power supply with quick discharge capability or use a discharge resistor.
- A maximum current of 400mA is specified during programming.
- When an external power supply is used, the supply is recommended to be applied after the processor power supplies ramp and are stable.
- When external power supply is used, recommend adding on-board bulk capacitor, decoupling capacitor and discharge resistor near to the processor VPP supply pin. Add a test point to connect external power supply and provision to connect one of the processor GPIO to control timing of the external supply.
- Recommendation is to disable the VPP supply (left floating (HiZ) or grounded) when not programming the OTP eFuses.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding VPP eFuse programming power supply selection and application

The FAQ is generic and can also be used for AM62Lx processor family.

For more information, see the *VPP Specifications for One-Time Programmable (OTP) eFuses* section in the *Specifications* chapter of the device-specific data sheet.

3.3 Determining Board Power Requirements

The current (maximum and minimum) requirements for each of the supply rails are not provided in the device-specific data sheet. These requirements are highly application dependent and are required to be estimated using TI provided tools for a specific use case.

3.4 Power Supply Filters

For implementing processor power supply rails filtering, decoupling and bulk capacitors, see the EVM *TMDS62LEVM* schematic.

3.5 Power Supply Decoupling and Bulk Capacitors

To decouple the processor and attached device supplies from board noise, decoupling and bulk capacitors are recommended.

For guidance on optimizing and placement of the decoupling and bulk capacitors, see the *Sitara Processor Power Distribution Networks: Implementation and Analysis* application note.

3.5.1 Note on PDN Target Impedance

The PDN target impedance values are provided for specific supplies. The PDN target impedance values are not provided for all supply rails since the target impedance calculation includes reference to the maximum current on the power rails and is dependent on use case.

For updates on the PDN target impedance supplies and values, see the following FAQ:

[FAQ] AM62L: Custom board hardware design – Collaterals to Get started

Look for PDN target impedance values (VDD_CORE).

3.6 Power Supply Sequencing

A detailed diagram of the required *Power Supply Sequencing* (Power-Up and Power-Down) are provided in the device-specific data sheet. All associated processor power supplies are expected to allow for controlled supply ramp (see the supply slew rate) and supply sequencing (using a PMIC-based power supply or using on-board logic when discrete power architecture is used).

For more information, see the *Power Supply Requirements, Power Supply Slew Rate Requirement, Power Supply Sequencing* section of the device-specific data sheet.

For more information, see the following FAQ:

[FAQ] AM625/AM623 Custom board hardware design – Processor power-sequencing requirements for power-up and power-down

The FAQ is generic and can also be used for AM62Lx processor family.

3.7 Supply Diagnostics

Voltage monitors internal to the processor are not available.

3.8 Power Supply Monitoring

For optimizing the custom board performance, provide provision for external monitoring of supply rails and load currents.

For implementation, see the EVM *TMDS62LEVM* schematic.

Now that the power supply architecture and the devices for generating the supply rails have been finalized, update the block diagram to include the power supply rails and interconnection. Recommendation is to create a power supply sequence (power-up and power-down) diagram and verify the sequence with the device-specific data sheet.

4 Processor Clocking

The next stage of the custom board design is proper clocking of processor and attached devices. The processor clock can be generated internally using external crystal or an LVCMOS compatible clock input can be used. Follow the connection recommendations in the device-specific data sheet when using an external clock. The section describes the available processor clock sources and the requirements.

4.1 Processor External Clock Source

The recommended processor clock sources and recommended connections are summarized in the *Clock Specifications* section in the *Specifications* chapter of the device-specific data sheet.

A 25MHz external crystal interface pins connected to the internal high frequency oscillator (WKUP_HFOSC0) or WKUP_OSC0 LVCMOS digital clock, is the default clock source for internal reference clock HFOSC0_CLKOUT.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding MCU_OSC0 Start-up Time

The FAQ is generic and can also be used for AM62Lx processor family.

Low-frequency oscillator (LFOSC0) has limited use case. Based on the use case, select a 32.768kHz crystal as clock source.

For more information, see the following FAQ:

[FAQ] AM625: LFOSC usage in the device

The FAQ is generic and can also be used for AM62Lx processor family.

Note

MCU_OSC0 (High frequency oscillator) for AM62x is WKUP_OSC0 for AM62Lx.

WKUP_LFOSC0 (Low frequency (32.768kHz) oscillator) for AM62x is LFOSC0 for AM62Lx.

4.1.1 Unused LFOSC0

For guidance on the recommended connections, see the *LFOSC0 Not Used* section in the *Specifications* chapter of the device-specific data sheet.

4.1.2 LVCMOS Digital Clock Source

The WKUP_OSC0_XI and LFOSC0_XI clock inputs can be sourced from a 1.8V LVCMOS square-wave digital clock source. For more details, see the *Timing and Switching Characteristics, Clock Specifications, Input Clocks / Oscillators* section in the *Specifications* chapter of the device-specific data sheet.

Note

Be sure to connect the WKUP_OSC0_XO and LFOSC0_XO pins as per the device-specific data sheet recommendation.

Note

For more information, see the Note provided in the *WKUP_OSC0 LVCMOS Digital Clock Source* section of device-specific data sheet.

4.1.3 Crystal Selection

When selecting a crystal, the board designer must consider the temperature and aging characteristics based on the worst case operating environment and expected life expectancy of the board. Verify the crystal load and the crystal load cap value including the PCB capacitance (for WKUP_OSC0) used matches the data sheet recommendations. Select a crystal load to allow selection of a standard capacitor value. Mismatch in value can introduce clock frequency PPM errors.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Queries regarding Crystal selection

The FAQ is generic and can also be used for AM62Lx processor family.

For more information, see the *WKUP_OSC0 Crystal Circuit Requirements* and *LFOSC0 Crystal Electrical Characteristics* tables of the device-specific data sheet.

Recommendation is to verify the crystal selection with the crystal manufacturer as required.

4.2 Processor Clock Outputs

Processor IOs (Pins) named CLKOUT0 and WKUP_CLKOUT0 can be configured as clock outputs. The clock outputs can be used as clock source for attached devices (external peripherals).

For more details, see the device-specific data sheet and TRM.

5 Joint Test Action Group (JTAG)

TI supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support.

See the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1/ AM6442 / AM2432 Custom board hardware design – JTAG

The FAQ is generic and can also be used for AM62Lx processor family.

Although JTAG is not required for operation, recommendation is to include the JTAG connection in the custom board design.

5.1 JTAG / Emulation

Relevant documentation for the JTAG/Emulation:

- *Emulation and Trace Headers Technical Reference Manual*
- *XDS Target Connection Guide*
- *Boundary Scan Test Specification (IEEE-1149.1)*
- *AC Coupled Net Test Specification (IEEE-1149.6)*

5.1.1 Configuration of JTAG / Emulation

The IEEE Standard 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) interface can be used for boundary scan and emulation. The boundary scan implementation is compliant with both IEEE-1149.1 and 1149.6. Boundary scan can be used regardless of the processor configuration.

As an emulation interface, the JTAG port can be used in different modes:

- Standard emulation: requires only five standard JTAG signals.
- HS-RTDX emulation: requires five standard JTAG signals plus EMU0 and/or EMU1. EMU0 and/or EMU1 are bidirectional in the mode.
- Trace port: The trace port allows real-time dumping of certain internal data. The trace port uses the EMU pins to output the trace data.

Emulation can be used regardless of the processor configuration.

For supported JTAG clocking rates, see the device-specific TRM.

The required BSDL file for boundary scan testing can be downloaded from the below section.

5.1.1.1 AM62Lx

- AM62Lx Sitara BSDL

5.1.2 Implementation of JTAG / Emulation

The JTAG and Emulation signals are referenced to the same IO group supply. The TDI, TDO, TCK, TMS, TRSTn, EMU0 and EMU1 signals are powered by the VDDS0.

For proper implementation of the JTAG interface, see the *Emulation and Trace Headers Technical Reference Manual*.

5.1.3 Connection of JTAG Interface Signals

For connecting the JTAG interface signals, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

Note

In case JTAG interface is not used, recommendation is to always provide provision for connecting the JTAG interface signals using test points for development testing and the required pulls as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

6 Configuration (Processor) and Initialization (Processor and Device)

Recommendation is to deassert (release) the processor cold reset input (PORz) only after all the processor supplies ramp and delay of recommended hold time (in ms) for the crystal or oscillator to start-up and stabilize (see the device-specific data sheet) to start the processor boot process.

6.1 Processor Reset

The processor family supports three external reset inputs PORz (WKUP domain cold reset input), RESETz (main domain warm reset input) and RTC_PORz (RTC Power-on Reset input).

Be sure to make the recommended connections as per the *Pin Connectivity Requirements* section of the device-specific data sheet.

The supported reset configurations are described in detail in the device-specific data sheet and TRM.

The processor provides a combined, single reset status output RESETSTATz (main domain warm reset status output). RESETSTATz reflects the internal reset state of the device, and is low when either cold reset PORz or warm reset RESETz is low, and goes high after a delay (see the device-specific data sheet) after PORz or RESETz is deasserted.

Reset status output when not used can be left unconnected. Recommendation is to provide provision for a test point for testing or future enhancements. An optional pulldown is recommended.

For PORz (3.3V tolerant, fail-safe input), a 3.3V input can be applied. The input thresholds are a function of the 1.8V IO supply voltage (VDDS_OSC0).

Recommendation is to hold the PORz low during the supply ramp-up and crystal or oscillator start-up. Follow the recommended PORz timing requirement in the *Power-Up Sequencing* diagram of the device-specific data sheet.

Additional reset modes are available through processor internal registers and emulation.

6.1.1 RTC Power-on Reset (RTC_PORz)

RTC Power-on Reset and is not recommended or allowed to float. RTC_PORz pin is required to be connected as described below:

1. The RTC_PORz input needs to be sourced from the PG output of VDD_RTC and VDDS_RTC power sources when operating in RTC Only mode. The PG open-drain outputs are released once both supplies are valid and the RTC domain is released from reset.

2. The RTC_PORz input needs to be sourced from a PMIC GPO (follow the power sequence diagrams in the processor-specific data sheet when alternate power architecture is used) when operating in RTC + IO + DDR Self-refresh mode. The PMIC is sourcing both the RTC power supplies. One of the PMIC's open-drain outputs is released at the appropriate time in the power-up sequence (check the PMIC used and the supported implementation).
3. Recommendation is to connect RTC_PORz input to the same signal connected to PORz when not using low-power modes. Assumes VDD_RTC is connected to the same source as VDD_CORE, and VDDS_RTC is connected to the same source as VDDS0, VDDS1.

The potential applied to the VDD_RTC power supply rail must always be greater than or equal to the potential applied to VDD_CORE. The only power supply (rail) sequence requirement for VDD_RTC.

The RTC_PORz must be held low until the RTC power rails are valid.

6.2 Latching of Boot Mode Configuration

For more details about the processor boot mode options, see above Section 2.2.

Boot mode configurations for processor are latched at the rising edge of PORz. The device configuration and boot mode input pins have alternate functions that are multiplexed. After the status (level) on these pins are latched into the configuration registers, these pins are available to be used for their alternate functions. RESETSTATz optionally can be used for latching the pin strap configuration for attached devices.

6.3 Resetting the Attached Devices

Using an ANDing logic to reset the attached devices as applicable (on-board media and data storage devices, and other peripherals) is recommended. Processor general purpose input/output (GPIO) pin is connected to one of the AND gate input with provision for 0Ω to isolate the GPIO input for testing or debug. Processor IO buffers are off during reset. Recommendation is to place a pullup near to the AND gate input to prevent the AND gate input from floating and enabling the reset logic controlled by the processor IO during power-up. Main domain warm reset status output (RESETSTATz) signal can be connected as the other input to the AND gate. Make sure the processor IO supply and the pullup supply used near to the AND logic input are sourced from the same power source.

In case an ANDing logic is not used and the processor main domain warm reset status output (RESETSTATz) is used to reset the attached device, match the IO voltage level of the attached device and RESETSTATz. A level translator is recommended to match the IO voltage level.

Recommendation is to provision for a software enabled (controlled) power switch (load switch) that sources the SD card power supply (VDD). A fixed 3.3V supply (IO supply connected to the processor) is connected as an input to the power switch.

Use of power switch allows power cycling of the SD card (since resetting the power switch is the only way to reset the SD card) and resetting the SD card to the default state.

For more information on implementing reset logic for the attached devices and power switch enable logic for SD card, see the EVM *TMDS62LEVM* schematic.

6.4 Watchdog Timer

Use of watchdog timer is based on the application requirement. Consider using internal or external watchdog timer.

7 Processor Peripherals

Processor peripherals section covers the processor peripherals and modules, and is intended to be used in addition to the information provided in the device-specific data Sheet, TRM, and relevant application notes. The three types of documents can be used are:

- Data Sheet: Pin Description, Processor operational modes, AC Timings, Guidance on pin functions, Pin mapping
- TRM: Functional Description, Programming Guide, Information regarding registers and configuration
- Application Notes: Board-level understanding and resolving commonly observed issues

7.1 Selecting Peripherals Across Domains

The processor architecture includes multiple domain, each domain includes specific processing cores and peripherals:

- MAIN Domain
- RTC Domain
- Wakeup (WKUP) Domain

7.2 Memory Controller (DDRSS)

DDR Subsystem supports LPDDR4 or DDR4 memory interface. For data bus width, inline ECC support, speed and max addressable range selection, see the *Memory Subsystem, DDR Subsystem (DDRSS)* section in the *Features* chapter of device-specific data sheet.

The allowed memory configurations for DDR4 are 1x 16-bit or 2x 8-bit. 1x 8-bit memory configuration is not a valid configuration.

The allowed memory configuration for LPDDR4 is 1x 16-bit.

Based on the application requirements, same memory (LPDDR4) device can be used with the AM625 / AM623 / AM625-Q1 / AM620-Q1 , AM62A7 / AM62A3, AM62P / AM62P-Q1 and AM62L32 / AM62L31 processors due to the availability of 1x 16-bit configuration.

When LPDDR4 or DDR4 is used, see the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

For connecting the DDRSS signals when not used see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more details, see the *DDR Subsystem (DDRSS)* section in the *Memory Controllers* chapter of the device-specific TRM.

LPDDR4 memory is used in the current EVM design.

For more information on DDR4 / LPDDR4 memory interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Custom board hardware design – DDR4 / LPDDR4 MEMORY Interface

7.2.1 Processor DDR Subsystem and Device Register Configuration

The DDR controller and DDR PHY have a large number of parameters to configure. To facilitate the configuration, an online tool *(SysConfig tool)* is provided that generates an output file that is consumed by the driver. Choose the *DDR Subsystem Register Configuration* from the *Software Product* pulldown menu and choose the required processor. The tool takes board information, timing parameters from DDR device-specific data sheet, and IO parameters as inputs and then outputs a header file that the driver uses to program the DDR controller and DDR PHY. The driver then initiates the full training sequence.

The SDK has an integrated configuration file for the memory (LPDDR4) device mounted on the EVM. If you need a configuration file for a different memory (LPDDR4) device, a new configuration file has to be generated using the DDR Register Configuration tool.

For more information, see the following FAQ:

[FAQ] AM62A7 or AM62A3 Custom board hardware design – Processor DDR Subsystem and Device Register configuration

The FAQ is generic and can also be used for AM62Lx processor family.

7.2.2 Calibration Resistor Connection for DDRSS

Follow the DDR0_CAL0 (IO Pad Calibration Resistor) connection recommendations in the device-specific data sheet.

7.2.3 Attached Memory Device ZQ and Reset_N Connection

Follow the device-specific EVM schematics for connecting the recommended resistors (ZQ (Impedance calibration) and Reset_N (Memory reset input)) to the memory devices and the values.

7.3 Media and Data Storage Interfaces

The processor family supports below memory interfaces:

7.3.1 Multi-Media Card/Secure Digital (MMCSD) Interface

The processor family supports 3x Multi-Media Card/Secure Digital (MMC/SD/SDIO) ((8b+4b+4b) interfaces, 8-bit eMMC on MMC0 (for speed, see the *MMC0 - eMMC/SD/SDIO Interface* section of device-specific data sheet), 4-bit SD/SDIO on MMC1 and MMC2 (for speed, see the *MMC1/MMC2 - SD/SDIO Interface* section of the device-specific data sheet).

For information on eMMC memory interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – eMMC MEMORY Interface

The FAQ is generic and can also be used for AM62Lx processor family.

For more details, see the *Multi-Media Card Secure Digital (MMCSD) Interface* sub-section in the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3.2 Octal Serial Peripheral Interface (OSPI) / Quad Serial Peripheral Interface (QSPI)

The processor family supports connecting x1 memory device (1x OSPI or QSPI) or connecting up to x2 memory (Example: 1x OSPI + 1x QSPI) devices over the OSPI0 interface. The OSPI0 IOs are referenced to VDDS1 and support fixed 1.8V IO level.

Below are the valid combinations:

- OSPI + OSPI (Faster - DQS)
- QSPI + OSPI (Faster - DQS)
- OSPI (Faster - DQS)
- QSPI (Faster - LBCLKO)

For information related to OSPI or QSPI, see the following FAQs:

[FAQ] AM62L: Custom board hardware design – OSPI0 interface implementation on TMDS62LEVM and guidelines

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – OSPI/QSPI MEMORY Interface

[FAQ] OSPI FAQ for Sitara/Jacinto devices

The FAQs are generic and can also be used for AM62Lx processor family.

For more details, see the *Octal Serial Peripheral Interface (OSPI)* sub-section in the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.3.3 General-Purpose Memory Controller (GPMC) Interface

The processor family supports 1x General-Purpose Memory Controller (GPMC) up to 133MHz interface.

Refer *Media and Data Storage* section in the *Features* chapter, *Device Comparison* table in the *Device Comparison* chapter and *GPMC0 Signal Descriptions* table in the *Terminal Configuration and Functions* chapter of device-specific data sheet, for supported memory interfaces.

The GPMC IOs are referenced to VDDSHV0.

For more details, see the *General-Purpose Memory Controller (GPMC)* sub-section in the *Memory Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.4 Common Platform Ethernet Switch 3-port Gigabit (CPSW3G - for Ethernet Interface)

7.4.1 AM62Lx

The CPSW3G0 interface IOs are referenced to VDDS0 and supports fixed 1.8V IO level.

The CPSW3G0 interface can be configured either as a 3-port switch (interfaces to two external Ethernet ports (port 1 and 2)) or a dual independent MAC interface having their own MAC address.

CPSW3G0 supports RMII (10/100) or RGMII (10/100/1000) interface for each of the external Ethernet interface port.

For implementation of a RMII interface, see the *CPSW0 RMII Interface* section of the device-specific TRM.

CPSW3G0 RMII interface supports interfacing processor to Ethernet PHY configured as controller (master) or device (slave).

CPSW3G0 when configured for RMII interfaces, interfaces to EPHY configured for an external 50MHz (connected to a buffered external oscillator or processor clock output CLKOUT0) clock input (one of the buffered clock output connects to processor MAC) or EPHY configured for 25MHz crystal or clock input with 50MHz clock output from EPHY connected to the processor MAC.

One of the CPSW3G0 port is an internal Communications Port Programming Interface (CPPI) host port. CPPI is a streaming interface to provide data from DMA to CPSW3G0 and vice versa.

CPSW3G0 allows using mixed RGMII/RMII interface topology for the 2x external interface ports.

RGMII_ID is not timed, tested, or characterized. RGMII_ID is enabled by default for Transmit data (TDn). Processor MAC does not implement Internal delay for the RDn (Receive data) path.

For more details on the CPSW3G0 Ethernet interface, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

7.5 Programmable Real-Time Unit Subsystem (PRUSS)

The processor family does not support PRUSS.

7.6 Universal Serial Bus (USB) Subsystem

The processor family supports up to two USB 2.0 Ports. These Ports are configurable as host or device or Dual-Role Device (DRD). USBn_ID (identification) functionality is supported using any of the processor GPIO.

Follow the *USB VBUS Design Guidelines* section of the device-specific data sheet to scale the USB VBUS voltage (supply near the USB interface connector) before connecting to USBn_VBUS [n = 0-1] pins as applicable.

Connecting VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) input is recommended to be connected when the USB interface is configured for device mode. Connection of VBUS (VBUS supply input including Voltage Scaling Resistor Divider / Clamp) is optional for processor USB host mode.

A power switch with OC (over current) output indication is recommended when the USB interface is configured as host for VBUS control. The USB DRVVBUS drives the power switch. The recommendation is to connect the OC output to a processor GPIO (input), when the USB interface is configured as host.

For details related to USB connections and On-The-Go feature support, see the device-specific TRM.

For more details, see the *High-speed Serial Interfaces* section in the *Peripherals* chapter of the device-specific TRM.

When USB0 and USB1 are not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the USB supply pins.

When USB0 or USB1 is not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the interface signals and USB supply pins.

For more information on USB2.0 interface, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – USB2.0 interface

The FAQ is generic and can also be used for AM62Lx processor family.

7.7 General Connectivity Peripherals

The processor family supports multiple instances of UART, Multichannel Serial Peripheral Interface (MCSPI), I2C, Multichannel Audio Serial Port (MCASP), Enhanced Pulse Width Modulator (EPWM), Enhanced Quadrature Encoder Pulse (EQEP), Enhanced Capture (ECAP), MCAN (Modular Controller Area Network) with Full CAN-FD support and GPIO. All LVCMOS IOs can be configured as GPIO.

The number of peripheral instances available depends on the processor selection. The required interfaces can be configured using the SysConfig-PinMux tool based on the application.

For more details, see the *Peripherals* chapter of the device-specific TRM.

7.7.1 I2C (Open-Drain and Emulated Open-Drain) Interface

7.7.1.1 AM62Lx

An external pullup is recommended for the I2C interfaces (I2C2 with I2C OD FS IO buffers) with open-drain output type buffers **only** when the IOs are configured for I2C interface or IOs. A pullup is not required in case the IOs (inputs) are being actively driven.

When open-drain output type buffer (I2C2) is pulled to 3.3V supply, the inputs have slew rate limit specified. An RC is recommended to limit the slew rate. For implementation, see the EVM *TMDS62LEVM* schematic.

An external pullup is recommended for emulated open-drain outputs (LVCMOS IOs) I2C interfaces (I2C0, I2C1, I2C3 and WKUP_I2C0) when the IOs are configured for I2C interface. For the available emulated open-drain output I2C instances, refer the device-specific data sheet.

7.7.1.2 Additional Information

For more information, see the following FAQ:

[FAQ] AM62L: Custom board hardware design – I2C interface

7.8 Analog-to-Digital Converter (ADC)

7.8.1 AM62Lx

The processor family supports 1x 12-bit Analog-to-Digital Converter (ADC), Up to 4MSPS, 4x analog inputs (time-multiplexed).

For the allowed ADC input range and electrical characteristics, see the *ADC Electrical Characteristics* section of device-specific data sheet.

For more information, see the *General Connectivity Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

Note

ADC inputs are not fail-safe. Recommendation is to apply the inputs only after the ADC supply ramps.

Take note of the allowed ADC input range while connecting the external inputs.

For connecting the ADC supply and ADC inputs when entire ADC or any of the ADC inputs are not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more information, see the following FAQ:

[FAQ] AM62L, AM64x Custom board hardware design – ADC0 design guidelines

7.9 Display Subsystem (DSS)

7.9.1 AM62Lx

The processor family provides pin outs (pin attributes defined) for DPI and DSI interfaces. The processor family supports interfacing to either the MIPI DSI (4 lanes DPHY) or DPI (24-bit RGB LVCMOS) display (external) and the selection of the processor display interface is required to be done at boot time.

For connecting the DSITX0 signals when not used, see the *Pin Connectivity Requirements* section of the device-specific data sheet.

For more details, see the *Display Subsystem and Peripherals* section in the *Peripherals* chapter of the device-specific TRM.

For more information on DPI, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 Custom board hardware design – Display Parallel Interface (DPI) 24-bit RGB

The FAQ is generic and can also be used for AM62Lx processor family.

7.10 Connection of Processor Power Supply Pins, Unused Peripherals and IOs

All the processor power supply pins are required to be supplied with the supply voltages specified in the *Recommended Operating Conditions* section of the device-specific data sheet, unless otherwise specified in the *Pin Connectivity Requirements* section.

The processor has pins (package balls) that have specific connectivity requirements and pins that are recommended to be left unconnected or can be left unconnected.

For information on connecting specific unused processor peripherals and IOs, see the *Pin Connectivity Requirements* section in the *Terminal Configuration and Functions* chapter of the device-specific data sheet.

For more information on processor unused peripherals and IOs, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P Design Recommendations / Commonly Observed Errors during Custom board hardware design – SOC Unused peripherals and IOs

The FAQ is generic and can also be used for AM62Lx processor family.

7.10.1 External Interrupt (EXTINTn)

EXTINTn is an open-drain output type buffer, fail-safe IO. Recommendation is to connect an external pullup resistor when a PCB trace is connected to the pad and an external input is not being actively driven. Open-drain output type buffer IO has slew rate specified when the IO is pulled up to 3.3V. An RC is recommended for limiting the slew.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1/ AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1 Custom board hardware design – EXTINTn pin pullup connection

The FAQ is generic and can also be used for AM62Lx processor family.

7.10.2 External Wakeup Inputs (EXT_WAKEUP0 and EXT_WAKEUP1)

EXT_WAKEUP0 and EXT_WAKEUP1 signals are the External Wakeup Inputs. These inputs are active low inputs and the recommendation is to connect as per the connectivity requirements.

Refer *Pin Connectivity Requirements* section of the device-specific data sheet for connecting the EXT_WAKEUP0 and EXT_WAKEUP1 signals.

7.10.3 Reserved (RSVD) Pin

Pin named RSVD are Reserved. Leave the RSVD pin unconnected (no TP) as recommended in the device-specific data sheet.

Recommendations are to not connect any PCB trace or test point to RSVD pin.

For more information, see the following FAQ:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 Custom board hardware design – Connection recommendations for RSVD pins

The FAQ is generic and can also be used for AM62Lx processor family.

8 Interfacing of Processor IOs (LVCMOS or Open-Drain or Fail-Safe Type IO Buffers) and Simulations

An important check point during the custom board design start of the schematics design and capture is to confirm electrical compatibility (DC and AC) between the processor and attached devices.

- The device-specific (processor and attached devices) data sheet has important information with regards to timing and electrical characteristics.
- For high-speed interfaces, recommendation is to run simulations using IBIS model provided.

For more information, see the *General Termination Details* section in the *Hardware Design Guide for KeyStone II Devices*.

For information related to drive strength configuration support, see the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62D-Q1 / AM64x / AM243x Design Recommendations / Custom board hardware design - I/O Drive Strength Configuration for SDIO and LVCMOS

The FAQ is generic and can also be used for AM62Lx processor family.

The required IBIS model can be downloaded from the link provided in the below section.

8.1 IBIS Model

- AM62Lx Sitara IBIS Model

8.2 IBIS-AMI Model

- AM62Lx Sitara AMI Model

9 Processor Current Rating and Thermal Analysis

The board power consumption depends on selected processor, peripherals connected, features implemented, application, operating temperature requirements, and temperature/voltage variations.

9.1 Power Estimation

For estimating the processor power, use AM62Lx Power Estimation Tool.

9.2 Maximum Current Rating for Different Supply Rails

For information on the maximum current rating for different supply rails, see the below:

AM62L Maximum Current Ratings

9.3 Power Modes

For more details on the available power modes (including RTC only, RTC + IO + DDR Self-refresh, DeepSleep, and so forth), see the *Power Modes* sub-section, *Power* section in the *Device Configuration* chapter of the device-specific TRM.

9.4 Thermal Design Guidelines

The *Thermal Design Guide for DSP and Arm Application Processors* application note provides guidance for successful implementation of a thermal solution for custom board designs using Sitara family of processors. The application note provides background information on common terms and methods. Any follow-up design support that may be required is provided only for board designs that follow thermal design guidelines contained in the application note.

Download the required Thermal model from the below section.

9.4.1 AM62Lx

- AM62Lx Sitara Thermal Model

9.4.2 Voltage Thermal Management Module (VTM)

A single (x1) temperature sensor is available.

See the following FAQ:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM62L / AM64x / AM243x Design Recommendations / Custom board hardware design – VTM

10 Schematic:- Design, Capture, Entry and Review

At the stage of the custom board design, schematic design, capture and entry can be started.

The following FAQ summarizes key collaterals that can be referenced during schematic design and review of the schematics.

[FAQ] AM64x, AM243x, AM62x, AM62Ax, AM62Px Custom board hardware design - Collaterals for Reference during Schematic design and Schematics Review

For guidelines on component selection, schematic capture and review, see the following sections during the schematic design and capture stage.

10.1 Selection of Components and Values

Be sure to use the recommended values including the tolerance and voltage rating in the device-specific data sheet as applicable when selecting the passive components.

10.2 Schematic Design and Capture

During the schematic design and capture stage of the custom board design, the schematic can be drawn newly or EVM schematic can be reused. For more information, see the EVM *TMDS62LEVM* schematic.

During schematic design and capture, follow below checklist and device-specific silicon errata.

AM62L (AM62L32, AM62L31) Processor Family Schematic Design Guidelines and Schematic Review Checklist

The following FAQ summarizes the considerations board designers are required to be familiar when reusing TI EVM design files.

[FAQ] AM62L: Custom board hardware design - Reusing TI EVM design files

Note

When the EVM design (schematics) is reused, make sure of completeness of functionality and change in net name due to the redesign being reviewed. Read the notes added on the schematics pages near to the circuit implementation.

When the EVM schematics is reused, the DNI settings for the components can be reset. Make sure the DNIs are reconfigured (populating DNIs can affect the functionality). Read the notes added on the schematics pages near to the circuit implementation.

10.3 Schematic Review

After completing the schematic design and capture, perform self-review using the *AM62L (AM62L32, AM62L31) Processor Family Schematic Design Guidelines and Schematic Review Checklist*.

The FAQ lists the collaterals and steps that can be followed for performing self-review of custom board schematics:

[FAQ] AM62L: Design Recommendations / Custom board hardware design - Custom board schematics self-review

For more information on handling used pins / unused pins / peripherals, see the following FAQ:

[FAQ] AM62x, AM64x, AM243x, Custom board hardware design – How to handle Used / Unused Pins / Peripherals ? (GPIOs, SERDES, USB, CSI, MMC (eMMC, SD-card), CSI, OLDI, DSI, CAP_VDDSn, ...)

The FAQ is generic and can also be used for AM62Lx processor family.

Plan a schematic review internally to review the schematic with reference to the *Schematic Design Guidelines and Schematic Review Checklist*. Verify circuit implementation for design errors, value or connection inaccuracies, missing net connections, and so forth.

Be sure to verify the schematic follows the recommendations in the *Pin Connectivity Requirements* section of the device-specific data sheet.

11 Floor Planning, Layout, Routing Guidelines, Board Layers and Simulation

After completing the schematic design, capture, entry and review (self, team and external (devices suppliers)), the recommendation is to perform floor planning of the board to determine the interconnect distances between the different devices, board size and outline.

The next stage in the custom board design is the board layout. Refer below sections for recommendations related to the board layout.

11.1 Escape Routing for PCB Design

The *AM62Lx Escape Routing for PCB Design* provides a sample PCB escape routing for the AM62Lx family of processors.

11.2 DDR Design and Layout Guidelines

For more information, see the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*. The goal of the guide is to simplify the LPDDR4 or DDR4 implementation. Requirements have been captured as a set of layout (placement and routing) guidelines that allow board designers to successfully implement a robust design for the topologies supported by the processor. Any follow-up design support that may be required will be provided only for board designs using LPDDR4 or DDR4 memory that follow the guidelines.

For the recommended target impedance for the LPDDR4 or DDR4 memory devices, see the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

For the propagation delay, the delay to be considered for LPDDR4 or DDR4 is the delay related to the traces on the board. On a need basis, the package delay that has been included in the *Additional Information: Package Delays* of *AM62x, AM62Lx DDR Board Design and Layout Guidelines* when required can be referenced.

For DDR4 data rate, device bit width, device count and LPDDR4 Count, Channel Width, Channels, Die, Ranks, see the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*. Guidelines for bit swapping/swizzling are also included.

The recommendation is to perform signal integrity (SI) simulations during board schematic design and layout stage.

Note

DDR2 and DDR3 interfaces are not supported.

11.3 High-Speed Differential Signals Routing Guidelines

The *High-Speed Interface Layout Guidelines* application note provides guidelines for successful routing of the high-speed differential signals. Guidelines include PCB stack-up and materials guidance as well as routing skew, length, and spacing limits. Any follow-up design support that is required is only provided for board designs that follow *High-Speed Interface Layout Guidelines*.

Note

Consider using the EVM *TMDS62LEVM* layout as reference as required.

11.4 Board Layer Count and Stack-up

An important constraint in determining layer count is the number of layers required to implement the high-speed DDR4 / LPDDR4 memory interface. Memory layout meeting the recommended guidelines typically requires the number of layers used in the EVM (TI recommended). Optimization of layer count can be considered based on the custom board design and functionalities.

Refer the *AM62x, AM62Lx DDR Board Design and Layout Guidelines* available on TI.com for further guidance and recommendations for implementing the DDR4 / LPDDR4 memory interface.

Refer the *AM62Lx Escape Routing for PCB Design* as a guideline during board layout. Use of TI Via Channel Array (VCA) technology with the ANB package supports layer optimization.

11.4.1 Simulation Recommendations

Simulation is recommended for any layout changes or optimizations done with respect to the EVM layout.

11.5 Reference for Steps to be Followed for Running Simulation

To get an overview of the board extraction, simulation, and analysis methodologies for high-speed LPDDR4 memory interface, see the *LPDDR4 Board Design Simulations* chapter of the *AM62x, AM62Lx DDR Board Design and Layout Guidelines*.

See the following FAQs:

[FAQ] AM625 / AM623 / AM625SIP / AM625-Q1 / AM620-Q1 / AM62A7 / AM62A3 / AM62P / AM62P-Q1/ AM6442 / AM2432 Custom board hardware design – S-parameter and IBIS model of IO-buffer

[FAQ] Using DDR IBIS Models for AM64x, AM62x, AM62Ax, AM62Px

The FAQs are generic and can also be used for AM62Lx processor family.

12 Custom Board Assembly and Testing

The next phase of custom board design is board assembly, board bring-up, functional and performance testing.

Before powering the custom board, verify that no components marked as DNP or DNI in the design are mounted.

Do not apply external input before the processor IO supplies ramps.

Validate that none of the processor IO pullups have the supply rail referenced to the power source that is available before the processor IO supplies ramp.

12.1 Guidelines and Board Bring-up Tips

For more information, see the following FAQs during board bring-up:

[FAQ] AM625 / AM623 / AM62A / AM62P / AM64x / AM243x Design Recommendations / Commonly Observed Errors during Circuit Optimization of Custom board hardware design

[FAQ] Board bring up tips for Sitara devices (AM64x, AM243x, AM62x, AM62Ax, AM62Px)

[FAQ] AM625 / AM623 / AM62A Design Recommendations / Commonly Observed Errors during Custom board hardware design – SK Schematics Design Update Note

The FAQs are generic and can also be used for AM62Lx processor family.

13 Device Handling and Assembly

Moisture Sensitivity Level (MSL) rating/peak reflow rating depends on the package dimensions (thickness and volume).

Recommended reviewing the device thickness information, ball pitch, lead finish/ball material and the recommended MSL rating/peak reflow to be followed.

For more information, see the link below:

- AM62L Ordering & quality

Look for AM62L32 in the Ordering and Quality section.

13.1 Soldering Recommendations

Note the MSL rating/Peak reflow recommendation on TI.com for the selected processor.

13.1.1 Additional References

For more information on Moisture sensitivity level, see the following:

- *MSL Ratings and Reflow Profiles*
- Moisture sensitivity level search

14 References

14.1 Processor-Specific

- Texas Instruments: *AM62Lx Sitara Processors Data Sheet*
- Texas Instruments: *AM62L Sitara Processors Technical Reference Manual*
- Texas Instruments: *AM62Lx Sitara Processors Silicon Errata*
- Texas Instruments: *AM62L32, AM62L31 Processor Family Schematic Design Guidelines and Schematic Review Checklist*
- Texas Instruments: *EVM TMDS62LEVM*
- Texas Instruments: *AM62x, AM62Lx DDR Board Design and Layout Guidelines*
- Texas Instruments: *AM62Lx Escape Routing for PCB Design*
- Texas Instruments: *AM62L Maximum Current Ratings*
- Texas Instruments: *AM62L Power Supply Implementation*
- Texas Instruments: *AM62L Product Overview*
- Texas Instruments: *Sitara AM62L Benchmarks*

14.2 Common

- Texas Instruments: *AM623, AM625, AM625SIP, AM620-Q1, AM625-Q1, AM62A3, AM62A7, AM62A7-Q1, AM62D-Q1, AM62P-Q1 Schematic, Design Guidelines and Review Checklist*
- Texas Instruments: *Thermal Design Guide for DSP and Arm Application Processors*
- Texas Instruments: *Sitara Processor Power Distribution Networks: Implementation and Analysis*
- Texas Instruments: *Emulation and Trace Headers Technical Reference Manual*
- Texas Instruments: *XDS Target Connection Guide*
- Texas Instruments: *High-Speed Interface Layout Guidelines*
- Texas Instruments: *High-Speed Layout Guidelines*
- Texas Instruments: *Jacinto7 AM6x, TDA4x, and DRA8x High-Speed Interface Design Guidelines*
- Texas Instruments: *General Hardware Design/BGA PCB Design/BGA Decoupling*
- Texas Instruments: *MSL Ratings and Reflow Profiles*
- Texas Instruments: *Moisture sensitivity level search*
- Texas Instruments: *TIDA-01413 - ADAS 8-Channel Sensor Fusion Hub Reference Design*
- Texas Instruments: *Jacinto™ 7 DDRSS Register Configuration Tool*
- Texas Instruments: *Hardware Design Guide for KeyStone II Devices*
- Texas Instruments: *Clocking Design Guide for KeyStone Devices*
- Texas Instruments: *Using IBIS Models for Timing Analysis*
- Texas Instruments: *Display Interfaces: A Comprehensive Guide to Sitara MPU Visualization Designs*

15 Terminology

ADC	Analog-to-Digital Converter
BSDL	Boundary-Scan Description Language
CAN	Controller Area Network
CAN-FD	Controller Area Network Flexible Data-Rate
CPPI	Communications Port Programming Interface
CPSW3G	Common Platform Ethernet Switch 3-port Gigabit
DPI	Display Parallel Interface
DSI	Display Serial Interface
DSITX	Display Serial Interface Transmitter
DRD	Dual-Role Device
E2E	Engineer to Engineer
ECAP	Enhanced Capture
ECC	Error-Correcting Code
eMMC	embedded Multi-Media Card
EMU	Emulation Control
EPWM	Enhanced Pulse-Width Modulator
EQEP	Enhanced Quadrature Encoder Pulse
FAQ	Frequently Asked Question
GPIO	General Purpose Input/Output
GPMC	General-Purpose Memory Controller
HS-RTDX	High-Speed Real Time Data eXchange
I2C	Inter-Integrated Circuit
IBIS	Input/Output Buffer Information Specification
JTAG	Joint Test Action Group
LDO	Low-Dropout
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
MAC	Media Access Controller
MCASP	Multichannel Audio Serial Ports
MCSPI	Multichannel Serial Peripheral Interfaces
MCU	Micro Controller Unit
MMC	Multi-Media Card
MSL	Moisture Sensitivity Level
OSPI	Octal Serial Peripheral Interface
OTP	One-Time Programmable
PCB	Printed Circuit Board
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-on Reset
QSPI	Quad Serial Peripheral Interface
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface

ROC	Recommended Operating Condition
RTC	Real-Time Clock
SD	Secure Digital
SDIO	Secure Digital Input Output
SDK	Software Development Kit
SPI	Serial Peripheral Interface
TCK	Test Clock Input
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select Input
TRM	Technical Reference Manual
TRSTn	Test Reset
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VCA	Via Channel Array
VTM	Voltage Thermal Management Module
WKUP	Wakeup
XDS	eXtended Development System

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