TMS320UC5402/TMS320VC5402

Digital Signal Processors

Silicon Errata

SPRZ155D
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Contents

1 Introduction

This document describes the silicon updates to the functional specifications for the TMS320UC5402/TMS320VC5402. The updates are applicable to:

- TMS320UC5402 (144-pin LQFP, PGE suffix)
- TMS320UC5402 (144-pin MicroStar BGA™, GGU suffix)
- TMS320VC5402 (144-pin LQFP, PGE suffix)
- TMS320VC5402 (144-pin MicroStar BGA™, GGU suffix)

1.1 Quality and Reliability Conditions

TMX Definition

Texas Instruments (TI) does not warranty either (1) electrical performance to specification, or (2) product reliability for products classified as “TMX.” By definition, the product has not completed data sheet verification or reliability performance qualification according to TI Quality Systems Specifications.

The mere fact that a “TMX” device was tested over a particular temperature and voltage ranges should not, in any way, be construed as a warranty of performance.

TMP Definition

TI does not warranty product reliability for products classified as “TMP.” By definition, the product has not completed reliability performance qualification according to TI Quality Systems Specifications; however, products are tested to a published electrical and mechanical specification.

TMS Definition

Fully-qualified production device.

1.2 Revision Identification

The device revision can be determined by the lot trace code marked on the top of the package. The locations for the lot trace codes for the PGE and the GGU packages are shown in Figure 1 and Figure 2, respectively. The location of other markings may vary per device.

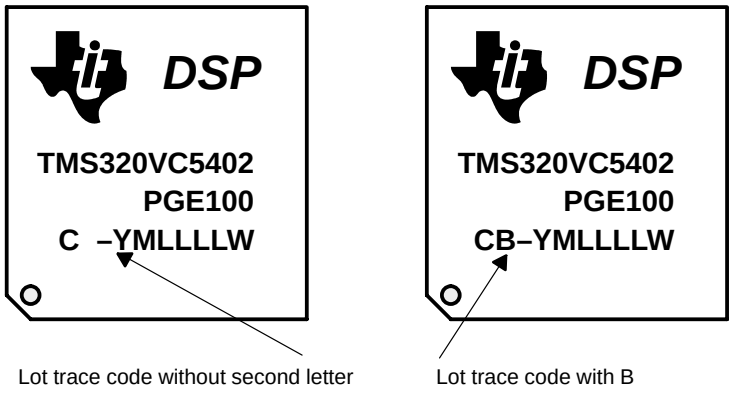

Figure 1. Example, Typical Lot Trace Code for TMS320VC5402 (PGE)

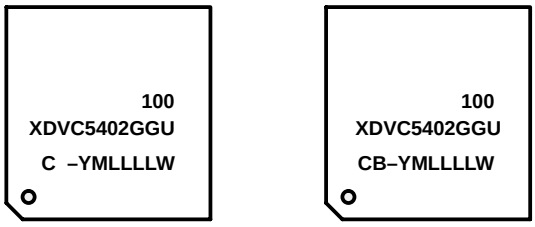

Figure 2. Example, Typical Lot Trace Code for TMS320VC5402 (GGU)

NOTE: Qualified devices in the PGE package are marked with the letters “TMS” at the beginning of the device name, while nonqualified devices in the PGE package are marked with the letters “TMX” or “TMP” at the beginning of the device name. Similarly, qualified devices in the GGU package are marked with the letters “DV” at the beginning of the device name, and nonqualified devices in the GGU package are marked with the letters “XDV” or “PDV” at the beginning of the device name.

Lot Trace Code	Silicon Revision	Comments
Blank (no second letter in prefix)	Initial Silicon	This silicon revision is available as TMX only.
A (second letter in prefix is A)	Silicon Revision A	No revision A silicon ever existed for this device.
B (second letter in prefix is B)	Silicon Revision B	This silicon revision is available as TMX and TMS.
C (second letter in prefix is C)	Silicon Revision C	This silicon revision is available as TMS only.
D (second letter in prefix is D)	Silicon Revision D	This silicon revision is available as TMS only and is 100% functionally equivalent to Revision C.
E (second letter in prefix is E)	Silicon Revision E	This silicon revision is available as TMS only and is 100% functionally equivalent to Revision D.

2 Known Design Marginality/Exceptions to Functional Specifications

Table 1. Summary of Exceptions

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Bootloader End-of-Boot Detection in 8-Bit I/O Mode	Initial Silicon	10
Bootloader Block Size in 8-Bit Parallel Mode	None	10

† This bootloader feature is not available in the initial silicon.

Advisory *DMPREC*

Revision(s) Affected: Initial Silicon, Revisions B, C, D, and E Silicon

Details: When updating the DE bits of the DMPREC register while one or more DMA channel transfers are in progress, it is possible for the write to the DMPREC to cause an additional transfer on one of the active channels.

The problem occurs when an active channel completes a transfer at the same time that the user updates the DMPREC register. When the transfer completes, the DMA logic attempts to clear the DE bit corresponding to the complete channel transfer, but the register is instead updated with the CPU write (usually an ORM instruction) which can set the bit and cause an additional transfer on the channel. Refer to the example below for further clarification:

Example:

DMPREC value = 00C1h, corresponding to the following channel activity:

Channel 0 – enabled and running.	(DE0 = 1)
Channel 1 – disabled.	(DE1 = 0)
Channel 2 – disabled.	(DE2 = 0)
Channel 3 – disabled.	(DE3 = 0)
Channel 4 – disabled.	(DE4 = 0)
Channel 5 – disabled.	(DE5 = 0)

If the following conditions occur simultaneously:

Channel 0 transfer completes and DMA logic clears DE0 internally.

User code attempts to enable another channel (e.g., ORM #2, DMPREC)

The user code will re-enable channel 0 (DMPREC value written = 00C3h), and an additional, unintended transfer will begin on channel 0.

Workaround: There are a few use conditions under which this problem does not occur. If all active DMA channels are configured in ABU mode or in auto initialization mode, then the problem does not occur because the channels remain enabled until they are disabled by user code. The problem is also avoided in applications that use only one DMA channel at a time.

Systems that use multiple DMA channels simultaneously in multiframe mode, without autoinitialization are most likely to have this problem. In such systems one of the following methods can be used to avoid the problem:

- Always wait for all channels to complete existing transfers before re-enabling any channels, and always enable all channels at the same time.
- Before enabling a channel, check the progress of any on-going transfers by reading the element and frame counts of each active channel. If any active channel is within two element transfers of completing a block transfer, then wait until the active channel completes the block transfer before writing to the DMPREC register. Otherwise, if all active channels have more than two element transfers left in a block transfer, it is safe to update the DMPREC register.

Advisory *Round (RND) Instruction Clears Pending Interrupts*

Revision(s) Affected: Initial Silicon, Revisions B, C, D, and E Silicon

Details: The round (RND) instruction opcode is decoded incorrectly and will write to the interrupt flag register (IFR) with the data from the data write bus (E bus). Therefore, it could cause the pending interrupt to be missed.

Workaround: Replace the RND instruction with an ADD instruction as follows:

For this instruction ...	**Use ...**
`RND src[,dst]`	`ADD #1,15,src[,dst]`

Advisory *Far Branches/Calls/Interrupts from Active Repeat Blocks (BRAF)*

Revision(s) Affected: Initial Silicon, Revisions B, C, D, and E Silicon

Details: When a block repeat is interrupted by a far call, far branch, or interrupt to another page; and a program memory address in the called routine happens to have the same lower 16 bits as the block-repeat end address (REA), a branch to the 16-bit block-repeat start address (RSA) is executed on the current page until the block-repeat counter decrements to 0. The XPC is ignored during these occurrences.

Workaround: Use one of the following workarounds:

1. If the called routine must be on a different page and has a program memory address that has the same lower 16 bits as the REA, save ST1 and clear the BRAF in the vector table before entering the called routine with the following two instructions:

   ```
   PSHM ST1
   RSBX BRAF
   ```

   Then, restore ST1 before returning from the called routine. In the case of an interrupt service routine, these two instructions can be included in the delay slots following a delayed-branch instruction (BD) at the interrupt vector location. Then, the ST1 is restored before returning from the routine. With this method, BRAF is always inactive while in the called routine. If BRAF was not active at the time of the call, the RSBX BRAF has no effect.
2. Put the called routine on the same page as the interruptible block-repeat code. This can be achieved automatically by placing the interrupt vector table and the interrupt service routines or other called routines on the overlay pages. If this approach is used, far branches/calls are not necessary and the bug is completely avoided.
3. Avoid putting the called routine on other pages where a program memory address has the same lower 16 bits as the REA.
4. Use the BANZ instruction as a substitute for the block repeat.

Advisory *NMI*

Revision(s) Affected: Initial Silicon, Revisions B, C, D, and E Silicon

Details: An NMI can be ignored if the internal CPU interrupt logic is not adequately prepared.

Workaround: Avoid generating an NMI during the time when other interrupts are being serviced. Alternatively, use one of the other external interrupts, appropriately enabled, to serve the NMI function.

Advisory *HPI Hint*

Revision(s) Affected: Initial Silicon, Revisions B, C, D, and E Silicon

Details: The HPI will become locked up, with HRDY stuck low, if both the host processor and the 5402 CPU write a one (1) to HINT at the same time.

Workaround: Do not perform redundant operations to the HINT bit. Both the HOST and the CPU should check to see if HINT is set before trying to write a one (1) to this bit.

For ...	IF ...	Then ...
the HOST	HINT is ***not*** set ...	Do not try to clear HINT by writing a one (1) to it, because the CPU may try to set it.
the CPU	HINT is ***already*** set...	Do not try to set HINT again by writing a one (1) to it, since the HOST may try to clear it.

Advisory *Bootloader Destination Address in 8-Bit Parallel Mode*

Revision(s) Affected: Initial Silicon and Revision B Silicon

Details: When the bootloader is used in 8-bit parallel mode, the destination address may be incorrectly generated due to a sign extension error. This problem depends on the contents of the boot table and may not occur in all cases.

Workaround: D8–D15 should be pulled down or driven low during boot load in this mode.

This problem is corrected in Revision C silicon.

Advisory *Bootloader Serial EEPROM Mode*

Revision(s) Affected: Revision B Silicon (This feature is not available in the Initial silicon.)

Details: The McBSP drives data on the rising edge of the clock, and latches input data on the falling edge; while the SPI-based EEPROMs latch input data on the rising edge of the clock, and drive data on the falling edge. This causes unreliable operation since both the McBSP and EEPROM are latching data at the same clock edge that the data signal transitions.

Workaround: Using an external inverter to invert the BCLKX signal provides a reliable boot-load setup. This workaround has the disadvantage of requiring an external component.

This problem is corrected on Revision C silicon.

Advisory *Bootloader 8-Bit Standard Serial Boot Mode*

Revision(s) Affected: Initial Silicon

Details: The McBSP1 8-bit standard serial port mode is configured incorrectly. McBSP1 cannot be used for bootloading in standard serial port boot mode.

Workaround: None. This problem is corrected in Revision B silicon.

Advisory *IDLE3 Current*

Revision(s) Affected: Initial Silicon

Details: The quiescent power supply current on the CVDD (1.8 V) supply of the initial silicon has been observed to range from several hundred microamps (μA) to approximately 1 mA.

Workaround: None. This problem is corrected in Revision B silicon.

Advisory *Boundary Scan*

Revision(s) Affected: Initial Silicon

Details: Two problems have been discovered in the boundary scan feature of the initial silicon.

1. The test output (TDO) signal is derived from the rising edge of the test clock (TCK) signal, while IEEE Standard 1149.1† requires TDO to be derived from the falling edge of TCK. This shift of the TDO waveform can cause timing violations for some boundary scan testing systems.
2. The sampling circuit for inputs can be affected. In the existing implementation of the boundary scan chain, indeterminate values are captured for input pins.

Workaround: None. This problem is corrected in Revision B silicon.

Advisory *Bootloader End-of-Boot Detection in 8-Bit I/O Mode*

Revision(s) Affected: Initial Silicon

Details: In 8-bit I/O boot mode, the bootloader incorrectly interprets the end of the first data block because of a failure to mask the upper bits in the accumulator when the end-of-block marker (0000h) is evaluated. The result is that code can be loaded using this mode, but the bootloader will not branch to the loaded code.

Workaround: None. This problem is corrected in Revision B silicon.

Advisory *Bootloader Block Size in 8-Bit Parallel Mode*

Revision(s) Affected: None

Details: This problem does not affect any 5402 silicon revisions. This text remains as an override note for the previous revision of this document, which incorrectly states that the initial silicon is affected.

Workaround: Not applicable

† IEEE Standard 1149.1 – 1990, IEEE Standard Test-Access Port

3 Documentation Support

For device-specific data sheets and related documentation, visit the TI web site at: **http://www.ti.com.**

For further information regarding the TMS320UC5402/TMS320VC5402, please refer to:

- *TMS320UC5402 Fixed-Point Digital Signal Processor* data sheet, literature number SPRS096
- *TMS320VC5402 Fixed-Point Digital Signal Processor* data sheet, literature number SPRS079
- *TMS320C54x™ DSP Functional Overview,* literature number SPRU307

The five-volume *TMS320C54x DSP Reference Set,* literature number SPRU210, consisting of:

- *Volume 1: CPU and Peripherals,* literature number SPRU131
- *Volume 2: Mnemonic Instruction Set,* literature number SPRU172
- *Volume 3: Algebraic Instruction Set,* literature number SPRU179
- *Volume 4: Applications Guide,* literature number SPRU173
- *Volume 5: Enhanced Peripherals,* literature number SPRU302

The reference set describes in detail the TMS320C54x™ DSP products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

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