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Want to optimize and improve efficiency of an automated factory setup, increase overall performance in a data-acquisition system, or efficiently detect and correct faults to reduce downtime? If the answer is yes to any or all of the above, you may want to consider enabling clock synchronization with a [network synchronizer](#).

What Is Clock Synchronization?

Ethernet traditionally connected wired local area networks in telecommunications systems; of late, it has become the de facto standard for connecting subsystems in industrial and automotive applications. A reference clock is required for an Ethernet link to operate and is usually generated from a free-running clock source. Clock synchronization is the ability to generate clocks in a subsystem that are traceable to a single master clock in the overall system.

Clock synchronization is useful for many end applications. For example:

- In factory automation, clock synchronization enables the synchronization of tasks and events over programmable logic controllers, sensors, actuators, drives and remote inputs/outputs.
- In medical imaging, clock synchronization enables fast data acquisition with multiple detectors.
- In software-defined radios, clock synchronization enables object detection with the utmost precision.
- In a communications infrastructure, clock synchronization enables the exchange of time-critical information at a high data rate with the least amount of interference.

Ethernet is a popular serial communication standard due to its cost-effectiveness and ability to support links as low as 10 Mbps or as high as 400 Gbps. Since the Ethernet standard doesn't natively support synchronization, there are multiple ways to enable synchronization via Ethernet links. There are two aspects of synchronization:

- Time synchronization is handled via the Institute of Electrical and Electronics Engineers 1588 Precision Time Protocol or Network Time Protocol. In modern systems, time synchronization is handled as part of a software stack residing in the central processing unit or a field-programmable gate array.
- Frequency synchronization is handled via synchronous Ethernet, where the reference clock for a serializer-deserializer block is traceable to a single master clock. [Clock jitter cleaners](#) are typically implemented for frequency synchronization.

An Ethernet link is established by embedding a clock into the serialized data stream on the transmit section and then recovering the embedded clock before deserializing the data stream on the receive section. In synchronous Ethernet, it is important for designers to choose a clocking device that generates the reference clock for the subsystem. If the recovered clock from the receive Ethernet physical layer (PHY) exhibits poor jitter performance, phase-locked loops (PLLs) with external voltage-controlled crystal oscillators (VCXOs) can clean the excess jitter and present a clean clock to the transmit Ethernet PHY and other parts of the system. [Figure 1](#) shows such a setup, with a Gigabit Ethernet link between the different nodes.

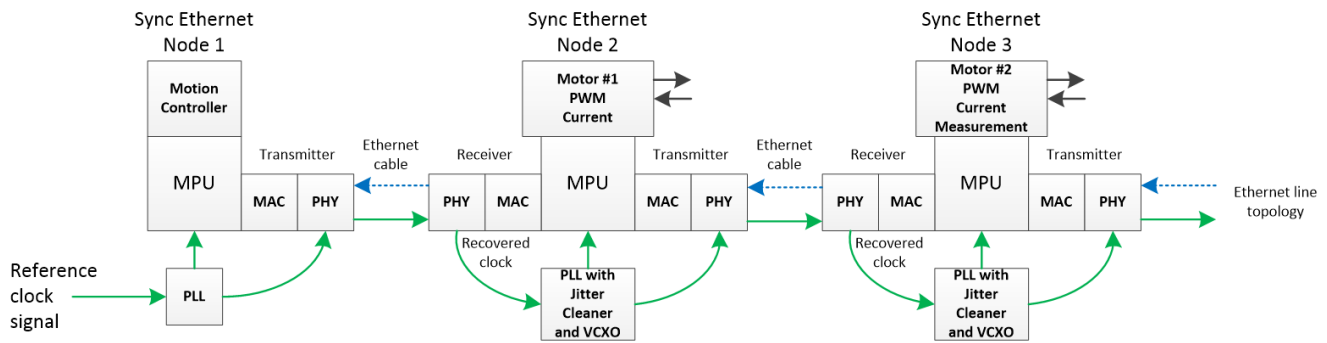


Figure 1. Frequency Synchronization Using a VCXO-based Jitter Cleaner

The main challenges of such a setup are:

- Increased cost, because you need an external VCXO to meet the phase-noise mask of the Ethernet transmit PHY.
- Increased board space, because you need external analog loop-filter components for jitter cleaning.
- Increased overall design complexity and time, because multiple external components require a more thoughtful design.

The [LMK05318 network synchronizer clock](#) is an ultra-high-performance clock generator and jitter cleaner that can address the challenges I described above and still exceed the stringent requirements of telecom and industrial applications. The device features TI's proprietary [bulk acoustic wave \(BAW\)](#) resonator as a voltage-controlled oscillator (VCO). The BAW resonator is a high-quality-factor (high-Q) resonator that replaces the inductor-capacitor oscillator commonly found in network synchronizer integrated circuits. It is a thin-film resonator similar to a quartz crystal, sandwiched between metal films and other layers to confine the mechanical energy. The result is a high-Q, ultra-low-noise resonator that can achieve ultra-low jitter performance.

[Figure 2](#) shows the basic structure of the LMK05318. Using the ability to set a low loop bandwidth either on the digital phase-locked loop (DPLL) or the all-digital PLL (APLL) with the BAW VCO, the LMK05318 cleans reference clock jitter and simplifies overall printed circuit board (PCB) design by relying on inexpensive off-the-shelf components around the device.

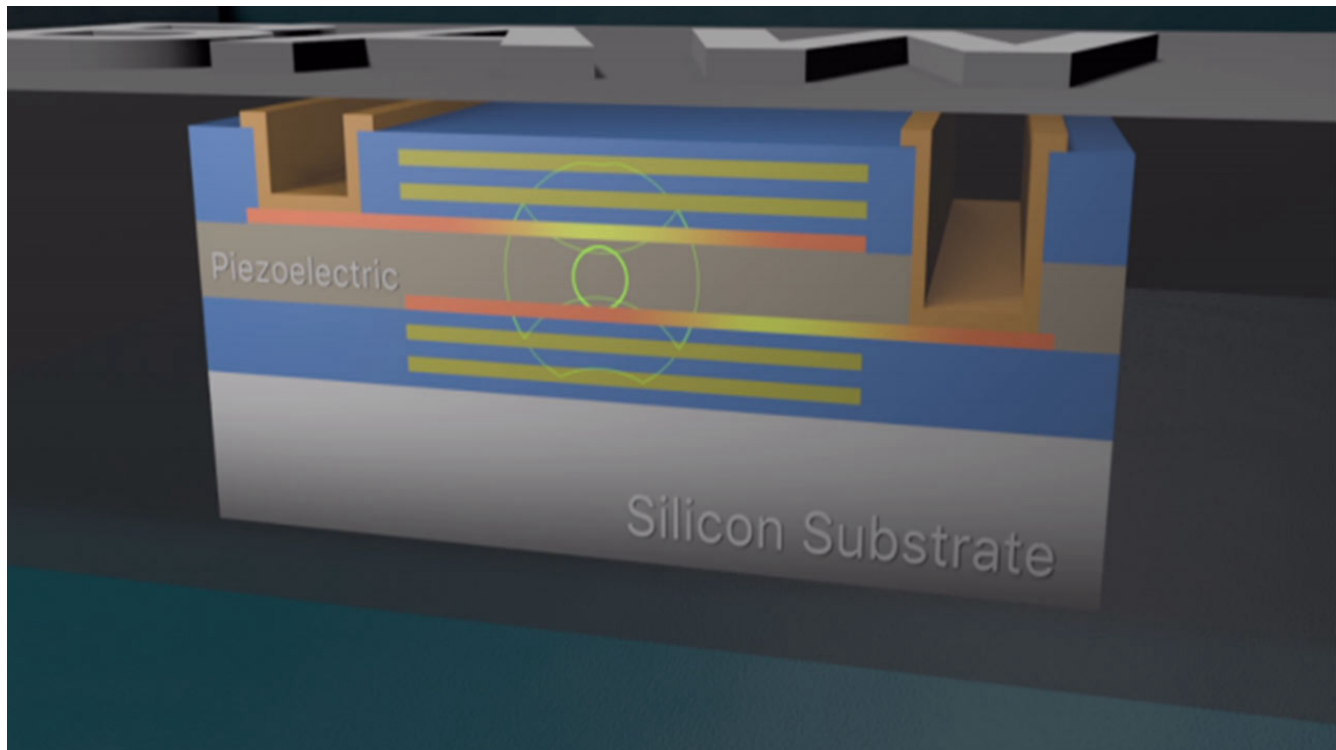


Figure 2. Basic Structure of a BAW Resonator

The LMK05318 can act as a jitter cleaner in two configurations:

- With a DPLL loop bandwidth greater than 10 Hz, the reference input clock jitter can be cleaned with a crystal oscillator as reference to the APLLs. The advantage of this configuration is the ability to clean low-frequency noise present on the reference input clock. In addition, if there is a phase-noise requirement for the low offset frequencies, jitter cleaning with the DPLL provides the lowest possible in-band phase noise.
- With the DPLL powered down, you can use APLL1 with a loop bandwidth in the range of 100 Hz to 1 kHz to clean high-frequency noise on the reference input clock. The advantage of this configuration is the ability to clean high-frequency noise without an external crystal oscillator, even when there is no explicit phase-noise requirement for the low offset frequencies. The APLL1 configuration enables a cost-effective solution that occupies a small overall area. Reliability improves because you do not need any crystal-based component and no external loop-filter components, unlike competing jitter cleaners.
- [Figure 3](#) shows a simpler clocking scheme with the LMK05318 providing the reference clocks for the Gigabit Ethernet link between the different nodes, the [AM6548](#) system on chip as the processing unit, and the [DP83869HM with high-immunity gigabit Ethernet PHY](#) acting as the Ethernet PHY.

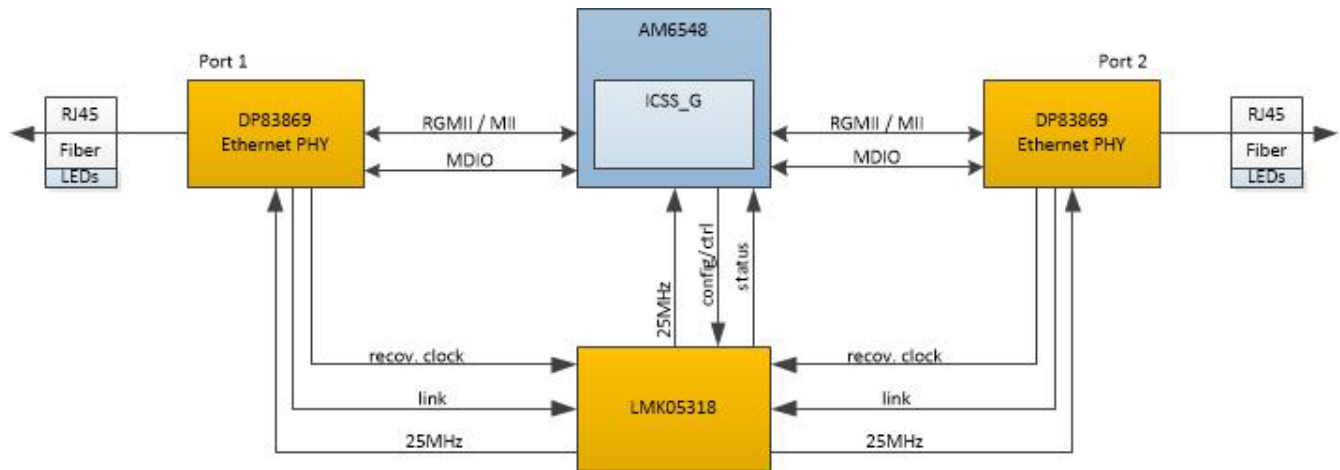


Figure 3. Frequency Synchronization Using the LMK05318

Ultra-high-performance clock jitter cleaners and synchronizers from TI like the LMK05318 simplify the clock tree for enabling clock synchronization in real-time Ethernet while reducing the design cycle, PCB real estate and overall system costs.

Additional Resources

- Check out the white paper, [“TI BAW technology enables ultra-low jitter clocks for high-speed networks.”](#)
- Read these application reports:
 - [“Understanding clocking needs for high-speed 56G PAM-4 serial links.”](#)
 - [“How to use the LMK05318 as a jitter cleaner.”](#)
- Watch the video, [“TI’s Bulk Acoustic Wave Clocking Technology.”](#)

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