Technical Article

Four-switch Buck-boost Layout Tip No. 1: Identifying the Critical Parts for Layout

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Layout is very critical to the successful operation of a buck-boost converter. A good layout begins by identifying these critical components, as shown in Figure 1:

- High di/dt loops or hot loops.
- High dv/dt nodes.
- Sensitive traces.

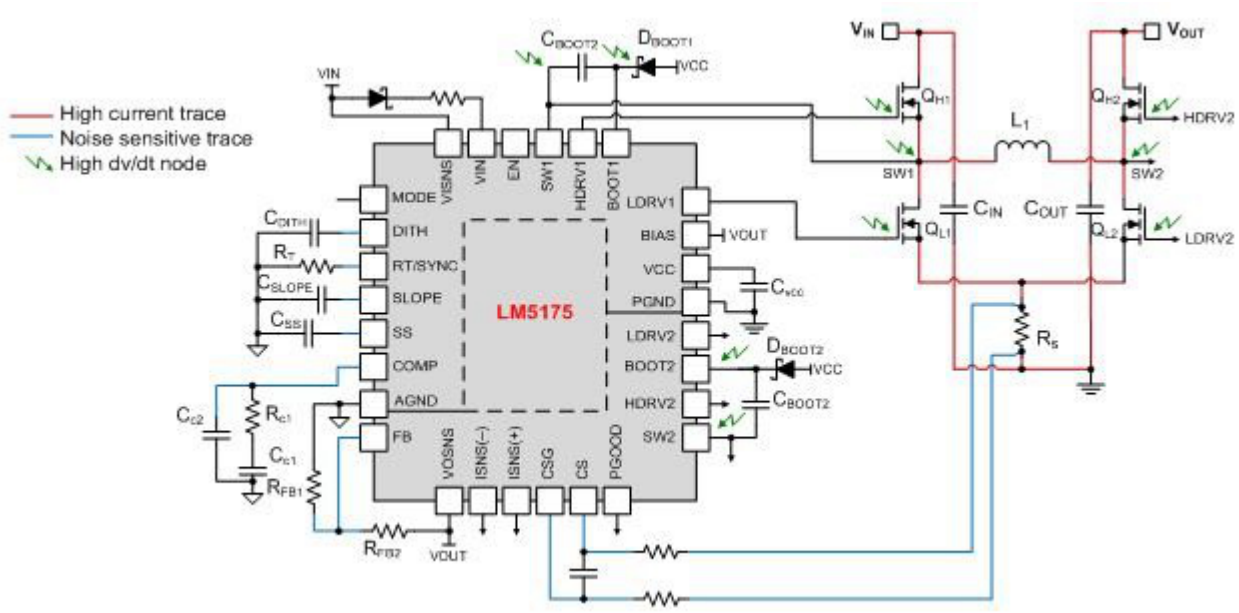

Figure 1. Identifying High Di/dt Loops, High Dv/dt Nodes and Sensitive Traces

Figure 1 shows the high di/dt paths in the LM5175 four-switch buck-boost converter. The most dominant high di/dt loops are the input-switching current loop and output-switching current loop. The input loop consists of an input capacitor (C_{IN}), MOSFETs (Q_{H1} and Q_{L1}), and a sense resistor (R_s). The output loop consists of an output capacitor (C_{OUT}), MOSFETs (Q_{H2} and Q_{L2}), and a sense resistor (R_s).

The high dv/dt nodes are those with fast voltage transition. These nodes are switch nodes (SW1 and SW2), boot nodes (BOOT1 and BOOT2), and gate-drive traces (HDRV1, LDRV1, HDRV2 and LDRV2), along with their return paths.

The current-sense traces from resistor R_s to the integrated circuit (IC) pins (CS and CSG), the input and output sense traces (VISNS, VOSNS, FB), and the controller components (SLOPE, R_{c1}, C_{c1}, C_{c2}) form the noise-sensitive traces. They are shown in blue in Figure 1.

For good layout performance, minimize the loop areas of high di/dt paths, minimize the surface areas of high dv/dt nodes, and keep the noise-sensitive traces from the noisy (high di/dt and high dv/dt) portions of the circuit. In the other two installments of this series, I'll look at each of these in detail in the context of the four-switch buck-boost converter. My next topic will include an example for optimizing hot loops.

Additional Resources

- Check out my 2016-2017 Power Supply Design Seminar topic, “Under the hood of a non-inverting buck-boost converter.”

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