Technical Article

Differential Pairs: How an Equalizer Solves Insertion-loss Impairment

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In T.K. Chin's blog post, "Differential pairs: what you really need to know," he talked about the requirements for a differential pair. In the real world, differential pairs are implemented with either copper traces in a printed circuit board (PCB) or copper wires in a cable assembly. Long PCB traces or cables exhibit high transmission loss that degrades signal quality. In this post, I will explain how insertion loss of a differential pair impacts signal quality, and how an equalizer corrects this impairment.

What Is Insertion Loss?

Transmission loss consists of two parts: skin loss at low frequency and dielectric loss at high frequency. Skin loss depends on the cross-sectional area of an interconnect; for example, the width and metal thickness of a PCB trace, or a cable's wire diameter. At frequencies below a few hundred megahertz, skin loss is dominant and proportional to the square root of the frequency. At higher frequencies, dielectric loss becomes the dominant transmission loss. The amount of dielectric loss depends on the material property of the dielectric and is directly proportional to the frequency.

Insertion loss is a common term used to describe the transmission loss of an interconnect. It is a ratio of the voltages at the load with and without the interconnect. A network analyzer measures insertion loss in amplitude and phase. Figure 1 shows the typical insertion loss of two PCB traces on FR4 substrate: one being 5 inches long (blue) and the other 10 inches (red), but both having equal width of 5 mil. As you can see from Figure 1, the loss characteristic behaves as a low-pass filter, with higher signal attenuation as the frequency increases. The loss increases linearly with the length of the PCB trace.

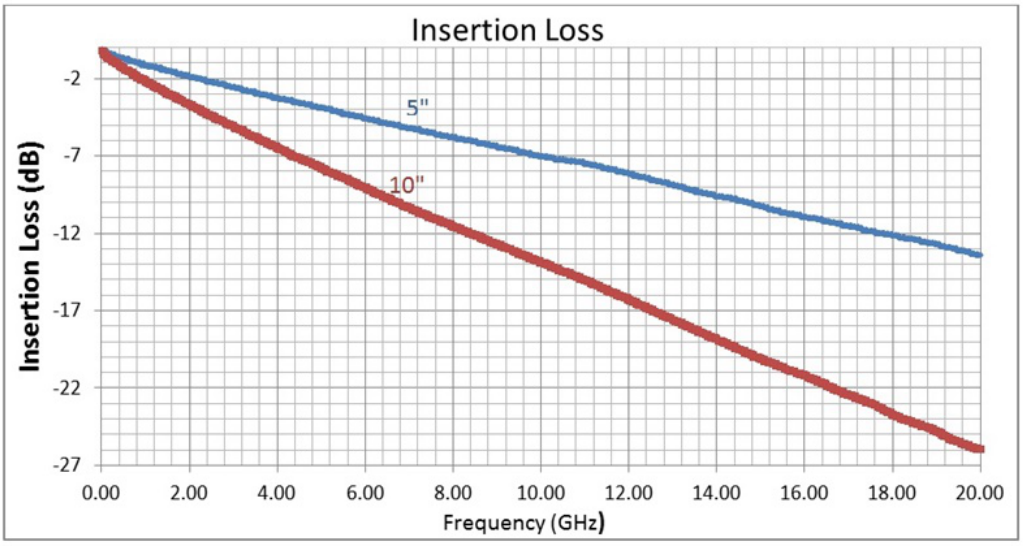

Figure 1. Insertion Loss of FR4 PCB Traces

Why Insertion Loss Hurts Signal Quality

Data traffic consists of logic 1s and 0s of various durations in a serial bit-stream. In Figure 2, you can see that the transmitter waveform consists of data bits of longer duration (lower-frequency pulses) and shorter duration (higher-frequency pulses). Their amplitudes are approximately equal and the transition paths are almost identical, resulting in a clean and wide-open data eye.

When the signal propagates through the PCB trace, the low-pass-filter effect slows down the pulses' transition times – there is not enough time for the short-duration pulses to reach their full amplitudes. The high-frequency pulses are also attenuated more than the low-frequency pulses: their amplitudes are quite different when they reach the destination. With different amplitudes from longer and shorter pulses, the transition paths vary and result in timing jitter. This timing jitter is data-dependent and is commonly called inter-symbol interference (ISI). Figure 2 illustrates the receiver waveform and the corresponding eye diagram with significant added jitter caused by the insertion loss of the differential pair.

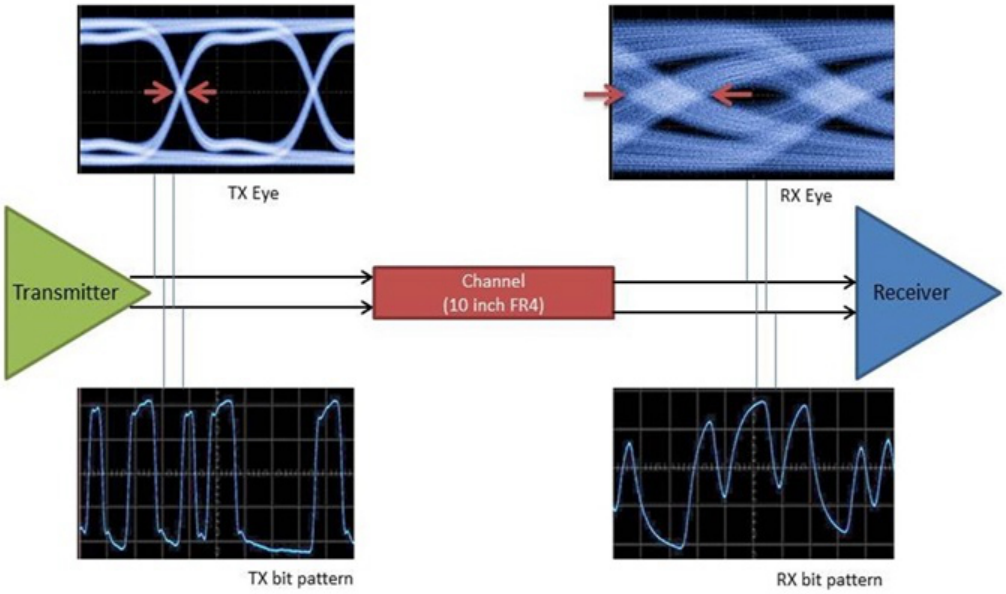

Figure 2. Signal Integrity Degradation Caused by Insertion Loss

How a TI Equalizer Solves This Impairment

The fundamental problem of signal degradation is caused by unequal pulse amplitudes resulting from a low-pass filter. The solution to this problem is to correct the signal attenuation, with the goal to achieve an equal pulse amplitude. An equalizer is a high-pass filter designed with a transfer function equal to the reciprocal of the interconnect's low-pass filter. There are many common implementations of equalizers. You could use a continuous-time linear equalizer (CTLE) implemented with a high-gain active filter that provides more gain at high frequency and less gain at low frequency. Or you could use a high-pass filter implemented with attenuation at lower frequencies, commonly used as a transmitter equalizer in many de-emphasis driver designs. There are also many digital implementations with finite impulse response filters (FIRs) or decision feedback equalizers (DFEs) commonly used in retimers.

Figure 3 illustrates the TI DS125BR800A with a CTLE to correct the ISI caused by the interconnect. By choosing the proper amount of equalization comparable to the insertion loss characteristic of the interconnect, the repeater cleans up the ISI and delivers a clean data eye at the receive destination.

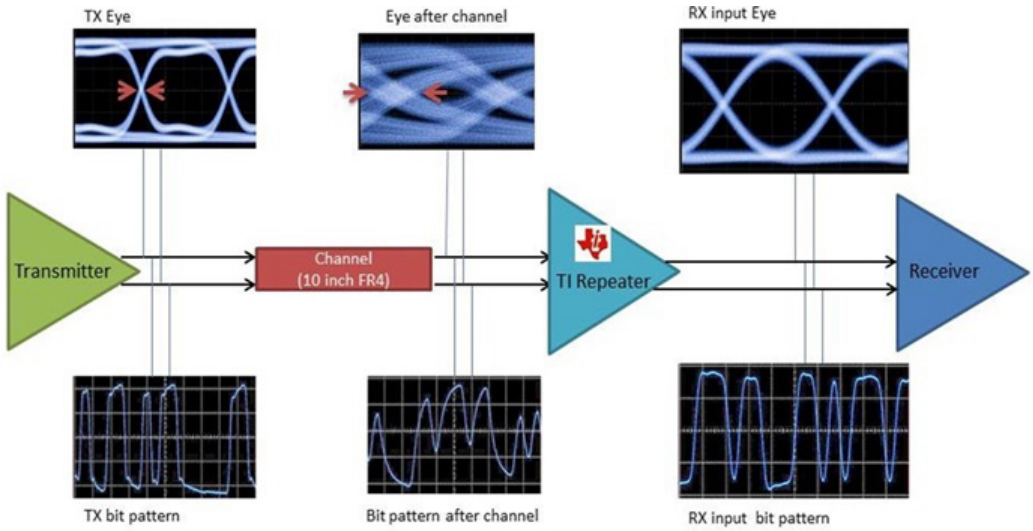

Figure 3. A CTLE repeater corrects ISI

Texas Instruments' broad portfolio of signal-conditioning devices can enable you to compensate for differential pair impairments and address the needs of many common communication protocols.

Additional Resources

- To learn more about Peripheral Component Interconnect Express (PCIe) repeaters, check out the PCIe redrivers/repeaters product selection tool.
- To learn more about multiprotocol repeaters, check out the redrivers/repeaters product selection tool.
- See an overview of TI retimers with advanced adaptive CTLE and DFE equalization.
- See an overview of broadcast video equalizers and reclockers for SMPTE applications.
- Read more about the WEBENCH® Interface Designer tool, an easy way to run simulations with TI signal-conditioning integrated circuits (ICs) to solve differential pair impairments.

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