Technical Article
Oh Yes! My FPGA Application Is Safe

TEXAS INSTRUMENTS

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We all know that new technologies in our life pose great opportunities and possibilities but also new challenges. For example, smartphones and tablets give us 24/7 access to the world around us but also create such dependency that it might be impossible to put them down.

In the same way, advances in chip-level technology help create endless opportunities but also create challenges. With new, smaller process nodes and lower-core voltage rails, we are seeing the benefits of greater integration and higher efficiency. At the same time, it has also created challenges with variations in silicon performance due to corner spread and process variations. To combat these silicon process variations, vendors are specifying power-supply rails with tighter tolerances (See Table 1).

Table 1. Xilinx Virtex-7 Power-supply Requirements

Power rail	Nominal voltage (V)	Tolerance	Description
VCCINT	1.0	±3%	Voltage supply for the internal core logic
VCCAUX	1.8	±5%	Voltage supply for auxiliary logic

From a voltage monitoring/supervision perspective, lower supply rails with tighter tolerances pose challenges for system designers, requiring them to protect the data and move the system to a safe mode when FPGAs, ASICs or memory banks are exposed to high voltage spikes.

A typical voltage-monitor integrated circuit (IC) will have wide voltage threshold accuracy, varying hysteresis, poor glitch immunity and no overvoltage detection. These inaccuracies cause reset to occur outside the narrow tolerance band (Figure 1), trigger false resets within the nominal supply range, and create susceptibility to overvoltage and undervoltage transients, which might put the system at risk.
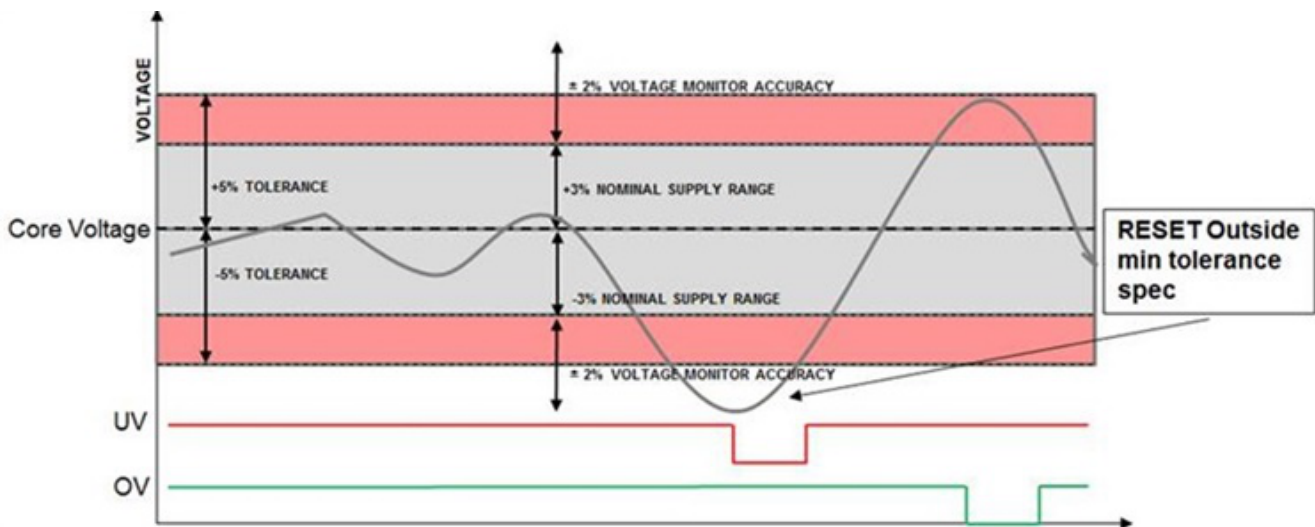

Figure 1. Reset Occurs outside the Safe Core-voltage Tolerance

Additionally, more and more safety standards in industrial and automotive applications, such as ISO26262 and ISO61508, require highly accurate voltage monitoring with integrated overvoltage detection.

To address these multiple challenges, TI has developed the TPS3702, an overvoltage and under voltage window comparator with fixed threshold voltages in a small SOT-23-6 package. This high accuracy window comparator provides FPGA designers with benefits including:

- FPGA/ASIC tight tolerances – the TPS3702 has a 0.9% maximum threshold voltage accuracy over temperature. This is accomplished by trimming the internal resistor dividers at factory level. Other voltage monitors require external resistor dividers that contribute to threshold voltage inaccuracies. The TPS3702 is ideal for systems that operate on low-voltage supply rails and have tight supply tolerances. Its very high accuracy guarantees a safe RST before the FPGA minimum/maximum supply tolerances are overruled.
- False reset within the nominal voltage window – low threshold hysteresis options of 0.55% or 1.0% prevent nuisance interrupts while making sure that the RST will be released only when V_{CC} is back to the safe window.
- Immunity to overshoot and undershoot spikes – internal glitch immunity filters further eliminate false resets resulting from erroneous signals.
- ASIL and SIL risk classes require accurate overvoltage and undervoltage – the TPS3702 enables you to choose the window-wide threshold options around the selected voltage option (+/-3%, +/-5%, +/-7%, +/-10%) according to your application requirements and safety standard needs.
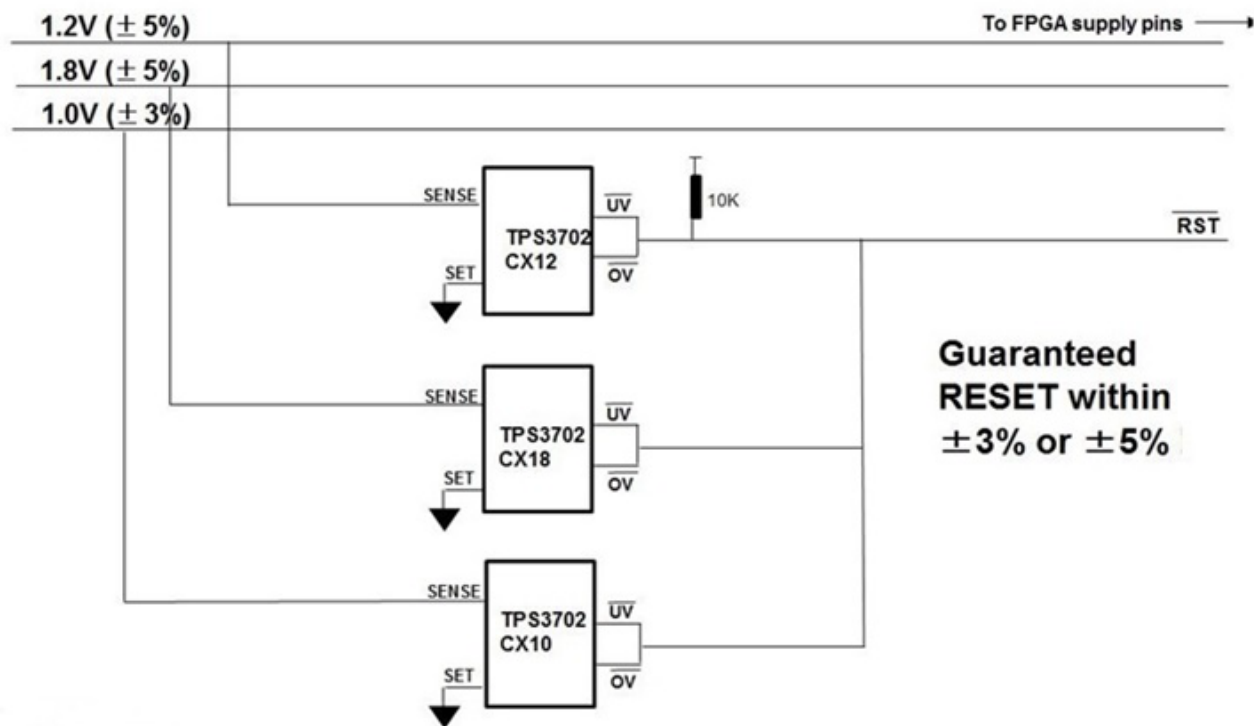
Figure 2. A Possible Application with the TPS3702

To learn more about how to solve these challenges in your next design, check out the TPS3702 or the resources below.

Additional Resources:
- Download the TPS3702 datasheet.
- Learn about TI's monitors and the rest of the supervisors and reset ICs in this quick reference guide.
- Find application notes about voltage supervisors.

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