Technical Article

How to reduce the THD of a PFC

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Total harmonic distortion (THD) is the harmonic distortion present in a signal, defined as the ratio of the root-mean-square (RMS) amplitude of a set of higher harmonic frequencies to the RMS amplitude of the first harmonic, or fundamental frequency. Equation 1 expresses THD:

$$THD = \frac{\sqrt{V_2{}^2 + V_3{}^2 + V_4{}^2 + \cdots}}{V_1} \quad (1)$$

where V_n is the RMS value of the nth harmonic and V_1 is the RMS value of the fundamental component.

In power systems, these harmonics can cause problems ranging from telephone transmission interference to conductor degradation; therefore, it is important to control the total THD. A lower THD means a lower peak current, less heating, lower electromagnetic emissions, and less core loss in motors.

Reducing THD needs power factor correction (PFC), which is required for AC/DC power supplies that have input power greater than 75 W. PFC forces the input current to follow the input voltage such that the electronics load draws a sinusoidal current waveform that contains minimal harmonics.

THD requirements have become stricter, especially in server applications. The Modular Hardware System-Common Redundant Power Supply (M-CRPS) specification defines a very strict THD requirement across the entire load range, as shown in Table 1. This is much stricter than the previous CRPS THD specification.

Table 1. The M-CRPS THD specification. Source: Texas Instruments

Output power	< 5%	5%≤In≤10%	10%<Iin≤20%	20%<Iin≤50%	50%<Iin≤100%
Current iTHD (240VAC) Capacity Levels ≥ 1400W	< 20%	< 8.5%	< 7.5%	< 5%	< 3.5%
Current iTHD (240VAC) Capacity Levels < 1400W	< 25%	< 10%	< 10%	< 7.5%	< 4%
Current iTHD (120VAC)	< 25%	< 10%	< 7.5%	< 5%	< 4%

Meeting such strict THD specifications is a big challenge in PFC designs where traditional loop tuning may not be enough. In this article, I'll suggest a few extra methods to help reduce THD.

Make sure that the sensed signals are clean

The PFC controller senses the AC input voltage, inductor current and PFC output voltage. These sensed signals need to be clean; otherwise, they will affect THD. For example, because the AC input voltage signal generates a sinusoidal current reference, any spikes on the sensed signal will cause current reference distortion and affect THD.

Although the output voltage (V_{OUT}) signal is not used for generating a current reference, it can affect THD because the spikes on V_{OUT} will cause a ripple on the voltage-loop output, which affects the current-loop reference and eventually THD. If the spike's magnitude is large enough, it may trigger a voltage-loop nonlinear gain, significantly raising THD.

One common practice is to put a decoupling capacitor close to the sense pin of the controller. You will have to carefully select the capacitance such that it will effectively reduce the noise but not cause too much delay. Using

a digital infinite impulse response filter to process the sensed V_{OUT} signal will further reduce the noise; because the PFC voltage loop is slow, the extra delay caused by this digital filter is acceptable.

For AC voltage sensing, however, it is not recommended to add a digital filter because it will cause a delay on the current reference. In this case, you can use a firmware phase-locked loop (PLL) to generate an internal sine wave signal in phase with the AC voltage, and then use that generated sine-wave signal to modulate the current reference. Since the PLL-generated sine wave is clean, even if there is some noise on the sensed AC voltage, the current-loop reference will also be clean.

Reduce the current spikes at AC zero crossing

Current spikes at AC zero crossing are an inherent issue for the totem-pole bridgeless PFC. These spikes can be so big that it becomes impossible to pass M-CRPS THD specifications. I've analyzed the root cause of these spikes, and noted that a pulse-width modulation (PWM) soft-start algorithm, as shown in Figure 1, will effectively reduce them.

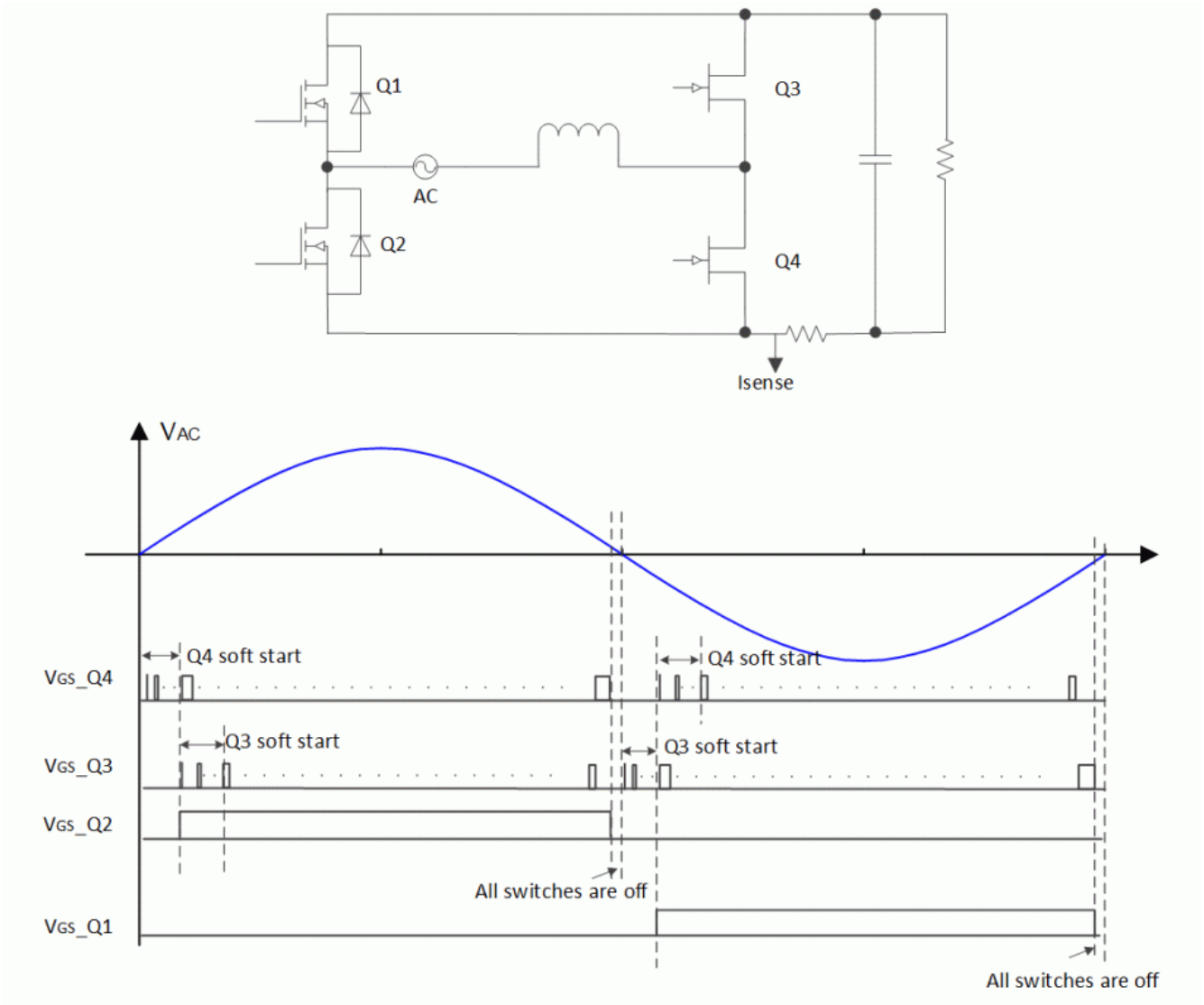

Figure 1. Gate signal timing for AC zero crossing. Source: Texas Instruments

In this solution, when V_{AC} changes from a negative to a positive cycle after AC zero crossing, active switch Q4 turns on first with a very small pulse width, then gradually increases to the duty cycle (D) generated by the control loop. A soft start on Q4 gradually discharges the switch-node drain-to-source voltage (V_{DS}) to zero.

Once Q4's soft start is complete, synchronous transistor Q3 starts to turn on. It begins with a tiny pulse width and gradually increases until the pulse width reaches 1-D. When Q4's soft start is complete and Q3's soft start begins, the low-frequency switch Q2 turns on.

The zero-crossing detection could be undesirably triggered by noise. For safety purposes, at the end of the half AC cycle, turn off all of the switches. This leaves a small dead zone that will prevent the input AC from short-circuiting. The transition from the AC positive cycle to the negative cycle is the same. Figure 2 shows the test result.

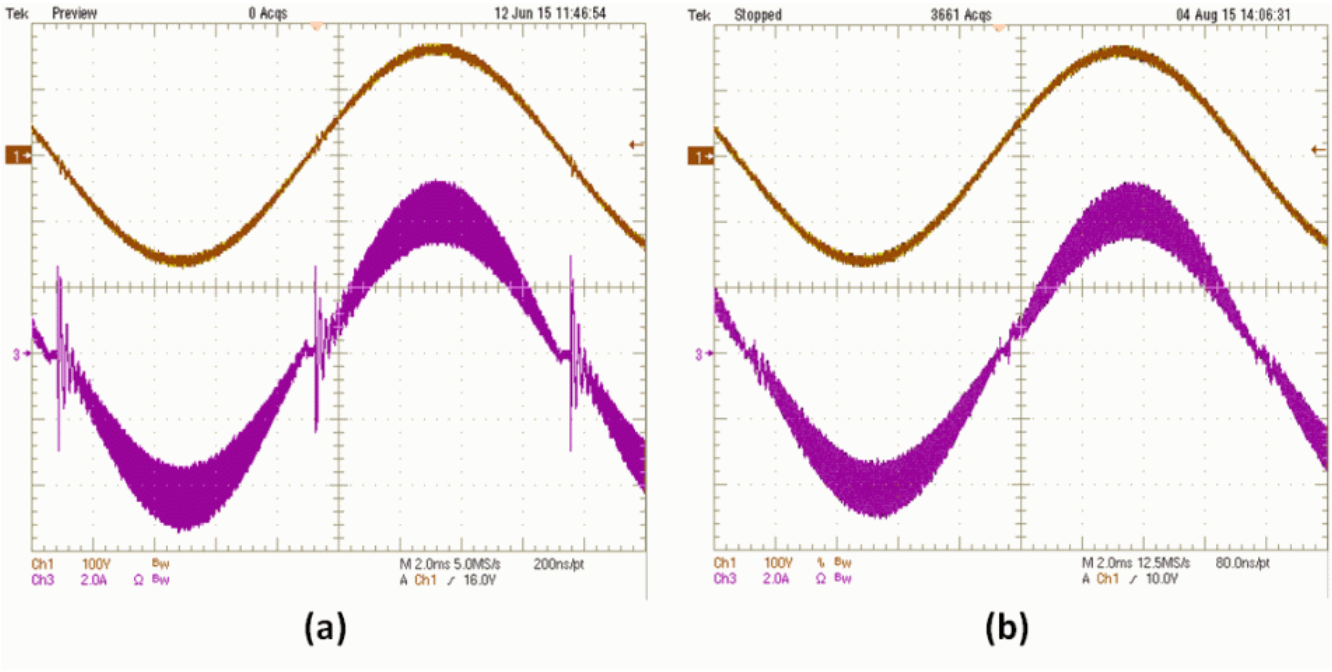

Figure 2. Current waveforms without and with a PWM soft start: the traditional control method (a) and PWM soft start (b). Source: Texas Instruments

Reduce voltage-loop effects

The double-line frequency ripple on the voltage-loop output can affect the current reference and thus THD. To reduce this frequency ripple effect as much as possible - while at the same time not sacrificing the load transient response - you could add a digital notch (band-stop) filter between the V_{OUT} sensed signal and the voltage loop. This notch filter can effectively attenuate the double-line frequency ripple while still passing all other frequency signals, including the sudden V_{OUT} change caused by the load transient. The load transient will not be affected.

Another approach is to sense V_{OUT} at the AC zero-crossing instance. Since the V_{OUT} value at AC zero-crossing instance Vout_zc(t) equals its average value and it is a "constant" in steady-state, it is the perfect feedback signal for voltage-loop control. To handle the load transient, use this voltage-loop control law:

```
If ((Vref – Vout(t) < Threshold)
{
Error = Vref – Vout_zc(t);
VoltageLoop_output = Gv(Error, Kp, Ki);
}
Else
{
Error = Vref – Vout(t);
```

VoltageLoop_output = Gv(Error, Kp_nl, Ki_nl);

}

If the instantaneous V_{OUT} error is small, use the V_{OUT} value at the AC zero-crossing instance Vout_zc(t) and small proportional-integral (PI) loop gain Kp, Ki for voltage-loop compensator Gv. When a load transient occurs causing an instantaneous V_{OUT} error greater than the threshold, use the instantaneous Vout(t) value and PI loop gain Kp_nl, Ki_nl for Gv to rapidly bring V_{OUT} back to its nominal value.

Oversampling

The PFC inductor current is a saw wave with DC offset in each switching cycle; the current then goes to a signal-conditioning circuit such as an operational amplifier to make the signal suitable for the PFC control circuit. However, this signal-conditioning circuit does not provide sufficient attenuation to the input current ripple. The current ripple still appears at the output of the amplifier. If this signal is sampled only once in each switching period, there is no perfect, fixed location where the signal represents the average current all of the time. Thus, with a single sample, it is very difficult to achieve good THD.

To get a more accurate feedback signal, I recommend an oversampling mechanism. Figure 3 shows that it is possible to evenly sample the current feedback signal eight times in every switching cycle, average the results, and send them to the control loop. This oversampling effectively averages the current ripple out such that the measured current signal gets closer to the average current value. Also, the controller becomes less sensitive to noise - both signal noise and measurement noise. Oversampling is one of the most effective ways to reduce current waveform distortions.

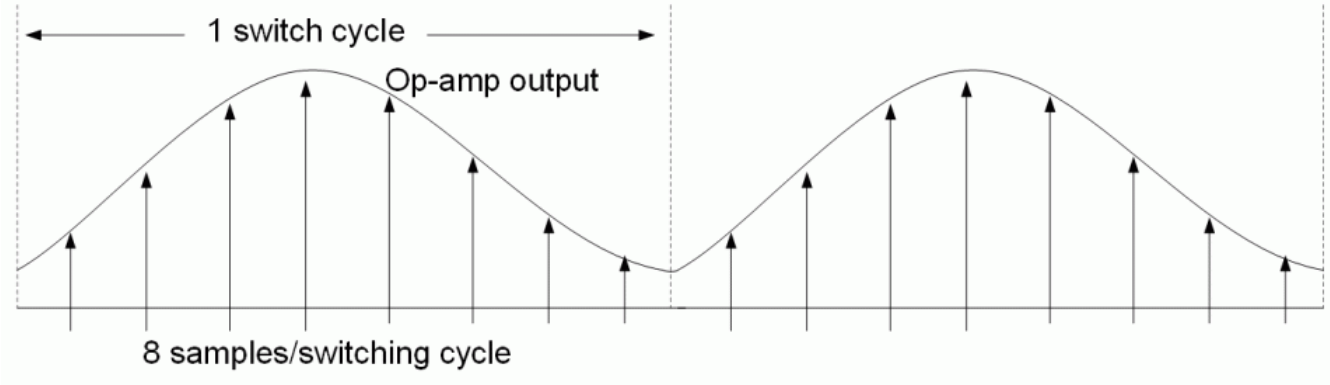

Figure 3. Oversampling eight times in every switching cycle. Source: Texas Instruments

Duty-ratio feedforward

The basic idea of duty-ratio feedforward control is to pre-calculate a duty ratio, then add this duty ratio to the feedback controller. For a boost topology operating in continuous conduction mode, Equation 2 gives the duty ratio (d_{FF}) as:

$$d_{ff} = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (2)$$

This duty-ratio pattern effectively produces a voltage across the switch whose average over a switching cycle is equal to the rectified input voltage. A regular current-loop compensator changes the duty ratio around this calculated duty-ratio pattern.

Figure 4 depicts the resulting control scheme. After using Equation 2 to calculate d_{FF}, it is then added to the traditional average current-mode control output (d_I). You could then use the final duty ratio (d) to generate a PWM waveform to control PFC.

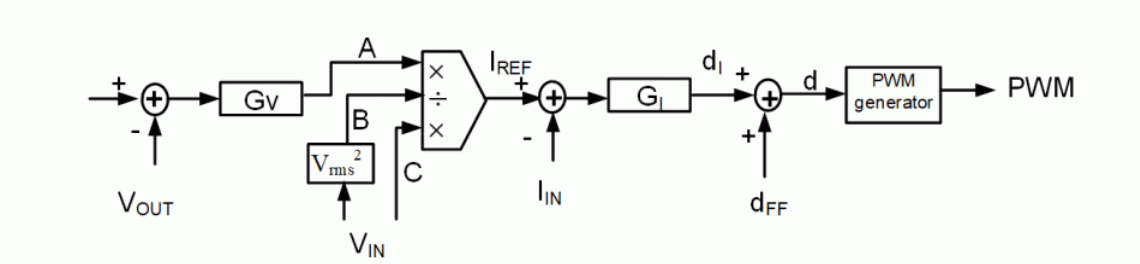

Figure 4. Average current-mode control with d_{FF}. Source: Texas Instruments

Since the majority of the duty cycle is generated by duty-ratio feedforward, the control loop only adjusts the calculated duty slightly. This technique can help improve THD for applications with a limited controller loop bandwidth.

AC cycle skipping

In general, it's harder to meet light-load THD requirements than heavy-load THD requirements; this is especially true for the 5% load THD requirement in the M-CRPS specification. If the PFC meets all other THD requirements except at a 5% load, even if you have tried all the methods mentioned so far, an AC cycle-skipping method can help.

Think of AC cycle skipping as a special burst mode: when the load is less than a pre-defined threshold, the PFC enters this mode and, depending on the load, skips one or more AC cycles. In other words, the PFC turns off for one or more AC cycles and turns back on for the next AC cycle. The turnon and turnoff instance is at the AC zero crossing such that the whole AC cycle is skipped. Since PFC turnon and turnoff at current equal zero, there is less stress and electromagnetic interference. AC cycle skipping is different than the traditional PWM pulse-skipping burst mode, where you skip PWM pulses randomly.

The number of AC cycles to skip is reverse-proportional to the load; the less load, the more AC cycles skipped. Figure 5 shows the skipping of one AC cycle. Channel 1 is the AC voltage, and channel 4 is the AC current.

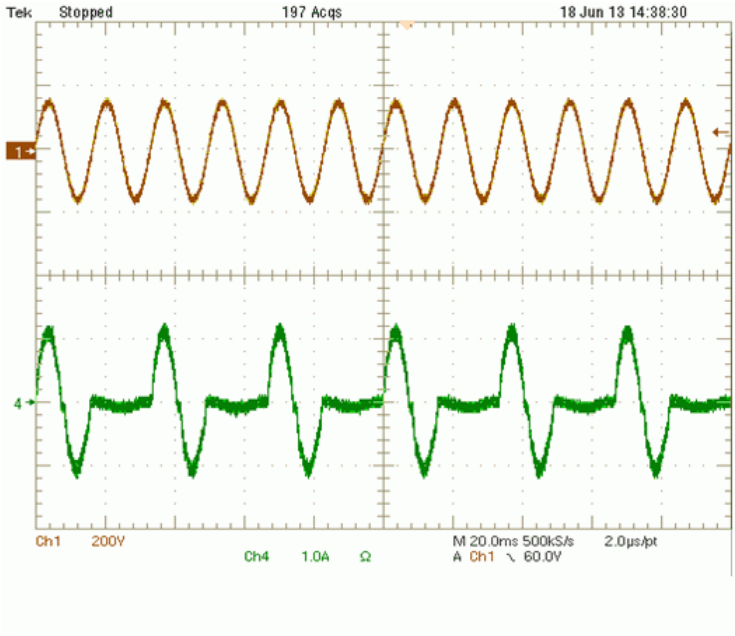

Figure 5. AC cycle skipping at a light load. Source: Texas Instruments

When the PFC turns off because the current is zero, THD is zero. Since the PFC needs to compensate for the turnoff period, it delivers a large amount of power when it turns on, which is greater than the average value.

Essentially, this operates the PFC either at medium load, or it completely turns off. Since THD is much lower at a middle load than at a light load, light-load THD is reduced.

Test results

I implemented the methods described in this article on a 3-kW totem-pole bridgeless PFC [5] controlled by a Texas Instruments C2000™ microcontroller. Figure 6 shows the THD test result at 240 V_{AC}.

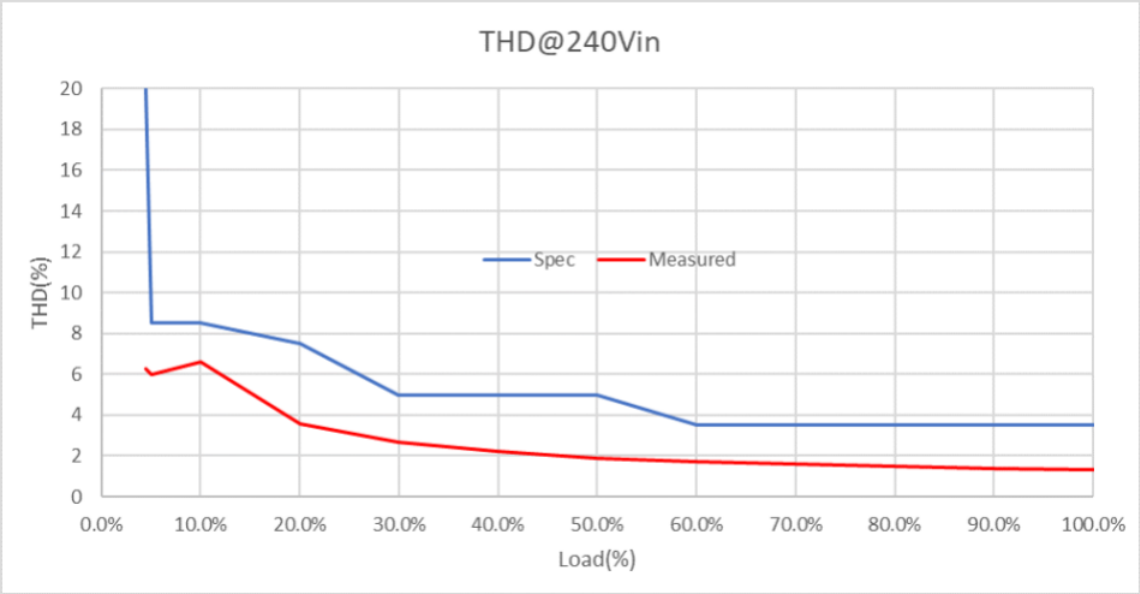

Figure 6. THD test results. Source: Texas Instruments

The THD not only meets the latest M-CRPS THD specifications but also has plenty of margin, which guarantees that the PFC will meet specifications during mass production, even with hardware tolerance.

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References

1. The Open Compute Project. n.d. Open Possibilities. Accessed April 10, 2023.
2. Sun, Bosheng. "How to Reduce Current Spikes at AC Zero Crossing for Totem-Pole PFC." Texas Instruments Analog Design Journal article, literature No. SLYT650, 4Q 2015.
3. Van de Sype, D.M., Koen De Gusseme, A.P.M. Van den Bossche, and J.A. Melkebeek. "Duty-Ratio Feedforward for Digitally Controlled Boost PFC Converters." Published in IEEE Transactions on Industrial Electronics 52, no. 1 (February 2005): pp. 108-115.
4. Sun, Bosheng. "AC Cycle Skipping Improves PFC Light-Load Efficiency." Texas Instruments Analog Design Journal article, literature No. SLYT585, 3Q 2014.
5. Texas Instruments. n.d. "3-kW, 180-W/in3 Single-Phase Totem-Pole Bridgeless PFC Reference Design with 16-A Max Input." Texas Instruments reference design No. PMP23069. Accessed April 10, 2023.

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