Technical Article

Designing a high voltage DC-link capacitor active precharge circuit

Tilden Chen, Hrag Kasparian

Introduction

Electric vehicles (EVs) typically feature a large DC link capacitor ($C_{DC\ LINK}$) to minimize voltage ripple at the input of the traction inverter. When powering up an EV, the purpose of precharging is to safely charge up $C_{DC\ LINK}$ before operating the vehicle. Charging $C_{DC\ LINK}$ up to the battery stack voltage (V_{BATT}) prevents arcing on the contactor terminals, which can lead to catastrophic failures over time.

The conventional precharge method involves implementing a power resistor in series with the $C_{DC\ LINK}$ to create a resistor-capacitor (RC) network. However, as the total $C_{DC\ LINK}$ capacitance and V_{BATT} increase, the required power dissipation grows exponentially. In this article, we'll present a straightforward approach to designing an efficient, active pre-charge circuit using a spreadsheet calculator.

Understanding active precharge

While passive precharge employs a power resistor to create an RC circuit that charges the capacitor asymptotically, active precharge can employ a switching converter with a buck topology that uses hysteretic inductor current control to deliver a constant charge current to the capacitor (Figure 1).

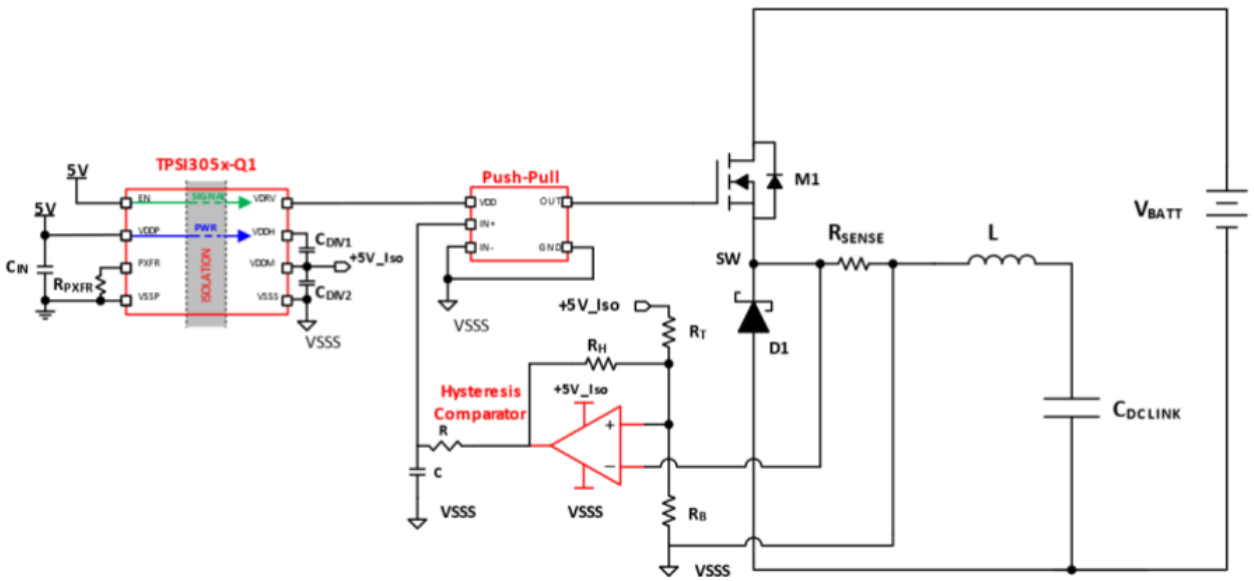

Figure 1. The active precharge circuit where a buck converter uses a hysteretic inductor current control to deliver a constant charge current to the capacitor to enable the linear charge of the capacitor voltage (V_{CAP}) up to the same voltage potential as the battery (V_{BATT}). Source: Texas Instruments

This constant current enables linear charging of the capacitor voltage (V_{CAP}) up to the same voltage potential as that of the battery. Figure 2 and Equation 1 characterize this linear behavior.

$$\frac{dV}{dt} = \frac{I_{\text{CHARGE}}}{C_{\text{DC LINK}}} \quad (1)$$

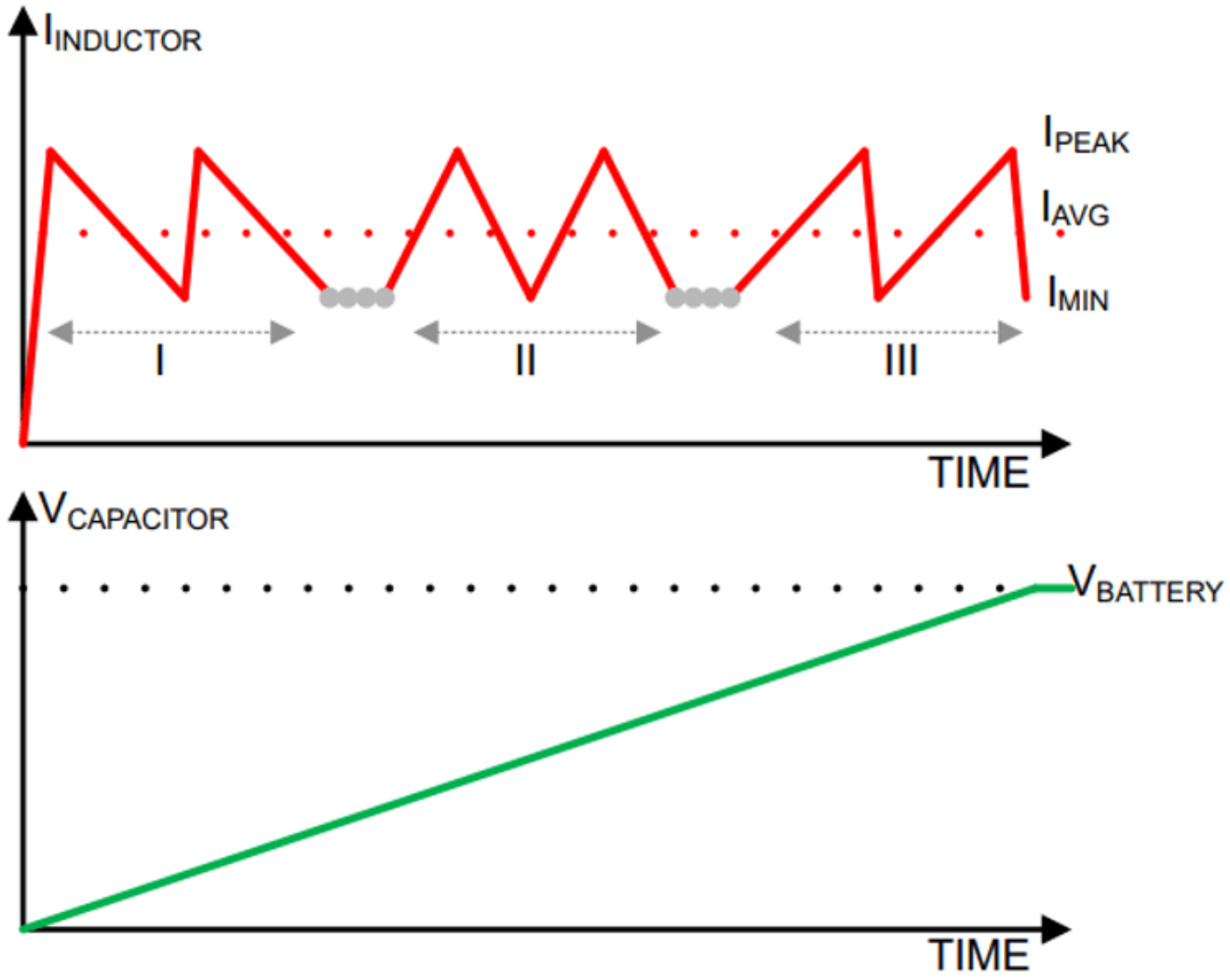

Figure 2. Active precharge linear behavior using a buck topology with hysteretic inductor current control. Source: Texas Instruments

The first step is to determine the required charge current (I_{CHARGE}). I_{CHARGE} is the quotient of the total DC link charge ($Q_{DC\ LINK}$) and the required precharge time (t_{CHARGE}) shown in Equation 2.

$$I_{CHARGE} = \frac{Q_{DCLINK}}{t_{CHARGE}} \quad (2)$$

$Q_{DC\ LINK}$ is the product of $C_{DC\ LINK}$ and V_{BATT}, as shown in Equation 3.

$$Q_{\text{DC LINK}} = C_{\text{DC LINK}} \times V_{BATT} \quad (3)$$

Calculator overview

This active hysteretic buck circuit has a floating ground potential riding on the switch node, so powering the control system requires an isolated bias supply. The calculator tool will ensure that the power consumption of this control circuitry stays within the sourcing capability of the isolated bias supply, or else the voltage will collapse.

The High-Voltage Solid-State Relay Active Precharge Reference Design from Texas Instruments (TI) introduces an active solution that enhances energy transfer efficiency and reduces practical charge time. TI's TPSI3052-Q1 is a fully integrated isolated bias supply used in the active precharge reference design, which can source and supply up to 83 mW of power to the isolated secondary. Gate drive current, device quiescent currents, and resistor dividers are the primary contributors to power consumption. Equation 4 characterizes the gate drive power ($P_{GATE\ DRIVE}$) as the product of the gate drive current ($I_{GATE\ DRIVE}$) and gate drive voltage ($V_{S\ GATE\ DRIVER}$) which is 15V, in the case of the reference design.

$$P_{\text{GATE DRIVE}} = I_{\text{GATE DRIVE}} \times V_{\text{S GATE DRIVER}} \tag{4}$$

Equation 5 characterizes gate drive current as the product of the metal-oxide semiconductor field-effect transistor (MOSFET) total gate charge (Q_G) and switching frequency (F_{SW}).

$$I_{GATEDRIVE} = Q_G \times F_{SW} \tag{5}$$

Equation 6 expresses how F_{SW} varies according to V_{CAP} throughout the charging period, creating the upside-down parabola in the F_{SW} versus V_{CAP} curve in Figure 3. As shown in the figure below, the gate drive current peaks at the maximum switching frequency (F_{SW_MAX}), which occurs when V_{CAP} reaches half of V_{BATT}. Equation 7 expresses the relationship between F_{SW_MAX}, V_{BATT}, inductance (L) and peak-to-peak inductor current (dI):

$$F_{SW} = \frac{V_{CAP} - \frac{V_{CAP}^2}{V_{BATT}}}{L \times dI} \tag{6}$$

$$F_{SW\_MAX} = \frac{V_{BATT}}{4 \times L \times dI} \tag{7}$$

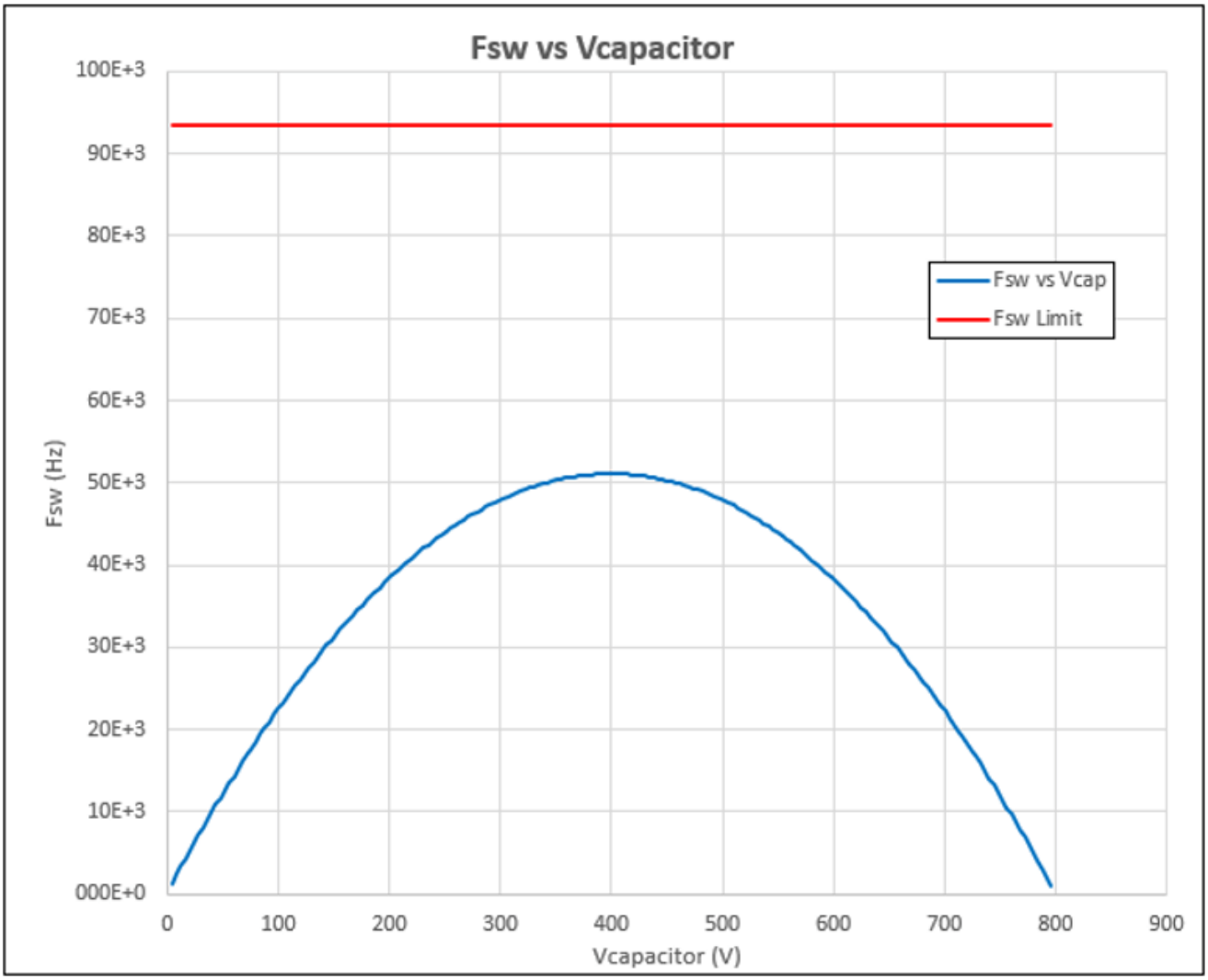

Figure 3. Calculator curve showing F_{SW} versus V_{CAP} and $F_{SW\ LIMIT}$. Source: Texas Instruments

Using the calculator tool

The calculator prompts you to input various design parameters. The yellow cells are the required inputs while gray cells signify optional inputs. The default values in the gray cells reflect the parameters of the reference design. A user can change the gray cell values as needed. The white cells show the calculated values as outputs. A red triangle in the upper-right corner of a cell indicates an error; users will be able to see a pop-up text on how to fix them. The objective is to achieve a successful configuration with no red cells. This can be an iterative process where users can hover their mouse over each of the unit cells to read explanatory information.

Precharge system requirements

The first section of the calculator, shown in Figure 4, computes the required charge current ($I_{CHARGE\ REQUIRED}$) based on the V_{BATT}, t_{CHARGE}, and $C_{DC\ LINK}$ system parameters.

Parameter	Value	Units
V_{BATT}	800	V
t_{CHARGE}	400.0E-3	sec
$C_{DC\ LINK}$	2.0E-3	F
$Q_{DC\ LINK}$	1.6E+0	C
$I_{CHARGE\ REQUIRED}$	4.00E+0	A

Battery or supply voltage, which will also be the final voltage the capacitor gets charged up to.

Figure 4. The required charge current ($I_{CHARGE\ REQUIRED}$) based on the V_{BATT}, t_{CHARGE}, and $C_{DC\ LINK}$ system parameters. Source: Texas Instruments

Inductance and charge current programming

The section of the calculator shown in Figure 5 calculates the actual average charging current (I_{CHARGE}) and F_{SW_MAX}. The average inductor current essentially equates to I_{CHARGE} where I_{CHARGE} must be equal to or greater than $I_{CHARGE\ REQUIRED}$, this was calculated in the previous section to meet the desired t_{CHARGE}.

Be mindful of the relationship between L, dI, and F_{SW_MAX} as expressed in Equation 7. L and dI are each inversely proportional to F_{SW}, so it is important to select values that do not exceed the maximum switching frequency limit ($F_{SW\ LIMIT}$). Your inductor selection should accommodate adequate root-mean-square current ($I_{RMS} > I_{CHARGE}$), saturation current ($I_{SAT} > I_{L\ PEAK}$), and voltage ratings, with enough headroom as a buffer for each.

L	560.0E-6	H
$I_{L\ PEAK}$	7.5E+0	A
$I_{L\ VALLEY}$	500.0E-3	A
$V_{HYSTERISIS\ +\ OFFSET\ COMP.}$	22.00E-3	V
V_F	1.25	V
$I_{L\ PK\text{-}TO\text{-}PK}$	7.00E+0	A
I_{CHARGE}	4.00E+0	A
$F_{SW\ MIN.}$	1.0E+3	Hz
$F_{SW\ MAX.}$	51.1E+3	Hz
$F_{SW\ MAX.\ LIMIT}$	93.5E+3	Hz

Figure 5. Inductance and charge current programming parameters. Source: Texas Instruments

Current sensing and comparator setpoints

The section of the calculator shown in Figure 6 calculates the bottom resistance (R_B), top resistance (R_T), and hysteresis resistance (R_H) around the hysteresis circuit needed to meet the peak ($I_{L\ PEAK}$) and valley ($I_{L\ VALLEY}$) inductor current thresholds specified in the previous section. Input the current sense resistance (R_{SENSE}) and R_B. These are flexible and can be changed as needed. Make sure that the comparator supply voltage ($V_{S\ COMPARATOR}$) is correct.

R_{SENSE}	100.0E-3	Ω
$P_{AVG.\ Rsense}$	1.60E+0	W
$V_{COMP.\ LOW}$	50.00E-3	V
$V_{COMP.\ HIGH}$	750.00E-3	V
$V_{s\ COMPARATOR\ IC}$	5.00	V
R_B	2.37E+3	Ω
R_T	201.45E+3	Ω
R_H	14.39E+3	Ω

Figure 6. Section that calculates the bottom resistance (R_B), top resistance (R_T), and hysteresis resistance (R_H) around the hysteresis circuit needed to meet the peak ($I_{L\ PEAK}$) and valley ($I_{L\ VALLEY}$) inductor current thresholds. Source: Texas Instruments

Bias supply and switching frequency limitations

The section of the calculator shown in Figure 7 calculates the power available for switching the MOSFET ($P_{REMAINING\ FOR\ FET\ DRIVE}$), by first calculating the total power draw (P_{TOTAL}) associated with the hysteresis circuit resistors ($P_{COMP.\ RESISTORS}$), the gate driver integrated circuit (IC) ($P_{GATE\ DRIVER\ IC}$), and the comparator IC ($P_{COMPARATOR\ IC}$), and subtracting it from the maximum available power of the TPSI3052-Q1 ($P_{MAX\_ISOLATED\ BIAS\ SUPPLY}$). Input the MOSFET total gate charge ($Q_{G\ TOTAL}$), device quiescent currents ($I_{S\ GATE\ DRIVER\ IC}$ and $I_{SUPPLY\ COMP\ IC}$), and gate driver IC supply voltage ($V_{S\ GATE\ DRIVER\ IC}$). The tool uses these inputs to calculate $F_{SW\ LIMIT}$ displayed as a red line in Figure 3.

$V_{s\ COMPARATOR\ IC}$	5.00	V
R_B	2.37E+3	Ω
R_T	201.45E+3	Ω
R_H	14.39E+3	Ω
$V_{s\ GATE\ DRIVER\ IC}$	15.00	V
$I_{s\ GATE\ DRIVER\ IC}$	750.00E-6	A
$I_{SUPPLY\ COMP.}$	10.00E-6	A
$P_{MAX\ ISOLATED\ BIAS\ SUPPLY}$	83.00E-3	W
$R_{DIVIDER\ MIN.}$	15.80E+3	Ω
$I_{MAX\ R\_DIVIDERS}$	316.46E-6	A
$P_{GATE\ DRIVER\ IC}$	11.25E-3	W
$P_{COMPARATOR\ IC}$	50.00E-6	W
$P_{COMP.\ RESISTORS}$	1.58E-3	W
P_{TOTAL}	12.88E-3	W
$P_{REMAINING\ FOR\ FET\ Drive}$	70.12E-3	W
$Q_{G\ TOTAL}$	50.00E-9	Q
$I_{GATE\ DRIVE}$	4.67E-3	A

Figure 7. Isolated bias supply and switching frequency limitations parameters. Source: Texas Instruments

The calculator tool makes certain assumptions and do not account for factors such as comparator delays and power losses in both the MOSFET and the freewheeling diode. The tool assumes the use of rail-to-rail input and output comparators. Make sure to select a MOSFET with an appropriate voltage rating, R_{DSON}, and parasitic capacitance parameters. Ensure the power loss in both the MOSFET and freewheeling diode are within acceptable limits. Finally, select a comparator with low offset and low hysteresis voltages with respect to the current sense peak and valley-level voltages. Simulating the circuit with the final calculator values ensures the intended operation.

Achieved the desired charge profile

Adopting an active hysteretic buck circuit significantly improves efficiency and reduces the size of the charging circuitry in high voltage DC-link capacitors found in EVs. This helps potentially lower the size, cost, and thermals of a precharge solution.

This article presents the design process to calculate the appropriate component values that help achieve the desired charge profile.

By embracing these techniques and tools, engineers can effectively improve the precharge functionality in EVs, leading to improved power management systems to meet the increasing demands of the automotive industry.

Related Content

- Power Tips #127: Using advanced control methods to increase the power density of GaN-based PFC
- Power Tips #126: Hot plugging DC/DC converters safely
- Power Tips #125: How an opto-emulator improves reliability and transient response for isolated DC/DC converters
- Teardown: The nuances of variable-frequency drives

Previously published on EDN.com.

Trademarks

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265